SN54HCT74, SN74HCT74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS
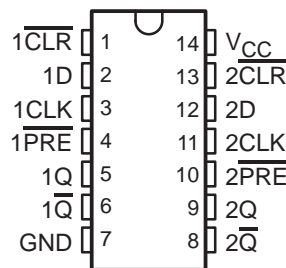## WITH CLEAR AND PRESET

SCLS169E – DECEMBER 1982 – REVISED APRIL 2004

- **Operating Voltage Range of 4.5 V to 5.5 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 40-μA Max I_{CC}**
- **Typical t_{pd} = 17 ns**
- **$\pm$4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
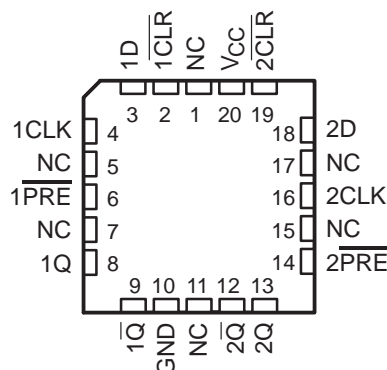- **Inputs Are TTL-Voltage Compatible**

description/ordering information

The 'HCT74 devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

SN54HCT74 . . . J OR W PACKAGE
SN74HCT74 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

```
        _____
1CLR [ 1    14 ] V_CC
  1D [ 2    13 ] 2CLR
1CLK [ 3    12 ] 2D
1PRE [ 4    11 ] 2CLK
  1Q [ 5    10 ] 2PRE
  1Q [ 6     9 ] 2Q
 GND [ 7     8 ] 2Q
       _____
```

SN54HCT74 . . . FK PACKAGE
(TOP VIEW)

```
             1D  1CLR  NC  V_CC  2CLR

          3    2    1   20   19
1CLK [ 4                        18 ] 2D
  NC [ 5                        17 ] NC
1PRE [ 6                        16 ] 2CLK
  NC [ 7                        15 ] NC
  1Q [ 8                        14 ] 2PRE
          9   10   11   12   13

             1Q  GND  NC  2Q  2Q
```

NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube of 25	SN74HCT74N	SN74HCT74N
	SOIC – D	Tube of 50	SN74HCT74D	HCT74
		Reel of 2500	SN74HCT74DR	
		Reel of 250	SN74HCT74DT	
	SOP – NS	Reel of 2000	SN74HCT74NSR	HCT74
	SSOP – DB	Reel of 2000	SN74HCT74DBR	HT74
	TSSOP – PW	Tube of 90	SN74HCT74PW	HT74
		Reel of 2000	SN74HCT74PWR	
		Reel of 250	SN74HCT74PWT	
−55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCT74J	SNJ54HCT74J
	CFP – W	Tube of 150	SNJ54HCT74W	SNJ54HCT74W
	LCCC – FK	Tube of 55	SNJ54HCT74FK	SNJ54HCT74FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

SN54HCT74, SN74HCT74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH CLEAR AND PRESET

SCLS169E – DECEMBER 1982 – REVISED APRIL 2004

FUNCTION TABLE

INPUTS				OUTPUT	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

logic diagram (positive logic)
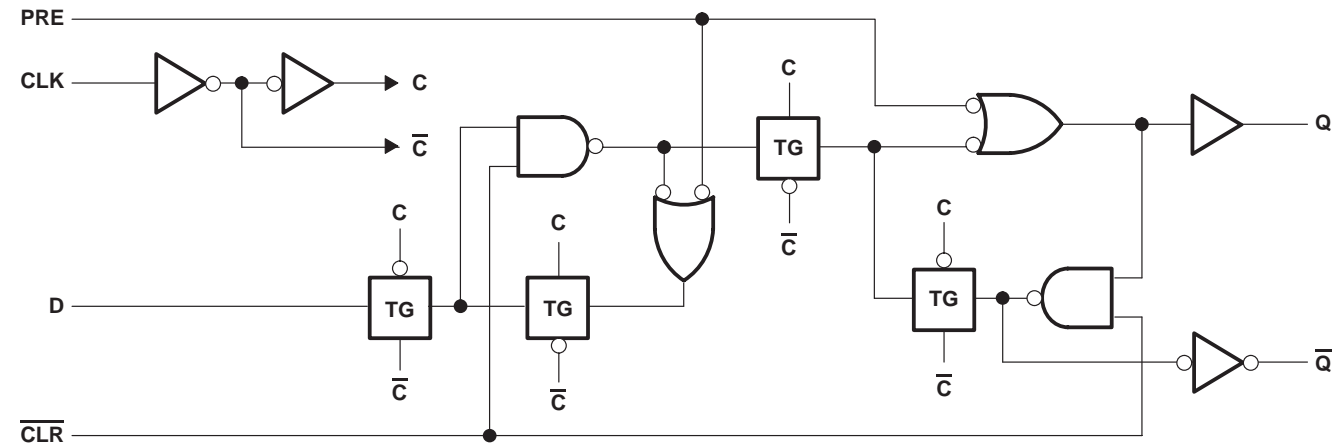
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) .... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±25 mA
Continuous current through V_{CC} or GND .... ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 86°C/W
                                                 DB package .... 96°C/W
                                                 N package .... 80°C/W
                                                 NS package .... 76°C/W
                                                 PW package .... 113°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HCT74			SN74HCT74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8			0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time				500			500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT74		SN74HCT74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = −4 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	5.5 V			4		80		40	μA
$\Delta I_{CC}^\dagger$	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HCT74		SN74HCT74		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		4.5 V		27		18		22	MHz
			5.5 V		30		20		24	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4.5 V	16		24		20		ns
			5.5 V	14		21		18		
		CLK high or low	4.5 V	18		27		23		
			5.5 V	16		24		21		
t_{su}	Setup time before CLK↑	Data	4.5 V	12		18		15		ns
			5.5 V	11		16		14		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	4.5 V	0		0		0		
			5.5 V	0		0		0		
t_h	Hold time, data after CLK↑		4.5 V	0		0		0		ns
			5.5 V	0		0		0		

TEXAS INSTRUMENTS

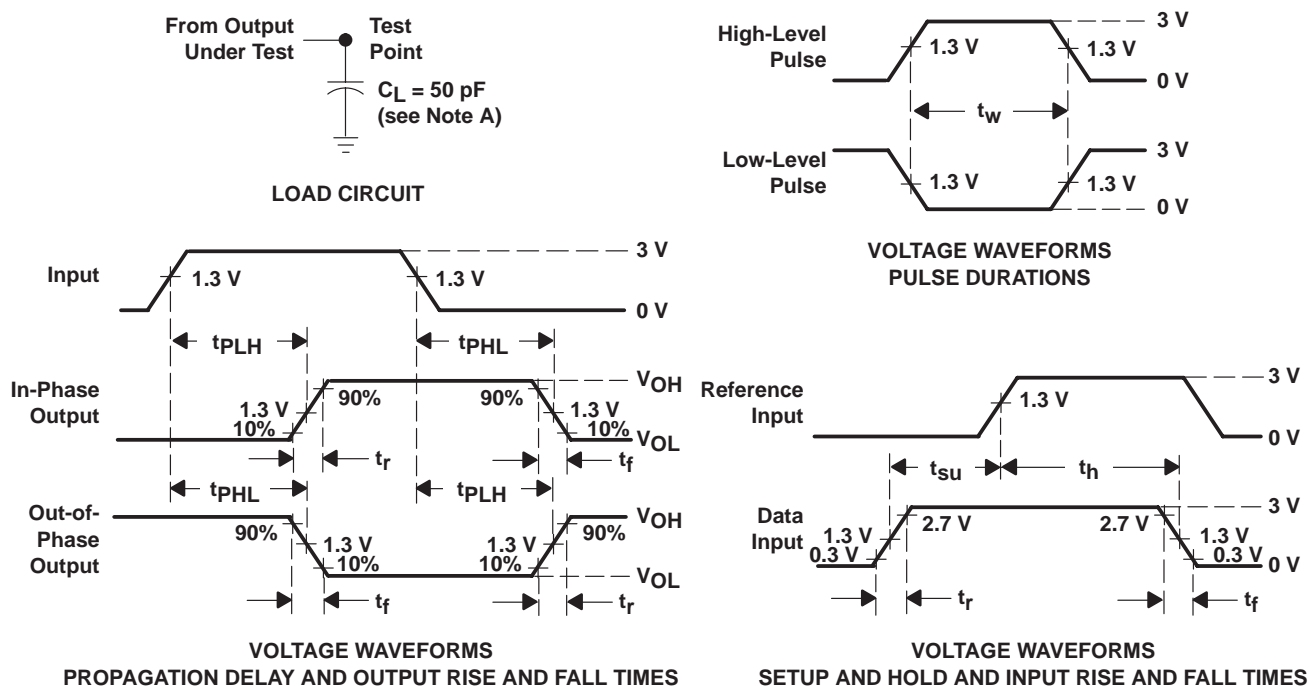## switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT74		SN74HCT74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	27	40		18		22		MHz
			5.5 V	30	46		20		24		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	4.5 V		21	35		53		44	ns
			5.5 V		17	31		48		40	
	CLK	Q or $\overline{Q}$	4.5 V		20	28		42		35	
			5.5 V		18	25		38		31	
t_t		Q or $\overline{Q}$	4.5 V		8	15		22		19	ns
			5.5 V		7	14		20		17	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES**

**VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES**

NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
 C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 D. The outputs are measured one at a time, with one input transition per measurement.
 E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/65352B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65352B2A	Samples
JM38510/65352BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65352BCA	Samples
JM38510/65352BDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65352BDA	Samples
M38510/65352B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65352B2A	Samples
M38510/65352BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65352BCA	Samples
M38510/65352BDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65352BDA	Samples
SN74HCT74D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74	Samples
SN74HCT74DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT74	Samples
SN74HCT74DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74	Samples
SN74HCT74DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74	Samples
SN74HCT74DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74	Samples
SN74HCT74DT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74	Samples
SN74HCT74N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT74N	Samples
SN74HCT74NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT74N	Samples
SN74HCT74NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74	Samples
SN74HCT74PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT74	Samples
SN74HCT74PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT74	Samples
SN74HCT74PWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT74	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HCT74, SN74HCT74 :

● Catalog : SN74HCT74

● Military : SN54HCT74

NOTE: Qualified Version Definitions:

 ● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

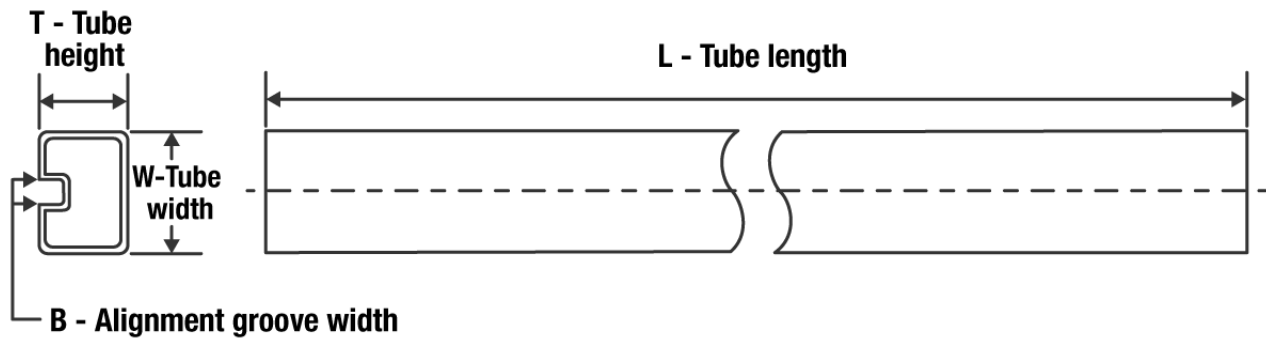| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT74DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HCT74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT74DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT74NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HCT74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT74PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT74DBR	SSOP	DB	14	2000	853.0	449.0	35.0
SN74HCT74DR	SOIC	D	14	2500	853.0	449.0	35.0
SN74HCT74DT	SOIC	D	14	250	210.0	185.0	35.0
SN74HCT74NSR	SO	NS	14	2000	853.0	449.0	35.0
SN74HCT74PWR	TSSOP	PW	14	2000	853.0	449.0	35.0
SN74HCT74PWT	TSSOP	PW	14	250	853.0	449.0	35.0

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
JM38510/65352B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
M38510/65352B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74HCT74D	D	SOIC	14	50	506.6	8	3940	4.32
SN74HCT74DG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74HCT74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT74NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT74NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT74PW	PW	TSSOP	14	90	530	10.2	3600	3.5
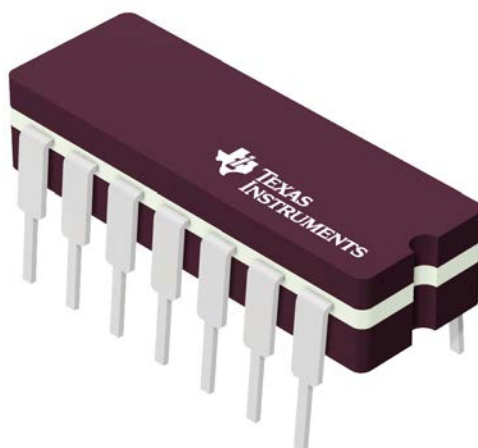
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

TEXAS
INSTRUMENTS

PIN 1 ID
(OPTIONAL)

A

4X .005 MIN
[0.13]

.015-.060 TYP
[0.38-1.52]

1

14

12X .100
[2.54]

14X .045-.065
[1.15-1.65]

14X .014-.026
[0.36-0.66]

⊕ .010 [0.25] C A B

.754-.785
[19.15-19.94]

7

8

B

.245-.283
[6.22-7.19]

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

C

SEATING PLANE

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015
[0.38]

GAGE PLANE

0°-15°
TYP

14X .008-.014
[0.2-0.36]

4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

(.300) TYP
[7.62]

SEE DETAIL A

SEE DETAIL B

1

14

12X (.100)
[2.54]

14X (∅ .039)
[1]

SYMM
℄

7

8

SYMM
℄

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

.002 MAX
[0.05]
ALL AROUND

(.063)
[1.6]

SOLDER MASK
OPENING

METAL

(R.002) TYP
[0.05]

DETAIL A
SCALE: 15X

METAL

(∅ .063)
[1.6]

SOLDER MASK
OPENING

.002 MAX
[0.05]
ALL AROUND

DETAIL B
13X, SCALE: 15X
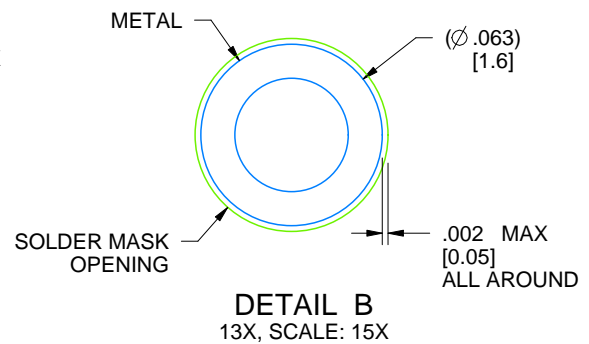
4214771/A   05/2017

D (R−PDSO−G14) PLASTIC SMALL OUTLINE
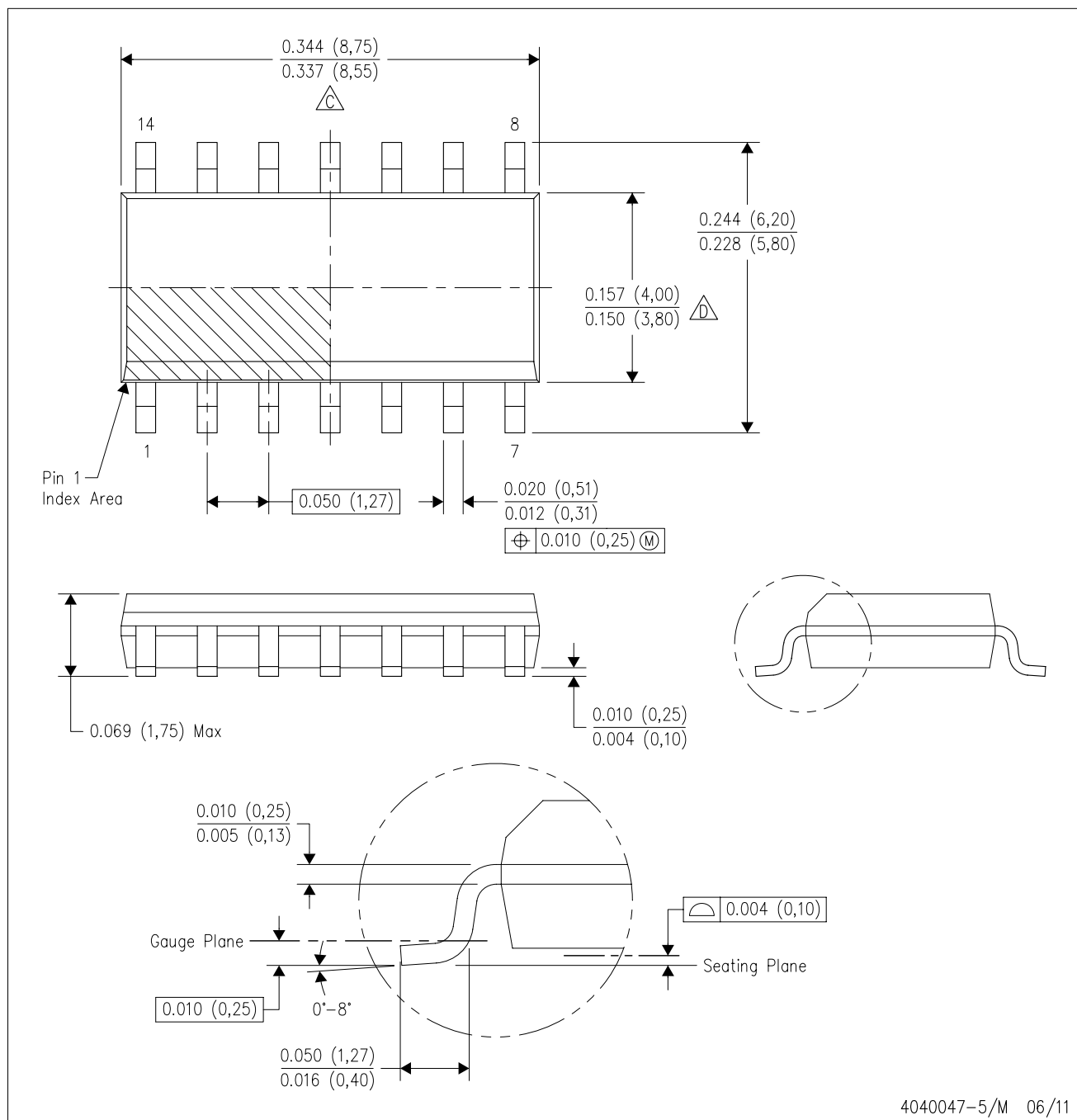
4040047−5/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
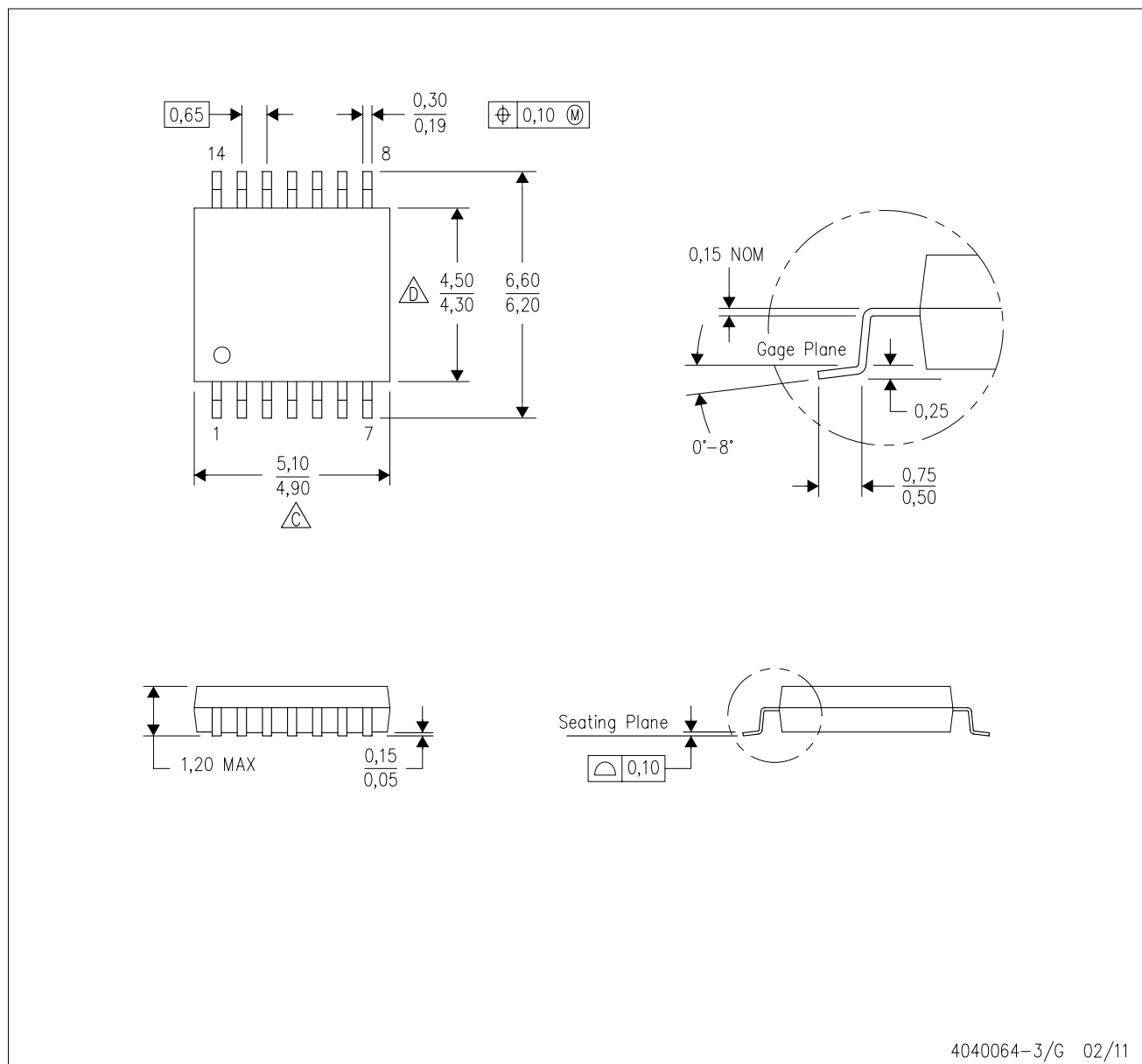   E.   Reference JEDEC MS−012 variation AB.

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INSTRUMENTS
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D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x1,27

14x0,55

12x1,27

14x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

Example
Solder Mask Opening
(See Note E)

1,55

0.07
All Around

4211283−3/E   08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
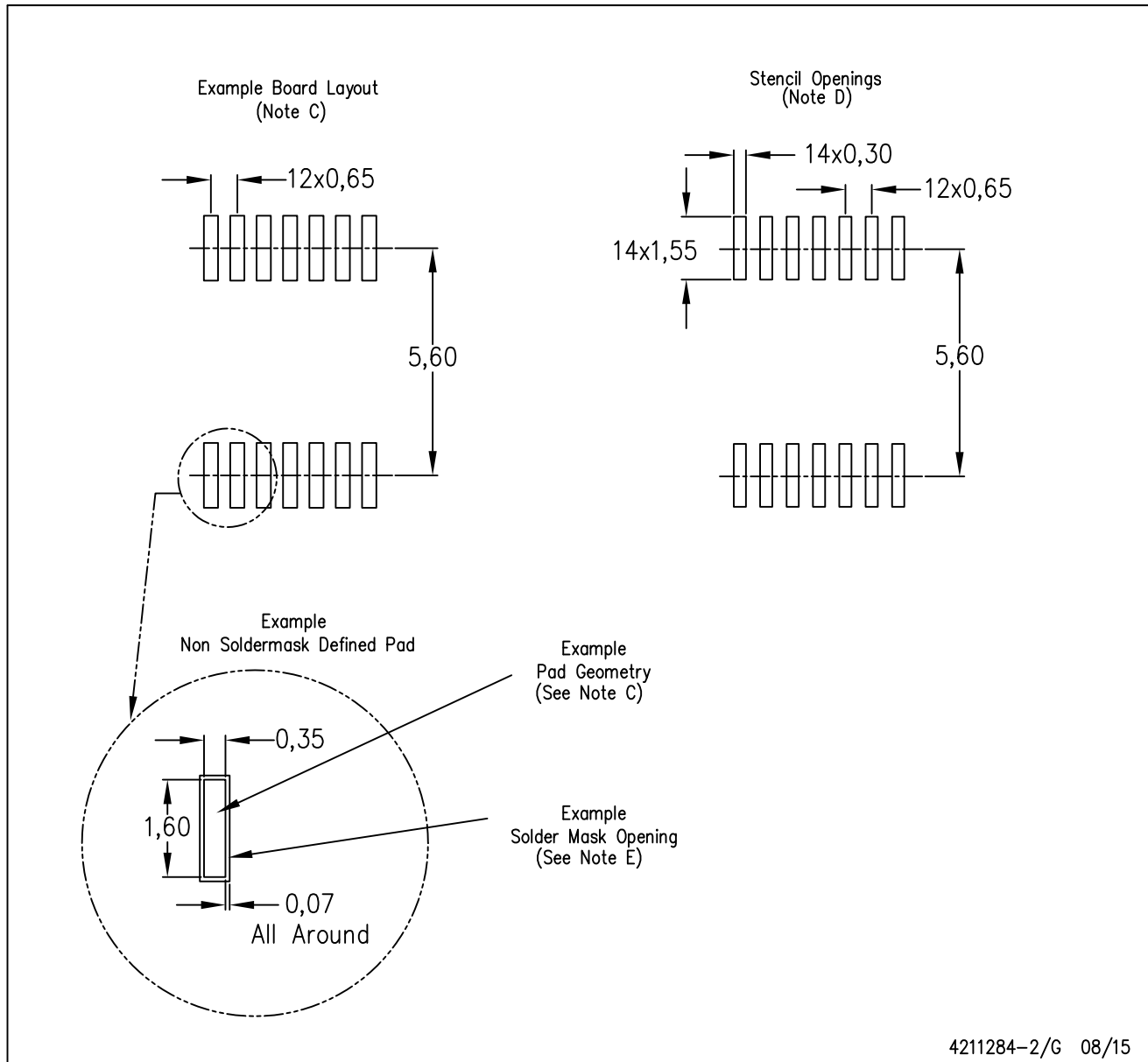
TEXAS
INSTRUMENTS
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PW (R–PDSO–G14)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

14   8

Ⓓ 4,50
4,30

6,60
6,20

1   7

5,10
4,90

Ⓒ

0,15 NOM

Gage Plane

0°–8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ 0,10

4040064–3/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
         B.   This drawing is subject to change without notice.
        Ⓒ   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
        Ⓓ   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO–153

PW (R–PDSO–G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x0,65

5,60

Stencil Openings
(Note D)

14x0,30

12x0,65

14x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

0,07
All Around

Example
Solder Mask Opening
(See Note E)

4211284–2/G   08/15

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC–7351 is recommended for alternate designs.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM ＼ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS−001 VARIATION	AA	BB	AC	AD

A

16　　　　　　　9

0.260 (6,60)
0.240 (6,10)

1　　　　　　　8

0.070 (1,78)
0.045 (1,14) △D

0.045 (1,14)
0.030 (0,76) △D

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option △D

4040049/E 12/2002

NOTES:　A.　All linear dimensions are in inches (millimeters).
　　　　　B.　This drawing is subject to change without notice.
　　△C　Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
　　△D　The 20 pin end lead shoulder width is a vendor option, either half or full width.

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MECHANICAL DATA

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
         D. Falls within JEDEC MO-150

TEXAS INSTRUMENTS

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FK (S−CQCC−N**)   LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.080\ (2,03)}{0.064\ (1,63)}$

$\frac{0.055\ (1,40)}{0.045\ (1,14)}$

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

$\frac{0.028\ (0,71)}{0.022\ (0,54)}$

0.050 (1,27)

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$
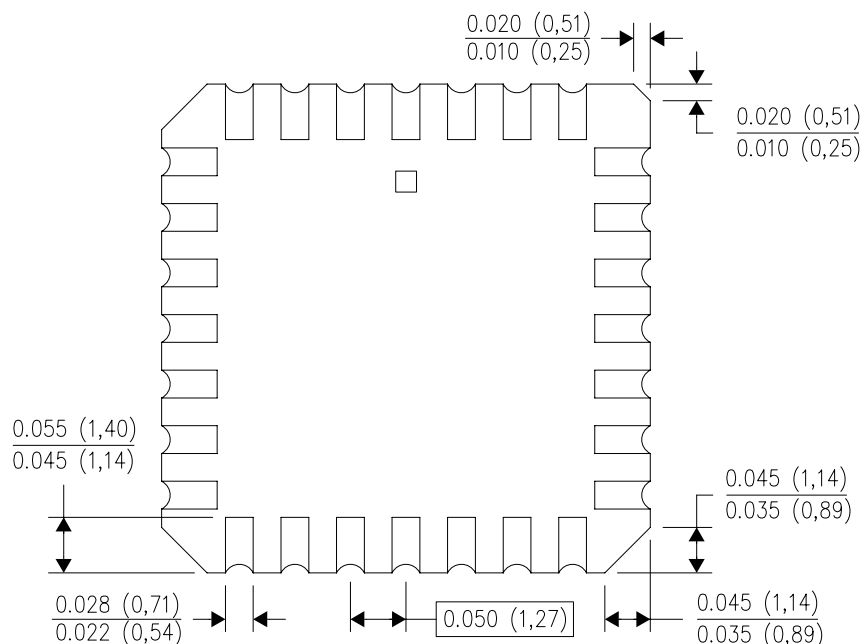
4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package can be hermetically sealed with a metal lid.
          D.   Falls within JEDEC MS−004

NS (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
            B. This drawing is subject to change without notice.
            C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14)   CERAMIC DUAL FLATPACK

Base and Seating Plane

0.045 (1,14) / 0.026 (0,66)

0.260 (6,60) / 0.235 (5,97)

0.080 (2,03) / 0.045 (1,14)

0.008 (0,20) / 0.004 (0,10)

0.280 (7,11) MAX

0.019 (0,48) / 0.015 (0,38)

0.050 (1,27)

0.390 (9,91) / 0.335 (8,51)

0.005 (0,13) MIN
4 Places

0.360 (9,14) / 0.250 (6,35)

0.360 (9,14) / 0.250 (6,35)

1   14   7   8

4040180–2/F 04/14

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only.
        E. Falls within MIL STD 1835 GDFP1–F14

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