HaoChen Yu

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Education

- **University of Chinese Academy of Sciences, Beijing, China** Aug 2022 - Present
  Masters in Electronic Engineering, expected June 2025, GPA: 3.66/4.0
  Courses: Computer Architecture, Soc Design, Very Large Scale Integration (VLSI) and System Design, Advanced Analog Integrated Circuits, Advanced Digital Integrated Circuits, Deep Learning, Digital Image Processing.
- **Nanjing University of Posts and Telecommunications, Nanjing, China** Aug 2018 - June 2022
  Bachelor of Electronic Engineering, GPA: 3.84/5.0
  Courses: Signals and Systems, Analog Electronics Circuits, Digital Circuits and Logic Design, Circuit Analysis Fundamentals, Semiconductor Physics, Photonics.

Research Experience

- **Institute of Microelectronics, Perception and Chip R&D Center**
  Master Student *Aug 2022 - Current*
  - **Micro UAV: Sound Source Localization and Multispectral Object Detection**: The UAV is equipped with an array of microphones and visible and far-infrared cameras. We implement noise reduction and sound source location algorithm based on microphone array. The reparameterization method is adopted to reduce the parameter requirements of object detection neural network and meet the computing power and real-time requirements of UAV platform. The multi-camera complementary redundant design and decision fusion method is used to improve the generalization ability of target detection network in practical application scenarios. (Autumn 2024)
  - **Robust RGB-T Object Detection**: We aim to present a robust multispectral object decision fusion method to perform effectively on both interference-free datasets and those affected by sensor interference or failure data. We incorporate evidential deep learning into one-stage object detection allowing the network to naturally express uncertainty in its predictions. Subsequently, quality-aware Generalized D-S evidence theory is employed to reassign background confidence within the belief framework, effectively addressing the one-vote veto problem commonly encountered in traditional D-S combination rules. (Summer 2024)
  - **4-Way Video Mosaicing Using FPGA**: A 4-way video Mosaicing based on heterogeneous FPGA, implemented through the DDR AXI interface provided by the development board, uses 3 frames of ping-pong buffering for each video stream. It can splice, rotate, and adjust the brightness of each video stream with different interfaces (2x HDMI, MIPI) and resolutions. (Summer 2022)
- **Department of Electronics and Optical Engineering**
  Undergraduate *Aug 2018 - June 2022*
  - **Sinusoidal Frequency Modulation and Controllable Distortion Teaching System**: Using electronic components, a controlled 1k-10k sinusoidal frequency modulation and various distortions as described in textbooks was achieved, and the switch between distortions and normal sinusoidal output was completed using relays. Finally, the FFT function was implemented using FPGA programming to test the waveform distortion degree, and an interface for external distortion testing was left. (Spring 2021)

Honors and Awards

- National Collegiate Embedded Chip and System Design Competition and Intelligent Interconnection Innovation Contest, National First Prize, 2020.
- 4th National Collegiate FPGA Innovation Design Competition, National Third Prize, 2020.
- TI Cup National Collegiate Electronic Design Contest, Jiangsu Province Second Prize, 2020.

Publications

- **Robust RGB-T Object Detection via Quality-aware Decision Fusion Based on Dempster-Shafer Theory (IEEE Transaction on Multimedia, Submitted: Under review)**: HaoChen Yu, Rui Luo, XiaoQin Wang, DingYi Wang, Qiang Li, ShuShan Qiao. (Sep 2024)

Other Information

- **Languages**: Chinese, English.
- **Programming**: Python, C, VerilogHDL.
- **Software**: Matlab, Vivado, Altium Designer, Cadence Allegro.
- **Hobbies**: Jogging, Cycling.