TC1 Is a common 16 Bit timer counter module support PWM Output waveform can be generated accurately. TC1 contain 1 More 16 Bit counter, waveform generation mode control unit, 2 Separate outputs and the comparison unit 1 Input capture unit. Simultaneously, TC1 With TC0 Common 10 Bit prescaler, can be used independently 10 Bit prescaler. The system clock prescaler clkio Or high-speed clock rcm2x (internal 32M RC Clock oscillator output rc32m of 2 Frequency) for frequency-dividing the count clock Clkt1 . Waveform generating mode generates the control unit controls the operation mode of the counter and comparing the output waveform. Depending on the mode of operation, a counter for counting each clock Clkt1 Cleared, incremented or decremented. Clkt1 It may be generated by an internal clock or an external clock source. When the count value of the counter TCNT1 It reached its maximum value (equal to the maximum value 0xFFFF Or a fixed value or output compare register OCR1A Or the input capture register ICR1 ,defined as TOP , The maximum value of the definition MAX When to distinguish), the counter is cleared or decremented. When the count value of the counter TCNT1

Reaches a minimum value (equal to 0x0000 ,defined as BOTTOM), The counter will be incremented by one operation. When the count value of the counter TCNT1 Arrivals OCR1A or OCR1B When, also referred to compare match, set or cleared by the output signal of the comparison
OC1A or OC1B To produce PWM Waveform. When the enable insertion of dead time, the dead time is set (DTR1 Count clock number corresponding to the register) will be inserted into the generated PWM Waveform. When the input capture function is turned on, i.e. the counter is activated to start or stop counting, ICR1 Register records the captured count values trigger period signal. Software by clearing COM1A / COM1B Bit close to zero OC1A / OC1B The waveform output, or set the respective trigger source, when a triggering event occurs automatically cleared by hardware COM1A / COM1B Bit to close OC1A / OC1B The waveform output.

Count clock can be internal or external clock source to generate, select, and divided by the selected frequency clock source located TCCR1B Register CS1 Control bits, see the detailed description TC0 with TC1 Prescaler section.

Length counter is 16 Bit, supporting bi-directional counter. I.e., Waveform generating mode by the operation mode counter is located TCCR1A with TCCR1B Register WGM1 Bit to control. Depending on the mode of operation, a counter for counting each clock Clkt1
Cleared, incremented or decremented. When an overflow occurs count Located TIFR1 Counter register overflow flag TOV1
Bit is set. When the interrupt is enabled may produce TC1 Counter overflow interrupt.

Count value output of the comparison unit TCNT1 And output compare register OCR1A with OCR1B The value, when TCNT1
equal OCR1A or OCR1B When referred to as Comparative match occurs, it is located TIFR1 Output compare flag register OCF1A or OCF1B Bit is set. When the interrupt is enabled may produce TC1 Output Compare match interrupt. It should be noted that, in the PWM Under work mode, OCR1A with OCR1B Register is double buffered. In the normal mode and
CTC Mode, double buffering function failure. When the count reaches maximum or minimum value of the buffer register is updated simultaneously comparing register OCR1A with OCR1B Go. See section describes the operating modes.

Waveform generator and comparator generates a mode control output waveform control pattern matching and Comparative counter overflow signal to generate an output waveform comparison OC1A with OC1B . DETAILED generation mode and the operation mode register, see section below. We should compare the output signal waveform OC1A with OC1B Corresponding to the output pin, the data direction register must be set to the output pin.

Operating mode

Timing counter 1 There are six different modes, including normal mode (Normal), Cleared on compare match (CTC) Mode, fast pulse width modulation (FPWM) Mode, a phase correction pulse width modulation (PCPWM) Mode, a phase correction pulse width modulation frequency (PFCPWM) Mode, and input capture (ICP)mode. Mode control bit is generated by the waveform
WGM1 [3: 0] To choose. This is described in detail below six modes. Since there are two separate output of the comparison unit, respectively "A" with "B" Represented by lowercase "X" To represent the two channel outputs the comparison unit.