TCCR1C -TC1 Control register C

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address: 0x82					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	FOC1A	FOC1B	DOC1B	DOC1A	DTEN1	-	-	-
R / W	W	W	R / WR /	WR / W		-	-	-

Bit	Name	description
7	FOC1A	Force Output Compare A . In non PWM Mode, the force output by comparing bits FOC1A write "1" The way to compare match. Forcing compare match will not set OCF1A Flag or reload or clear the timer, but the output pin OC1A Will be in accordance with COM1A It sets the appropriate update, just compare match had really happened. Work on PWM When mode, write TCCR1A Cleared when you want to register. Read FOC1A The return value is always zero.
6	FOC1B	Force Output Compare B . In non PWM Mode, the force output by comparing bits FOC1B write "1" The way to compare match. Forcing compare match will not set OCF1B Flag or reload or clear the timer, but the output pin OC1B Will be in accordance with COM1B It sets the appropriate update, just compare match had really happened. Work on PWM When mode, write TCCR1A Cleared when you want to register. Read FOC1B The return value is always zero.
5	DOC1B	TC1 Close control of the high output of the comparator is enabled. When set DOC1B Bit "1" It is triggered off the output comparison signal source OC1B It is enabled. When a trigger event occurs, the hardware is automatically cleared COM1B Position, close OC1B The waveform output. Software by setting COM1B Re-open PWM Output. When set DOC1B Bit "0" It is triggered off the output comparison signal source OC1B Prohibited.
4	DOC1A	TC1 Close control of the low output of the comparator is enabled. When set DOC1A Bit "1" It is triggered off the output comparison signal source OC1A It is enabled. When a trigger event occurs, the hardware is automatically cleared COM1A Position, close OC1A The waveform output. Software by setting COM1A Re-open PWM Output. When set DOC1A Bit "0" It is triggered off the output comparison signal source OC1A Prohibited.
3	DTEN1	TC1 Dead time enable control bit. When set DTEN1 Bit "1" When, enabling dead-time insertion. OC1A with OC1B They are in B Insertion of dead time waveform of the comparison output is generated based on the channel, inserted by the dead time interval DTR1 Register corresponding to the count time determined. OC1A The polarity of the output waveform COM1A with COM1B The correspondence between the decision, see OC1A After insertion of dead time waveform table shown polarity. When set DTEN1 Bit "0" Is prohibited dead-time insertion, OC1A with OC1B Comparing each of the generated output waveforms.
2: 0	-	Retention

The following table is a dead time enabled OC1A Polarity control signal output waveform.