SECTION 2
LGT8XM ARCHITECTURE

- Low Power Design
- High Efficency RISC Archatecture
- 16 Bit LD/ST Extension (Dedicated uDSU)
- 130 Instructions, Over 80% execute in a Single Cycle
- Embedded In-Circuit Debugger (OCD)

Overview

This section discusses the LGT8XM CPU architecture. The main function of the CPU is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.

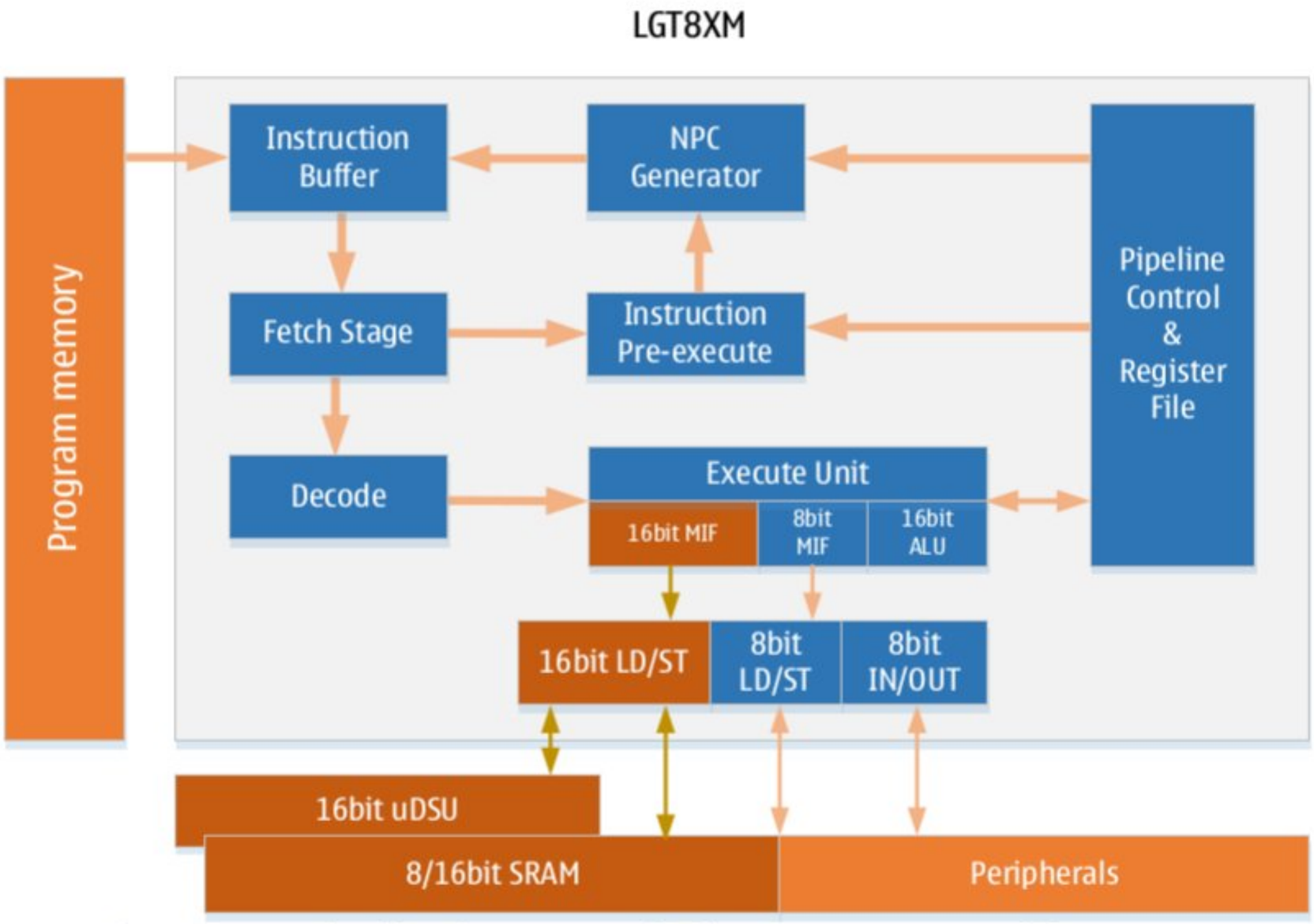

Figure 2. Block Diagram of the LGT8XM Architecture

The LGT8XM uses a Harvard like architecture – with separate buses for program and data. Instructions in program memory are executed with single level pipelining. While one instruction is being executed, the next instruction is prefetched from program memory. This concept enables instructions to be executed every clock cycle. The program memory is reprogrammable in circuit. The Register File contains 32 x 8-bit General Purpose Registers with single clock cycle access times. This allows single-cycle operation of the Arithmetic Logic Unit (ALU). In a typical ALU operation, two operands are fetched from the Register File, the operation is executed, and the result is pushed back in the Register File – in one CPU system clock cycle.