LD	Rd, Z +	Indirect load, the address is incremented	Rd ← (Z), Z ← Z + 1	None	1/2
LD	Rd, -Z	Address decrement, indirect load	Z ← Z - 1, Rd ← (Z)	None	1/2
LDD	Rd, Z + q Indirect with offset loading		Rd ← (Z + q)	None	1/2
LDS	Rd, k	Directly from SRAM Loaded	Rd ← (k)	None	2
ST	X, Rr	Indirect storage	(X) ← Rr	None	1
ST	X +, Rr	Indirect storage, address increment	(X) ← Rr, X ← X + 1	None	1
ST	-X, Rr	Address decrement, indirect storage	X ← X - 1, (X) ← Rr	None	1
ST	Y, Rr	Indirect storage	(Y) ← Rr	None	1
ST	Y +, Rr	Indirect storage, address increment	(Y) ← Rr, Y ← Y + 1	None	1
ST	-Y, Rr	Address decrement, indirect storage	Y ← Y - 1, (Y) ← Rr	None	1
STD	Y + q, Rr	Indirect storage tape offset	(Y + q) ← Rr	None	1
ST	Z, Rr	Indirect storage	(Z) ← Rr	None	1
ST	Z +, Rr	Indirect storage, address increment	(Z) ← Rr, Z ← Z + 1	None	1
ST	-Z, Rr	Address decrement, indirect storage	Z ← Z - 1, (Z) ← Rr	None	1
STD	Z + q, Rr	Indirect storage tape offset	(Z + q) ← Rr	None	1
STS	k, Rr	Directly to a memory SRAM in	(K) ← Rr	None	2
LPM		Spatial Data Loader	R0 ← (Z)	None	2
LPM	Rd, Z	Spatial Data Loader	Rd ← (Z)	None	2
LPM	Rd, Z +	Loader data, address increment	Rd ← (Z), Z ← Z + 1	None	2
LD	Rd, Z +	Indirect load, the address is incremented	Rd ← (Z), Z ← Z + 1	None	1
LD	Rd, -Z	Address decrement, indirect load	Z ← Z - 1, Rd ← (Z)	None	1
LDD	Rd, Z + q Indirect with offset loading		Rd ← (Z + q)	None	1
LDS	Rd, k	Directly from SRAM Loaded	Rd ← (k)	None	2
IN	Rd, P	Read Port	Rd ← P	None	1
OUT	P, Rr	Write port	P ← Rr	None	1
PUSH	Rr	Push	STACK ← Rr	None	1
POP	Rd	Pop	Rd ← STACK	None	1/2
SBI	P, b	Set up IO register	I / O (P, b) ← 1	None	1
CBI	P, b	Clear IO register	I / O (P, b) ← 0	None	1
LSL	Rd	Logical Shift Left	Rd (n + 1) ← Rd (n), Rd (0) ← 0	Z, C, N, V	1
LSR	Rd	Logical Shift Right	Rd (n) ← Rd (n + 1), Rd (7) ← 0	Z	1
ROL	Rd	Carry the left loop comprising	Rd (0) ← C, Rd (n + 1) ← Rd (n), C ← Rd (7)	Z	1
ROR	Rd	Rotate Right carry bit comprising	Rd (7) ← C, Rd (n) ← Rd (n + 1), C ← Rd (0)	Z	1
ASR	Rd	Arithmetic shift right	Rd (n) ← Rd (n + 1), n = 0: 6	Z	1
SWAP	Rd	Bit exchange	Rd (3: 0) ← Rd (7: 4), Rd (7: 4) ← Rd (3: 0) None		1
BSET	s	Status bit is set	SREG (s) ← 1	SREG (s)	1
BCLR	s	Status bit is cleared	SREG (s) ← 0	SREG (s)	1
BST	Rr, b	Storage to T Place	T ← Rr (b)	T	1
BLD	Rd, b	read out T Bit to register	Rd (b) ← T	None	1
SEC		We carry flag	C ← 1	C	1
CLC		Clear carry flag	C ← 0	C	1