	1	0	0	0	0	1	0	S	DA = NEG (DA)
	1	0	0	0	1	0	0	S	DA = DX ^ 2
	1	0	0	0	1	0	1	S	DA = DY ^ 2
	1	0	1	0	0	0	0	S	DA = ABS (DA)
	1	0	1	1	0	0	0	0	DA = DA / DY
	1	0	1	1	0	0	0	1	DA = DA / DY, DY = DA% DY
SHIFT	1	1	0	0	N3	N2	N1	N0	DA = DA << N
	1	1	S	1	N3	N2	N1	N0	DA = DA >> N

Description:

1. S Operation, it represents a signed arithmetic operation or an unsigned

2. S1 Show DX Whether as signed, S2 Show DY Whether it is a signed number

3. N3 ... 0 Is a four-digit shift can be achieved up to 15 Bit shift operation

4. - Represents the value of this bit is not insignificant, can be set 0 or 1 , Recommended setting 0

Register Definition

name	IO address	Functional Description
DCSR	0x20 (0x00)	uDSC Control Status Register
DSIR	0x21 (0x01) Arithmetic instruction register	
DSSD	0x22 (0x02) accumulator DSA of 16 Bit saturation operation result	
DSDX	0x10 (0x30) Operand DSDX, 16 Bit read and write access	
DSDY	0x11 (0x31) Operand DSDY, 16 Bit read and write access	
DSAL	0x38 (0x58)	32 Bit accumulator DSA [15: 0], 16 Bit read and write access
DSAH	0x39 (0x59)	32 Bit accumulator DSA [31:16], 16 Bit read and write access

DSCR - Control Status Register

DSCR - uDSC Control Status Register								
address: 0x20 (0x00)						Defaults: 0010_xxxx		
Bit	7	6	5	4	3	2	1	0
Name DSUEN		MM	D1	D0	- N		Z	C
R / W	R / W	R / W	R / W	R / W	- R / W		R / W	R / W

Bit	Name	description
7	DSUEN uDSC Enable control module; 1 = Enable, 0 = Disable	
6	MM	uDSC Register map mode; refer to the detailed definition 16 Introduction bit mode of operation. 0 = Fast access mode, 1 = IO Mapping mode
5	D1	Division operation completion flag, 1 = Operation completed
4	D0	In addition to division 0 Flag
3	-	Unimplemented
2	N	Operation result is negative flag
1	Z	Flag value to zero
0	C	32 Adder carry / borrow flag