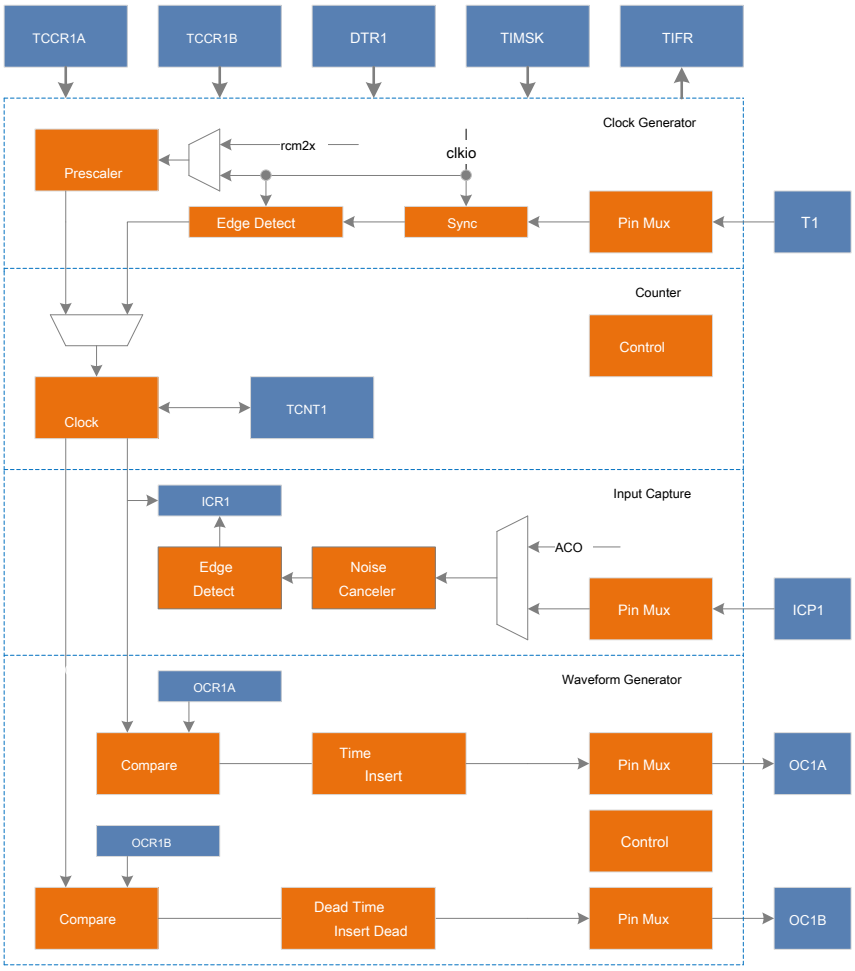
Timer / Counter 1 (TMR1)

- truly 16 Digital design, allowing 16 Bit PWM
- 2 Separate outputs the comparison unit
- Double buffered output compare register
- 1 Input capture unit
- Input Capture Noise Suppressor
- The counter is automatically cleared when compare match and automatically load
- No disturb pulse phase correction PWM
- Variable PWM cycle
- Frequency generator
- External event counter
- 4 Independent interrupt sources
- Support dead time control PWM
- 6 Selectable trigger source automatically shut down PWM Export
- Generating a high-resolution high-speed (high-speed clock mode @ 7BIT 500KHZ) the PWM

Outline



TC1 Structure chart