LGT8FX8P Series – Programming Manual 1.0.4J
Errata Page 15
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The second type of interrupts will continue to respond as long as the interrupt condition persists. This interrupt does not require an interrupt flag bit. If the interrupt condition disappears before the interrupt is enabled, the interrupt will not be triggered.

The second type of interrupts will trigger as long as the interrupt condition is present. These interrupts do not necessarily have Interrupt Flags. If the interrupt condition disappears before the interrupt is enabled, the interrupt will not be triggered.

The second type of interrupt is that the interrupt will continue to respond when the interrupt condition persists. This interrupt does not require an interrupt flag bit. If the interrupt condition disappears before the interrupt is enabled, the interrupt will not get a response.
第二种中断类型是当中断条件一直存在时,中断就一直响应。这种中断不需要中断标志位。如果中断条件在中断使能之前消失,这个中断将不会得到响应。

When the LGT8XM CPU exits from the interrupt service routine, the execution flow is returned to the main program. After executing one more instruction in the main program, it can respond to other pending interrupt requests.

When the AVR exits from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

When the LGT8XM core exits from the interrupt service routine, the execution flow is returned to the main program. After executing one or several instructions in the main program, it can respond to other pending interrupt requests.
Note: This is probably a translation issue with the phrase “one more” mistranslated as ‘one (and) more’ instead of ‘one-more,’ and is probably not an actual feature difference. I’m going with the “one” instruction statement.
当 LGT8XM 内核从中断服务子程序中退出后,执行流程会返回到主程序中。在主程序中执行一条或几条指令后,才能响应其他等待的中断请求。

It should be noted that the System Status Register (SREG) is not automatically saved after entering or returning from an interrupt routine. Managing the SREG must be handled in software.

Note that the Status Register is not automatically stored when entering an interrupt routine, nor restored when returning from an interrupt routine. This must be handled by software.

It should be noted that the System Status Register (SREG) is not automatically saved after entering the interrupt service and will not be automatically restored after returning from the interrupt service. It must be handled by the software.
需要注意的是,系统状态寄存器(SREG)在进入中断服务后并不会自动保存,也不会在从中断服务返回后自动恢复。它必须由软件负责处理。

The CLI command clears the Global Interrupt Flag (I) in SREG (Status Register). When interrupts are disabled using the CLI instruction, interrupts will be immediately disabled. Interrupts that occur after the CLI instruction will not get a response, nor will interrupts that occur simultaneously with the CLI instruction.

When using the CLI instruction to disable interrupts, the interrupts will be immediately disabled. No interrupt will be executed after the CLI instruction, even if it occurs simultaneously with the CLI instruction. The following example shows how this can be used to avoid interrupts during the timed EEPROM write sequence.

When the interrupt is disabled using the CLI instruction, the interrupt will be immediately disabled. Interrupts that occur after the CLI instruction will not get a response. Even interrupts that occur simultaneously with the execution of the CLI instruction will not be responded to. The following example shows how to use the CLI to avoid interrupts that interrupt the EEPROM write timing:
Note: rather comically this is an obvious copy and paste translation blunder. The Atmel datasheet has assembly and C code examples here that are the “following examples.” There is nothing whatsoever as far as examples in the LGT datasheet. I’m omitting their blunder. The LGT8FX328P doesn’t actually have EEPROM anyways only the 88P and 168P versions. I doubt anyone reading this is using these versions anyways.
当使用 CLI 指令禁止中断后,中断将会被立即禁止。在 CLI 指令之后发生的所以中断都不会得到响应。即使是和 CLI 指令执行时同时发生的中断,也不会被响应。下面的例子中说明如何利用 CLI 避免中断打乱 EEPROM 的写时序:

Interrupt response time 中断响应时间

*Any LGT8XM enabled interrupt will respond **within** 4 CPU clock cycles*. After these CPU clock cycles, the interrupt service routine enters the actual interrupt service routine. In these four clocks, the Program Counter value from before the interrupt is Pushed onto the Stack, and the system execution flow Jumps to the interrupt vector address and corresponding interrupt service routine. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served. If the interrupt occurs while the system is in sleep mode (SLEEP), the interrupt response requires an additional 4 clock cycles. This increase comes in addition to the start-up time from the selected sleep mode. For a detailed description of the sleep mode, please refer to the relevant chapter on power management.

The interrupt execution response for all the enabled AVR interrupts is four clock cycles minimum. After four clock cycles the program vector address for the actual interrupt handling routine is executed. During this four clock cycle period, the Program Counter is pushed onto the Stack. The vector is normally a jump to the interrupt routine, and this jump takes three clock cycles. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served. If an interrupt occurs when the MCU is in sleep mode, the interrupt execution response time is increased by four clock cycles. This increase comes in addition to the start-up time from the selected sleep mode.

The LGT8XM core is optimized for interrupt response so that any interrupt will respond within 4 system clock cycles. After 4 system clock cycles, the interrupt service routine enters the execution cycle. In these four clocks, the PC value before the interrupt is pushed onto the stack, and the system execution flow jumps to the interrupt vector corresponding interrupt service routine. If an interrupt occurs during the execution of a multi-cycle instruction, the kernel will ensure that the correct execution of the current instruction ends. If the interrupt occurs while the system is in Sleep (SLEEP), the interrupt response requires an additional 4 clock cycles. This increased clock period is

used to wake up the synchronization period of the operation from the selected sleep mode. For a detailed description of the sleep mode, please refer to the relevant chapter of power management.
NOTE: according to the LGT instruction set the JMP instruction takes less clock cycles than the Atmega (2 vs 3). I modified my text to say “”these” CPU clock cycles” instead of “within 4” as I am unable to test this at the moment.
LGT8XM 内核针对中断响应进行了优化,使得任何中断在 4 个系统时钟周期内一定得到响应。4 个系统时钟周期后,中断服务子程序进入执行周期。在这 4 个时钟内,中断之前的 PC 值被压入堆栈,系统执行流程流程跳转到中断向量对应中断服务程序。如果中断发生在一个多周期指令执行期间,内核将保证当前指令正确的执行结束。如果中断发生在系统处于休眠状态下(SLEEP),中断响应需要额外增加 4 个时钟周期。这增加的时钟周期用于从选择的休眠模式下唤醒操作的同步周期。休眠模式的具体描述,请参考功耗管理的相关章节。

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*It takes **2 clock cycles** to return from the interrupt service routine.* During these 2 clock cycles, the Program Counter (two bytes) is Popped back from the Stack, the Stack Pointer is incremented by two, and the I-bit in SREG is automatically set.

A return from an interrupt handling routine takes four clock cycles. During these four clock cycles, the Program Counter (two bytes) is popped back from the Stack, the Stack Pointer is incremented by two, and the I-bit in SREG is set.

It takes 2 clock cycles to return from the interrupt service routine. During these 2 clock cycles, the PC resumes from the stack, the stack pointer is incremented by 2, and the global interrupt control bit is automatically enabled.
从中断服务子程序中返回需要 2 个时钟周期。在这 2 个时钟周期内,PC 从堆栈中恢复,堆栈指针加 2,并自动使能全局中断控制位。