[7: 6]	-	Are reserved
5	HDR5	**PF5 Output driver control; 1 = 80mA drive, 0 = 12mA drive**
4	HDR4	**PF4 Output driver control; 1 = 80mA drive, 0 = 12mA drive**
3	HDR3	**PF2 Output driver control; 1 = 80mA drive, 0 = 12mA drive**
2	HDR2	**PF1 Output driver control; 1 = 80mA drive, 0 = 12mA drive**
1	HDR1	**PD6 Output driver control; 1 = 80mA drive, 0 = 12mA drive**
0	HDR0	**PD5 Output driver control; 1 = 80mA drive, 0 = 12mA drive**

Port multiplexing control register 0- PMX0

PMX0 - Port multiplexing control register 0								
PMX0: 0xEE				Defaults: 0x00				
Bit	WCE	C1BF4	C1AF5	C0BF3	C0AC0	SSB1	TXD6	RXD5
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
7	WCE	**PMX0 / 1 Update enable control; update PMX0 / 1 Before register, you need to write WCE Bit 1 , After the 6 Complete cycles of the systems PMX0 / 1 Updates.**						
6	C1BF4	OC1B Auxiliary output control **1 = OC1B Output to PF4 0 = OC1B Output to PB2**						
5	C1AF5	OC1A Auxiliary output control **1 = OC1A Output to PF5 0 = OC1A Output to PB1**						
4	C0BF3	OC0B Auxiliary output control **1 = OC0B Output to PF3 0 = OC0B Output to PD5**						
3	C0AC0	OC0A Auxiliary output control **0C0A Output from the C0AC0 Bits and TCCR0B Register C0AS Jointly control: {C0AC0, C0AS} = 00 = OC0A Output to PD6 01 = 0C0A Output to PE4 10 = 0C0A Output to PC0 11 = OC0A While the output to PE4 with PC0**						
2	SSB1	SPSS Auxiliary output control **1 = SPSS Output to PB1 0 = SPSS Output to PB2**						
1	TXD6	Serial ports TXD Auxiliary output control **1 = TXD Output to PD6 , 0 = TXD Output to PD1**						
0	RXD5	Serial ports RXD Auxiliary Input Control **1 = RXD Input from PD5 , 0 = RXD Input from PD0**						