TC0 Output Compare Register A- OCR0A

| address: | 0x47 | | | Defaults: 0x00 | | | | | | |
|----------|--------|---|--------|----------------|--------|--------|--------|--------|--|--|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Bit | OCR0A7 | OCR0A6 | OCR0A5 | OCR0A4 | OCR0A3 | OCR0A2 | OCR0A1 | OCR0A0 | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |
| | | | | | | | | | | |
| Bit | Name | description | | | | | | | | |
| 7: 0 O | CR0A | OCR0A It contains a 8 Bit data, with the counter value continuously TCNT0 Compare. Compare match can be used to generate an output compare interrupt, or to the OC0A Waveform generation pins. When PWM When mode, OCR0A Us double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR0A Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PV Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR0A When the buffer register, double buffering is disabled CPU Access is OCR0A itself. | | | | | | | | |

TC0 Output Compare Register B- OCR0B

| | | | OCROB - TCO | Output Compare | Register B | | | | | |
|----------|------------|--|-------------|----------------|------------|-----------|--------|-----|--|--|
| address: | 0x48 | | | Defaults: 0x00 | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Name | OCR0B7 OCR | 0B6 OCR0B | 5 OCR0B4 C | CR0B3 OC | R0B2 OCR0I | 31 OCR0B0 | R/WR/W | | | |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | | | | | | | | | | |
| Bit | Name | description | | | | | | | | |
| 7: 0 | OCROB | TC0 Output Compare B register. OCR0B It contains a 8 Bit data, with the counter value continuously TCNT0 Compare. Compare match can be used to generate an output compare interrupt, or to the OC0B Waveform generation pins. When PWM When mode, Ot Using double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR0B Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR0B When the buffer register, double buffering is disabled CPU Access is OCR0B itself. | | | | | | | | |