

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
\$5D	SPL	Stack Point Low							
\$5C	E2PD3	E2PCTL Data register byte 3							
\$5B	C1TR	AC1 trimming data							
\$5A	E2PD1	E2PCTL Data register byte1							
\$59	DSA[31:16]	DSA[31:16] access port of uDSC							
\$58	DSAL	DSA[15:0] access port of uDSC							
\$57	E2PD2	E2PCTL Data register byte 2							
\$56	ECCR	WEN	EEN	ERN	SWM	CP1	CP0	ECS1	ECS0
\$55	MCUCR	FWKEN	FPDEN	SWR	PUD	IRLD	IFAIL	IVSEL	WCE
\$54	MCUSR	SWDD	-	-	OCDRF	WDRF	BORF	EXTRF	PORF
\$53	SMCR	-	-	-	-	SM			SE
\$52	C0TR	AC0 Trimming register							
\$51	COXR	-	COOE	COHYSE	COP50	COWKE	COFEN	COFS1	COFS0
\$50	COSR	COD	COBG	COO	COI	COIE	COIC	COIS	
\$4F	DTR0	TC0 Dead-band timing control register							
\$4E	SPDR	SPI Data register							
\$4D	SPSR	SPIF	WCOL	-	-	-	DUAL	-	SPI2X
\$4C	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR	
\$4B	GPOR2	General Purpose Register 2							
\$4A	GPOR1	General Purpose Register 1							
\$49	TCCR0C	DSX07	DSX06	DSX05	DSX04	-	-	DSX01	DSX00
\$48	OCR0B	Timer 0 Output Compare Register B							
\$47	OCR0A	Timer 0 Output Compare Register A							
\$46	TCNT0	Timer 0 Counter							
\$45	TCCR0B	FOC0A	FOC0B	OC0A5	DTEN0	WGM02	CS02	CS01	CS00
\$44	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	DOC0B	DOC0A	WGM01	WGM00
\$43	GTCCR	TSM	-	-	-	-	-	PSRASY	PSRSYNC
\$42	EEARH	E2PCTL Address High							
\$41	EEARL	E2PCTL Address Low							
\$40	E2PD0	E2PCTL Data byte 0							
\$3F	EECR	EEPM2	EEPM2	EEPM1	EEPM0	EERIE	EEMWE	EEWE	EERE
\$3E	GPOR0	General Purpose Register 0							
\$3D	EIMSK	-	-	-	-	-	-	INT1	INT0
\$3C	EIFR	-	-	-	-	-	-	INTF1	INTF0
\$3B	PCIFR	-	-	-	-	PCIF3	PCIF2	PCIF1	PCIF0
\$3A	C1XR	-	C1OE	C1HYSE	C1PS0	C1WKE	C1FEN	C1FS1	C1FS0
\$39	SPFR	RDFULL	RDEMPT	RDPTR1	RDPTR0	WRFULL	WREMPT	WRPTR1	WRPTR0
\$38	TIFR3	-	-	ICF3	-	-	OCF3B	OCF3A	TOV3
\$37	TIFR2	-	-	-	-	-	OCF2B	OCF2A	TOV2
\$36	TIFR1	-	-	ICF1	-	-	OCF1B	OCF1A	TOV1
\$35	TIFR0	-	-	-	-	-	OCF0B	OCF0A	TOV0
\$34	PORTF	Port Output of Group F							