Port multiplexing control register 1- PMX1

			PMX1 - Port mi	ultiplexing contro	l register 1					
PMX1: 0xEI	D		Defaults: 0x00							
Bit	-	-	-	-	-	C3AC	C2BF7	C2AF6		
R/W	-	-	-	-	- R / W		R/W	R/W		
Bit Definitions										
[7: 3]	-	Are res	Are reserved							
		ОСЗА	OC3A Auxiliary output control							
2	C3AC	1 = O	1 = OC3A Output to QFP48 / AC0P 0 = OC3A Output							
		to PF1	to PF1							
		ОС2В	OC2B Auxiliary output control 1 = OC2B Output to PF7 0 =							
1	C2BF7	1 = O								
		OC2B	Output to PD3							
	C2AF6	OC2A	OC2A Auxiliary output control							
0		1 = O	1 = OC2A Output to PF6 0 =							
		OC2A	Output to PB3							
Instructions fo	r use									
PMX0 / 1 Sha	red register upd	ate the protection	n control bits PM	X0 [7], Update F	MX1 When, plea	se refer to PMX	0 Register on P	MX0 [7] The		
control instruc	tions.									

Port multiplexing control register 2 - PMX2

				PMX2 - Port m	ultiplexing contro	ol register 2					
PMX2: 0xF0	0				Defaults:	0x00					
Bit	WCE	STSC1		STSC0	-	-	XIEN	E6EN	C6EN		
R/W	R/W	R/W		R/W	-	- R / W		R/W	R/W		
Bit Definitions											
[7]	WCE		PMX2 Update enable control; update PMX2 Before register, you need to write WCE Bit 1 , After the 6 Complete cycles of the systems PMX2 Updates.								
[6]	STSC1		Fast Crystal IO Start-up circuit is controlled by PMCR After enabling high-speed oscillator, STSC1 Automatic enabled. When the system clock is switched to the external high speed oscillator, STSC1 Automatic clear. Software can also be stable in the crystal clear manual STSC1, Closed oscillator start-up circuit, save power.								
[5]	STSC0		Low-speed oscillator IO Start-up circuit is controlled by PMCR After low speed oscillator is enabled, STSC Automatically enabled. When the system clock is switched to the external low speed oscillator, STSCO Autolear. Software can also be stable in the crystal clear manual STSCO, Closed oscillator start-up circuit, save power.								
[4: 3]	-		Are reserved								
[2]	XIEN		Enable	external clock in	nput, you need to	o enable an exter	rnal crystal				
[1]	E6EN Er	nable Pl	E6 Unive	rsal IO Function	default PE6 for	AVREF Feature	s				
[0]	C6EN E	nable P	C6 Unive	ersal IO Function	; default PC6 E	xternal reset inpu	ıt				