Register Definition

GTCCR - General timer counter control register

GTCCR - General timer counter control register								
address: 0x43					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	TSM	-	-	-	-	-	PSRASY	PSRSYNC
R / W	R / W	-	-	-	-	- W		W

Bit	Name description	
7	TSM	Synchronous timing counter mode control bits. When set TSM Bit "1" When the timer counter is a synchronous mode. In synchronous mode, writing PSRASY Bit and PSRSYNC Bit value will remain, so that the corresponding prescaler has been reset. This ensures the appropriate timing counter and configured to abort the same value. When set TSM Bit "0" Time, PSRASY Bit and PSRSYNC Bit value will be cleared by hardware, and the timer counter and began to work.
6: 2	-	Reservations.
1	PSRASY See Timer TC2 Register description.	
0	PSRSYNC Prescaler CPS310 Reset control bits.	When set PSRSYNC Bit "1" When, prescaler CPS310 It will be reset. when TSM When the bit is not set, then the reset will clear the hardware PSRSYNC Bit. When set PSRSYNC Bit "0" When the setting is invalid. Multiplexing mode, TC0 / TC1 / TC3 Shared prescaler reset will affect the three timers. Stand-alone mode, the reset will only affect TC0 . Read this value will always be a "0" .

PSSR - Prescaler selection register

PSSR - Prescaler selection register								
address: 0xE2					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	PSS1	PSS3	-	-	-	-	PSR3	PSR1
R / W	R / W	R / W	-	-	-	- R / W		R / W

Bit	Name description	
7	PSS1	Prescaler select bit. When set PSS1 Bit "1" Time, TC1 Prescaler is used alone CPS1 . When set PSS1 Bit "0" When, for the prescaler multiplexed mode. TC0 with TC1 Shared prescaler CPS310 . Prescaler CPS1 Invalid, it will have to be reset. If the PSS3 Bit at the same time "0" , TC3 with TC0 , TC1 Shared prescaler CPS310 . Prescaler CPS1 with CPS3 They are invalid and will always be reset.
6	PSS3 Prescaler select bit.	When set PSS3 Bit "1" Time, TC3 Prescaler is used alone CPS3 .