32 A working register by 6 For paired together constituting a three 16 Bit registers, may be used for indirect addressing address pointers, and to access an external memory FLASH Program space. LGT8XM Single-cycle support 16 Bit arithmetic operations, greatly improves the efficiency of indirect addressing. LGT8XM These three special kernel 16 Bit registers is named X, Y, Z Register, will be described in detail later.

ALU Supported between the arithmetic logic operation between the register and the constant register, a single register may be operational in ALU In execution. ALU After the completion of the operation, the influence on the calculation result of the kernel state of the update to the state register (SREG) .

Program flow is controlled by conditional and unconditional jumps / call implementation, it can be addressed to the program area. most LGT8XM Instructions 16 Bit. Each corresponding to a program address space 16 Position or 32 Bit LGT8XM instruction.

After the kernel interrupt response or subroutine calls, the return address (PC) It is stored in the stack. Stack is allocated in the system general data SRAM And therefore limited only by the size of the stack system SRAM The size and usage. All applications support interrupt or subroutine call, you must first initialize the stack pointer register (SP) , SP able to pass IO Space access. data SRAM able to pass 5 Different addressing mode access. LGT8XM The internal storage space are mapped to a unified linear address space. For details, please refer to the introduction of the storage section.

LGT8XM A flexible core includes an interrupt controller, the interrupt function via a global state register interrupt enable bit. All interrupts have a separate interrupt vector. Interrupt priority and interrupt vector address corresponding relationship, the smaller the interrupt address, the higher the priority of the interrupt.

I / O Space contains 64 One can IN / OUT Instruction register direct addressing space. These control registers real kernel and the status register, SPI And other I / O Control function peripherals. This part of the space by IN / OUT Direct access instruction, the address may be mapped to the data memory space accessed through them (0x20 - 0x5F) . In addition, LGT8FX8P Also contains extended I / O Space, they are mapped to the data storage space 0x60 - 0xFF Here only use ST / STS / STD as well as LD / LDS / LDD Instruction accesses.

To enhance the LGT8XM Core computing power Instruction increased prevalence line 16 Bit LD / ST Extension. this 16 Place LD / ST Expand cooperation 16 Digital arithmetic acceleration unit (uDSU) Work to achieve efficient 16 Bit data operations. Concurrent kernel also increased RAM Spatial 16 Bit access capability. therefore 16 Place LD / ST Can be extended uDSU, RAM Transfer between the working register and 16 Bits of data. For details, refer " Digital arithmetic accelerator " chapter.

An arithmetic logic unit (ALU)

LGT8XM It contains an internal 16 Bit arithmetic logic unit, can be completed in one cycle 16 An arithmetic operation data. Efficient ALU versus 32 It is connected to general purpose working registers. To complete the arithmetic logic operation between the two registers or register with immediate data in one cycle. ALU Divided into three operations: arithmetic, logic, and bit operations. Simultaneously ALU Hardware multiplier section also includes a single-cycle can be achieved within a period of two 8 Direct register bit signed or unsigned operation. Refer to the instruction set of the detail portion.

Status Register (SREG)

Status register is mainly due to the implementation of the last preserved ALU Operation on the generated result information. The flow of information for controlling execution. It is a status register ALU Update operation is completely finished, so that the dispensed using a separate comparison instruction result is a more compact and efficient code. The status register does not automatically saved and restored in response to interrupts and exits from the interrupt, which requires software to be realized.