		ICR1 When, it should read ICR1L . When the input capture is triggered, the count value TCNT1 Will be updated to copy ICR1 Register. ICR1 Count register is also used to define the TOP value.

ICR1H -TC1 Input Capture MSB

ICR1H - TC1 Input Capture MSB								
address: 0x87					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	ICR1H7	ICR1H6	ICR1H5	ICR1H4	ICR1H3	ICR1H2	ICR1H1	ICR1H0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name description							
7: 0	ICR1H	TC1 Input capture high byte values. ICR1H with ICR1L Incorporated into the composition together 16 Bit ICR1 . Read and write 16 Bit register requires two operations. write 16 Place ICR1 When, you should write ICR1H . read 16 Place ICR1 When, it should read ICR1L . When the input capture is triggered, the count value TCNT1 Will be updated to copy ICR1 Register. ICR1 Count register is also used to define the TOP value.						

OCR1AL -TC1 Output Compare Register A Low byte

OCR1AL - TC1 Output Compare Register A Low byte								
address: 0x88					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR1AL7	OCR1AL6	OCR1AL5	OCR1AL4	OCR1AL3	OCR1AL2	OCR1AL1	OCR1AL0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name description							
7: 0	OCR1AL	Output Compare Register A The low byte. OCR1AL with OCR1AH Incorporated into the composition together 16 Bit OCR1A . Read and write 16 Bit register requires two operations. write 16 Place OCR1A When, you should write OCR1AH . read 16 Place OCR1A When, it should read OCR1AL . OCR1A Continuously with the counter value TCNT1 Compare. Compare match can be used to generate an output compare interrupt, or to the OC1A Waveform generation pins. When PWM When mode, OCR1A Using double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR1A Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR1A When the buffer register, double buffering is disabled CPU Access is OCR1A itself.							