Register Definition

SPI Register List

register	address	Defaults	description
SPCR	0x4C	0x00	SPI Control register
SPSR	0x4D	0x00	SPI Status Register
SPDR	0x4E	0x00	SPI Data register
SDFR	0x39	0x00	SPI Buffer

SPCR - SPI Control register

SPCR - SPI Control register								
address: 0x4C					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	SPIE	SPI Interrupt enable bit. When set SPIE Bit "1" Time, SPI Interrupt is enabled. When located SPSR Register SPIF When the bit is set and the Global Interrupt Enable, generated SPI Interrupted. When set SPIE Bit "0" Time, SPI Interrupts are disabled.
6	SPE	SPI Enable. When set SPE Bit "1" Time, SPI Module is enabled. Any SPI Must be set before the operation SPE . When set SPE Bit "0" Time, SPI Module is disabled.
5	DORD	Control data order bits. When set DORD Bit "1" , The data LSB Sent first. When set DORD Bit "0" , The data MSB Sent first.
4	MSTR	Master Slave selection control bits. When set MSTR Bit "1" When the master mode is selected. When set MSTR Bit "0" When the slave mode is selected. Host mode, SPSS Pin configured as an input and is driven low, MSTR Bit will be cleared, located SPSR Register SPIF Is set, the user must reset MSTR Enter host mode.
3	CPOL	Clock polarity control bit. When set CPOL Bit "1" When the idle state SPCK High. When set CPOL Bit "0" When the idle state SPCK Low.

CPOL	Starting along	Trailing Edge
0	Rising	Falling
1	Falling	Rising

Bit	Name	description
2	CPHA	Clock phase control bit. When set CPHA Bit "1" When, starting in the data set, an end edge sample data. When set CPHA Bit "0" When, a start edge sample data, setting data end edge.

CPHA	Starting along	Trailing Edge