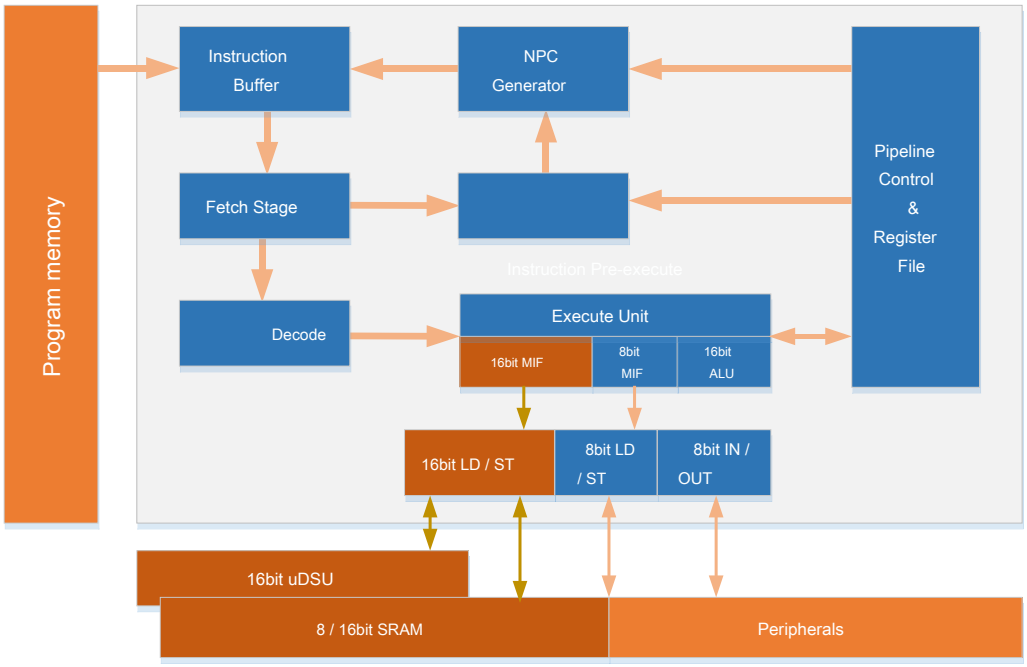
LGT8XM Kernel

- Low-power design
- high efficiency RISC Architecture
- 16 Place LD / ST Extension (uDSU dedicated)
- 130 Instructions, which 80% More than a single cycle
- Embedded In-Circuit Debugger (OCD) stand by

Outline

This chapter describes LGT8XM Core architecture and function. The kernel is MCU Brain, responsible for ensuring the correct implementation of the program, so the kernel must be able to perform accurate calculations, control peripherals and handle a variety of interrupts.

LGT8XM Kernel structure



In order to achieve greater efficiency and parallelism, LGT8XM Core uses Harvard architecture - Separate program and data buses. Through an optimized two instruction execution pipeline, the pipeline two pipeline is possible to reduce the number of invalid instructions, reduces the FLASH Views program memory, thus reducing power consumption of the core operation. Simultaneously LGT8XM Increased core before the instruction cache fetch stage (this can be cached simultaneously 2 Instructions), by the pre-execution module instruction fetch cycle further reduces the FLASH Program memory access frequency; by extensive testing, LGT8XM Can be reduced by about architecture than other similar kernel 50% Correct FLASH Access, greatly reducing the operating power consumption of the system.

LGT8XM Kernel has 32 More 8 General purpose working registers bit high-speed access (Register file) , Contributes to a single cycle of arithmetic and logic (ALU) . Under normal circumstances, ALU Two operands from the arithmetic average of general purpose working registers, ALU The result of the operation also written to the register file in one cycle.