16. SPI – Serial Peripheral Interface

16.1 Features

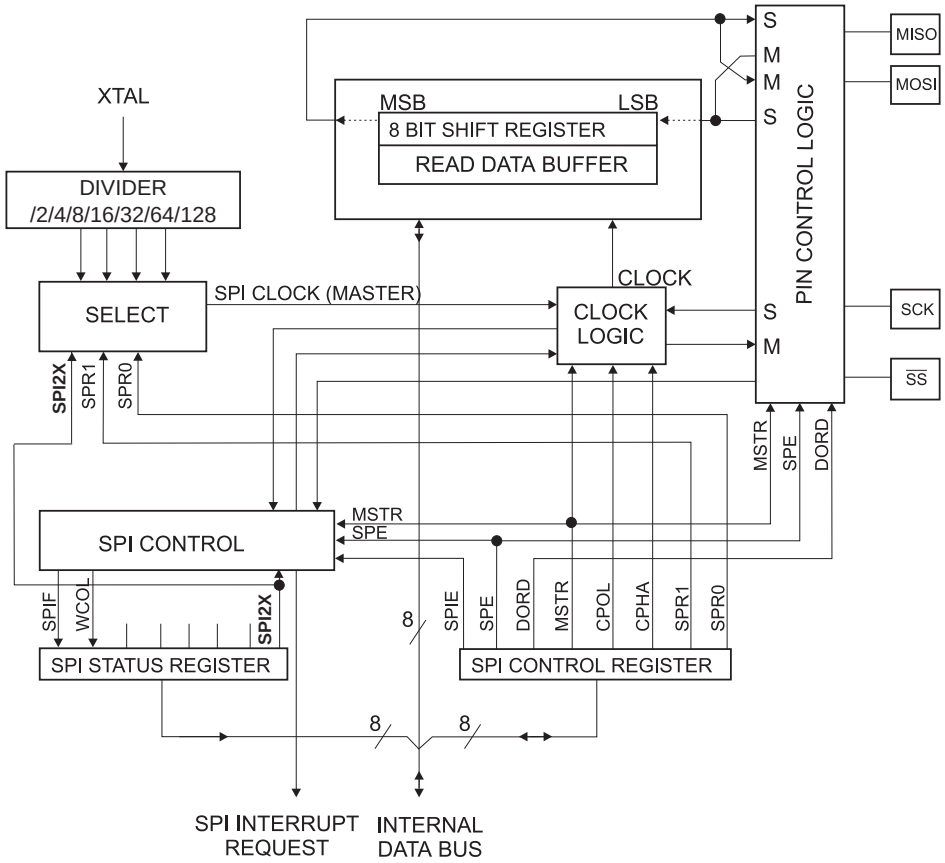
- **Full-duplex, Three-wire Synchronous Data Transfer**
- **Master or Slave Operation**
- **LSB First or MSB First Data Transfer**
- **Seven Programmable Bit Rates**
- **End of Transmission Interrupt Flag**
- **Write Collision Flag Protection**
- **Wake-up from Idle Mode**
- **Double Speed (CK/2) Master SPI Mode**

16.2 Overview

The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between the ATmega48P/88P/168P/328P and peripheral devices or between several AVR devices.

The USART can also be used in Master SPI mode, see “USART in SPI Mode” on page 204. The PRSPI bit in ”Minimizing Power Consumption” on page 42 must be written to zero to enable SPI module.

Figure 16-1. SPI Block Diagram[1]



Note: 1. Refer to Figure 1-1 on page 2, and Table 11-3 on page 82 for SPI pin placement.