## ATmega48P/88P/168P/328P

```
.org 0x3C00
0x3C00
       RESET: ldi
                      r16, high (RAMEND); Main program start
0x3C01
                      SPH,r16
                                      ; Set Stack Pointer to top of RAM
               out
0x3C02
               ldi
                      r16, low(RAMEND)
0x3C03
               out
                      SPL, r16
0x3C04
                                      ; Enable interrupts
               sei
0x3C05
               <instr> xxx
```

When the BOOTRST Fuse is programmed, the Boot section size set to 2K bytes and the IVSEL bit in the MCUCR Register is set before any interrupts are enabled, the most typical and general program setup for the Reset and Interrupt Vector Addresses in ATmega328P is:

```
Address Labels Code
                                       Comments
.org 0x3C00
0x3C00
                                        ; Reset handler
                jmp
                       RESET
0x3C02
                                        ; IRQ0 Handler
                jmp
                       EXT_INT0
0x3C04
                jmp
                       EXT_INT1
                                        ; IRQ1 Handler
                . . .
                       . . .
0x3C32
                       SPM_RDY
                                        ; Store Program Memory Ready Handler
                qmr
;
0x3C33
        RESET: ldi
                       r16, high (RAMEND); Main program start
0x3C34
                       SPH,r16
                                        ; Set Stack Pointer to top of RAM
                out.
0x3C35
                ldi
                       r16, low(RAMEND)
0x3C36
                out
                       SPL, r16
0x3C37
                sei
                                       ; Enable interrupts
0x3C38
                <instr> xxx
```

### 9.5 Register Description

# 9.5.1 Moving Interrupts Between Application and Boot Space, ATmega88P, ATmega168P and ATmega328P The MCU Control Register controls the placement of the Interrupt Vector table.

### 9.5.2 MCUCR – MCU Control Register

Bit	7	6	5	4	3	2	1	0	_
0x35 (0x55)	-	BODS	BODSE	PUD	-	-	IVSEL	IVCE	MCUCR
Read/Write	R	R	R	R/W	R	R	R/W	R/W	-
Initial Value	0	0	0	0	0	0	0	0	

#### • Bit 1 – IVSEL: Interrupt Vector Select

When the IVSEL bit is cleared (zero), the Interrupt Vectors are placed at the start of the Flash memory. When this bit is set (one), the Interrupt Vectors are moved to the beginning of the Boot Loader section of the Flash. The actual address of the start of the Boot Flash Section is determined by the BOOTSZ Fuses. Refer to the section "Boot Loader Support – Read-While-Write Self-Programming, ATmega88P, ATmega168P and ATmega328P" on page 277 for details. To avoid unintentional changes of Interrupt Vector tables, a special write procedure must be followed to change the IVSEL bit:

