

**SREG REGISTER DEFINITION**

SREG System Status Register								
Address: <b>0X3F (0X5F)</b>				Defaults: <b>0X00</b>				
Bit	7	6	5	4	3	2	1	0
Name	I	T	H	S	V	N	Z	C
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Definition								
[0]	C	Carry flag, indicating that the arithmetic or logic operation caused the carry. *						
[1]	Z	A zero flag indicating that the result of an arithmetic or logical operation is zero. *						
[2]	N	A negative flag indicates that an arithmetic or logic operation has produced a negative number. *						
[3]	V	The overflow flag indicates that the result of the two's complement operation has overflowed. *						
[4]	S	Sign bit, equivalent to the XOR operation result of N and V *						
[5]	H	Semi-carry flag, useful in BCD operations, indicating the semi-carry generated by byte operations*						
[6]	T	For temporary bits, bit copy (BLD) and bit store (BST) instructions, the T bit is used as a temporary memory bit to temporarily store the value of a bit in the general purpose register. *						
[7]	I	The global interrupt enable bit must be set to 1 to enable the core to respond to interrupt events. Different interrupt sources are controlled by independent control bits. The global interrupt enable bit is the last barrier that controls the interrupt signal into the core. The I bit is automatically cleared by the hardware after the core responds to the interrupt vector and is automatically set after the interrupt return instruction (RETI) is executed. The I bit can also be changed using the SEI and CLI instructions. *						

\* Please refer to the instruction description for details.

**GENERAL WORKING REGISTER**

The general purpose working registers are optimized according to the LGT8XM instruction set architecture. To achieve the efficiency and flexibility required for core execution, the LGT8XM's internal working registers support several access modes:

- An 8-bit read and an 8-bit write simultaneously
- Two 8-bit reads simultaneously with an 8-bit write
- Two 8-bit reads simultaneously one 16-bit write
- One 16-bit read and one 16-bit write simultaneously