		When using the double buffering feature CPU Access is OCR3B When the buffer register, double buffering is disabled CPU Access is OCR3B itself.

OCR3CL-TC3 Output Compare Register C Low byte

OCR3CL - TC3 Output Compare Register C Low byte								
address: 0x9E					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OCR3CL7	OCR3CL6	OCR3CL5	OCR3CL4	OCR3CL3	OCR3CL2	OCR3CL1	OCR3CL0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name description							
7: 0	OCR3CL	Output Compare Register C The low byte. OCR3CL with OCR3CH Incorporated into the composition together 16 Bit OCR3C . Read and write 16 Bit register requires two operations. write 16 Place OCR3C When, you should write OCR3CH . read 16 Place OCR3C When, it should read OCR3CL . OCR3C Continuously with the counter value TCNT3 Compare. Compare match can be used to generate an output compare interrupt, or Used in OC3C Waveform generation pins. When PWM When mode, OCR3C Using double buffered registers. The normal mode and clear mode match , The double buffering is disabled. Double buffering may be updated OCR3C The count register with the maximum or minimum time Step up, thereby preventing the generation of asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR3C When the buffer register, double buffering is disabled CPU Access is OCR3C itself.							

OCR3CH-TC3 Output Compare Register C High Byte

OCR3CH - TC3 Output Compare Register C High Byte								
address: 0x9F					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OCR3CH7	OCR3CH6	OCR3CH5	OCR3CH4	OCR3CH3	OCR3CH2	OCR3CH1	OCR3CH0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	OCR3CH	Output Compare Register C The high byte. OCR3CL with OCR3CH Incorporated into the composition together 16 Bit OCR3C . Read and write 16 Bit register requires two operations. write 16 Place OCR3C When, you should write OCR3CH . read 16 Place OCR3C When, it should read OCR3CL . OCR3C Continuously with the counter value TCNT3 Compare. Compare match can be used to generate an output compare interrupt, or Who used to OC3C Waveform generation pins. When PWM When mode, OCR3C Using double buffered registers. The normal mode and clear mode match , The double buffering is disabled. Double buffering may be updated OCR3C Register with the maximum or minimum counting time Synchronize, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR3C When the buffer register, double buffering is disabled CPU Access is OCR3C itself.							

DTR3L-TC3 Dead Time Register Low Byte

DTR3L - TC3 Dead Time Register Low Byte	
address: 0x9C	Defaults: 0x00