Out will remain low or high. If you use OCR3A As a TOP And set COM3A = 1 , The comparator output signal
OC3A It will have a duty cycle of 50% of PWM wave.

In order to ensure that the output PWM Wave BOTTOM Symmetry on both sides, a compare match does not occur, there will be two cases flipping OC3x signal. The first case is when OCR3x The value of the TOP When changes to other data. when OCR3x
for TOP , The count value reaches TOP Time, OC3x The same output result of the comparison in the previous match count in descending, i.e. holding OC3x constant. At this value will be updated relatively new OCR3x The value of the (non TOP), OC3x Value will remain set until the comparison match occurs ascending counting flip. at this time OC3x Signal to the minimum value as the center is not symmetrical, requiring the TCNT3
Flip reaches the maximum value OC3x Signal, namely when the comparator inverting no match occurs OC3x A first of the signal. The second case is when TCNT3 From the ratio OCR3x Counting high value, and thus will miss the compare match, thereby causing an asymmetric situation generated. Also you need to flip OC3x Signal to achieve symmetry of both sides of the minimum.

Phase frequency correction PWM mode

When set WGM3 [3: 0] = 8 or 9 When the timer counter 1 Into the phase frequency correction PWM Max mode, counting
TOP Respectively ICR3 or OCR3A . Bidirectional counter operation by BOTTOM Increments to TOP And then descending to
BOTTOM , Then repeat this operation. Count reaches TOP with BOTTOM Have to change direction when the count value TOP or
BOTTOM On average only stay a count clock. In the process increments or decrements the count value TCNT3 versus OCR3x Match, the comparison signal output OC3x It will be set or cleared, depending on the comparison output mode COM3 setting. Compared with the one-way operation, bidirectional operation obtainable maximum operation frequency, but its excellent symmetry is more suitable for motor control.

Phase frequency correction PWM Mode, when the count reaches BOTTOM When set TOV3 Flag, and comparing the value of the buffer to update the comparison value, the comparison value is updated frequency correction phase PWM And a phase correction mode PWM The biggest difference mode. If enabled, the interrupt service routine can be updated relatively buffer OCR3x Register. when CPU change TOP That value OCR3A or ICR3 When the value, you must ensure that the new TOP Value is not less than the already in use TOP Value, or compare match will not happen again.

Set up OC3x Pin data direction register as an output a comparison signal to obtain an output OC3x Waveform. Frequency of the waveform following formula can be calculated:

$$f_{OC3xcpfcpwm} = f_{sys} / (N * TOP * 2)$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024).

In up-counting process, when TCNT3 versus OCR3x Match, the waveform generator will be cleared (set) OC3x signal. In the process of counting down, when TCNT3 versus OCR3x When the match is set to the waveform generator (clear) OC3x signal. thus OCR3x The extremes will produce a special PWM wave. when OCR3x Set as TOP or BOTTOM Time, OC3x Output signal will remain low or high. If you use OCR3A As a TOP And set COM3A = 1 , The comparator output signal
OC3A It will have a duty cycle of 50% of PWM wave.

because OCR3x Register in BOTTOM Time updates, so TOP Value count ascending and descending on both sides are the same length, it generates the correct frequency and phase are symmetrical waveform.

When using a fixed TOP Value, is preferably used ICR3 Register as a TOP Value, that is set WGM3 [3: 0] = 8 ,at this time
OCR3A Only register used to generate PWM Output. If you want to generate a frequency change PWM Wave, must change TOP value, OCR3A Double buffering characteristics would be more suitable for this application.