Dead time enabled mode OC1A Polarity control signal output waveform

DTEN1	COM1A [1: 0]	COM1B [1: 0]	description			
0	-	-	OC1A Signal polarity by the OC1A Compare output mode control			
1	0	-	OC1A Disconnect, GM IO Port operations			
1	1	-	Retention			
1	2	2	OC1A Signals OC1B Signals with the same polarity			
		3	OC1A Signals OC1B Opposite signal polarity			
1	3	2	OC1A Signals OC1B Opposite signal polarity			
		3	OC1A Signals OC1B Signals with the same polarity			

## [note] :

OC1B The polarity of the signal output from the waveform OC1B Compare output control mode, so that the same can not dead time mode.

TCCR1D -TC1 Control register D

			TCCR1D -	TC Control regis	ter D							
address: 0	x83				Defaults: 0	x00						
Bit	7	6	5	4	3	2	1	0				
	DSX17 DS	DSX17 DSX16 DSX15 DSX14			-	-	DSX11 DSX10					
R/WR	/ W	R/W	R/W	R/W	-	- R / W		R/W				
Bit	Name descri	ption						·				
7	DSX17	output of the enabled. we Rising edg	TC1 Select the trigger source control enables the first 7 Bit. When set DSX17 Bit "1" Time, TC0 As the output of the comparator is off the overflow signal waveform OC1A / OC1B The trigger source is enabled. when DOC1A / DOC1B Bit "1"  Rising edge triggered interrupt source, the selected flag register bits will automatically shut down  OC1A / OC1B The waveform output. When set DSX17 Bit "0" Time, TC0 As the output of the comparator is off the overflow signal waveform OC1A / OC1B The trigger source is prohibited.									
6	DSX16	output of the enabled. we Rising edg	TC1 Select the trigger source control enables the first 6 Bit. When set DSX16 Bit "1" Time, TC2 As the output of the comparator is off the overflow signal waveform OC1A / OC1B The trigger source is enabled. when DOC1A / DOC1B Bit "1"  Rising edge triggered interrupt source, the selected flag register bits will automatically shut down  OC1A / OC1B The waveform output. When set DSX16 Bit "0" Time, TC2 As the output of the comparator is off the overflow signal waveform OC1A / OC1B The trigger source is prohibited.									
5	DSX15	a comparis	TC1 Select the trigger source control enables the first 5 Bit. When set DSX15 Bit "1" When, pin change 1 A a comparison output signal waveform is off OC1A / OC1B The trigger source is enabled. when DOC1A / DOC1B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC1A / OC1B The waveform output. When set DSX15 Bit "0" When, pin change 1 As a comparison output signal waveform is off OC1A / OC1B The trigger source is prohibited.									
4	DSX14	interrupt 1	TC1 Select the trigger source control enables the first 4 Bit. When set DSX14 Bit "1" When the external interrupt 1 As a comparison output signal waveform is off OC1A / OC1B The trigger source is enabled. when DOC1A / DOC1B Bit									