<table>
<tr><td></td><td></td><td>When set WDIE Bit "0" Time, WDT Interrupts are disabled.
WDIE Bit and WDE Together determine the watchdog-bit mode, as shown in the following table.
<table><tr><th>WDE</th><th>WDIE</th><th>mode</th><th>After the action overflow</th></tr><tr><td>0</td><td>0</td><td>stop</td><td>no</td></tr><tr><td>0</td><td>1</td><td>Interrupt Mode</td><td>Interrupt</td></tr><tr><td>1</td><td>0</td><td>Reset mode</td><td>Reset</td></tr><tr><td>1</td><td>1</td><td>Reset interrupt Reset Mode</td><td>Interrupt</td></tr></table></td></tr>
<tr><td>[5]</td><td>WDP3</td><td>WDT Prescale factor selection control section 3 Bit.
WDP [3] with WDP [2: 0] composition WDT Select bit prescale factor WDP [3: 0] , To set WDT The time-out period.</td></tr>
<tr><td>[4]</td><td>WDTOE</td><td>WDT Close enable control bit. When should WDE When cleared, WDTOE Bit to be set, otherwise WDT It will not be closed. when WDTOE After the bit is set, hardware will 4 After four clock cycles cleared WDTOE Bit.</td></tr>
<tr><td>[3]</td><td>WDE</td><td>WDT Enable control bit.
When set WDE Bit "1" Time, WDT It is enabled. When set WDE Bit "0" Time,
WDT Prohibited. only at WDTOE When the bit WDE In order to be cleared. To turn has enabled the

WDT , Must operate in accordance with the following sequence:
1. At the same time set WDTOE with WDE Bit, even if WDE It has been set in the closed
Before beginning operation also must WDE Bit is written "1" ;
2. In the following 4 Clock cycles, for WDE Bit is written "0" . This turns off
WDT . when WDE Bit "1" And WDT Overflow bit is set and reset WDT Reset system flag WDRF (lie in MCUSR register). when WDRF Will be set when the bit in the set state WDE Bit. So to be cleared WDE Bit must be cleared WDRF Bit.</td></tr>
<tr><td>[2: 0]</td><td>WDP</td><td>WDT Prescale factor selection control.
To set WDT The time-out period. Recommended WDT When the count is not changed WDP Values change during the counting WDP The value will produce unpredictable WDT overflow.</td></tr>
</table>

Watchdog prescaler selection list:

WDP3	WDP2	WDP1	WDP0	Watchdog timer overflow number of cycles	32KHz clock	2MHz clock
0	0	0	0	2K cycles	64ms	1ms
0	0	0	1	4K cycles	128ms	2ms
0	0	1	0	8K cycles	256ms	4ms
0	0	1	1	16K cycles	512ms	8ms
0	1	0	0	32K cycles	1s	16ms
0	1	0	1	64K cycles	2s	32ms
0	1	1	0	128K cycles	4s	64ms
0	1	1	1	256K cycles	8s	128ms
1	0	0	0	512K cycles	16s	256ms
1	0	0	1	1024K cycles	32s	512ms