To clear the global interrupt flag and ban SPI All interrupts.

During reinitialization or a frame structure such as changing the baud rate, must ensure that no data transmission. TXC Flag may be used to detect whether or not the sender all the transmission, RXC Flag may be used to detect whether there is data in the receive buffer is not read. in case TXC Flag used for this purpose, before each transmission of data (write UDR Before register) must be cleared TXC Flag.

initialization SPI Later, to UDR Write data register to start data transfer. Since the transmitter controlling the transmission clock, data transmission and reception operation is true. When the transmit shift register is ready to transmit a new data, the transmitter will be written to the UDR Register data move buffer from the transmission in the transmit shift register and transmitted. In order to ensure synchronous transmission data input buffer and, after the transmission of each byte of data must be read once UDR register. When the data overflow occurs, the most recently received data will be lost, not the data was first received.

Send Flags and Interrupts

SPI Transmitter has two flags: SPI Data register empty flag UDRE And the transmission end flag TXC , Two flags can generate interrupts.

Data register empty flag UDRE It is used to indicate whether the transmit buffer to write a new data. This bit is set when the transmit buffer is empty "1" Full time is set "0" . when UDRE Bit "1" Time, CPU Data can go register UDR Write new data, not vice versa.

when UCSRB Data register empty interrupt enable register bit UDRIE for "1" When, as long as UDRE Is set (and global interrupts are enabled), will produce SPI Data Register empty interrupt request. To register UDR The write operation will be cleared
UDRE . When the interrupt transmission of data in the data register empty interrupt service routine must write new data to a UDR To clear UDRE , Or disable the Data Register Empty interrupt. Otherwise, if the interrupt service routine ends, a new interrupt will occur again.

When the entire data frame is sent out of the shift register while the register and no new transmission data, the transmission end flag TXC It will be set.
when UCSRB Send the end of last interrupt enable bit TXCIE (And the Global Interrupt Enable) "1" When, as TXC Flag is set, SPI Transmit Complete Interrupt will be executed. Once in the interrupt service routine, TXC Flag, this is automatically cleared, CPU This bit can also write "1" Cleared.

Disable the transmitter

when TXEN When cleared, and all the data only after the completion of transmission the transmitter can really disabled, i.e., the transmit shift register and the transmit data buffer register are not to be transmitted. Transmitter disabled later, TxD Pin restore its versatility
IO Features.

Reception complete flag and interrupt

SPI The receiver has a flag: Reception complete flag RXC , To indicate whether or not the data read out of the receive buffer. When the receive buffer data is not read, this bit "1" , Otherwise "0" . If the receiver is disabled, the receive buffer will be flushed, RXC It will be cleared. Position UCSRB Receive Complete Interrupt Enable bit RXCIE After long RXC Flag is set (provided that global interrupts are enabled), it will have SPI Receive Complete interrupt. When interrupt-driven data reception, data reception from the end of the interrupt service routine must UDR Read data cleared RXC Logo, or as long as