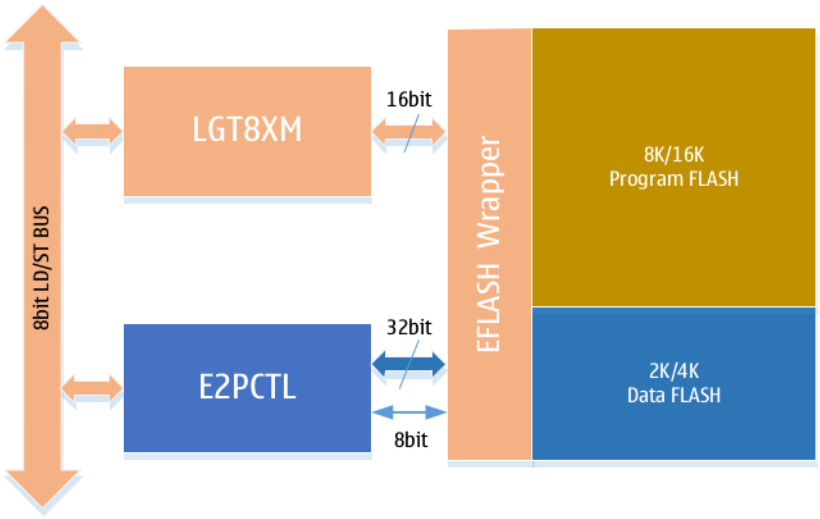
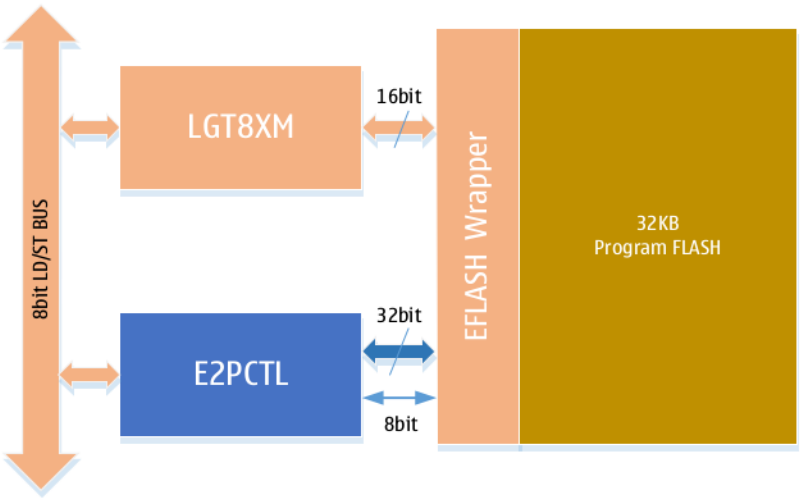
LGT8F88D/168D E2PCTL Controller Block Diagram



When the E2PCTL is in the emulated E2PROM mode, it supports 8-bit and 32-bit read/ write widths. It supports 32-bit read/write when accessing the FLASH Program Memory. The entire EFLASH Memory of the LGT8FX8P is mapped as 32 bits*. Therefore it is recommended to use 32-bit access, especially for programming operations. The 32-bit read and write operation is more efficient, and also helps ensure the erasing cycle life of the FLASH memory.*

LGT8F328P E2PCTL Controller Block Diagram



The entire Program Memory is monolithically integrated inside the LGT8F328P. The LGT8XM architecture in ***the LGT8F328P shares the internal 32K bytes of EFLASH memory with the emulated E2PROM****. Users can partition the 32K byte EFLASH Memory into separate Program Memory and emulated E2PROM Memory according to their needs.* ***By configuring the E2PCTL settings, you can adjust the partition size of the emulated E2PROM****.* ***The emulated E2PROM is implemented using a 1K byte page swap mode****. For instance, to simulate 1K bytes of E2PROM space, the E2PCTL controller requires 2K bytes of FLASH space. In this example a 1K byte page has programmed data. In order to erase or write changes an additional 1K byte page is required to make a page swap. Likewise, to achieve 4K bytes of E2PROM, 8K bytes of FLASH Program Memory are partitioned and reserved for E2PROM. For more information, please refer to the E2PCTL Algorithm Implementation description.*