R / W	R / W	
Bit Definitions		
[7: 0]	E2PD1	16 When the bit pattern for storing 16 High-bit data 8 Place 32 When used to store the low bit pattern 16 High-bit data 8 Place

FLASH Data Register - E2PD2

E2PD2 - FLASH Data register 2		
E2PD2: 0x57	Defaults: 0x00	
Bits	E2PD2 [7: 0]	
R / W	R / W	
Bit Definitions		
[7: 0]	E2PD2	32 When the bit pattern for storing high 16 Low-bit data 8 Place

FLASH Data Register - E2PD3

E2PD3 - FLASH Data register 3		
E2PD3: 0x5C	Defaults: 0x00	
Bits	E2PD3 [7: 0]	
R / W	R / W	
Bit Definitions		
[7: 0]	E2PD3	32 When the bit pattern for storing high 16 High-bit data 8 Place

FLASH Mode Control Register - ECCR

ECCR - FLASH / E2PROM Configuration Register								
ECCR: 0x36 (0x56)					Defaults: 0x0C			
bits	WEN	EEN	ERN	SWM	CP1	CP0	ECS1	ECS0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
The initial value	0	0	0	0	1	1	0	0

Bit Definitions		
[7]	WEN	ECCR Write enable control modification ECCR Before, you must first WEN write 1 And then 6 Within a periodic update ECCR Contents of the register
[6]	EEN	E2PROM Enabled, only LGT8F328P effective 1 :Enable E2PROM Simulation, will from 32KFLASH Reserved some space 0 : Disabled E2PROM simulation, 32KFLASH All for program space
[5]	ERN	write 1 Reset E2PCTL Controller
[4]	SWM	Continuous write mode for simulation E2PROM Controller Operation
[3]	CP1	Page exchange CP1 Regional enable control
[2]	CP0	Page exchange CP0 Regional enable control
[1: 0]	ECS [1: 0]	E2PROM Configuration space 00 : 1KB E2PROM, 30KB program FLASH 01 : 2KB E2PROM, 28KB program FLASH