2. Wait until the corresponding Update Busy flag is cleared;

3. Read TCNT2 .

- In asynchronous mode, interrupt synchronization requires flag 3 System clock cycles plus 1 Timer cycle. in MCU Causing the counter value may be read interrupt flag is set before the counter advanced by at least one clock. Comparison with the change in the output signal of the timer clock is not synchronized to the system clock.

TC2 Prescaler

TC2 Referred to input clock prescaler clkt2s By located ASSR Register AS2 Internal system clock select bit clkio Or external TOSC1 Clock source, the system defaults to the clock clkio Connected. If the AS2 Position, TC2 By TOSC1 Asynchronous drive. when TOSC1 Pin and TOSC2 An external pin 32.768KHz The watch crystal, TC2 Can be used RTC counter. Not recommended TOSC1 Applying an external clock signal on the pin.

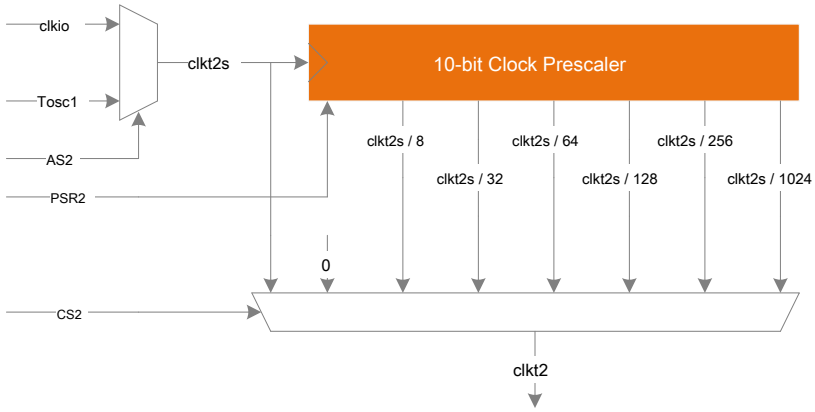

Figure 5 TC2 Prescaler structure diagram

Pictured TC2 Prescaler, as shown in FIG prescaler possible options are: clkt2s / 8, clkt2s / 32, clkt2s / 64, clkt2s / 128, clkt2s / 256, with clkt2s / 1024 . In addition you can also choose clkt2s with 0 (Stop counting). Position SFIOR Register PSR2 The reset bit prescaler, allowing the user to work from a predictable prescaler.

Register Definition

TC2 Register List

register	address	Defaults	description
TCCR2A	0xB0	0x00	TC2 Control register A
TCCR2B	0xB1	0x00	TC2 Control register B
TCNT2	0xB2	0x00	TC2 Count value register
OCR2A	0xB3	0x00	TC2 Output Compare Register A
OCR2B	0xB4	0x00	TC2 Output Compare Register B
ASSR	0xB6	0x00	TC2 Asynchronous Status Register
TIMSK2	0x70	0x00	Timer counter interrupt mask register
TIFR2	0x37	0x00	Timer counter Interrupt Flag Register