The following table is a waveform generation mode control.

Table 5 Waveform Generation Mode Control

WGM3 [3: 0]	Operating mode	TOP Value update	OCR1A time	Position TOV3 time
0	Normal	0xFFFF	immediately	MAX
1	8 Place PCPWM 0x00FF		TOP	BOTTOM
2	9 Place PCPWM 0x01FF		TOP	BOTTOM
3	10 Place PCPWM 0x03FF		TOP	BOTTOM
4	CTC	OCR3A	immediately	MAX
5	8 Place FPWM	0x00FF	BOTTOM	TOP
6	9 Place FPWM	0x01FF	BOTTOM	TOP
7	10 Place FPWM 0x03FF		BOTTOM	TOP
8	PFCPWM	ICR3	BOTTOM	BOTTOM
9	PFCPWM	OCR3A	BOTTOM	BOTTOM
10	PCPWM	ICR3	TOP	BOTTOM
11	PCPWM	OCR3A	TOP	BOTTOM
12	CTC	ICR3	immediately	MAX
13	Retention	-	-	-
14	FPWM	ICR3	TOP	TOP
15	FPWM	OCR3A	TOP	TOP

TCCR3C-TC3 Control register C

TCCR3C - TC3 Control register C								
address: 0x92					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	FOC3A	FOC3B	DOC3B	DOC3A	DTEN3	- DOC3C		FOC3C
R / W	W	W	-	-	-	-	-	-

Bit	Name description	
7	FOC3A	Force Output Compare A . In non PWM Mode, the force output by comparing bits FOC3A write "1" The way to compare match. Forcing compare match will not set OCF3A Flag or reload or clear the timer, but the output pin OC3A Will be in accordance with COM3A It sets the appropriate update, just compare match had really happened. Work on PWM When mode, write TCCR3A Cleared when you want to register. Read FOC3A The return value is always zero.
6	FOC3B Force Output Compare B .	In non PWM Mode, the force output by comparing bits FOC3B write "1" The way to compare match. Forcing compare match will not set OCF3B Flag or reload or clear the timer, but the output pin OC3B Will be in accordance with COM3B It sets the appropriate update, just compare match had really happened. Work on PWM When mode, write TCCR3A Cleared when you want to register. Read FOC3B The return value is always zero.
5	DOC3B Prohibit output of the comparator B Enable control bit.	