OFR1 - Offset compensation register 1

OFR1 - Offset compensation register 1								
address: 0xA4						Defaults: 0x00		
Bit	7	6	5	4	3	2	1	0
Name	OFR1 [7: 0]							
R / W	W / R							

Bit	Name	description
7: 0	OFR1	Offset compensation register 1 ; OFR1 As signed. Stored in twos complement format

ADMSC - ADC Monitoring channel status and control register

ADMSC - ADC Monitoring channel status and control register								
address: 0xAC						Defaults: 0x01		
Bit	7	6	5	4	3	2	1	0
Name	AMOF	-	-	-	AMFC3	AMFC2	AMFC1	AMFC0
R / W	-	-	-	- R / W		R / W	R / W	R / W

Bit	Name	description
7	AMOF	Automatic monitoring overflow event type flag; 1 = On overflow, 0 = Underflow
6: 4	-	Unimplemented
3: 0	AMFC	Automatic monitoring control bit Digital Filter: 0000 = Disable configuration 0001 = A conversion filterless 0010 = Two consecutive agreement 0011 = Three consecutive agreement ..... 1110 = 14 Consecutive agreement 1111 = 15 Consecutive agreement

ADT0L - Automatic monitoring low threshold underflow 8 Place

ADT0L - Automatic monitoring low threshold underflow 8 Place								
address: 0xA5						Defaults: 0x00		
Bit	7	6	5	4	3	2	1	0
Name	ADT0L [7: 0]							
R / W	W / R							

Bit	Name	description
7: 0	ADT0L	Overflow Threshold Register Low automatic monitoring 8 Place