COM1x [1: 0]	description
0	OC1x Disconnect, GM IO Port operations
1	Flip compare match OC1x signal
2	Clear compare match OC1x signal
3	When set compare match OC1x signal

The following table fast PWM Mode mode control comparator output waveform of the output comparator.

COM1x [1: 0]	description
0	OC1x Disconnect, GM IO Port operations
1	WGM1 for 15 When: Flip compare match OC1A signal, OC1B disconnect WGM1 When other values: OC1x Disconnect, GM IO Port operations
2	Clear compare match OC1x Signal is set to match the maximum value OC1x signal
3	When set compare match OC1x Signal is cleared when the maximum matching OC1x signal

The following table shows the comparison output of the phase correction mode the mode control output of the comparator waveform.

COM1x [1: 0]	description
0	OC1x Disconnect, GM IO Port operations
1	WGM1 for 9 or 11 When: Flip compare match OC1A signal, OC1B disconnect WGM1 When other values: OC1x Disconnect, GM IO Port operations
2	Match clears the count comparator ascending OC1x Signal, the match count comparator arranged in descending order bits OC1x signal
3	Comparison of the configuration bit match count ascending OC1x Down signal, in descending count comparator match clears OC1x signal

TCCR1B -TC1 Control register B

TCCR1B - TC1 Control register B								
address: 0x81						Defaults: 0x00		
Bit	7	6	5	4	3	2	1	0
	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10
R / W	R / W	R / W	- R / W		R / W	R / WR / WR / W		

Bit	Name	description
7	ICNC1	Input Capture noise suppressor enable control bit. When set ICNC1 Bit "1" When the enable input capture noise suppressor, when external pin ICP1 The input is filtered continuously 4 Sampling values of the input signal is valid when equal, the function input capture is delayed 4 Clock cycles. When set ICNC1 Bit "0" When prohibit input capture noise suppressor, this time external pin ICP1 Direct and effective input.
6	ICES1	Input Capture Edge Select control bits. When set ICES1 Bit "1" When the rising edge of selection level input capture trigger; provided when ICES1 Bit "0" When selecting the level of the falling edge of the input capture trigger. When a capture is triggered, the counter value is copied into ICR1 Register, while the set input capture flag ICF1 . If the interrupt is enabled, the input capture interrupt.
5	-	Reservations.