Voltage; divider input level may be selected from the external power supply system or from a port.

ADC Support for offset calibration. Offset calibration process is controlled by software. It includes a positive offset calibration, calibration of the amount of reverse two directions. Offset calibration is enabled, ADC The controller will automatically use the calibration values for both forward and reverse ADC Calibration sample results.

Offset calibration method in this section refer to the relevant section.

ADC Operations

ADC Conversion through successive approximation analog input voltage into a 12 Digital bits. The minimum value represents GND The maximum value represents the reference voltage minus 1LSB . A reference voltage source may be ADC Supply voltage AVCC External Reference AVREF Or internal 1.024V / 2.048V The reference voltage, by writing ADMUX Register REFS Bits to select.

The analog input channel by writing ADMUX Register CHMUX Bits to select. any ADC Input pins, the external reference voltage pin, and can be used as the internal reference voltage source ADC The single-ended input. By setting ADTMR Register DIFS Can be ADC Input channel to the internal switching of the differential amplifier. Related differential amplifier and a gain by input source DAPCR Register settings.

By setting ADCSRA Register ADEN Place to start ADC , ADEN When cleared ADC Not power, it is proposed to close in before entering sleep mode ADC .

ADC Conversion results 12 Bit, storage and ADC Data register ADCH and ADCL in. By default, the conversion result is right-aligned, but can be provided ADMUX Register ADLAR Bit becomes left-aligned.

If set to convert the result left-justified, and only the highest 8 Bit conversion accuracy, as long as the reading ADCH Will suffice. Otherwise first reading ADCL Then read ADCH To ensure that the contents of the data register is the result of the same conversion. Once read ADCL After the data register ADCL with ADCH Is latched read ADCH After the conversion result can then update the data register ADCL with ADCH .

ADC Conversion end interrupt can be triggered. Even if the conversion occurred at the end of reading ADCL versus ADCH Between the interrupt will trigger.

Start a conversion

to ADC Start Conversion bit ADSC Write bit "1" You can start a single conversion. In the conversion process this bit remains high until cleared by hardware after the end of the conversion. If you change the channel during the conversion process, so ADC This time the conversion will be completed before changing the channel.

ADC There are different sources of conversion trigger. Set up ADCSRA Register ADC Automatically trigger enable bit ADATE It can automatically triggered. Set up ADCSRB Register ADC Trigger select bit ADTS You can select the trigger source. When the selected trigger signal is a rising edge, ADC Prescaler reset and start the conversion. This provides a method of starting the conversion in a fixed time interval. Even after the conversion trigger signal is still present, it will not start a new conversion. If the trigger during the conversion process has produced a rising edge, the rising edge will be ignored. Even if the specific interrupt is disabled or the global interrupt enable bit "0" That interrupt flag will be set. This will trigger a conversion without generating an interrupt. But in order to trigger a new conversion at the next interrupt event occurs, the interrupt flag must be cleared.

use ADC Interrupt Flag as a trigger source, it can start the next time after the end of the conversion currently in progress ADC Conversion. after that ADC It works in continuous conversion mode, constantly sampling and ADC Data register is updated. First turn