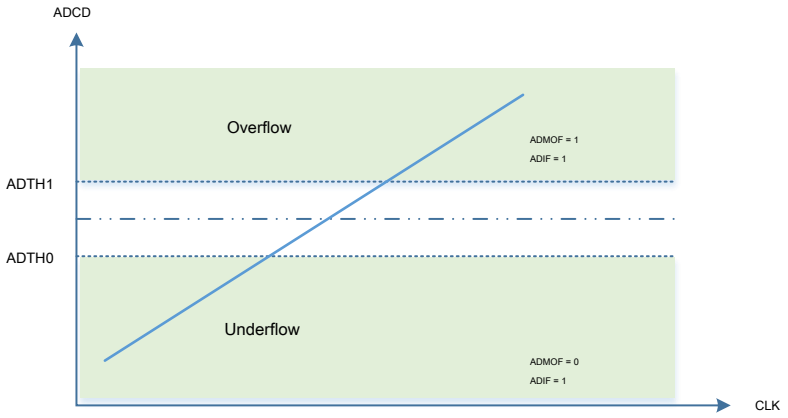
ADC A reference voltage source V_{ref} Reflects ADC The conversion range. If the single-channel level exceeds the end V_{ref} , Which is close to the maximum conversion result 0xFFF . V_{ref} It can be AVCC , External AREF Pin voltage, the internal voltage reference source.

Using the internal reference (1.024V / 2.048V / 4.096V) Precautions:

After the chip is powered on, as an internal reference calibrated by default 1.024V , If a user 1.024V The internal reference can be used directly without other operations. But if you need to use 2.048V or 4.096V Internal reference voltage, needing to update the calibration value of the internal reference. 2.048V / 4.096V The calibration value into a register after power VCAL2 / 3 (0xCE / 0xCC) In the program initialization, VCAL2 / 3 Value of the read and write VCAL (0XC8) Register complete calibration.

Automatic channel monitoring

Automatic channel monitoring mode for real-time monitoring of selected ADC Input voltage channels. Set software ADCSRC Register AMEN Channel bit enables automatic monitoring function, ADC Automatic conversion voltage of the selected channel, when given in addition to the conversion result of the overflow range, will set ADC Interrupt flag (ADIF) And at the same time stop the automatic monitoring. Software can respond to events by means of an overflow interrupt or query. ADMSC Register AMOF Bit is used to indicate the type of overflow events. ADIF Flag is automatically cleared by hardware when the service routine is reset; In query mode, by software written 1 Cleared. Only when ADIF Cleared, and by setting ADCSRC Register AMEN Bit, before re-enables automatic monitoring mode.



To overcome the single ADC Conversion result of unstable support for automatic detection of a digital filter function can be configured. Digital filtering by detecting continuous conversion results only in a continuous number of transitions have been defined in a consistent result, an overflow event is triggered only. Continuous Conversions can ADMSC Register AMFC [3: 0] Bit is set.

Automatic channel monitoring by ADCSRC Register AMEN Position control. register ADT0 For setting the underflow threshold; ADT1 For setting the overflow threshold. ADT0 / 1 for 16 Bit registers. Software Set AMEN After the bit will stop immediately ADC Current conversion operation, and a reset ADC Control state, after entering automatic conversion mode.

Before starting the automatic channel detection mode, detecting the need to set up channels and other relevant configuration. Software may at any time by clearing AMEN Register, disable automatic detection mode.

Multiple input dividing circuit (VDS)

ADC Internal dividing comprises a multiplexing module inputs. Dividing an input voltage from an external source may be selected ADC Input channels (ADC0 / 1/4/5), External reference AVREF Or an analog power supply. Dividing module while the output 4/5 as well as 1/5 Two voltages respectively to ADC internal 12 , 13 Input channels. among them 4/5 This road used for ADC Offset calibration; 1/5 In addition to the offset correction, the Similar applications used for a power supply voltage detection. Dividing circuit related functions mainly by ADCSRD Register control is realized.