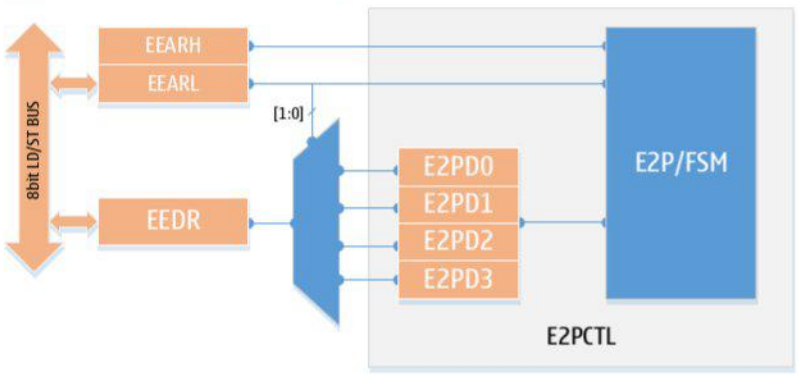
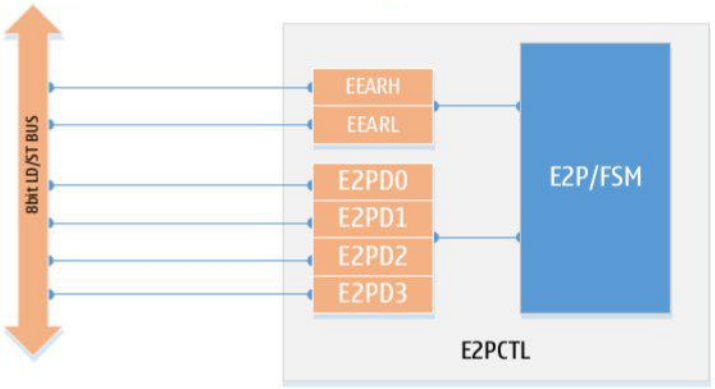
E2PCTL Data Register

The E2PCTL controller has an internal 4-byte data buffer (E2PD0~3). This 4-byte buffer forms the 32-bit data interface for accessing FLASH. This cache buffer requires an internal multiplexer the EEDR, to transition between 32-bit Word and 8-bit Byte access modes. When the E2PCTL controller is in 8-bit Read/Write Mode, the EEDR controls reading and writing byte data to the buffer. The E2PCTL's lower data register EEARL[1:0] contains the address information in the two LSB. These two bits are used to load the correct 8-bit Byte data into the correct data buffer location. The starting address is based on the current FLASH target address. After the E2PCTL fills in the other three bytes of data, it updates all 32-bits in FLASH. When the E2PCTL controller is in 32-bit Read/Write Mode, the EEDR register can still be used as a data interface. The internal data cache is addressed by EEARL[1:0] as an address to read and write a complete 32-bit data. In addition, you can use the data cache to directly access the registers of the IO space (E0~3).

E2PCTL ***8-bit Read/Write Mode:***



E2PCTL ***32-bit Read/Write Mode:***



Byte mode is used for backward compatibility with the byte read and write mode of the LGT8FX8D. The LGT8FX8P's built-in FLASH is 32-bits in width. Using 32-bit read/write mode will bring great benefits to read/write efficiency and extend the FLASH erasure life cycle. Therefore, 32-bit read/write mode is recommended.

E2PCTL Emulated E2PROM Read/Write Access

As mentioned previously FLASH Memory must be erased before writing, and the erase operation is performed in page size blocks. Each Page of Flash Memory inside the LGT8FX8P is 1K bytes. Updating a Byte of data within a single Page first requires erasing the data of the entire Page. Then the target address data can be updated while simultaneously restoring the other unchanged bytes from the page. The whole operation is not only time consuming, but also brings the risk of data loss if power is disconnected during the operation.

The E2PCTL controller internally uses a page exchange algorithm to implement the emulated E2PROM. The page exchange algorithm ensures that when the page erase operation is performed, the original data is not lost due to unexpected situations such as power failure. At the same time, the exchange algorithm uses two pages of space in the exchange. This increases the service life of the emulated E2PROM.