Districts:	Marine	E014:97							
OxF6	Mame GUID3	DICI	DILD	OLD	GUID.	Byte 3	BILL	Bit1	Bitto
0xF5	GUID2					Byte 2			
0xF4	GUID1				GUID	Byte 1			
0xF3	GUID0					Byte 0			
0xF2	PMCR	PMCE	CLKFS	CLKSS	WCLKS	OSCKEN	OSCMEN	RCKEN	RCMEN
0xF0	PMX2	WCE	STOSC1	STOSC0	(34)	19	XIEN	E6EN	C6EN
0xEE	PMX0	PMXCE	C1BF4	C1AF5	C0BF3	C0AC0	SSB1	TXD6	RXD5
0xED	PMX1	- 12	1 2	-	12	-	C3AC	C2BF7	C2AF6
0xEC	TCKCSR	1.5	F2XEN	TC2XF1	TC2XF0	- 15	AFCKS	TC2XS1	TC2XS
0xE2	PSSR	PSS1	PSS3	-	-			PSR3	PSR1
0xE1	OCPUE	PUE7	PUE6	PUE5	PUE4	PUE3	PUE2	PUE1	PUE0
0xE0 0xDE	HDR DAPTE	DAPTE		HDR5	HDR4	HDR3	HDR2	HDR1	HDR0
0xDD	DAPTE	DAPTE	~		DAD	Trimming		-	
0xDC	DAPCR	DAPEN	GA1	GA0	DNS2	DNS1	DNS0	DPS1	DPS0
0xCF	LDOCR	WCE	Oni	Ono	DIVOZ	PDEN	VSEL2	VSEL1	VSELO
0xCE	VCAL2		Cal	ibration va	alue for 2.				1 : 2 - 2 - 2
0xCD	VCAL1		Cal	ibration va	alue for 1.	024V inter	rnal refere	nce	
0xCC	VCAL3		Cal	ibration va	alue for 4.	096V inter	mal refere	nce	
0xC8	VCAL		Inte	ernal Volta	ige Refere	nce calibr		ster	
0xAF	DPS2R	-	-	-		DPS2E	LPRCE	TOS1	TOS0
0xAE	IOCWK	IOCD7	IOCD6	IOCD5	IOCD4	IOCD3	IOCD2	IOCD1	IOCDO
0xAD	ADCSRD	BGEN	REFS2	IVSEL1	IVSEL0		VDS2	VDS1	VDS0
0xAC	ADMSC	AMOF	400	-		AMFC3	AMFC2	AMFC1	AMEC
0xAB	ADT1H			Auto-moi					
0xAA 0xA9	ADT1L PORTE			C Auto-mo t Output E					
0xA9	DDRE			Direction					
0xA7	PINE			ort Input E					
0xA6	ADTOH			Auto-mon	and the second s				
0xA5	ADTOL			Auto-mor					
0xA4	OFR1					offset trim		**	
0xA3	OFR0			ADC	negative	offset trim	ming		
0xA1	DALR				DAC dat	a register			
0xA0	DACON	1.5	-		-	DACEN	DAOE	DAVS1	DAVS
0x9F	OCR3CH			e output r					
0x9E	OCR3CL			re output i					
0x9D	DTR3H			Dead-ban					
0x9C	DTR3L		Dead-band register low byte of Timer3						
		Compare output register high byte of Timer3 B channel Compare output register low byte of Timer3 B channel							
0x9B	OCR3BH						Timer3 B	channel	
0x9A	OCR3BL		Compa	re output i	register lo	w byte of	Timer3 B Timer3 B	channel channel	
0x9A 0x99	OCR3BL OCR3AH		Compa Compar	re output r e output r	register lo egister hi	w byte of gh byte of	Timer3 B Timer3 B Timer3 A	channel channel channel	
0x9A 0x99 0x98	OCR3BL OCR3AH OCR3AL		Compar Compar Compa	re output r e output r re output r	register lo egister hi register lo	w byte of gh byte of w byte of	Timer3 B Timer3 B Timer3 A Timer3 A	channel channel channel channel	
0x9A 0x99 0x98 0x97	OCR3BL OCR3AH OCR3AL ICR3H		Compar Compar Compa	re output r e output r re output r nput captu	register lo egister hi register lo ire registe	w byte of gh byte of w byte of r high byte	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer	channel channel channel channel	
0x9A 0x99 0x98	OCR3BL OCR3AH OCR3AL		Compar Compar Compa	re output i re output r re output i nput captu nput captu	register lo egister hi register lo ire registe ure registe	w byte of gh byte of w byte of r high byte	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer of Timer	channel channel channel channel	
0x9A 0x99 0x98 0x97 0x96	OCR3BL OCR3AH OCR3AL ICR3H ICR3L		Compar Compar Compa	re output r re output r re output r nput captu nput captu Counter	register lo egister hi register lo ire registe ire registe register h	w byte of gh byte of w byte of r high byte er low byte	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer of Timer f Timer3	channel channel channel channel	
0x9A 0x99 0x98 0x97 0x96 0x95	OCR3BL OCR3AH OCR3AL ICR3H ICR3L TCNT3H TCNT3L TCCR3D		Compar Compar Compa	re output r re output r re output r nput captu nput captu Counter Counter Con	register lo egister hid register lo ure registe ure register register l register l trol regist	w byte of gh byte of w byte of r high byte r low byte igh byte o ow byte o er D of Tir	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer e of Timer3 f Timer3 mer3	channel channel channel channel	
0x9A 0x99 0x98 0x97 0x96 0x95 0x94	OCR3BL OCR3AH OCR3AL ICR3H ICR3L TCNT3H TCNT3L		Compar Compar Compa	re output r re output r re output r nput captu nput captu Counter Counter Con	register lo egister hid register lo ure registe ure register register l register l trol regist	w byte of gh byte of w byte of r high byte er low byte igh byte o ow byte o	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer e of Timer3 f Timer3 mer3	channel channel channel channel	
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91	OCR3BL OCR3AH OCR3AH ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B		Compar Compar Compa	re output re output re output re output taptu nput captu Counter Counter Con Con	register lo egister hid register lo irre registe irre register register h register l trol regist trol regist trol regist	w byte of gh byte of w byte of r high byte r low byte igh byte o ow byte o er D of Tir er C of Tir er B of Tir	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer of Timer3 f Timer3 mer3 mer3 mer3	channel channel channel channel	
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90	OCR3BL OCR3AH OCR3AL ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A		Compa Compa Compa II	re output re output re output re output captu nput captu Counter Counter Con Con Con Con	register lo egister hi register lo ire registe register h register l trol regist trol regist trol regist	w byte of gh byte of w byte of r high byte r low byte igh byte o ow byte o er D of Tir er C of Tir er A of Tir	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer of Timer3 f Timer3 f Timer3 ner3 ner3 ner3	channel channel channel channel channel 3	
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D	OCR3BL OCR3AH OCR3AH ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3C TCCR3B TCCR3A DTR1H		Compa Compa Compa II	re output i re output i re output i nput captu nput captu Counter Counter Con Con Con Con	register lo egister hi register lo ire registe register h register l trol regist trol regist trol regist d register	w byte of gh byte of w byte of r high byte r low byte igh byte o ow byte o er D of Tir er C of Tir er A of Tir high byte	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer e of Timer f Timer3 f Timer3 mer3 mer3 mer3 ner3 of Timer1	channel channel channel channel 3	
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D	OCR3BL OCR3AH OCR3AL ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3C TCCR3B TCCR3A DTR1H DTR1L	DCV17	Compa Compar Compa II	re output re output re output re output raptu captu Counter Counter Con Con Con Con Con Con Dead-ban Dead-ban	register lo egister hi register lo ure registe ure register h register h register li trol regist trol regist trol regist trol regist d register lo d register lo	w byte of gh byte of w byte of r high byte r low byte igh byte o ow byte o er D of Tir er C of Tir er A of Tir	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer e of Timer f Timer3 f Timer3 mer3 mer3 mer3 ner3 of Timer1	channel channel channel channel 3 3	Devid
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C	OCR3BL OCR3AH OCR3AL ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D	DSX17	Compar Compar Compar II	re output re output re output re output raptu captu Counter Counter Con Con Con Con Con Dead-ban Dead-ban DSX15	register lo egister hi register lo re registe register h register h register l trol regist trol regist trol regist trol regist d register d register DAX14	w byte of gh byte of w byte of r high byte of r high byte of gh byte of the by	Timer3 B Timer3 A Timer3 A Timer3 A Timer3 A e of Timer f Timer3 f Timer3 ner3 ner3 ner3 of Timer1 of Timer1	channel channel channel channel 33 3	
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x80 0x8C 0x83 0x7D	OCR3BL OCR3AH OCR3AH ICR3H TCNT3H TCNT3L TCCR3C TCCR3B TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC	OFEN	Compar Compar Compa II	re output re output re output re output raptu captu Counter Counter Con Con Con Con Con Con Dead-ban Dead-ban	register lo egister hi register lo ure registe ure register h register h register li trol regist trol regist trol regist trol regist d register lo d register lo	w byte of gh byte of w byte of r high byte r low byte igh byte o ow byte o er D of Tir er C of Tir er A of Tir high byte	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer e of Timer f Timer3 f Timer3 mer3 mer3 mer3 ner3 of Timer1	channel channel channel channel 33 3	ADTM
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x83 0x7D	OCR3BL OCR3AH OCR3AH ICR3H ICR3L TCNT3H TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2		Compar Compar Compar II	re output re output re output re output re output re put captu funct captu Counter Counter Con	register lo egister hi register lo re registe register lo re register register l trol regist trol regist trol regist trol regist d register DAX14 AMEN	w byte of gh byte of w byte of r high byte r high byte gigh byte o ow byte o ow byte o or D of Tir er C of Tir er B of Tir er A of Tir high byte	Timer3 B Timer3 A Timer3 A Timer3 A Timer3 A Timer3 A Timer3 Time	channel channel channel channel 33 3	
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x80 0x8C 0x83 0x7D	OCR3BL OCR3AH OCR3AH ICR3H TCNT3H TCNT3L TCCR3C TCCR3B TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC	OFEN	Compar Compar Compa II	re output re output re output re output re output re put captu funct captu Counter Counter Con	register lo egister hi register lo re registe register lo re register register l trol regist trol regist trol regist trol regist d register DAX14 AMEN	w byte of gh byte of w byte of r high byte of r high byte of gh byte of the by	Timer3 B Timer3 A Timer3 A Timer3 A Timer3 A Timer3 A Timer3 Time	channel channel channel channel 33 3	ADTM
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x80 0x8D 0x85 0x7D 0x76 0x75	OCR3BL OCR3AH OCR3AH ICR3H ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE	OFEN	Compar Compar Compa II	re output re output re output re output re output re put captu funct captu Counter Counter Con	register lo egister hi register lo register lo register lo register register lo register lo register lo register lo register lo regist rol regist rol regist d register d register DAX14 AMEN rupt Vector	w byte of gh byte of w byte of r high byte r high byte gigh byte o ow byte o ow byte o or D of Tir er C of Tir er B of Tir er A of Tir high byte	Timer3 B Timer3 A Timer3 A Timer3 A Timer3 A Timer3 A Timer3 Time	channel channel channel channel 33 3	ADTM
0x9A 0x99 0x98 0x97 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x83 0x7D 0x76 0x75	OCR3BL OCR3AH OCR3AH ICR3H ICR3H TCNT3H TCNT3L TCCR3B TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4	OFEN	Compar Compar Compa II	re output re output re output re output re output raptu captu captu Counter Counter Con	register lo egister hi register lo register lo register lo register register lo register lo register lo register lo register lo regist rol regist rol regist d register d register DAX14 AMEN rupt Vector	w byte of gh byte of w byte of w byte of vr high byte of or high byte of ow byte of ow byte of the control of Tirer C of Tirer C of Tirer A of	Timer3 B Timer3 A Timer3 A Timer3 A Timer3 A Timer3 A Timer3 Time	channel channel channel channel 33 3	ADTM -
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x80 0x80 0x80 0x70 0x75 0x74 0x73	OCR3BL OCR3AH OCR3AH ICR3H ICR3H TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3	OFEN	Compar Compar Compa II	re output re output re output re output rnput captu nput captu nput captu Counter Counter Con Con Con Con Dead-ban Dead-bar DSX15 SPN - Inten	register lo egister hi register lo re registe register lo re register register lo regist rol register lo register DAX14 AMEN - rupt Vecto PCINT	w byte of gh byte of w byte of w byte of or high byte of or high byte of ow byte of Tirer B of Tirer B of Tirer B of the high byte of ow byte of Base Ad (39:32)	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer f Timer3 f Timer3 ner3 ner3 ner3 ner3 of Timer1 - SPD - dress	channel channel channel channel 3 3 3	ADTM -
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x8D 0x8C 0x8S 0x7D 0x76 0x75 0x74 0x73 0x71 0x67	OCR3BL OCR3AH OCR3AH ICR3H ICR3L TCNT3H TCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK4 PCMSK3 RCKCAL PRR1	OFEN -	Compar Compar Compar II I DSX16	re output re output re output re output rnput captu nput captu nput captu Counter Counter Con Con Con Con Dead-ban Dead-bar DSX15 SPN - Inten	register lo egister hi register lo re registe register lo re register register lo regist rol register lo register DAX14 AMEN - rupt Vecto PCINT	w byte of gh byte of w byte of w byte of r high byte of r high byte of r high byte of r high byte o ow byte o ow byte o or P of Tirer B of Tire	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer f Timer3 f Timer3 ner3 ner3 ner3 ner3 of Timer1 - SPD - dress	channel channel channel channel channel channel channel 3 3 3 DSX11 DIFS - OCIE3A PRPCI	TOIE3
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x80 0x80 0x70 0x76 0x75 0x74 0x73 0x71 0x67 0x65 0x62	OCR3BL OCR3AH OCR3AH ICR3H ICR3L TCNT3H TCRT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR	OFEN	Compar Compar Compa II	re output i e output i re outp	register lo egister hi register lo register lo re register register lo re register register lo trol register trol regist trol regist trol regist trol regist de register DAX14 AMEN - rupt Vecto PCINT - RC32K C	w byte of gh byte of w byte of w byte of r high byte of r high byte of r high byte of r high byte o ow byte o ow byte o or D of Tirer B of Tirer B of Tirhigh byte own byte o or Base Ad [39:32] OCIESC allibration PRTIM3 VDTS	Timer3 B Timer3 B Timer3 A Timer3 A Timer3 A Timer3 A Timer3 Time	channel channel channel channel 3 3 3 DSX11 DIFS	TOIE3
0x9A 0x99 0x99 0x97 0x96 0x95 0x94 0x93 0x90 0x8D 0x8C 0x75 0x76 0x75 0x71 0x65 0x65 0x62 0x95	OCR3BL OCR3AH OCR3AH ICR3H ICR3H TCNT3H TCNT3L TCCR3D TCCR3C TCCR3A DTR1H DTR1L TCCR1D ADCSRC IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3	OFEN -	Compar Compar Compar II I DSX16	re output i e output i re outp	register lo register hi register lo register do register do register do register DAX14 AMEN	w byte of gh byte of w byte of w byte of w byte of r high byte of ow byte of ow byte of ow byte of the role of Tirer C of Tirer C of Tirer C of Tirer B of Tirnhigh byte low byte of Base Ad (39:32) OCIE3C allibration PRTIM3 VDTS register by	Timer3 B Timer3 B Timer3 A Timer3 A Timer3 A Timer3 A Timer3 Time	channel channel channel channel channel channel channel 3 3 3 DSX11 DIFS - OCIE3A PRPCI	TOIE3
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x80 0x80 0x80 0x70 0x75 0x74 0x73 0x71 0x67 0x65 0x62 0x5C	OCR3BL OCR3AH OCR3AH ICR3H ICR3H TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B DTCR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR	OFEN -	Compar Compar Compar II I DSX16	re output captu Counter Counter Con Con Con Dead-ban Dead-ban DSX15 SPN Inten ICIE3 PRWDT E2Pe	register lo register hi register lo register lo re register register lo register lo register register lo register lo register lo register lo register register lo register register register lo regist	w byte of gh byte of w byte of w byte of w byte of r high byte of or high byte of ow byte of ow byte of ow byte of ow byte of or Tirer B of Tirer B of Tirer B of Tirer B of War and byte of the byte	Timer3 B Timer3 B Timer3 A Timer3 A e of Timer f Timer3 f Timer3 f Timer3 ner3 ner3 ner3 of Timer1 - SPD - dress OCIE3B PREFL	channel channel channel channel channel channel channel 3 3 3 DSX11 DIFS - OCIE3A PRPCI	TOIE3
0x9A 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x7D 0x75 0x74 0x73 0x71 0x67 0x65 0x65 0x5C 0x5B	OCR3BL OCR3AH OCR3AH ICR3H ICR3H TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3B TCCR3B TCCR3C ICR3H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR	OFEN -	Compar Compar Compar II I DSX16	re output captu captu Counter Counter Con Con Con Con Dead-ban Dead-bar DSX15 SPN Inten ICIE3 PRWDT E2P0	register lo egister hi register lo register lo re register register lo RCS14 AMEN - rupt Vector - CTL Data AC1 trim CTL Data	w byte of gh byte of w byte of w byte of r high byte of r high byte of relow byte of the company	Timer3 B Timer3 B Timer3 A Timer3 A Timer3 A Timer3 A Timer3 A Timer3 Ti	channel channel channel channel channel channel channel 3 3 3 DSX11 DIFS - OCIE3A PRPCI	TOIE3
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0x9A 0x99 0x99 0x97 0x96 0x97 0x96 0x95 0x91 0x90 0x8D 0x8C 0x83 0x7D 0x75 0x74 0x73 0x71 0x67 0x55 0x52 0x58 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50	OCR3BL OCR3AH OCR3AH OCR3AH ICR3H ICR3H TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR COTR COXR DTR0 TCCR0C C1XR SPFR TIFR3 PORTF	WEN - DSX07 - RDFULL	Compai Compai Compai II I DSX16 PB5D	re output captu. Counter Counter Counter Con Con Dead-ban Dead-ban Dead-ban Dead-ban Dead-ban Dead-ban DSX15 SPN Inten ICIE3 PRWDT - E2P DSA[3 DSA[2 ERN A COHYSE TC0 Deac DSX05 C1HYSE RDPTR1 ICF3 P	register lo register hi register lo register lo re register regist	w byte of gh byte of w byte of w byte of w byte of r high byte of r high byte of ow byte of ow byte of ow byte of ow byte of r D of Tirer B of	Timer3 B Timer3 B Timer3 A Timer3 A Timer3 A Timer3 A Timer3 A Timer3 Ti	channel channe	TOIE3 - VDTEN ECS0 C0FS0 D5X00 C1FS0 WRPTR
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0x9A 0x99 0x99 0x98 0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x80 0x70 0x76 0x75 0x74 0x73 0x71 0x67 0x65 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50	OCR3BL OCR3AH OCR3AH OCR3AH ICR3H ICR3H TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3B TCCR3C TCR3B TCCR3C IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR C0TR COTR COTR TCCR0C C1XR SPFR TIFR3 PORTF DDRF PINF DSDY	WEN - DSX07 - RDFULL	Compai Compai Compai II I DSX16 	re output i re out	register lo egister hir register hir register lo re register register lo re register register lo re register register lo register register lo register register lo register register lo register rol regist rol r	w byte of gh byte of w byte of r high byte of ow byte of er D of Tirer C of Tirer B of Tir	Timer3 B Timer3 B Timer3 A Timer3 A Timer3 A Timer3 A Timer3 A Timer3 A Timer3	channel channe	TOIE3 - VDTEN ECS0 C0FSC D5X00 C1FSC WRPTR
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0x9A 0x99 0x99 0x97 0x96 0x97 0x96 0x97 0x90 0x80 0x80 0x80 0x70 0x70 0x71 0x67 0x73 0x71 0x67 0x52 0x52 0x54 0x54 0x58 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50 0x50	OCR3BL OCR3AH OCR3AH OCR3AH ICR3H ICR3H TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3C TCCR3B TCCR3C TCCR3B TCCR3C TCCR3B TCCR3C TCCR3B TCCR3C TMSK3 RCKCAL PRR1 VDTCR E2PD1 DSAH DSAL ECCR COTR COXR DTR0 TCCR0C C1XR SPFR TIFR3 PORTF DDRF PINF DSDY DSDX C1SR PORTE DDRE	WEN - DSX07 - RDFULL	Compai Compai Compai II I DSX16 PB5D	re output i re output captu i re output captu i re output captu i re output captu i re output i re out	register lo register hir register hir register lo re register register lo re register register lo register lo register lo register lo register lo register lo register register lo register register lo register register lo r	w byte of gh byte of w byte of w byte of w byte of r high byte of r high byte of relow byte of ow byte of er D of Tirer G of Tirer B	Timer3 B Timer3 B Timer3 A Timer3 A Timer3 A Timer3 A Timer3 A Timer3 Ti	channel channe	TOIE3 - VDTEN ECS0 C0FS0 D5X00 C1FS0 WRPTR TOV3
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0x9A 0x99 0x98 0x97 0x96 0x97 0x96 0x95 0x92 0x91 0x90 0x8D 0x8C 0x7D 0x75 0x74 0x73 0x71 0x67 0x5C 0x5C 0x5S 0x5A 0x5Q 0x5S 0x5A 0x5Q 0x5C 0x5S 0x5A 0x5Q 0x5C 0x5S 0x5A 0x5Q 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5S 0x5C 0x5C 0x5S 0x5C 0x5S 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x3A 0x3A 0x3A 0x3A 0x3A 0x3C 0x3C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C 0x5C	OCR3BL OCR3AH OCR3AH OCR3AH ICR3H ICR3H TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3C TCCR3B TCCR3C TCCR3B TCCR3C TCCR3B TCCR3C TCCR3B TCCR3C TMSK3 RCKCAL PRR1 VDTCR E2PD1 DSAH DSAL ECCR COTR COXR DTR0 TCCR0C C1XR SPFR TIFR3 PORTF DDRF PINF DSDY DSDX C1SR PORTE DDRE	WEN - DSX07 - RDFULL	Compai Compai Compai II I DSX16 PB5D	re output re out	register lo egister hi register hi register lo registe	w byte of gh byte of w byte of w byte of w byte of r high byte of r high byte of relow byte of ow byte of er D of Tirer G of Tirer B	Timer3 B Timer3 B Timer3 A Timer3 A Timer3 A Timer3 A Timer3 A Timer3 A Timer3	channel channe	TOIE3 - VDTEN ECS0 C0FS0 D5X00 C1FS0 WRPTR TOV3

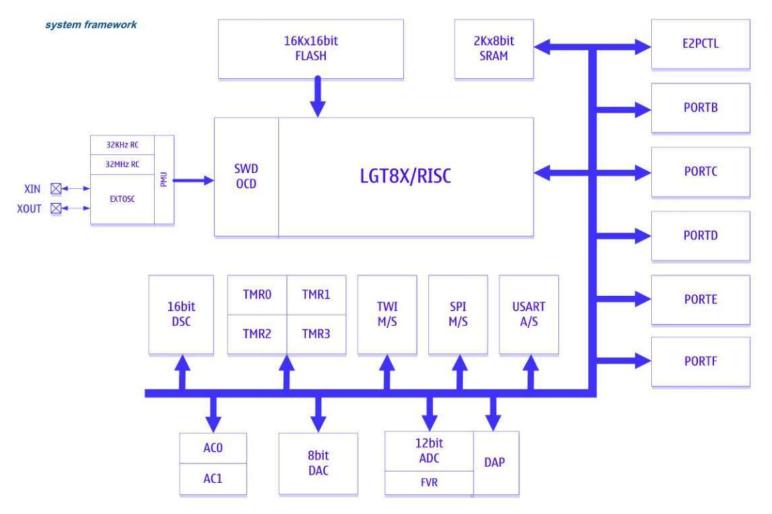
8-bit LGT8XM

RISC Microcontroller with In-System Programmable FLASH Memory

LGT8F88P LGT8F168P LGT8F328P

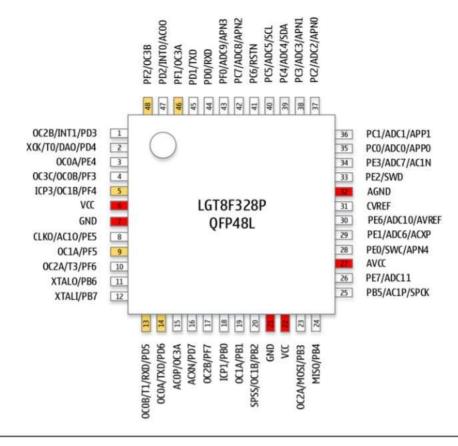
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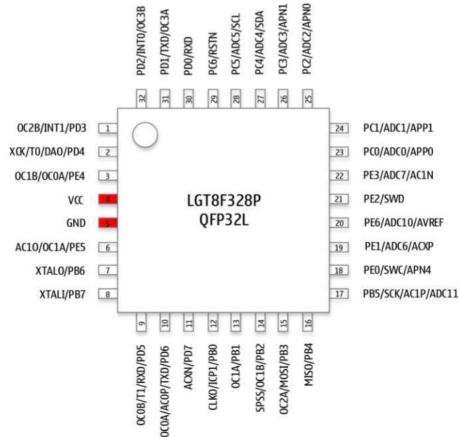
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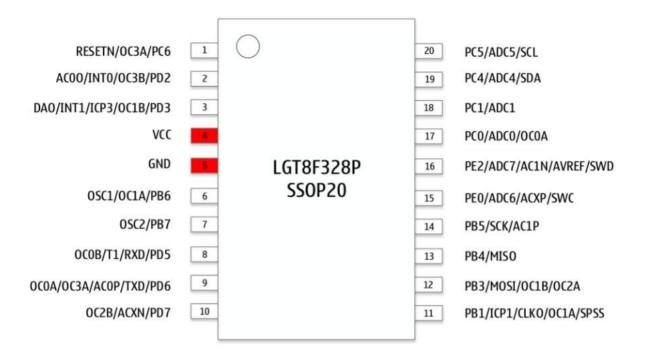


Module Name	Module features
SWD	Debug module, debugging and ISP Features
LGT8X	8Bit high performance RISC Kernel
E2PCTL	FLASH Data Access Interface Controller
PMU	Power management module
PORTB/C/D/E/F	General-purpose programmable input and output ports
DSC	16 Digit arithmetic acceleration unit
ADC	8 Channel 12 Bit ADC with programmable gain
DAP	Differential amplifier
IVREF	1.024V / 2.048V / 4.096V Internal Reference
ACO/1	Analog comparator
TMRO/ 1/2/3	8/16 Bit timer / counter, PWM Controller
WDT	Reset Watchdog module
SPIM/S	Master-slave SPI Controller
TWIM/S	Master-Slave two-wire interface controller, compatible I2C protocol
USART	Synchronous / Asynchronous Serial Transceiver
DAC	8 Bit DAC

Package defined







Pin Description

QFP48	QFP32	SSOP20			
01.10	Q113E	3301 20	PD3/INT1/OC2B*		
			PD3: I/O Pin D3		
01	01		INT1: External Interrupt 1 Input		
			OC2B: Timer/Counter 2 Output Compare Match Output B		
		03	PD4/DA0/T0/XCK		
			PD4: I/O Pin D4		
02	02		DAO: Digital to Analog Converter DAC		
			T0: Timer0 Timer/Counter 0		
			XCK: USART USART external clock		
			PE4/0C0A*		
03	03	:-	PE4: I/O Pin E4		
			OCOA: Timer/Counter 0 Output Compare Match Output A		
			PF3/0C3C/0C0B*		
04	-	_	PF3: I/O Pin F3		
			OC3C: Timer/Counter 3 Output Compare Match Output C		
			OCOB: Timer/Counter 0 Output Compare Match Output B		
			PF4/OC1B*/ICP3		
05	03	03	PF4: I/O Pin F4 OC1B: Timer/Counter 1 Output Compare Match Output B		
			ICP3: Timer 3 Capture Input		
06	04	04	VCC		
07	05	05	GND		
U1	03	05	PE5/AC10/CLKO*		
000,000			PE5: I/O Pin E5		
80					-
	06		CLKO: System Clock Output		
			PF5/0C1A*		
09		06	PF5: I/O Pin F5		
0.000		33.35	OC1A: Timer/Counter 1 Output Compare Match Output A		
			PF6/T3/OC2A*		
10			PF6: I/O Pin F6		
10		11 	T3: Timer 3 External clock input		
			OC2A: Timer/Counter 2 Output Compare Match Output A		
			PB6/XTALO		
11	07	06	PB6: I/O Pin B6		
			XTALO: Crystal Oscillator Output		

QFP48	QFP32	SSOP20	
	L2 08		PB7/XTALI
12		07	PB7: I/O Pin B7
			XTALI: Crystal Oscillator Input
			PD5/RXD*/T1/OC0B
			PD5: I/O Pin D5
13	09	08	RXD: USART Receive Data
			T1: Timer 1 External Clock Input
			OCOB: Timer/Counter 0 Output Compare Match B
			PD6/TXD*/OCOA
14			PD6: I/O Pin D6
14			TXD: USART Transmit Data
	10	09	OCOA: Timer/Counter 0 Output Compare Match A
			ACOP/OC3A
15			ACOP: Analog Comparator 0 Positive Input
			OC3A: Timer/Counter 3 Output Compare Match A
			PD7/ACXN
16	11		PD7: I/O Pin D7
		10	ACXN: Analog Comparator 0/1 Inverting Input
			PF7/OC2B
17	-		PF7: I/O Pin F7
			OC2B: Timer/Counter 2 Output Compare Match B
10	12		PBO/ICP1
18	12		PB0: I/O Pin B0
		11	ICP1: Timer 1 Capture Input
10	12		PB1/OC1A
19	13		PB1: I/O Pin B1 OC1A: Timer/Counter 1 Output Compare Match A
			PB2/OC1B/SPSS
			PB2: I/O Pin B2
20	14	12	OC1B: Timer/Counter 1 Output Compare Match B
			SPSS: SPI Slave Select
21	-	_	GND
22	-	-	VCC
			PB3/MOSI/OC2A
	22.22	12	PB3: I/O Pin B3
23	15		MOSI: SPI Master Output Slave Input
			OC2A: Timer/Counter 2 Output Compare Match A
		13	PB4/MISO
24	16		PB4: I/O Pin B4
27. 5			MISO: SPI Master Input Slave Output
			PB5/SPCK/AC1P
25	17	14	PB5: I/O Pin B5
25	17	7 14	SPCK: SPI Clock
			AC1P: Analog Comparator 1 Noninverting Input
QFP48	QFP32	SSOP20	
	8		-6-

QFP48	QFP32	SSOP20	
			PE7/ADC11
26	26 -	-	PE7: I/O Pin E7
		ADC11: ADC Input Channel 11	
27	•	-	AVCC: Internal Analog Circuit Positive Power Supply
			PEO/SWC/APN4
28	18		PEO: I/O Pin EO
20	10		SWC: SWD Debug Interface Clock
		15	APN4: Differential Amplifier Inverting Input Channel 4
		13	PE1/ADC6/ACXP
29	19		PE1: I/O Pin E1
23	19		ADC6: ADC Input Channel 6
			ACXP: Analog Comparator 0/1 Noninverting Input
			PE6/ADC10/AVREF
30	20	16	PE6: I/O Pin E6
30	20	10	ADC10: ADC Input Channel 10
			AVREF: ADC External Reference Voltage Input
31	-	-	CVREF: ADC Reference Voltage External Filter Capacitor (0.1uF)
32	-	-	AGND: Internal Analog Circuit Power Supply Ground
			PE2/SWD
33	21		PE2: I/O Pin E2
		16	SWD: SWD Debug Interface Data
		16	PE3/ADC7/AC1N
34	22		PE3: I/O Pin E3
			ADC7: ADC Input Channel 7 AC1N: Analog Comparator 1 Inverting Input
			PCO/ADCO/APPO
			PCO: I/O Pin CO
35	23	17	ADC0: ADC Input Channel 0
			APPO: Differential Amplifier Channel 0 Positive Input
			PC1/ADC1/APP1
		24 18	PC1: I/O Pin C1
36	24		ADC1: ADC Input Channel 1
			APP1: Differential Amplifier Channel 1 Positive Input
			PC2/ADC2/APN0
~=	25		PC2: I/O Pin C2
37	25		ADC2: ADC Input Channel 2
			APNO: Differential Amplifier Channel 0 Inverting Input
			PC3/ADC3/APN1
20	26	6 -	PC3: I/O Pin C3
38			ADC3: ADC Input Channel 3
			APN1: Differential Amplifier Channel 1 Inverting Input
QFP48	QFP32	SSOP20	

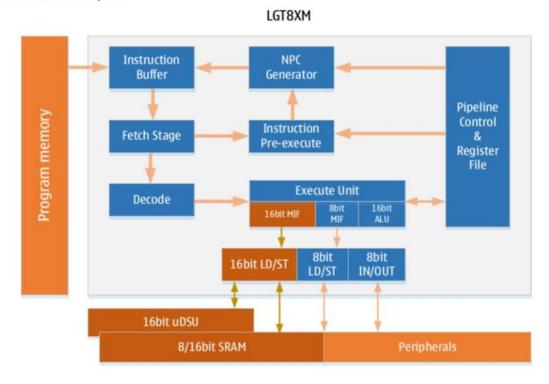
QFP48	QFP32	SSOP20	
			PC4/ADC4/SDA
20	27	10	PC4: I/O Pin C4
39	27	19	ADC4: ADC Input Channel 4
			SDA: I2C Data
			PC5/ADC5/SCL
40	28	20	PC5: I/O Pin C5
40	20	20	ADC5: ADC Input Channel 5
			SCL: I2C Clock
			PC6/RESETN
41	29	1	PC6: I/O Pin C6
			RESETN: External Reset Input
			PC7/ADC8/APN2
42	_	12	PC7: I/O Pin C7
72			ADC8: ADC Input Channel 8
			APN2: Differential Amplifier Channel 2 Inverting Input
			PF0/ADC9/APN3
43	-	-	PF0: I/O Pin F0
			ADC9: ADC Input Channel 9
			APN3: Differential Amplifier Channel 3 Inverting Input
	20		PDO/RXD
44	30	-	PD0: I/O Pin D0
			RXD: USART Receive
45			PD1/TXD
45		-	PD1: I/O Pin D1
	31		TXD: USART Transmit
16		1	PF1/0C3A PF1: I/O Pin F1
46		1	0C3A: Timer/Counter 3 Output Compare Match A
			PD2/INTO/ACOO
			PD2: I/O Pin D2
47			INTO: External Interupt 0 Input
	32	32 2	ACOO: Analog Comparator 0 Output
	JL	_	PF2/OC3B
48			PF2: I/O Pin F2
10			OC3B: Timer/Counter 3 Output Compare Match B
QFP48	QFP32	SSOP20	
Q1140	QITUE	3301 20	

LGT8XM

- Low Power Design
- High Efficency RISC Archatecture
- 16 Bit LD/ST Extension (Dedicated uDSU)
- 130 Instructions, Over 80% execute in a Single Cycle
- Embedded In-Circuit Debugger (OCD)

OVERVIEW

This section discusses the LGT8XM core architecture in general. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.



In order to maximize performance and parallelism, the LGT8XM uses a Harvard architecture – with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is prefetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Reprogrammable Flash memory. The fast-access Register File contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in one clock cycle.