Pin Change Interrupt

- 40 A pin change interrupt source
- 5 Interrupt entry

Overview

Pin Change interrupted by PBn , PCn , PDn, PEn with PFn Pin trigger. As long as pin change interrupt is enabled, even if these pins are configured as outputs can also trigger an interrupt. This software can be used to generate an interrupt.

Any enabled PBn Flip pin triggers an interrupt pin level PCI0 , Enabled PCn Flip the trigger pin PCI1 , Enabled PDn Flip the trigger pin PCI2 , Enabled PEn Flip the trigger pin PCI3 . Each pin change interrupt enable respectively, by PCMSK0 ~ 4 Control register. All pin change interrupts are asynchronous detection, wake-up source can be used under certain sleep mode.

Register Definition

Pin Change Interrupt Register List

register	address	Defaults	description
PCICR	0x68	0x00	Pin Change Interrupt Control Register
PCIFR	0x3B	0x00	Pin change interrupt flag register
PCMSK0	0x6B	0x00	Pin change interrupt mask register 0
PCMSK1	0x6C	0x00	Pin change interrupt mask register 1
PCMSK2	0x6D	0x00	Pin change interrupt mask register 2
PCMSK3	0x73	0x00	Pin change interrupt mask register 3
PCMSK4	0x74	0x00	Pin change interrupt mask register 4

PCICR - Pin Change Interrupt Control Register

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address: 0x68					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	PCIE4	PCIE3	PCIE2	PCIE1	PCIE0
R / W	-	-	-	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 5	-	Reservations.
4	PCIE4	Pin change interrupt enable control bit 4 . When set PCIE4 Bit "1" And when the global interrupt enable pin change interrupt 4 It is enabled. Any enabled PFn Pin level change will have PCI4 Interrupted. PFn Pin interrupts can be independently by the PCMSK4 Control register. When set PCIE3 Bit "0" When, pin change interrupt 3 Prohibited.
3	PCIE3	Pin change interrupt enable control bit 3 . When set PCIE3 Bit "1" And when the global interrupt enable pin change interrupt 3 It is enabled.