		Interrupted.
4	RXEN	**Receive Enable bit. After starting set USART receiver. RxD Universal pin IO Function is USART Receiving group. Disabling the Receiver will flush the receive buffer, and FE , DOR and PE Flag is not valid.**
3	TXEN	**Transmit Enable bit. After starting set USART Transmitter. TxD Universal pin IO Function is USART Transmitting the group. TXEN When cleared, only to wait until all the data is sent to truly complete ban** USART send.
2	UCSZ2	Control characters in length 2 Bit. **UCSZ2 versus UCSRC Register UCSZ1: 0 Together provided number of data bits contained in the frame.**
1	RXB8	**Receiving data of 8 Bit. When the data frame length 9 Bits, RXB8 Is the most significant bit of received data. Read UDR Low contained 8 Before reading the first bit of data RXB8 .**
0	TXB8	**The first transmit data 8 Bit. When the data frame length 9 Bits, TXB8 It is the highest transmit data. Write UDR Low contained 8 Written before the first bit of data TXB8 .**

UCSRC- USART Control and status registers C

***UCSRC* - USART Control and status registers C**								
address: 0xC2					Defaults: 0x06			
Bit	7	6	5	4	3	2	1	0
Name	UMSEL1	UMSEL0	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description	
7: 6	UMSEL1: 0	USART Mode Select bit. UMSEL Select synchronous or asynchronous modes of operation.	
		UMSEL	mode
		0	USART Asynchronous mode of operation
		1	USART Synchronous mode of operation
		2	SPI Slave modes of operation
		3	SPI The host operating mode
5: 4	UPM1: 0	**Parity mode selection bit. High UPM1 Select enable or disable parity, low UPM0 Select odd** or even parity.	
		UPM1: 0	mode
		0	Parity disabled
		1	Reserved
		2	Enable Enable odd
		3	parity even parity
3	USBS	Stop Bit Selection bit. Select the number of bits of stop bits.	
		USBS	Stop Bit
		0	1