		Value to be output to a polarity comparator waveform signal, and configure COM0B Bit and set FOC0B Bits to change its polarity, enabling to avoid OC0B Signal to its respective IO Unwanted disturb pulse produced after the pin.
5: 3		Retention
2	OCF0B	TC0 Output Compare B Matching flag. when TCNT0 equal OCR0B , The comparison unit signals a match, the comparison flag is set and OCF0B . If the output of the comparator at this time B Interrupt Enable OCIE0B for "1" And the Global interrupt flag is set, it will produce output compare B Interrupted. When you do this the interrupt service routine OCF0B Will be automatically cleared or OCF0B Write bit "1" Also clears the bit.
1	OCF0A	TC0 Output Compare A Matching flag. when TCNT0 equal OCR0A , The comparison unit signals a match, the comparison flag is set and OCF0A . If the output of the comparator at this time A Interrupt Enable OCIE0A for "1" And the Global interrupt flag is set, it will produce output compare A Interrupted. When you do this the interrupt service routine OCF0A Will be automatically cleared or OCF0A Write bit "1" Also clears the bit.
0	TOV0	TC0 Overflow flag. When the counter overflows, the overflow flag is set TOV0 . If this time overflow interrupt enable TOIE0 for "1" And the Global interrupt flag is set, it will generate an overflow interrupt. When you do this the interrupt service routine TOV0 Will be automatically cleared or TOV0 Write bit "1" Also clears the bit.

DTR0 - TC0 Dead time control register

DTR0 - TC0 Dead time control register								
address: 0x4F					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	DTR07	DTR06	DTR05	DTR04	DTR03	DTR02	DTR01	DTR00
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
[7: 4]	DTR0H	TC0 Dead time register high. when TCCR0B Register DTEN0 Bit "1" Time, OC0A with OC0B Composition complementary outputs, the insertion of dead time control is enabled, OC0B The upper channel dead time inserted by the DTR0H It determines the length of time for DTR0H Clock count corresponding to the time.
[3: 0]	DTR0L	TC0 Dead time register lower. when TCCR0B Register DTEN0 Bit "1" Time, OC0A with OC0B Composition complementary outputs, the insertion of dead time control is enabled, OC0A The upper channel dead time inserted by the DTR0L It determines the length of time for DTR0H Clock count corresponding to the time.