T1 / OC0B / PCINT21- port D Pin 5

T1: Timer / Counter 1 External count clock input

OC0B: Timer / Counter 0 of B Group match output. PD5 As timer / counter 0 Compare match outside. At this point must DDD5 The output pin is set. Simultaneously, OC0B Also timer 0 of PWM Mode output pin

PCINT21: Pin Change Interrupt twenty one

XCK / T0 / DAO / PCINT20- port D Pin 4

XCK: Synchronous mode USART The external clock signal

T0: Timer / Counter 0 External count clock input

DAO: internal 8 Place DAC Analog Output

PCINT20: Pin Change Interrupt 20

INT1 / OC2B / PCINT19- port D Pin 3

INT1: External interrupt input 1

OC2B: Timer / Counter 2 of B Group match output. PD3 As timer / counter 2 Compare match outside. At this point must DDD3 The output pin is set. Simultaneously, OC2B Also timer 2 of PWM Mode output pin

PCINT19: Pin Change Interrupt 19

INT0 / OC3B / AC0O / PCINT18- port D Pin 2

INT0: External interrupt input 0

OC3B: Timing counter 3 Compare Match Output B . only at QFP32 When the package, PD2 versus QFP48 / PF2 Merge into one IO ,therefore PF2 Up OC3B It will also feature PD2 Output

AC0O: Analog comparator 0 Direct comparison output. by AC0FR Register control

PCINT18: Pin Change Interrupt 18

TXD / OC3A / PCINT17- port D Pin 1

TXD: transfer data(USART Data output). USART After the transmitter is enabled, PD1 It is forced to output, from DDD1 control

OC3A: Timing counter 3 Compare Match Output A . only at QFP32 When the package, PD1 versus QFP48 / PF1 Merge into one IO ,therefore PF1 Up OC3A It will also feature PD1 Output

PCINT17: Pin Change Interrupt 17

RXD / PCINT16- port D Pin 0

RXD: transfer data(USART data input). USART The receiver is enabled, PD0 They will be forced to enter, without DDD0 control. When the pin is USART Forced to enter, via the pull-up resistors PORTD0 Level control

PCINT16: Pin Change Interrupt 16