by E2PCTL Access Interface E2PROM Simulated space:

E2PCTL Analog controller E2PROM Data access interface logic FLASH space. simulation E2PROM stand by 8 Position, 16 Bits and 32 Data read and write access bit width. 8 Byte mode E2PROM Better compatibility with the interface. 32 Bit mode and will help improve storage efficiency FLASH Of life, and therefore 32 Bit reads and writes for the proposed read-write mode. E2PROM Analog interface supports continuous write mode, the need to update multiple consecutive address data applications, the obvious advantages, is recommended.

for LGT8F88P / 168P ,data FLASH Independent storage space. Without going through ECCR And enable register configuration FLASH Data space. LGT8F328P And no independent data FLASH Space data FLASH And procedures FLASH shared 32K byte FLASH space. Need ECCR Enabling data register FLASH Partition function, and by ECCR Register ECS [1: 0] Bit configuration data FLASH the size of. The configuration takes effect, use other methods and LGT8F88P / 168P the same.

FLASH The controller in the realization E2PROM Interface, the interior has been achieved automatically erased when the necessary data FLASH The logic, EPROM Erase command is optional, this command is only used when the user needs to perform individually erased.

EECR Register control FLASH Erase / write timing, including program FLASH with E2PROM . The particular type of operation required by EECR Register EEPME with EEPM [3: 0] set up. Correct E2PROM Read operation is relatively simple, after setting a good destination address and patterns, write EERE Will come into target address corresponding 32 Bit data read FLASH An internal controller, the user can EEDR Read byte register interest. FLASH The controller does not implement the program FLASH Read space, the user can easily use LPM Or by program FLASH At unified mapping space using address data

LD / LDD / LDS Instruction read.

1.8 Bit mode, programming E2PROM

- To set the target address EEARH / L register
- To set up new data EEDR register
- Set up EEPM [3: 1] = 000 , EEPM [0] Can be set 0 or 1
- Set up EEMPE = 1 , Simultaneously EEPE = 0
- Within four cycles, provided EEPE = 1

When the setting is completed, FLASH The controller will start the programming operation, the programming period CPU It will remain on the current instruction address, will continue to run until after the operation is completed. During programming, if the data needs to be erased FLASH , FLASH The controller will start erasing process automatically.

2.32 Bit mode, programming E2PROM

- by E2PD0 ~ 3 ,ready 32 Bit data
- To set the target address EEARH / L register. Note that this is byte-aligned address, FLASH Controller with EEAR [15: 2] As access FLASH the address of.
- Set up EEPM [3: 1] = 010 , EEPM [0] Can be set 0 or 1
- Set up EEMPE = 1 , Simultaneously EEPE = 0
- Within four cycles, provided EEPE = 1

3.8 Bit mode, Reading E2PROM

- To set the target address EEARH / L register
- Set up EEPM [3: 1] = 000
- Set up EERE = 1 start up E2PROM Read
- wait 2 Cycles (two execution NOP operating)
- Data corresponding to the target address is updated to EEDR register