Change is through to the ADCSRA Register ADSC Write bit "1" To start. In this mode, subsequent ADC Conversion does not depend on ADC Interrupt flag ADIF Whether set.

If enabled automatic trigger set ADCSRA Register ADSC Will start a single conversion. ADSC Flag may also be used to detect the conversion is in progress. Regardless of how the conversion is started, during the conversion process ADSC Has been "1" .

Prescaler and ADC Conversion Timing

By default, the successive approximation circuitry requires an 300KHz To 3MHz The input clock to get maximum resolution. If the conversion is less than the desired accuracy 12 Bits, then the input clock frequency may be higher than 3MHz In order to achieve a higher sampling rate.

ADC Module comprises a prescaler, which may be generated by the system clock acceptable ADC The input clock. By prescaler ADCSRA Register ADPS Bit set. Position ADCSRA Register ADEN Will enable ADC The prescaler starts counting. as long as ADEN Bit "1" The prescaler will continue counting until ADEN Is cleared.

ADCSRA Register ADSC After being set, the next single-ended conversion ADC The rising edge of the clock cycle started. A normal conversion takes 15 More ADC Clock cycle. ADC Enable(ADCSRA Register ADEN Rear-bit) need 50 More ADC Initializing analog circuits of input clock cycles before it can first be converted effectively.

in ADC The conversion process, the sample-hold after the conversion starts 1.5 More ADC Enter the clock starts, and for the first time ADC The output of the conversion takes place after the start of 14.5 More ADC The input clock. After the conversion, ADC The results are fed ADC Data register, and ADIF Flag is set. ADSC While being cleared. After the software can be set again ADSC Logo or automatic trigger, which initiates a new conversion.

And a reference voltage sampling channels

ADMUX Register MUX and REFS Single buffered through a temporary register. CPU It may be random access to a temporary register. Before starting the conversion, CPU Channel at any time and may be selected reference source is arranged. to ensure that ADC A sufficient sampling time, soon after the start of the conversion, you can not configure a selected channel and reference. In the conversion is complete (ADCSRA Register ADIF After the set), and select the reference channel sources will be updated. The conversion starts to ADSC The next set after ADC Edge of the clock input. Therefore, we recommend users set ADSC After a ADC Input clock cycles, do not operate ADMUX To select the new channel and the reference source.

With automatic trigger, time trigger events is uncertain. In order to control the impact of the new set of conversion, updated ADMUX Be careful when register. If the ADATE and ADEN Are set, the downtime can occur at any time, thereby triggering automatic start ADC Conversion. If you change during this period ADMUX Contents of the register, then the user will not be able to distinguish a conversion is old or new configuration based on the configuration. It is recommended for the following security time ADMUX Updated:

1) ADATE or ADEN Bit "0" ;

2) During the conversion process, but at least after the occurrence of a trigger event ADC Input clock period;

3) After the conversion is complete, but before the interrupt trigger source flag is cleared. If the update in either case mentioned above ADMUX Before, the new configuration will take effect the next conversion. select ADC It should be noted when the input channel, before starting the conversion to selected passages in ADSC After a set ADC After the clock cycle you can choose a new analog input channels, but the easiest way is to wait until after the end of the conversion and then change the channel.