

## LGT8XM GENERAL PURPOSE REGISTER

	7	0	Addr.	
G E N E R A L  W O R K I N G  R E G I S T E R	R0		0x00	
	R1		0x01	
	R2		0x02	
	...			
	R13		0x0D	
	R14		0x0E	
	R15		0x0F	
	R16		0x10	
	R17		0x11	
	...			
	R26		0x1A	<b>X</b> Register Low Byte
	R27		0x1B	<b>X</b> Register High Byte
	R28		0x1C	<b>Y</b> Register Low Byte
	R29		0x1D	<b>Y</b> Register High Byte
	R30		0x1E	<b>Z</b> Register Low Byte
	R31		0x1F	<b>Z</b> Register High Byte

Most of the instructions operating on the Register File have direct access to all registers, and most of them are single cycle instructions. As shown in the figure above, each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y- and Z-Pointer registers can be set to index any register in the file.

### X/Y/Z REGISTER

Registers R26...R31 can be combined in pairs to form three 16-bit registers. These three 16-bit registers are mainly used as address pointers for indirect addressing access. The X/Y/Z registers are structured as follows:

	15	XH		XL	0
<b>X REGISTER</b>	7	0	7	0	
	R27 (0x1B)		R26 (0x1A)		
	15	YH		YL	0
<b>Y REGISTER</b>	7	0	7	0	
	R29 (0x1D)		R28 (0x1C)		
	15	ZH		ZL	0
<b>Z REGISTER</b>	7	0	7	0	
	R31 (0x1F)		R30 (0x1E)		

These registers are used as fixed offset, auto-increment, and auto-decrement address pointers in different addressing modes. See the Instruction Description section for details.