UCSRB - USPI Control and status registers B

		· ·	ICSRB - USPI Co	ontrol and statu	s registers B				
address:	0xC1			Defaults	Defaults: 0x00				
Bit	7	6	5	4	3	2	1	0	
Name RXCIE		TXCIE	UDRIE	RXEN	TXEN	-	-	-	
R/W	R/W	R/W	R/W	R/W	R/W	-	-	-	
Bit Nam	ne description	1							
7	RXCIE	Receive Complete interrupt enable bit. After setting enabling RXC Interruption, after clearing ban RXC Interrupted. when R for "1", The global interrupt enable, UCSRA Register RXC for "1" Can generate when USPI Receive Complete interrupt.							
6	TXCIE	End of Transmit Interrupt Enable bit. After setting enabling TXC Interruption, after clearing ban TXC Interrupted. when for "1", The global interrupt enable, UCSRA Register TXC for "1" Can generate when USPI Transmit Complete interruption.							
5 UD	PRIE	Data Register Empty when UDRIE for "1" Empty interrupt.	·	-	•	•	•	·	
4	RXEN	Receive Enable bit. After starting set USPI receiver. RxD Universal pin IO Function is USPI Receiving group. Disabling the Receiver will flush the receive buffer.							
3	TXEN	Transmit Enable bit. After starting set USPI Transmitter. TxD Universal pin IO Function is USPI Transmitting the group. TXEN When cleared, only to wait until all the data is sent to truly complete ban USART send.							

UCSRC- USART Control and status registers C

		ucs	RC - USART C	ontrol and statu	s registers C					
address:	: 0xC2		Defaults: 0x86							
Bit	7	6	5	4	3	2	1	0		
Name	UMSEL1 UMS	SELO -		-	-	DORD UCPHA UCPOL				
R/W	R/W	R/W	-	-	- R / W		R/W	R/W		
Bit	Name descripti	on								
		UMSEL Select synchronous or asynchronous modes of operation. UMSEL mode								
7: 6 U	MSEL1: 0	0123		USART Asynchronous mode of operation USART Synchronous mode of operation						
				SPI Slave modes of operation SPI The host operating mode						
5: 3	-	USPI Under Rese	erved.							