		OCR3AL with OCR3AH Incorporated into the composition together 16 Bit OCR3A . Read and write 16 Bit register requires two operations. write 16 Place OCR3A When, you should write OCR3AH . read 16 Place OCR3A When, it should read OCR3AL . OCR3A Continuously with the counter value TCNT3 Compare. Compare match can be used to generate an output compare interrupt, or Who used to OC3A Waveform generation pins. When PWM When mode, OCR3A Using double buffered registers. The normal mode and clear mode match , The double buffering is disabled. Double buffering may be updated OCR3A Register with the maximum or minimum counting time Synchronize, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR3A When the buffer register, double buffering is disabled CPU Access is OCR3A itself.

OCR3BL-TC3 Output Compare Register B Low byte

OCR3BL - TC3 Output Compare Register B Low byte								
address: 0x9A					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OCR3BL7	OCR3BL6	OCR3BL5	OCR3BL4	OCR3BL3	OCR3BL2	OCR3BL1	OCR3BL0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	OCR3BL	Output Compare Register B The low byte. OCR3BL with OCR3BH Incorporated into the composition together 16 Bit OCR3B . Read and write 16 Bit register requires two operations. write 16 Place OCR3B When, you should write OCR3BH . read 16 Place OCR3B When, it should read OCR3BL . OCR3B Continuously with the counter value TCNT3 Compare. Compare match interrupt can be used to generate an output compare, Or used OC3B Waveform generation pins. When PWM When mode, OCR3B Using double buffered registers. The normal mode and the mode matching cleared Type, the double buffering is disabled. Double buffering may be updated OCR3B The count register when the maximum or minimum value Engraved synchronize, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR3B When the buffer register, double buffering is disabled CPU Access is OCR3B itself.							

OCR3BH-TC3 Output Compare Register B High Byte

OCR3BH - TC3 Output Compare Register B High Byte								
address: 0x9B					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OCR3BH7	OCR3BH6	OCR3BH5	OCR3BH4	OCR3BH3	OCR3BH2	OCR3BH1	OCR3BH0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	OCR3BH	Output Compare Register B The high byte. OCR3BL with OCR3BH Incorporated into the composition together 16 Bit OCR3B . Read and write 16 Bit register requires two operations. write 16 Place OCR3B When, you should write OCR3BH . read 16 Place OCR3B When, it should read OCR3BL . OCR3B Continuously with the counter value TCNT3 Compare. Compare match can be used to generate an output compare interrupt, or Who used to OC3B Waveform generation pins. When PWM When mode, OCR3B Using double buffered registers. The normal mode and the mode matching cleared Type, the double buffering is disabled. Double buffering may be updated OCR3B The count register when the maximum or minimum value Engraved synchronize, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses.							