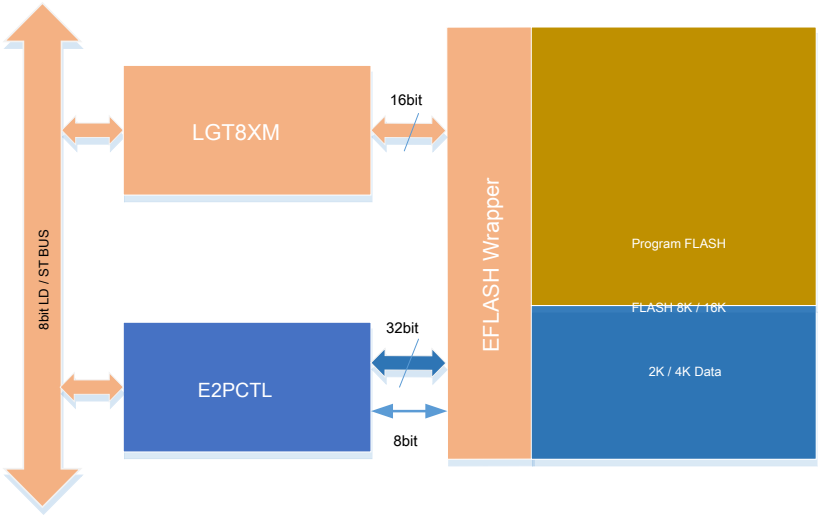
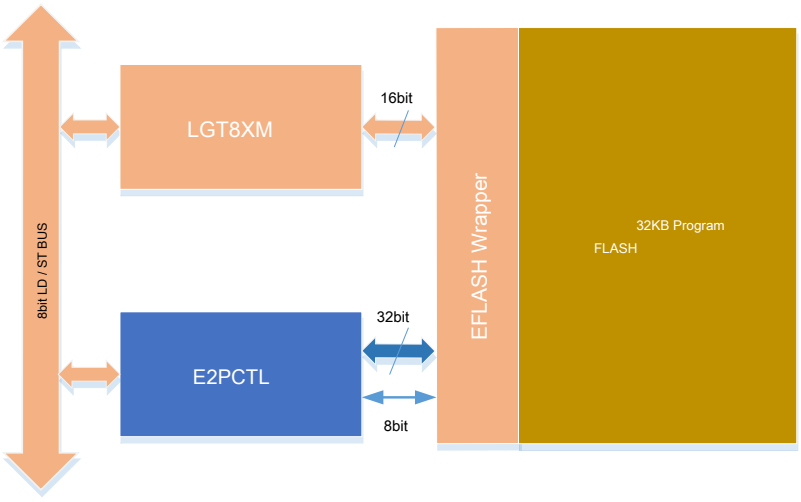
Dynamic firmware upgrade function. by FLASH Controller Access Program FLASH Space program, supports only Page Erase (1024 Byte) and 32 Read and write access bit width.

LGT8F88D / 168D E2PCTL FIG controller architecture



E2PCTL simulation E2PROM Function to access data FLASH When the space can support 8 Position, 32 Write bit width. Access program FLASH When space, support and page erase 32 Bit data read and write. due to LGT8FX8P internal FLASH The minimum storage unit 32 Position, it is recommended use 32 Bit access, especially for write operations. 32 Read and write operations not only efficient bit access, but also conducive to the protection of FLASH Endurance memory cell.

LGT8F328P E2PCTL FIG controller architecture



LGT8F328P No extra internal data FLASH. therefore, LGT8XM Core and E2PCTL Share internal 32K byte FLASH storage. Users can, will 32K byte FLASH Space is divided into program space and data space. By configuring E2PCTL The controller may set the analog E2PROM The size of the space. E2PCTL Use paging mode analog E2PROM Logic algorithm page (1K Bytes). Therefore simulation 1K Byte E2PROM Space, need to occupy 2K Byte FLASH Space, and so on, to achieve 4K Byte E2PROM , Take up 8K Byte

FLASH space. Specific implementations, please refer to E2PCTL Description of the algorithm implementation.