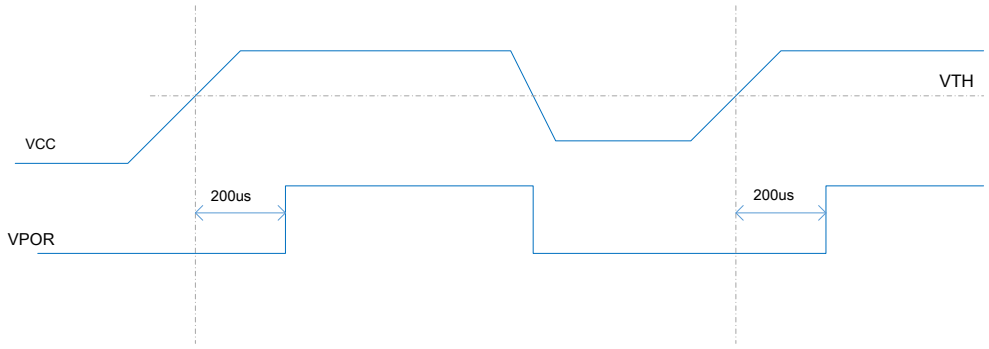
Power-On Reset

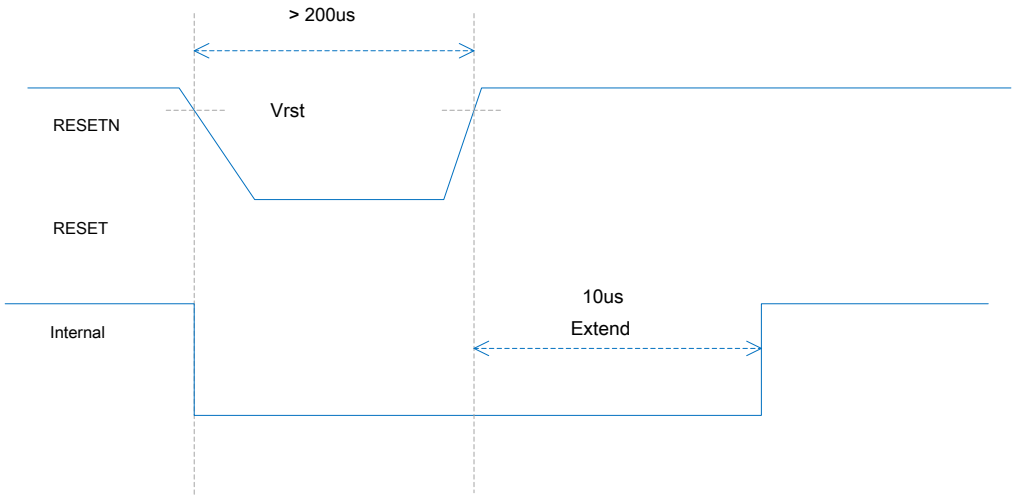
Power-on reset signal is generated internally by the voltage detection circuit. When the system power supply (VCC) Below detection threshold, the power-on reset signal is active. Power-on reset detection threshold, refer to the portion of electrical parameters.

On reset circuitry to ensure that the chip in the reset state during power-on, can be run from a known stable state After power. Power-on reset signal inside the chip will be broad exhibition counter, to ensure that after power inside the various analog blocks, such as RC Oscillator to enter the steady-state operation.



External reset

In the external reset pin (RSTN) Applying a low level on the external reset immediately effective. Greater than a width of the low minimum reset pulse width requirement. External reset is asynchronous reset, even if there is no clock chip, external reset will still be able to reset the chip. LGT8FX8P The external reset pin also can be used as general-purpose I / O use. After the chip is powered on, The default as an external reset function. Users can register configuration, external reset function off the pin, so that can be used as an ordinary I / O use. Please refer to the specific use IOCR Description section of the register.



Low-voltage detection (LVD) Reset

LGT8FX8P Internal comprises a programmable low voltage detector (LVD) Circuit. LVD The same is detected VCC Voltage variation, but different from the power reset is LVD Voltage threshold detector may be selected. The user can directly operate VDTCR
Register selection between different voltage threshold. LVD A voltage detection circuit having ± 10mV ~ ± 50mV Hysteresis characteristics for filtering VCC Jitter voltage. when LVD When enabled, if VCC The reset voltage drops to the set threshold, LVD Reset effective immediately. when VCC After reset is increased above the threshold, resetting the internal circuit starts to expand, will continue to stretch at least a reset 1 millisecond.