Receiver ignored. After each bit of the received data into the receive shift register receives the first stop bit, the receiver set positioned UCSRA Receive data register completion flag RXC Bit shift register and the complete data frame is transferred to the receive buffer, CPU By reading UDR Register may obtain received data.

receive 9 Bit data frame

If you set 9 Data frame bit data, from UDR Low reading 8 Bit register must be read before data UCSRB of RXB8 To get the first bit 9 Bit data. This rule also applies to the state flag FE , DOR as well as PE . Read UDR Location will change the state of the reception buffer, and then change likewise stored in the buffer TXB8 , FE , DOR and PE Bit.

Reception complete flag and interrupt handling

USART The receiver has a flag: Reception complete flag RXC , To indicate whether or not the data read out of the receive buffer. When the receive buffer data is not read, this bit "1" , Otherwise "0" . If the receiver is disabled, the receive buffer will be flushed, RXC It will be cleared. Position UCSRB Receive Complete Interrupt Enable bit RXCIE After long RXC Flag is set (provided that global interrupts are enabled), it will have USART Receive Complete interrupt. When interrupt-driven data reception, data reception from the end of the interrupt service routine must UDR Read data cleared RXC Logo, or as long as the interrupt handler to an end, a new interrupt will occur.

Receive error flag

USART The receiver has three error flags: Frame Error FE The data overflow DOR And parity error PE . They are located in UCSRA register. Error flag together with the frame in a receive buffer them. All error flags can generate interrupts. Framing Error FE The first bit indicates that a state in which a stop-readable frame stored in the reception buffer. Stop bits correctly (value "1")then FE Flag "0" ,otherwise FE Flag "1" . This flag is used to detect loss of synchronization, the transmission is interrupted, the protocol handling. Data overflow flag DOR Due to indicate that the receive buffer is full caused data loss. When the receiving buffer is full, the receive shift register existing data, if detected at this time a new start bit, data overrun occurs. DOR That flag is set to indicate that a read recently UDR And next read UDR Lost between one or more data frames. When the data frame is successfully transferred to the receive buffer from the shift register, DOR Flag is cleared. Parity Error Flag PE Next frame indicates that the received data had a parity error buffer upon reception. If parity is not enabled, PE Is cleared.

Parity Checker

Parity mode bits set UPM1 Will launch parity checker. Check pattern (even or odd) of UPM0 Decision. After the parity is enabled, the verifier calculates parity data input and the result of the parity bit data frame is compared. The verification result is stored in the reception buffer with the data and stop bits. CPU By reading PE Check whether the received frame bit parity error among them. If a next data read out from the receive buffer had a parity error, and parity is enabled, then UPE Is set, the receive buffer remain valid UDR To be read.