"1" .

Clock frequency determined in the following formula:

BAUD = f_{sys} / (2 * (UBRR + 1))

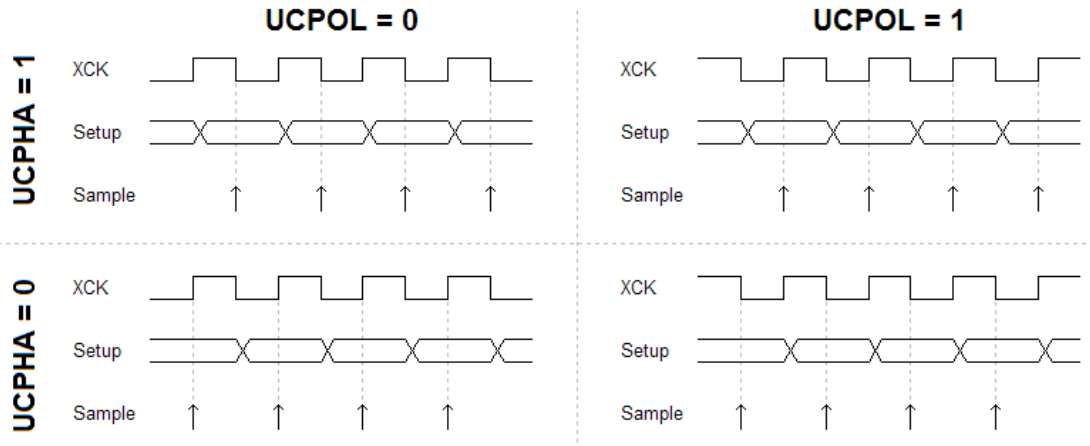
when SPI Operating in slave mode, the communication clock provided by the external host, from XCK Pin input, XCK Pin data direction register (DDR_XCK) Must be set "0" .

SPI Data mode and timing

SPI There are four kinds of combinations of polarity and clock phase, there are control bits UCPHA with UCPOL Determined, specific control and shown below in the following table:

SPI Operating mode

SPI mode	UCPOL	UCPHA	Starting along	Trailing Edge
0	0	0	The rising edge of sampling	Setting falling
1	0	1	Rising settings	Sampling falling
2	1	0	Sampling falling	Rising settings
3	1	1	Setting falling	The rising edge of sampling



SPI Work mode icon

Frame format

SPI A serial frame may start from the lowest or highest position, to the high or low end position, a total of 8 Bit data. After the end of a frame to be transmitted immediately a new frame, end of transmission to the data line pulled to the idle state.

data transmission

SPI Put UCSRB Register TXEN Bit "1" To enable the transmitter, TxD Pin is occupied by a transmitter transmits the serial output data. At this time, the receiver may not be enabled.

SPI Put UCSRB Register RXEN Bit "1" To enable the receiver, RxD Pin occupied by the receiver to receive the serial input data. At this point the transmitter must be enabled.

SPI Are used to send and receive XCK To as the transfer clock.

Before the first of the communication SPI Initialized. The initialization process normally includes setting the baud rate setting, the bit transmission order of the frame data, and if necessary, to enable the receiver or transmitter. For interrupt-driven SPI Operation, initialization