SREG Register Definition

SREG System status register								
address: 0x3F (0x5F)				Defaults: 0x00				
Bit	7	6	5	4	3	2	1	0
Name	I	T	H	S	V	N	Z	C
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit Definitions		
[0]	C	The carry flag indicates arithmetic or logic operation results in a carry Refer INSTRUCTIONS
[1]	Z	Zero flag indicating the result of an arithmetic or logic operation is zero, refer to the instruction description section
[2]		N Negative flag indicating arithmetic or logic operation produces a negative number, please refer to the instruction described Said portion
[3]		V Overflow flag, two's-complement operation result indicates overflow, refer to the instructions described Said portion
[4]	S	Sign bit, equivalent to N versus V XOR operation result, specific instructions refer to the description section
[5]		H Half Carry Flag, in BCD Useful in the operation, it indicates a half-byte Operations produced into Place
[6]	T	Temporary, bit copy (BLD) And bit memory (BST) Instructions for use, T Bit position as a temporary storage for temporarily storing the value of a general register bit. Refer to command description section
[7]	I	Global interrupt enable bit, this bit must be set to 1 In order to enable the kernel interrupt response events. Different interrupt sources are controlled by independent control bits. Global interrupt enable bit is the interrupt signal control entered the final barrier kernel. I Interrupt vector bit is automatically cleared by hardware in response to the kernel, in the interrupt return instruction (RETI) After automatically set. I Bit can also be used SEI with CLI Instruction changes, refer to the instruction description section

General purpose working registers

The general purpose registers LGT8XM Instruction set architecture optimization. In order to achieve efficiency and flexibility needed to execute the kernel, LGT8XM Internal general purpose working registers to support what several access modes:

- One 8 Read a bit at the same time 8 Bit write operation

- Two 8 Read a bit at the same time 8 Bit write operation

- Two 8 Read a bit at the same time 16 Bit write operation

- One 16 Read a bit at the same time 16 Bit write operation