		when TCNT2 equal OCR2B , The comparison unit signals a match, the comparison flag is set and OCF2B . If the output of the comparator at this time B Interrupt Enable OCIE2B for "1" And the Global interrupt flag is set, it will produce output compare B Interrupted. When you do this the interrupt service routine OCF2B Will be automatically cleared or OCF2B Write bit "1" Also clears the bit.
1	OCF2A	TC2 Output Compare A Matching flag. when TCNT2 equal OCR2A , The comparison unit signals a match, the comparison flag is set and OCF2A . If the output of the comparator at this time A Interrupt Enable OCIE2A for "1" And the Global interrupt flag is set, it will produce output compare A Interrupted. When you do this the interrupt service routine OCF2A Will be automatically cleared or OCF2A Write bit "1" Also clears the bit.
0	TOV2	TC2 Overflow flag. When the counter overflows, the overflow flag is set TOV2 . If this time overflow interrupt enable TOIE2 for "1" And the Global interrupt flag is set, it will generate an overflow interrupt. When you do this the interrupt service routine TOV2 Will be automatically cleared or TOV2 Write bit "1" Also clears the bit.

ASSR - Asynchronous Interface Status Register

ASSR - TC2 Asynchronous Interface Status Register								
address: 0xB6					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	INTCK	-	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB
R / W	R / W	-	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	INTCK	Asynchronous clock selection control bits. When set INTCK Bit 1 , The internal selection RC32K An asynchronous clock source. When set INTCK Bit 0 When selecting the external asynchronous crystal clock as the clock source.
6	-	Reservations.
5	AS2	Timer 2 Asynchronous mode selection control bits. When set AS2 Bit 1 When the timer 2 Work for asynchronous mode, clock source INTCK Bits to select. When set AS2 Bit 0 When the timer 2 Working synchronous mode, the clock source Clk $_{IO}$. when AS2 The value changes, TCNT2 , OCR2A , OCR2B , TCCR2A with TCCR2B Value of the register may be incorrect, you need to be reconfigured.
4	TCN2UB	TCNT2 Register update flag. When the timer 2 Work in asynchronous mode, for TCNT2 When a write operation, TCN2UB Bit is set. when TCNT2 After the updated value of the hardware will be cleared TCN2UB Bit. Only when TCN2UB Bit 0 When, available for TCNT2 Updated.
3	OCR2AUB	OCR2A Register update flag. When the timer 2 Work in asynchronous mode, for OCR2A When a write operation, OCR2AUB Bit is set. when OCR2A After the updated value of the hardware will be cleared OCR2AUB Bit. Only when OCR2AUB Bit 0 When, available for OCR2A Updated.
2	OCR2BUB	OCR2B Register update flag. When the timer 2 Work in asynchronous mode, for OCR2B When a write operation, OCR2BUB Bit is set. when OCR2B After the updated value of the hardware will be cleared OCR2BUB Bit. Only when OCR2BUB Bit 0 When, available for OCR2B Updated.