	08	07	PB7 / XTALI PB7: Programmable port B7`
12			
			XTALI: Crystal IO Input port
	09	08	PD5 / RXD * / T1 / OC0B PD5: Programmable
13			port D5 RXD: USART Receiving data
			(optional)
			T1: Timer 1 External clock input
			OC0B: Timer 0 Compare Match Output B
14			PD6 / TXD * / OC0A PD6: Programmable port D6
	10	09	TXD: USART Data transmission (optional)
			No. 30 at 1 Data tanonicon (optional)
			OC0A: Timer 0 Compare Match Output A
			ACOP / 0C3A ACOP: Analog comparator 0 Positive
			input
			OC3A: Timer 3 Compare Match Output A
			PD7 / ACXN PD7: Programmable port D7 ACXN: Analog
16	11	10	comparator 0/1 Public negative input
	••		os. parace of the association and
17	-		PF7 / OC2B PF7: Programmable port F7 OC2B: Timer 2
			Compare Match Output B
			Compare materi output D
			PB0 / ICP1 PB0: Programmable port B0
18	12	11	ICP1: Timer 1 Capture input
			13. II. Iiilida T Gaptaid Input
19	13		PB1 / OC1A PB1: Programmable port B1 OC1A: Timer 1
			Compare Match Output A
	14	12	PB2 / OC1B / SPSS PB2: Programmable port B2
			OC1B: Timer 1 Compare Match Output B SPSS: SPI Slave
20			Chip Select Mode
twenty	twenty one		GND
twenty t	twenty two		vcc
	thre d 5	12	PB3 / MOSI / OC2A PB3: Programmable port
£			B3 MOSI: SPI Master Out / Slave
twenty t			
			OC2A: Timer 2 Compare Match Output A
twenty f	four16	13	PB4 / MISO PB4: Programmable port B4 MISO:
			SPI A host input / output slave
25	17	14	PB5 / SPCK / AC1P PB5: Programmable
			port B5 SPCK: SPI Clock signal
			AC1P: Analog comparator 1 Positive input