Transmission of a complete frame.

send 9 Bit data frame

If you send 9 Bit data frame, the data should first of 9 Bit write register UCSRB of TXB8 Bit, then low 8

Data written to the transmit data register bit UDR . The first 9 Communication in a multi-bit data for indicating an address frame, the synchronous communications protocol may be used for processing.

Parity bit is sent

Parity generation circuit to generate a serial data frame corresponding check bits. When the parity bit is enabled (UPM1 = 1), The transmission control logic circuit inserts the parity bits between the last and the first data word of a stop bit.

Send flag and interrupt handling

USART Transmitter has two flags: USART Data register empty flag UDRE And the transmission end flag TXC , Two flags can generate interrupts. Data register empty flag UDRE It is used to indicate whether the transmit buffer to write a new data. This bit is set when the transmit buffer is empty "1" Full time is set "0" . when UDRE Bit "1" Time, CPU Data can go register UDR Write new data, not vice versa. when UCSRB Data register empty interrupt enable register bit UDRIE for "1" When, as long as UDRE Is set (and global interrupts are enabled), will produce USART Data Register empty interrupt request. To register UDR The write operation will be cleared UDRE . When the interrupt transmission of data in the data register empty interrupt service routine must write new data to a UDR

To clear UDRE , Or disable the Data Register Empty interrupt. Otherwise, if the interrupt service routine ends, a new interrupt will occur again.

When the entire data frame is sent out of the shift register while the register and no new transmission data, the transmission end flag TXC It will be set. when UCSRB Send the end of last interrupt enable bit TXCIE (And the Global Interrupt Enable) "1" When, as TXC Flag is set, USART Transmit Complete Interrupt will be executed. Once in the interrupt service routine, TXC Flag, this is automatically cleared, CPU This bit can also write "1" Cleared.

Disable the transmitter

when TXEN When cleared, and all the data only after the completion of transmission the transmitter can really disabled, i.e., the transmit shift register and the transmit data buffer register are not to be transmitted. Transmitter disabled later, TxD Pin restore its versatility IO Features.

receiver

Position UCSRB Receive register enable bits (RXEN) To start USART receiver. After the can RxD Universal pin IO Function is USART Functionality substituent's serial input port of the receiver. Before receiving the data must first set the baud rate, and the operating mode frame format. If synchronous receive mode, XCK On the clock pin is used as transfer clock.

receive 5 To 8 Bit data frame

Once the receiver detects a valid start bit, they start to receive data. Each bit that follows the start bit will be set or baud XCK Clock received until the stop bit is received the first frame data, the second stop bit will be