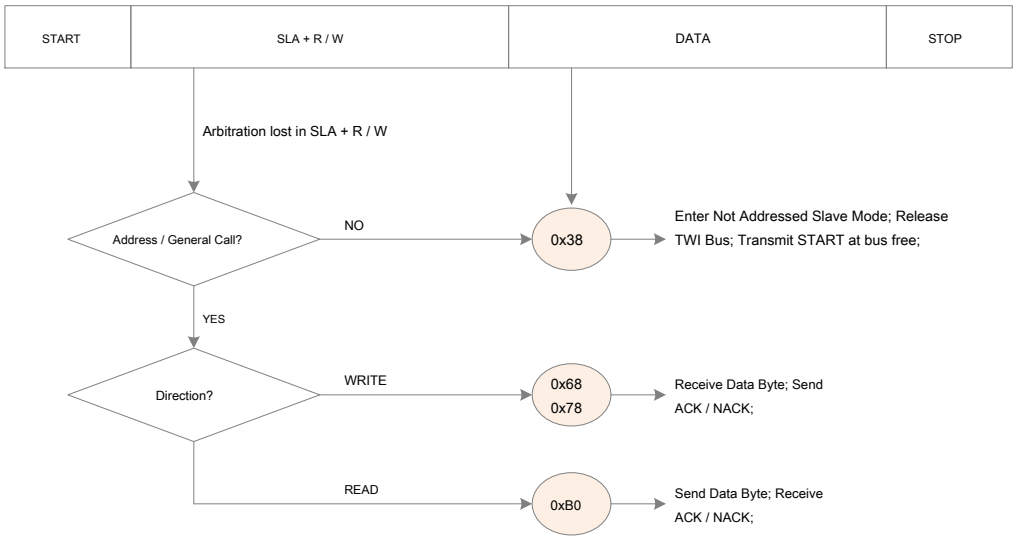
Site, it will switch to a new transmission not addressed slave mode, or idle waiting for the bus from START Signal, depending on the operation of the application software.

The following diagram describes a bus arbitration procedure:



Bus arbitration process map

Register Definition

TWI Register List

register	address	Defaults	description
TWBR	0x B8	0x00	TWI Bit Rate Register
TWSR	0xB9	0x00	TWI Status Register
TWAR	0xBA	0x00	TWI Address register
TWDR	0xBB	0x00	TWI Data register
TWCR	0xBC	0x00	TWI Control register
TWAMR	0xBD	0x00	TWI Address mask register

TWBR - TWI Bit Rate Register

TWBR - TWI Bit Rate Register								
address: 0xB8					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	TWBR7	TWBR6	TWBR5	TWBR4	TWBR3	TWBR2	TWBR1	TWBR0
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	TWBR [7: 0]	TWI Bit rate select bit. TWBR It is a bit rate generator division factor. Bit rate generator is a frequency divider, for generating in the host mode SCL clock. The bit rate is calculated as follows: $f_{scl} = f_{sys} / (16 + 2 * TWBR * 4^{TWPS})$.