

LGT8XM GENERAL WORKING REGISTER

	7	0	Addr.	
G E N E R A L W O R K I N G R E G I S T E R		R0	0x00	
		R1	0x01	
		R2	0x02	
		...		
		R13	0x0D	
		R14	0x0E	
		R15	0x0F	
		R16	0x10	
		R17	0x11	
		...		
		R26	0x1A	X Register Low Byte
		R27	0x1B	X Register High Byte
		R28	0x1C	Y Register Low Byte
		R29	0x1D	Y Register High Byte
		R30	0x1E	Z Register Low Byte
		R31	0x1F	Z Register High Byte

Most of the instructions have direct access to all of the general working registers, and most of them are also single-cycle instructions. As shown in the figure above, each register corresponds to the address of a data storage space, and these general working registers are mapped to the data storage space. These registers only really exist in SRAM, but this unified mapping storage organization gives them a lot of flexibility. The X/Y/Z register can be indexed as a pointer to any general purpose register.

X/Y/Z REGISTER

Registers R26...R31 can be combined in pairs to form three 16-bit registers. These three 16-bit registers are mainly used as address pointers for indirect addressing access. The X/Y/Z registers are structured as follows:

	15	XH		XL	0
X REGISTER	7	0	7	0	
	R27 (0x1B)		R26 (0x1A)		
	15	YH		YL	0
Y REGISTER	7	0	7	0	
	R29 (0x1D)		R28 (0x1C)		
	15	ZH		ZL	0
Z REGISTER	7	0	7	0	
	R31 (0x1F)		R30 (0x1E)		

These registers are used as fixed offset, auto-increment, and auto-decrement address pointers in different addressing modes. See the Instruction Description section for details.