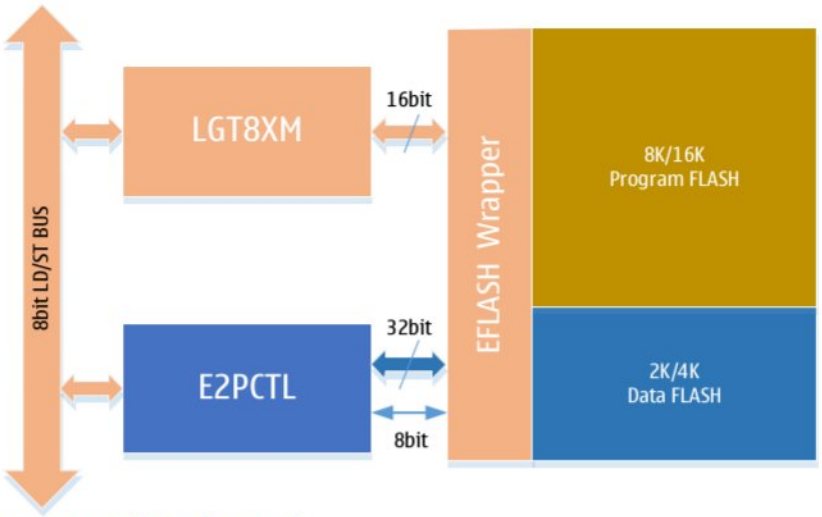
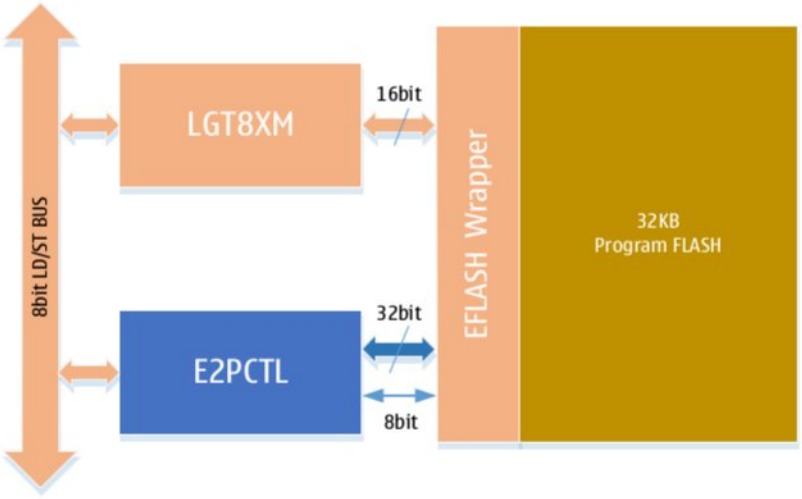
Figure 7. LGT8F88D/168D MemCon (E2PCTL) Block Diagram



MemCon FLASH Controller (Cont.)

When the MemCon (E2PCTL) is in the emulated E2PROM mode, it supports 8-bit and 32-bit read/write widths. It supports 32-bit read/write when accessing FLASH Program Memory. The entire FLASH Memory of the LGT8FX8P is mapped as 32 bits. Therefore it is recommended to use 32-bit access, especially for programming operations. The 32-bit read and write operation is more efficient, and also helps ensure optimal cycle life for the FLASH memory.

Figure 8. LGT8F328P MemCon (E2PCTL) Block Diagram



The entire Program Memory is monolithically integrated inside the LGT8F328P. The LGT8F328P CPU shares the internal 32K bytes of FLASH memory with the emulated E2PROM. Users can partition the 32K bytes into separate Program Memory and emulated E2PROM Memory according to their needs. By configuring the MemCon settings, the partition size of the emulated E2PROM can be adjusted. The emulated E2PROM is implemented using a 1K byte page swap system. For example, to emulate 1K bytes of E2PROM memory, the MemCon requires 2K bytes of FLASH space. In this example a 1K-Byte Page has Current programmed data. In order to erase or write changes an additional 1K-Byte Swap Page is required for implementation and data security. Likewise, to achieve 4K bytes of emulated E2PROM, 8K bytes of FLASH Program Memory are partitioned and reserved. For more information, please refer to the E2PROM Read/Write Access section on page 20.