After then read the value of the high register, the reading TCNT1 When the value of the counter when the counting is still in progress, TCNT1 The value changes with a high speed clock, pause counter (provided CS1 Zero) then read TCNT1 Value.

Read OCR1A , OCR1B with ICR1 When, according to the following steps:

1) Read OCR1AL / OCR1BL / ICR1L ;

2) Waiting for a system clock (NOP);

3) Read OCR1AH / OCR1BH / ICR1H .

Read TCNT1 When, according to the following steps:

1) Set CS1 Zero;

2) Waiting for a system clock (NOP);

3) Read TCNT1L Value;

4) Waiting for a system clock (NOP); Reading TCNT1H

Value.

Register Definition

TC1 Register List

register	address	Defaults	description
TCCR1A *	0x80	0x00	TC1 Control register A
TCCR1B *	0x81	0x00	TC1 Control register B
TCCR1C *	0x82	0x00	TC1 Control register C
DSX1	0x83	0x00	TC1 Trigger source control register
TCNT1L *	0x84	0x00	TC1 Low byte count value register
TCNT1H *	0x85	0x00	TC1 High byte count value register
ICR1L *	0x86	0x00	TC1 Input Capture Register Low Byte
ICR1H *	0x87	0x00	TC1 Input Capture MSB
OCR1AL *	0x88	0x00	TC1 Output Compare Register A Low byte
OCR1AH *	0x89	0x00	TC1 Output Compare Register A High Byte
OCR1BL *	0x8A	0x00	TC1 Output Compare Register B Low byte
OCR1BH *	0x8B	0x00	TC1 Output Compare Register B High Byte
DTR1 *	0x8C	0x00	TC1 Dead time control register
TIMSK1	0x6F	0x00	Timer counter interrupt mask register
TIFR1	0x36	0x00	Timer counter Interrupt Flag Register
TCKCSR1	0xEC	0x00	TC1 Clock Control Status Register

【note】

band "*" The register operation at high speed clock and a system clock domains, not with "*" The working register only at the system clock domain.