TWDR - TWI Data register

TWDR - TWI Data register								
address: 0xBB							Defaults: 0xFF	
Bit	7	6	5	4	3	2	1	0
Name	TWD7	TWD6	TWD5	TWD4	TWD3	TWD2	TWD1	TWD0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	TWD [7: 0]	TWI Data register. TWD Is the next byte to be transmitted on the bus, or just received on the bus one byte.

TWCR - TWI Control register

TWCR - TWI Control register								
address: 0xBC							Defaults: 0x00	
Bit	7	6	5	4	3	2	1	0
Name	TWINT	TWEA	TWSTA	TWSTO	TWWC		TWEN	- TWIE
R / WR / W		R / W	R / W	R / W	R		R / W	- R / W

Bit	Name	description
7	TWINT	TWI Interrupt flag. when TWI Upon completion of the current job and expects application software intervention, the hardware will set TWINT Bit. If the global interrupt set and TWIE When bit, generated TWI Interruption, MCU Will perform TWI Interrupt service routine. when TWINT When the flag is set, SCL Low-level signal will be extended. TWINT Flag can only be written to this bit "1" The way is cleared. Even if the interrupt service routine, the hardware does not automatically clear the bit. Note also that clearing this bit will immediately open TWI Operation. Therefore, in the clear TWINT Before bit, to complete the first TWAR , TWAMR , TWSR with TWDR Access to the register.
6	TWEA	TWI Enable response control bit. TWEA Control response bits generated pulses. When set TWEA Bit "1" When, and meet one of the following conditions will TWI Generating a response pulse on the bus: 1) Received slave address of the device; 2) TWGCE Receives a broadcast call set; 3) Or receiving a byte of data received from the host machine in the receive mode. When set TWEA Bit "0" , The device temporarily and TWI Bus disconnected. After the device is set to resume address recognition.
5	TWSTA	TWI Initial status control bits. when CPU I want to be TWI Needs to be set when the bus master bit TWSTA Bit. Hardware detects whether the bus is available, when the bus is free, the initial state is generated on the bus. When the bus is not idle, TWI Will wait until after the Stop condition occurs, then generate the initial state to declare themselves want to be the host. After completion of sending the initial state of the software must be cleared TWSTA Bit.