5	UDRE	Data register empty flag. when UDRE for "1" When the show USART Transmission data buffer is empty, data can be written. when UDRE for "0" When the show USART Transmit data buffer is full, you can not write data. When the Data Register Empty Interrupt Enable bit UDRIE for "1" Time, UDRE Used to generate the data register empty interrupt.
4	FE	Framing error flag. when FE for "1" , It indicates that the reception data buffer the received data framing error, i.e., the first stop bit "0" . when FE for "0" , It indicates that the reception data buffer the received data frame is not erroneous, i.e., the first stop bit "1" . FE After being set remains in effect to UDR To be read. Correct UCSRA When writing, FE This is a write "0" .
3	DOR	Data overflow flag. When the receiving buffer is full (two characters), the receive shift register data, if detected at this time a new start bit, data overflow, DOR It is set, to remain in effect UDR To be read. Correct UCSRA When writing, DOR This is a write "0" .
2	PE	Parity error flag. When parity is enabled (UPM1 for "1"), The receive buffer and the received data frame has a parity error, PE It is set, to remain in effect UDR To be read. Correct UCSRA When writing, PE This is a write "0" .
1	U2X	Speed transmit enable bit. when U2X for "1" , The transmission rate of the asynchronous communication mode is doubled. when U2X for "0" , The transmission rate of the asynchronous communication mode for the normal rate. This bit is only valid in asynchronous mode of operation, this bit to zero when using synchronous mode of operation.
0	MPCM	Multiprocessor communication mode enable bit. Set up MPCM The start bit multiprocessor communication mode. MPCM After the set, USART Those received by the receiver input frame does not contain address information will be ignored. The transmitter is not MPCM Effects of the setting.

UCSRB - USART Control and status registers B

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address: 0xC1					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R	R / W

Bit	Name	description
7	RXCIE	Receive Complete interrupt enable bit. After setting enabling RXC Interruption, after clearing ban RXC Interrupted. when RXCIE for "1" , The global interrupt enable, UCSRA Register RXC for "1" Can generate when USART Receive Complete interrupt.
6	TXCIE	End of Transmit Interrupt Enable bit. After setting enabling TXC Interruption, after clearing ban TXC Interrupted. when TXCIE for "1" , The global interrupt enable, UCSRA Register TXC for "1" Can generate when USART Transmit Complete interrupt.
5	UDRIE	Data Register Empty interrupt enable bit. After setting enabling UDRE Interruption, after clearing ban UDRE Interrupted. when UDRIE for "1" , The global interrupt enable, UCSRA Register UDRE for "1" Can generate when USART Data Register Empty