SRAM Data Memory (continued)

The five different addressing modes for the data memory are: Direct, Indirect, Indirect with Displacement, Indirect with Pre-decrement, and Indirect with Post-increment. In the Register File, registers R26 to R31 are the indirect addressing pointer registers. Indirect access can address the entire data storage space.

The Indirect with Displacement addressing mode incorporates a 6 bit address as part of the the instruction word. These six bits are added to the the address given by the Y or Z Registers to access up to 63 address locations from the Y or Z Register base address.

When using the Indirect with Post-Increment or Pre-Decrement Adressing Modes, the X, Y, and Z registers are incremented or decremented. Please refer to the Instruction Set Description section for more details.

The 16-bit register X/Y/Z and its associated automatic addressing mode (increment, decrement) also play a very important role in the 16-bit extended mode. The 16-bit extended mode can use the LD/ST increment/decrement mode to implement auto-increment and decrement addressing with variables. This mode is very effective when performing operations on arrays. For details, please refer to the chapter, "Digital Operational Accelerator (uDSU)".

General Purpose I/O Registers

The I/O space of the LGT8FX8P has three general-purpose I/O registers GPIOR2/1/0. These three registers can be accessed using the IN/OUT instruction to store user-defined data.

I/O Memory

All LGT8FX8P I/Os and peripherals are mapped to the I/O space. All I/O locations may be accessed by the LD/LDS/LDD and ST/STS/STD instructions, transferring data between the 32 general purpose working registers and the I/O space. I/O Registers within the address range of 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked using the SBIS and SBIC instructions. When using the Direct I/O specific commands IN and OUT, the only the Direct I/O Register addresses 0x00 - 0x3F may be used. When addressing any I/O Registers with the LD and ST data space instructions, 0x20 must be added to these addresses. Peripheral registers allocated in the Extended I/O space (0x60~0xFF) can only be accessed using ST/STS/STD and LD/LDS/LDD instructions.

For more details about the I/O space, please refer to the "Register Summary" section.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the Status Flags are cleared by writing a logical one to them. Note that, the CBI and SBI instructions will only operate on the specified bit, and can be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

MemCon FLASH Controller (E2PCTL)

The LGT8FX8P has a special internal memory access controller, the E2PCTL. The names E2PCTL, Memory Controller, and MemCon are used throughout this document and are synonymous. Th Memory controller has access to the entire FLASH Memory, and handles the emulated E2PROM read and write access within the FLASH. The emulated E2PROM includes a system for memory equalization that might increase the life cycle of FLASH Memory by an order of magnitude, and hopefully more than 100,000 erase cycles.

In addition to managing the emulated E2PROM, the MemCon manages FLASH Program Memory and in circuit programming features for upgrading software inside the microcontroller. FLASH Program Memory supports Page erase only. Each page is 1024 bytes. FLASH Program Memory is 32-bits wide, although the MemCon supports Byte level access.