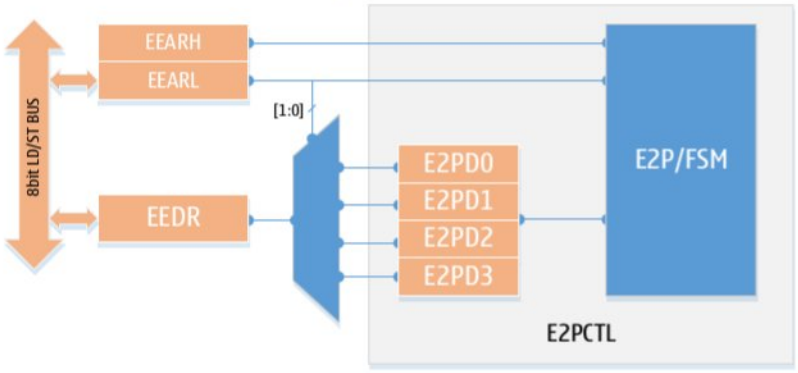
MemCon Data Register

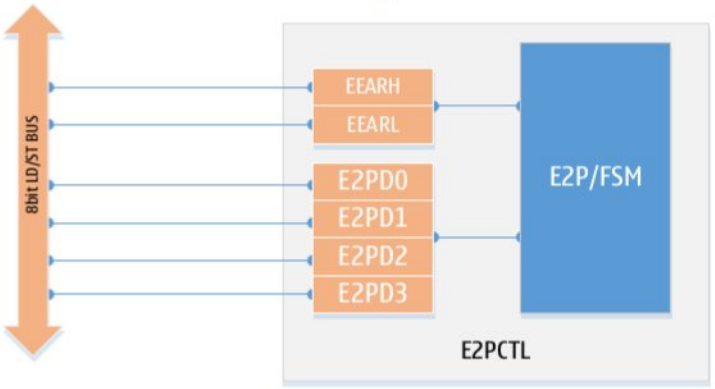
The E2PCTL Memory Controller (MemCon) has an internal 4-byte data buffer (E2PD0~E2PD3). This 4-byte buffer forms the 32-bit data interface for accessing FLASH. This cache buffer has an internal multiplexer the EEDR. It is used to transition between 32-bit Word and 8-bit Byte access modes. When the memory controller is in 8-bit Read/Write Mode, the EEDR controls reading and writing byte data to the buffer. The MemCon's lower data register EEARL[1:0] contains the buffer address information in the two least significant bits. These two bits are used to load the 8-bit Byte data into the correct data buffer location. The starting address is based on the current FLASH target address. After the MemCon fills in the buffer's other three bytes of data, it updates all 32-bits in FLASH.

When the MemCon is in 32-bit Read/Write Mode, the EEDR (MUX) register can still be used as a data interface. The internal data cache is still addressed by EEARL[1:0] for access to the complete 32-bit word. In addition, you can use the data cache to directly access the registers of the IO space (E0~3).

MemCon *8-bit Read/Write Mode:*



MemCon *32-bit Read/Write Mode:*



Byte mode is used for backward compatibility with the byte read and write mode of the LGT8FX8D. The LGT8FX8P's built-in FLASH is 32-bits in width. Using 32-bit read/write mode will bring great benefits to read/write efficiency and extend the FLASH cycle life. Therefore, 32-bit read/write mode is recommended.

E2PROM Read/Write Access

As mentioned previously FLASH Memory must be erased before writing, and the erase operation is performed in page size blocks. Each Page of Flash Memory inside the LGT8FX8P is 1024 bytes. Updating a Byte of data within a single Page first requires erasing the data of the entire Page. Then the target address data can be updated while also restoring the other unchanged bytes from the page. The whole operation is not only time consuming, but also brings the risk of data loss if power is disconnected during the operation.

The E2PCTL MemCon has an integrated page exchange system specificly designed for emulated E2PROM. The page exchange system is designed to mitigate data loss during the page erase operation due to unexpected situations like user initiated system power loss. The page exchange system requires two pages of space in the exchange. While this data protection system comes at a managed memory cost, the system also increases the service life of the emulated E2PROM.