ADCH - ADC High Byte Data Register

			ADC	H - ADC High	Byte Data Re	gister				
address: 0x79						Defaults: 0x00				
Bit		7	6	5	4	3	2	1	0	
Name0		-	-	-	-	ADC11 ADC10 ADC9			ADC8	
Name1		ADC11	ADC10 ADC9		ADC8	ADC7	ADC6	ADC5	ADC4	
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial		0	0	0	0	0	0	0	0	
Bit	Na	ame	description							
7: 0 ADC [11: 8] /		ADC Data low byte register. when ADLAR Bit "0" Time, ADC Output data are aligned in the low								
ADC [11: 4]		storage register, i.e., ADCH Low 4 Bit ADC [11: 8] ,high 4 Bit meaningless, as Name0								
	Shown; if ADLAR Bit "1" Time, ADC High output data are stored in the register are aligne									
	for ADC [11: 4] ,Such as Name1 Fig.									

ADCSRA - ADC Control and status registers A

		AD	CSRA - ADC Cor	ntrol and status	registers A						
address: 0x7A Defaults: 0x05											
Bit	7	6	5	4	3	2	1	0			
Name	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2 ADPS1 ADPS0					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Initial	0	0	0	0	0	0	1	0			
Bit	Name	description									
7	ADEN	ADC Enable control bit. When set ADEN Bit "1" Time, ADC It is enabled. When set ADEN Bit "0" Time, ADC Prohibited.									
6	ADSC	ADC Start the conversion. In the CPA mode, ADSC Set to start a conversion. In continuous conversion mode, ADSC Set to start the first conversion.									
5	ADATE	enabled. Ti	ADTS To control. When set ADATE Bit "0" When the automatic trigger function is								
4	ADIF	If the ADC	ADC Interrupt flag. when ADC After completion of the conversion and update the data register setting ADIF. If the ADC Interrupt enable bit ADIE for "1" And Global Interrupt set, ADC An interrupt is generated. carried out ADC Interrupt cleared ADIF Bits can also be written to the bit "1" Cleared.								
3	ADIE	ADC Interrupt enable control bit. When set ADIE Bit "1" And the Global Interrupt When set, ADC Interrupt is enabled. When set ADIE Bit "0" Time, ADC Interrupts are disabled.									