Arithmetic accelerator (uDSC)

- 16 Bit memory model (LD / ST)
- 32 Bit accumulator (DX)
- Single cycle 16 Bit multiplier (MUL)
- 32 Bit arithmetic logic unit (ALU)
- 16 Bit saturation operation (SD)
- 8 cycle 32/16 Divider
- Single-cycle multiply-add / multiply-subtract operation (MAC / MSC)

Outline

Digital arithmetic accelerator (uDSC) As LGT8XM An arithmetic coprocessor kernel module, with LGT8XM Kernel 16 Place LD / ST Model to achieve a 16 Bit digital signal processing unit. Most of the control process to meet Class A digital signal.

uDSC Internal functions and features:

1.16 Bit operand registers DX / DY

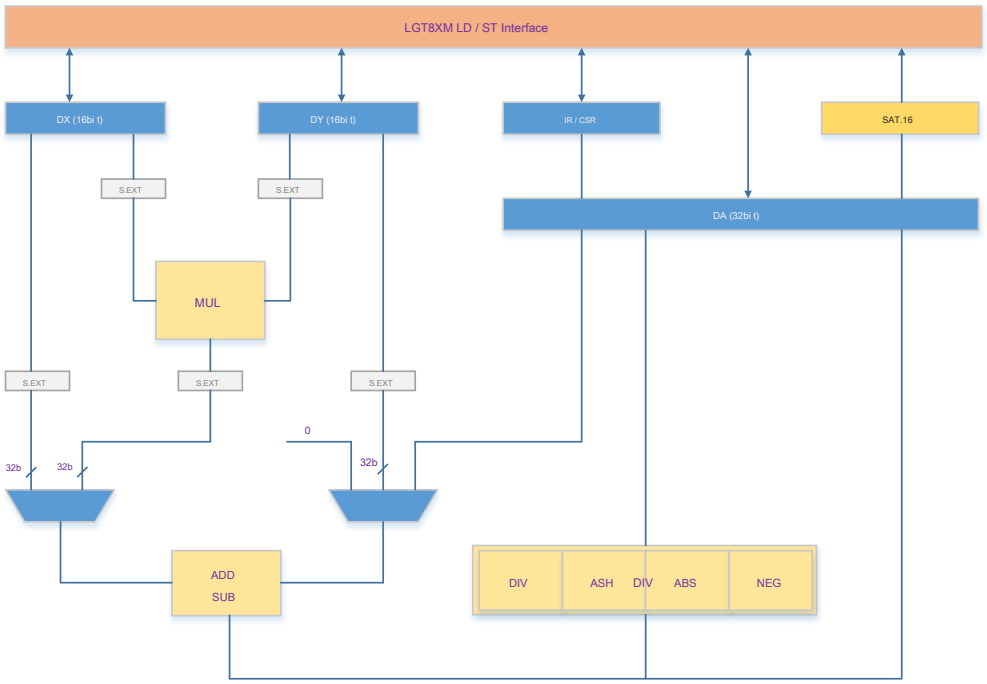
2.32 Bit accumulator register DA

3. Single cycle 17 Bit multiplier (can be achieved 16 Bit / unsigned multiplication)

4.32 Place ALU (can be realised 16/32 Bit addition, subtraction and shift operations)

5.16 Bit saturation operation (For the calculation result is stored into RAM space)

6. 32/16 Divider, 8 The complete operation cycles



uDSC Structure chart