ATmega48P/88P/168P/328P

```
; If RWWSB is set, the RWW section is not ready yet
 sbrs temp1, RWWSB
 ; re-enable the RWW section
 ldi spmcrval, (1<<RWWSRE) | (1<<SELFPRGEN)
 call Do_spm
 rjmp Return
Do_spm:
 ; check for previous SPM complete
Wait_spm:
 in temp1, SPMCSR
 sbrc temp1, SELFPRGEN
 rjmp Wait_spm
 ; input: spmcrval determines SPM action
 ; disable interrupts if enabled, store status
 in
     temp2, SREG
 cli
 ; check that no EEPROM write access is present
Wait_ee:
 sbic EECR, EEPE
 rjmp Wait_ee
 ; SPM timed sequence
 out SPMCSR, spmcrval
 ; restore SREG (to enable interrupts if originally enabled)
 out SREG, temp2
 ret
```

