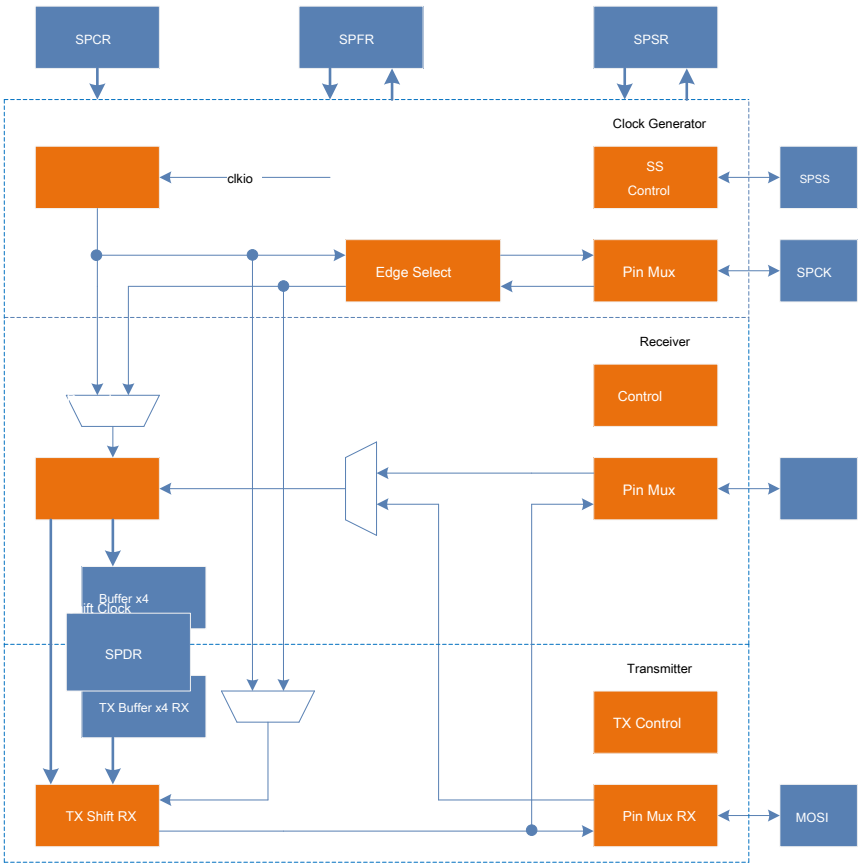
Synchronous Serial Peripheral Interface (SPI)

- Full duplex, three-wire synchronous data transfer
- Master or slave operation
- The least significant bit or MSB-first transfer
- 7 Programmable Bit rate
- End of Transmit Interrupt Flag
- Write collision flag protection mechanisms
- Wake-up from idle mode
- Having a double-speed mode operation of the host
- Host mode supports two-wire input
- Input / Output are 4 A buffer register

Overview

SPI Mainly includes three parts: a clock prescaler, the clock detector, slave select the detector, the transmitter and the receiver.



SPI Structure chart

Control and status registers are shared by these three portions. Clock prescaler operating in Master mode only, the bit rate control bits to select the division ratio, thereby generating a corresponding divided clock, output to SPCK Pin on. Detector operating at a clock slave operation mode is only detected from the SPCK Clock edge on input pin, according to SPI Data transmission mode for transmitting and receiving shift register shift operations. Slave selection detector of the slave select signal SPSS Is detected, to obtain