		When the input capture is triggered, the count value TCNT3 Will be updated to copy ICR3 Register. ICR3 Also be used to register Defined count TOP value.

ICR3H-TC3 Capture register high byte

ICR3H - TC3 Input Capture MSB								
address: 0x97					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	ICR3H7	ICR3H6	ICR3H5	ICR3H4	ICR3H3	ICR3H2	ICR3H1	ICR3H0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	ICR3H	TC3 Input capture high byte values. ICR3H with ICR3L Incorporated into the composition together 16 Bit ICR3 . Read and write 16 Bit register requires two operations. write 16 Place ICR3 When, you should write ICR3H . read 16 Place ICR3 When, it should read ICR3L . When the input capture is triggered, the count value TCNT3 Will be updated to copy ICR3 Register. ICR3 Also be used to register Defined count TOP value.						

OCR3AL-TC3 Output Compare Register A Low byte

OCR3AL - TC3 Output Compare Register A Low byte								
address: 0x98					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OCR3AL7	OCR3AL6	OCR3AL5	OCR3AL4	OCR3AL3	OCR3AL2	OCR3AL1	OCR3AL0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	OCR3AL	Output Compare Register A The low byte. OCR3AL with OCR3AH Incorporated into the composition together 16 Bit OCR3A . Read and write 16 Bit register requires two operations. write 16 Place OCR3A When, you should write OCR3AH . read 16 Place OCR3A When, it should read OCR3AL . OCR3A Continuously with the counter value TCNT3 Compare. Compare match can be used to generate an output compare interrupt, or Who used to OC3A Waveform generation pins. When PWM When mode, OCR3A Using double buffered registers. The normal mode and clear mode match , The double buffering is disabled. Double buffering may be updated OCR3A Register with the maximum or minimum counting time Synchronize, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR3A When the buffer register, double buffering is disabled CPU Access is OCR3A itself.							

OCR3AH-TC3 Output Compare Register A High Byte

OCR3AH - TC3 Output Compare Register A High Byte								
address: 0x99					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR3AH7	OCR3AH6	OCR3AH5	OCR3AH4	OCR3AH3	OCR3AH2	OCR3AH1	OCR3AH0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	OCR3AH Output Compare Register A The high byte.							