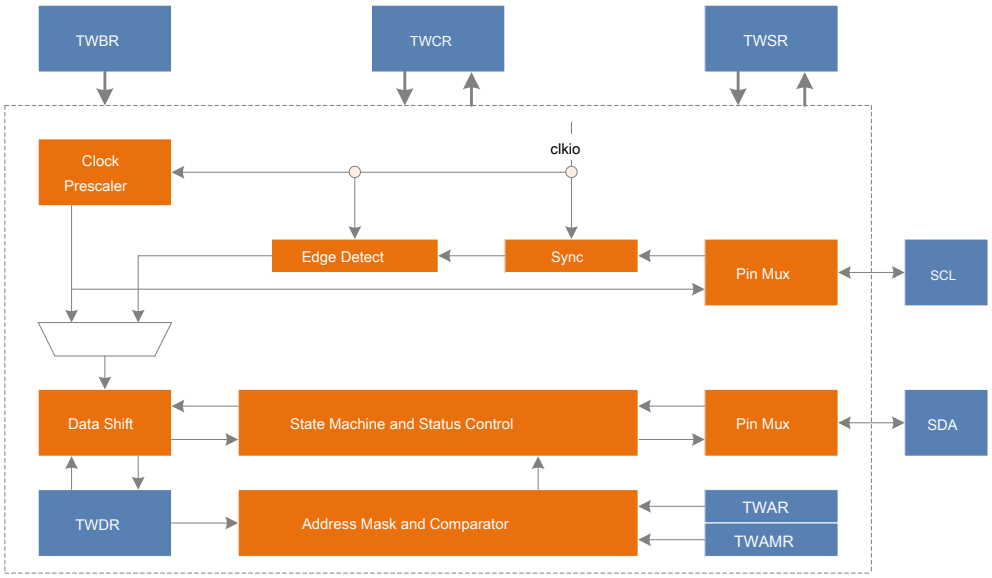

TWI Block Structure chart

TWI Generator module includes a bit rate, the bus interface unit, the address comparator and the control unit or the like. See in particular the following detailed description.

Bit Rate Generator Unit

Bit rate generator mode control host unit is mainly SCL Clock cycle. SCL Clock cycle by the TWI Bit Rate Register TWBR with TWI Status Register TWSR The prescaler control bits joint decision. From the operating bit rate or not affect the frequency prescaler setting, but to ensure that the slave clock working at least SCL Frequency of 16 Times. Note that the slave may be extended SCL LOW period, thereby reducing TWI The average frequency of the bus clock. SCL Clock frequency is generated has the following formula:

$$f_{scl} = f_{sys} / (16 + 2 * TWBR * 4^{TWPS})$$

among them, TWBR for TWI Register bit rate value, TWPS for TWI Status register pre-division control bits.

Bus Interface Unit

Bus interface unit includes a data shift register and an address TWDR , START / STOP And the controller determines the arbitration hardware.

TWDR It contains the address or data bytes to be sent, or an address or data byte has been received. In addition to containing 8 Bit TWDR The bus interface unit further includes a transmission or reception of ACK / NACK register. This one ACK / NACK Register can not be accessed applications. When data is received, it can be TWI Control register TWCR To set or cleared. When transmitting data, received ACK / NACK Value of TWI Status Register TWSR middle TWS Value to reflect.

START / STOP Controller is responsible for generation and detection START , REPEATED START with STOP status. when MCU While in some sleep modes, START / STOP The controller can still be detected START with STOP State, when the TWI Addressing on the bus master when MCU Wake-up from sleep mode.

in case TWI Host-initiated data transfer mode, arbitration detection circuit will continue to monitor the bus to determine if still has control of the bus. when TWI After the loss of control of the bus module, the control unit will perform the proper operation and generate the appropriate status code to notify MCU .