**	Th	is is the fi	Hai HSCOL	new Regis	reis mar i	ne avk ad	JES HOLHA	ve.		
Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
0xF6	GUID3					Byte 3				
0xF5	GUID2					Byte 2				
0xF4	GUID1					Byte 1				
0xF3 0xF2	GUID0 PMCR	PMCE	CLKFS	CLKSS	WCLKS	Byte 0 OSCKEN	OSCMEN	RCKEN	RCMEN	
0xF0	PMX2	WCE	STOSC1	STOSC0	-		XIEN	E6EN	C6EN	
0xEE	PMX0	PMXCE	C1BF4	C1AF5	C0BF3	C0AC0	SSB1	TXD6	RXD5	
0xED	PMX1	-	-	-	-	-	C3AC	C2BF7	C2AF6	
0xEC	TCKCSR	-	F2XEN	TC2XF1	TC2XF0	-	AFCKS	TC2XS1	TC2XS0	
0xE2	PSSR	PSS1	PSS3	-	-	-	-	PSR3	PSR1	
0xE1	OCPUE	PUE7	PUE6	PUE5	PUE4	PUE3	PUE2	PUE1	PUE0	
0xE0	HDR	-	-	HDR5	HDR4	HDR3	HDR2	HDR1	HDR0	
0xDE	DAPTE	DAPTE	-	-	-	-	-	-	-	
0xDD	DAPTR	DAPTP	C 4 1	640		Trimming	DNCO	DDC1	DDCO	
0xDC 0xCF	DAPCR LDOCR	DAPEN	GA1	GA0	DNS2	DNS1 PDEN	DNS0 VSEL2	DPS1 VSEL1	DPS0 VSEL0	
0xCF	VCAL2	VVCE	Cal	ibration va	alue for 2				VSELU	
0xCD	VCAL2	Calibration value for 2.048V internal reference Calibration value for 1.024V internal reference								
0xCC	VCAL3	Calibration value for 4.096V internal reference								
0xC8	VCAL		Inte	ernal Volta	ge Refere	nce calibr	ation regi	ster		
0xAF	DPS2R	-	-	-	-	DPS2E	LPRCE	TOS1	TOS0	
0xAE	IOCWK	IOCD7	IOCD6	IOCD5	IOCD4	IOCD3	IOCD2	IOCD1	IOCD0	
0xAD	ADCSRD	BGEN	REFS2	IVSEL1	IVSEL0	-	VDS2	VDS1	VDS0	
0xAC	ADMSC	AMOF	-	-	-	AMFC3	AMFC2	AMFC1	AMFC0	
0xAB	ADT1H		ADC Auto-monitor Overflow threshold high byte ADC Auto-monitor Overflow threshold low byte							
0xAA	ADT1L PORTE									
0xA9 0xA8	PORTE			t Output E Direction						
0xA6	PINE		10/10/00	nt Input E						
0xA6	ADT0H			Auto-mon	-					
0xA5	ADT0L			Auto-mor						
0xA4	OFR1					ffset trim		2.00		
0xA3	OFR0			ADC	negative	offset trim	ming			
0xA1	DALR				DAC data	a register				
0xA0	DACON	-	-	-		DACEN	DAOE	DAVS1	DAVS0	
0x9F	OCR3CH		-	e output r						
0x9E	OCR3CL		Compare output register low byte of Timer3 C channel							
0x9D 0x9C	DTR3H DTR3L		Dead-band register high byte of Timer3							
0x9C	OCR3BH	Dead-band register low byte of Timer3 Compare output register high byte of Timer3 B channel								
0x9A	OCR3BL	Compare output register high byte of Timer3 B channel Compare output register low byte of Timer3 B channel								
0x99	OCR3AH	Compare output register low byte of Timer3 A channel								
0x98	OCR3AL	Compare output register low byte of Timer3 A channel								
0x97	ICR3H	Input capture register high byte of Timer3								
		Input capture register low byte of Timer3								
0x96	ICR3L						e of Time			
0x95	TCNT3H			nput captu Counter	ıre registe register h	er low byte igh byte o	e of Timer e of Timer f Timer3			
0x95 0x94	TCNT3H TCNT3L			nput captu Counter Counter	re registe register h register le	er low byte igh byte o ow byte of	e of Timer e of Timer f Timer3 f Timer3			
0x95 0x94 0x93	TCNT3H TCNT3L TCCR3D			nput captu Counter Counter Cont	register h register h register le trol registe	er low byte igh byte o ow byte of er D of Tin	e of Timer e of Timer f Timer3 f Timer3 ner3			
0x95 0x94 0x93 0x92	TCNT3H TCNT3L TCCR3D TCCR3C			nput captu Counter Counter Cont	register h register h register le trol registe trol regist	er low byte igh byte o ow byte of er D of Tin er C of Tin	e of Timer e of Timer f Timer3 f Timer3 ner3 ner3			
0x95 0x94 0x93 0x92 0x91	TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B			nput captu Counter Counter Cont Cont	register heregister heregister le register le trol registe trol register trol regist	er low byte igh byte of ow byte of er D of Tin er C of Tin er B of Tin	e of Timer e of Timer f Timer3 f Timer3 ner3 ner3			
0x95 0x94 0x93 0x92	TCNT3H TCNT3L TCCR3D TCCR3C			nput captu Counter Counter Cont Cont Cont	register hegister hegister legister leg	er low byte igh byte of ow byte of er D of Tin er B of Tin er A of Tin	e of Timer e of Timer f Timer3 f Timer3 ner3 ner3 ner3	3		
0x95 0x94 0x93 0x92 0x91 0x90	TCNT3H TCNT3L TCCR3D TCCR3C TCCR3C TCCR3B TCCR3A			nput captu Counter Cont Cont Cont Cont Dead-band	register he register le register le trol	er low byte igh byte of ow byte of er D of Tin er B of Tin er A of Tin	e of Timer of Timer3 f Timer3 ner3 ner3 ner3 of Timer1			
0x95 0x94 0x93 0x92 0x91 0x90 0x8D	TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H	DSX17		nput captu Counter Cont Cont Cont Cont Dead-band	register he register le register le trol	er low byte igh byte of ow byte of er D of Tin er B of Tin er A of Tin high byte	e of Timer of Timer3 f Timer3 ner3 ner3 ner3 of Timer1		DSX10	
0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C	TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L	DSX17 OFEN		nput captu Counter Conf Conf Conf Dead-ban Dead-ban	register he register le regist	er low byte igh byte of ow byte of er D of Tin er B of Tin er A of Tin high byte	e of Timer of Timer3 f Timer3 ner3 ner3 ner3 of Timer1	3	DSX10 ADTM	
0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x8C 0x83 0x7D 0x76	TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2			nput captu Counter Cont Cont Cont Dead-ban Dead-ban DSX15 SPN	register he register for register trol register trol register description of the register of register	er low byte of ow byte of ow byte of er D of Tiner B of Tiner B of Tiner A of Tiner A of Tiner A of Tiner A of Tiner B of Tiner A of Tiner B of Tiner A of	e of Timer of Timer3 f Timer3 ner3 ner3 of Timer1 of Timer1 - SPD -	3 DSX11		
0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x8S 0x7D 0x76 0x75	TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE		DSX16	nput captu Counter Cont Cont Cont Dead-ban Dead-ban DSX15 SPN	register he register for register trol register trol register description of the register of register	er low byte igh byte of ow byte of er D of Tin er B of Tin er A of Tin high byte	e of Timer of Timer3 f Timer3 ner3 ner3 of Timer1 of Timer1 - SPD -	DSX11 DIFS		
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8-bit LGT8XM

RISC Microcontroller with In-System Programmable FLASH Memory

LGT8F88P LGT8F168P LGT8F328P

Data book Version 1.0.4 (J)

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