

*LGT8XM General purpose working registers*

	7	0	Addr.	
	R0		0x00	
	R1		0x01	
	R2		0x02	
	...			
	R13		0x0D	
	R14		0x0E	
General	R15		0x0F	
purpose	R16		0x10	
working	R17		0x11	
registers	...			
	R26		0x1A	X Register Low Byte
	R27		0x1B	X High byte register
	R28		0x1C	Y Register Low Byte
	R29		0x1D	Y High byte register
	R30		0x1E	Z Register Low Byte
	R31		0x1F	Z High byte register

Most instructions can directly access to all of the general-purpose working registers, they are also the most single-cycle instruction. As shown above, each register address corresponds to a data memory space, these general purpose registers are mapped into the data storage space. As soon as they do not really exist in SRAM But such storage unified organization mapped to visit them a lot of flexibility. X / Y / Z Index register pointer can be used as any general purpose registers.

**X / Y / Z register**

register R26 ... R31 It can be combinations of two, three configuration 16 Bit registers. These three 16 Bit register used primarily to access the address pointer indirection, X / Y / Z Register structure as follows:

	15	XH	XL	0
X register	7 0		7 0	
	R27 (0x1B)		R26 (0x1A)	
	15	YH	YL	0
Y register	7 0		7 0	
	R29 (0x1D)		R28 (0x1C)	
	15	ZH	ZL	0
Z register	7 0		7 0	
	R31 (0x1F)		R30 (0x1E)	

In the different addressing modes, These registers are used as a fixed offset, the auto-increment and auto-decrement of the address pointer described details, refer to the instruction portion.