TWSR - TWI Status Register

TWSR - TWI Status Register								
address: 0xB9					Defaults: 0xF8			
Bit	7	6	5	4	3	2	1	0
Name	TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 3	TWS [7: 3]	TWI State flag. **5 Bit TWS reaction TWI And the logic state of the bus. Different states have different meanings values, see the specific TWI Described mode of operation. From TWSR Read values 5 Bit state value and 2 Bit prescaler control bits, the mask detection state when bit prescaler "0" . This is** independent of the state detection prescaler setting.
2	-	Reservations.
1	TWPS1	TWI Prescaler high. **TWPS1 with TWPS0 Together form TWPS [1: 0] , For controlling the bit rate of the prescale factor, and TWBR** Together control the bit rate.
0	TWPS0	TWI Prescaler low. **TWPS0 with TWPS1 Together form TWPS [1: 0] , For controlling the bit rate of the prescale factor, and TWBR** Together control the bit rate.

TWPS [1: 0]	Prescale factor
0	1
1	4
2	16
3	64

TWAR - TWI Address register

TWAR - TWI Address register								
address: 0xBA					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	TWAR6	TWAR5	TWAR4	TWAR3	TWAR2	TWAR1	TWAR0	TWGCE
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 1	TWA [6: 0]	TWI Slave address bits. **TWA for TWI Slave address. when TWI Works in the slave mode, the TWI This address will respond. Host mode** does not require this address. However, in multi-master system, also set for other hosts to access the slave address.
0	TWGCE	**TWI Broadcasting discrimination enable control bit. When set TWGCE Bit "1" , Enable TWI Bus broadcast identification. When set TWGCE Bit "0" Is prohibited TWI Bus broadcast identification. when TWGCE Set and the address frame is received 0x00 Time, TWI In response to this broadcast bus module.**