		1	2
2: 1	UCSZ1: 0	Character data frame length selection bits. **UCSZ1: 0 versus UCSRB Register UCSZ2 Combined set of data bits contained in the data frame.**	
		UCSZ2: 0	Data frame length
		0	5 Place
		1	6 Place
		2	7 Place
		3	8 Place
		4	Retention
		5	Retention
		6	Retention
		7	9 Place
0	UCPOL	**Clock Polarity Select bit. in USART Synchronous mode of operation, UCPOL Sampling and synchronization clock is provided to change the input data and output data XCK The relationship between. Use asynchronous mode of** operation and **UCPOL Nothing to do, this bit to zero**	
		UCPOL	Transmit data changes / Receiving data samples
		0	XCK The rising edge / XCK Of falling
		1	XCK Of falling / XCK The rising edge

UBRRL - USART Baud Rate Register Low Byte

***UBRRL* - USART Baud Rate Register Low Byte**								
address: 0xC4					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	UBRR7	UBRR6	UBRR5	UBRR4	UBRR3	UBRR2	UBRR1	UBRR0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	UBRR [7: 0]	USART Low byte portion of register baud rate. **USART Baud rate register comprising UBRRL with UBRRH Two parts, joined together to set the baud** rate.

UBRRH - USART Baud Rate Register High Byte

***UBRRH* - USART Baud Rate Register High Byte**								
address: 0xC5					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	UBRR11	UBRR10	UBRR9	UBRR8
R / W	-	-	-	-	R / W	R / W	R / W	R / W

Bit	Name	description
7: 4	-	Reservations.