SPI Host initialization

SPI Host mode initialization process is as follows:

1. Position MSTR Bit, set the bit rate selection control bits, data transmission mode, the transmission order of data, the interrupt is enabled or not,
   And two-enabled or not;
2. Set up MOSI with SPCK Pin as an output;
3. Position SPE Bit. Host mode, when you do not want SPI Other modules are selected as the host machine from the time, can be set SPSS Pin output.

SPI Slave initialization

SPI Slave mode initialization process is as follows:

1. Clear MSTR Bit, the data transfer mode, the transmission order of data, the interrupt is enabled or not;
2. Set up MISO Pin as an output;
3. Position SPE Bit.

SPI Interrupt

When one of the following events occur or more, SPI Interrupt flag SPIF It will be set:

1. When configured as a host and SPSS An input pin, the external circuit down SPSS Pin;
2. When the transmit buffer status is full, the software continues to SPDR Register write transactions;
3. When the receive buffer full state;
4. When data is written in the transmit buffer have been sent, the transmit buffer is empty status.

when SPIF Bit is set, and SPI Interrupt enable bit SPIE When and global interrupt enable bits are high, it will produce SPI Interrupted. After entering the interrupt service routine, the hardware will SPIF Cleared. If the SPIF It is set by the above-mentioned event 1 with 2 To set in, SPIF Will be cleared; if SPIF It is set by the above-mentioned event 3 with 4 To set in, SPIF Will not be cleared, because the reception or transmission buffer status is not changed, the bit will still be set SPIF Bit, then you need to be cleared by software operations.

SPI Interrupt service routine, the software is cleared SPIF Bit sequence of operations:

1) Read SPIF Status bits, if it is low, indicating that SPIF Bit has been cleared by hardware, no software is cleared again; if it is high,
   Continue to operate it;

2) Read SPFR Register, if RDFULL Bit is high, indicating that the current status of the receive buffer is full, read SPDR Deposit
   Obtains received data, RDFULL Bit becomes low, the software can continue to read SPDR Register obtain received data until the RDEMPT Bit high;

3) Read SPFR Register, if RDFULL Bit is low, and WREMPT Bit is high, indicating that the current status of the receive buffer
   Non-full, the transmission buffer status is empty, the software can read SPDR Register obtain received data until the RDEMPT Bit high;

4) After the software acquires the received data, and then performed is cleared SPIF Bit. because SPIF Bit is read-only and can not directly SPIF
   Bit is cleared, and the need to read SPSR Register before accessing SPDR (Read or write SPDR Register) to clear the way SPIF Bit.