External Interrupt

- 2 External interrupt sources
- Level or edge-triggered interrupts can be configured
- Wake-up source can be used in sleep mode

Outline

External interrupted by INT0 with INT1 Pin trigger. As long as the external interrupt is enabled, even if it 2 Configured as an output pin can also trigger an interrupt. This software can be used to generate an interrupt. External interrupts may be rising and falling edge or level-triggered, the external interrupt control register EICRA To configure. When the external interrupt is enabled and configured as level triggered (only INT0 with INT1 When the pin), as long as the pin is low, the interrupt will have been produced. INT0 with INT1 Rising or falling edge triggers an interrupt pin needs IO Clock work, and INT0 with INT1 Low pin triggers an interrupt is asynchronous detection. In addition to the idle mode, sleep mode under other IO The clock is stopped. Therefore, this 2 It can be used as external interrupt wake-up source in other sleep modes other than Idle mode.

If the level of the trigger level as a wake-up interrupt source in the power saving mode, the change must be held for some time to wake up MCU To reduce MCU Sensitivity to noise. The required level must be maintained long enough time for the MCU The end of the wake-up process, then the trigger level interrupts.

Register Definition

Register List

register	address	Defaults	description
EICRA	0x69	0x00	External Interrupt Control Register A
EIMSK	0x3D	0x00	External interrupt mask register
EIFR	0x3C	0x00	External Interrupt Flag Register

External Interrupt Control Register A- EICRA

EICRA - External Interrupt Control Register A								
address: 0x69				Defaults: 0x00				
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	ISC11	ISC10	ISC01	ISC00
R / W	-	-	-	- R / W		R / W	R / W	R / W

Bit	Name description	
7: 4	-	Reservations.
3	ISC11	INT1 Pin interrupt trigger control bit high.
2	ISC10	INT1 Pin interrupt trigger control bit low. When the global interrupt set and GICR The respective control bit interrupt mask register is set when the external interrupt 1 by INT1 Pin excited. See table describes interrupt trigger mode. Prior to edge detection MCU First sampling INT1 Level on the pin. If the selected edge trigger or level trigger changes in the way, that last longer than 1 A system clock cycle pulse will trigger an interrupt. Shorter pulses are not guaranteed to trigger an interrupt. If you choose low