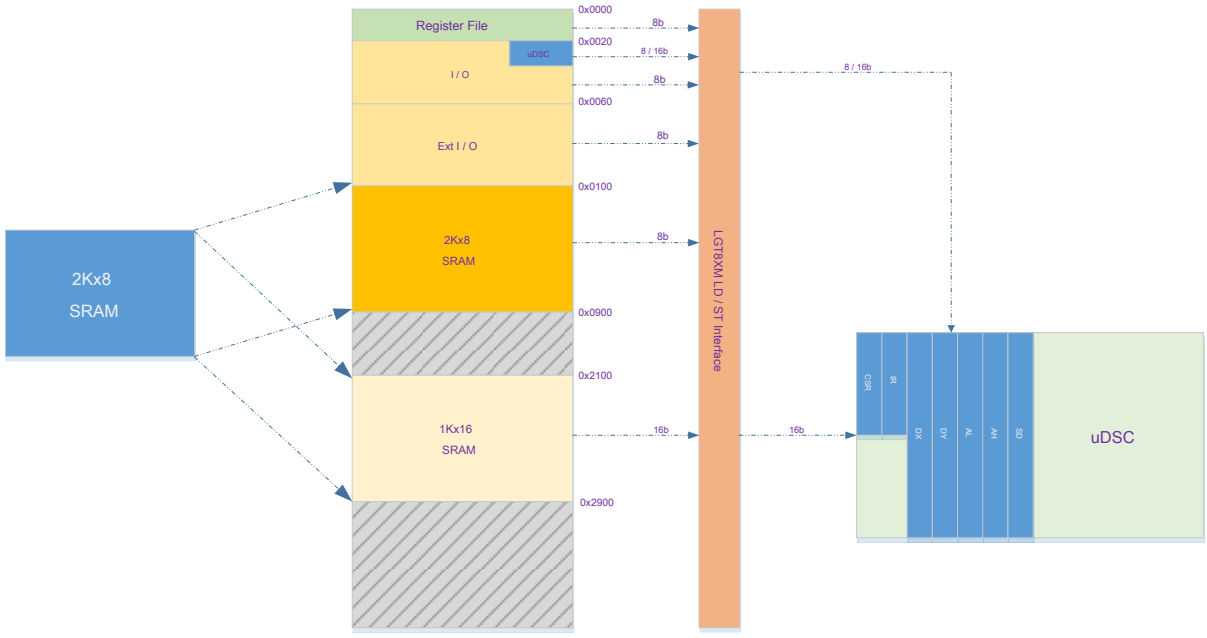
16 Place LD / ST Operating mode

To improve uDSC Efficiency of operation of a large number of data processing, LGT8XM Kernel implementation of a dedicated 16 Place LD / ST Memory channel may be used LDD / STD Efficient instruction in uDSC versus SRAM And a general register file for between 16 Bit data exchange.

In order not to disrupt the normal LD / ST Instruction, LGT8XM The kernel SRAM Space to remap 0x2100 ~ 0x28FF . use LD / ST Instruction from 0x2100 ~ 0x28FF Space Access SRAM When the kernel automatically open 16 Place LD / ST Function, open SRAM versus uDSC Between the direct access channel.

The figure below shows LGT8XM Kernel address space distribution of data:



As shown in FIG, LGT8XM The kernel can use LD / ST Instructions in uDSC of DX / DY / DA Register with SRAM Between direct 16 Access data stored bit access. Simultaneously uDSC Internal registers to be mapped I / O Space access uDSC Register divided 8/16 Two modes.

uDSC In addition to the internal operation DX / DY / DA External register, further comprising the additional 2 More 8 Bit register: uDSC Control Status Register CSR And an operation instruction register IR . CSR / IR Only through I / O Space Access bytes; Access DX / DY / AL / AH When 16 Bit mode. can use IN / OUT as well as LD / ST / LDD / STD / LDS / STD And other commands access.

uDSC Related control and status registers are mapped into data IO Space, directly IN / OU Instruction addressing can be done in one instruction cycle 8/16 Bits of data access.

CSR For control uDSC Working mode and record the current uDSC State flag to perform operations. IR control uDSC Computing specific implementation. uDSC Support of the majority of operations will be completed in a single cycle, the division needs to run 7 A waiting period, you can also CSR Register flag bit determines whether the current division operation is completed.

standard LD / ST Use instructions LGT8XM The internal general purpose registers as LD / ST Data use X / Y / Z As the destination address. When the destination address falls 16 Place SRAM When mapping space, this time LD / ST Meaning instruction operands vary, wherein X / Y / Z Still according to the destination address as the meaning, purpose working registers addressable uDSC Mapping mode will have two approaches. uDSC The mapping mode of action only in the 0x2100 ~ 0x28FF Address access visit. By mapping mode CSR The first register 6 Bit (MM) Settings.