ADC Noise Reduction

when SM2 ... 0 Set as 001 ,carried out SLEEP Instruction, MCU enter ADC Noise suppression mode. In this mode, the kernel and most of the peripherals will stop working, ADC ,External Interrupt, TWI Address match, WDT And operating in asynchronous clock mode, timer / counter 2 They can work properly.

ADC Noise has been mainly used as a model ADC Transformation provides a good working environment. Reduce high frequency interference digital to analog conversion module. After entering this mode, ADC Save automatically starts sampling conversion, the converted data to ADC After the data register, ADC End of Conversion interrupt MCU From ADC Wake-up mode noise.

Power-saving mode (Save)

when SM2 ... 0 Set as 010 ,carried out SLEEP Instruction, MCU Enter Save mode. In this mode, the system will shut off all the work of the clock module. This mode due to the closure of all the work the clock module, it can only be awakened by an asynchronous mode, external interrupts, TWI Address matching and operate at independent clock source mode WDT Wake-up signal can be generated in this mode.

This model can turn off all modules except that of the master clock source. To achieve more desirable operating power consumption, it is recommended herein before entering mode, the system will be switched to the internal clock master 32K RC Or external 32KHz Low frequency oscillator, then it is not used to close off the source clock and an analog module.

Power-down mode DPS0

when SM [2: 0] Set as 110 ,carried out SLEEP Instruction, MCU Will enter into DPS0 mode. enter DPS0 After, in addition to internal 32KHz RC , The other clock sources are closed. This mode can be interrupted by external INT0 / 1 Wake up; if enabled WDT Interrupt function, can also WDT Achieve timing wake.

Power-down mode DPS1

when SM [2: 0] Set as 011 ,carried out SLEEP Instruction, MCU Will enter into DPS1 mode. enter DPS1 After all clock sources are closed systems. This model can be used IO Level change, the watchdog wake.

Power-down mode DPS2

Set up SM [2: 0] for 111 And by DPSR2 Register DPS2EN Enable AWSON Module, execution SLEEP After entering the command DPS2 mode. enter DPS2 After the mode, the system power off the core. So register and RAM Data will be lost. From DSP2 Wake-up process with the same power-on reset process.

DPS2 Mode, Since the closed core voltage, the register information is lost, so the control status of the ports will all return to the input state, all IO The output drive and pull-up control will be closed.

FLASH Power control and fast wake-up

When the system is SLEEP After mode, the kernel will not continue executing instructions, then you can choose to close FLASH Power, in order to obtain lower power consumption standby. This function can be MCUCR Register FPDEN Position control is realized;

In power-down mode, The system can use external interrupt or WDT Wake-up, in order to filter out possible interference of the external signal, an internal wake-up circuit comprises a filter circuit can be configured, the user can select the appropriate filter width according to the needs. Filter circuit can be arranged MCUCR Register FWKPEN achieve.

MCUCR [FWKPEN] Filter width control: