SEN		Set the negative sign	N ← 1	N	1
CLN		Clear Negative flag	N ← 0	N	1
SEZ		Set zero flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Enable global interrupt	I ← 1	I	1
CLI		Global Interrupt ban	I ← 0	I	1
SES		Set Symbol Test mark	S ← 1	S	1
CLS		Clear sign symbol test	S ← 0	S	1
SEV		Set two's complement overflow flag	V ← 1	V	1
CLV		Clear twos complement overflow flag	V ← 0	V	1
SET		**Set up T Bit (SREG)**	T ← 1	T	1
CLT		**Remove T Bit (SREG)**	T ← 0	T	1
MCU Control instruction					
NOP		Dummy instruction		None	1
SLEEP		Goes into sleep mode		None	1
WDR		Watchdog reset		None	1
BREAK		Soft Breakpoints	For debugging purposes only	None	N / A
NOP		Dummy instruction		None	1
SLEEP		Goes into sleep mode		None	1