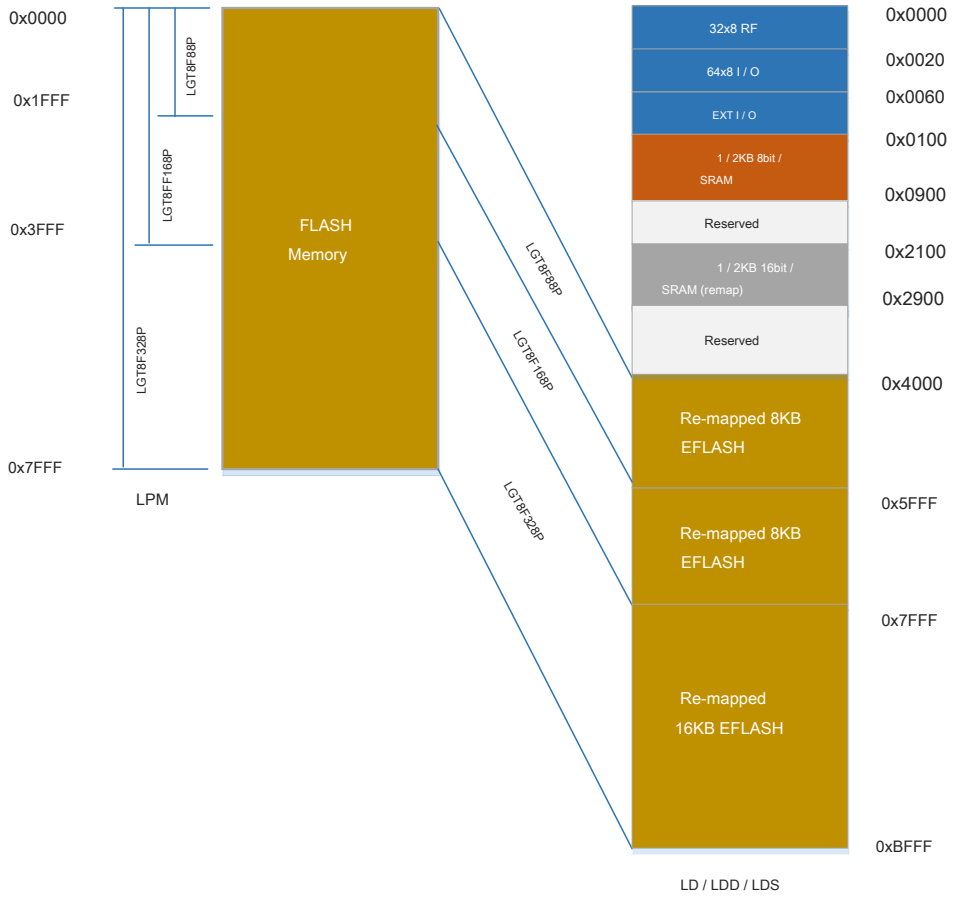
table. Simultaneously FLASH Program space is mapped to data memory space within the system, the user can also use LD / LDD / LDS To achieve FLASH Access to space. Program space is mapped to data memory space 0x4000 In the beginning of the address range. As shown below:



SRAM The data storage unit

LGT8FX8P Family of microcontrollers is a relatively complex microcontroller, which supports a plurality of different types of peripherals, which peripherals are allocated in the controller 64 More I / O Register space. Directly through IN / OUT Instruction accesses. Other peripheral control register allocation 0x60 ~ 0xFF Region, since this space is mapped into the data memory space, only through ST / STS / STD as well as LD / LDS / LDD And other commands access.

LGT8FX8P System data storage space from 0 Start address, the general purpose working registers are mapped file, I / O Space for expansion I / O Space and internal data SRAM space. initial 32 Bytes corresponding to the address LGT8XM Kernel 32
General purpose working registers. The following 64 Addresses can be achieved through IN / OUT Direct access to the standard instruction I / O space. Then the 160 Addresses is an extension I / O Space, the next step is up to 2K Bytes of data SRAM . From 0x4000 To begin 0xBFFF End of this space, mapped FLASH A program storage unit.

Within the system 1K / 2K byte SRAM They are respectively mapped to two spaces. From 0x0100 To begin 0x0900 This is the end of the space to the kernel 8 The width of the read bit bytes. From 0x2100 To begin 0x2900 This area is ended 16 Bit access space width. system RAM It is mapped to 0x2100 Mainly used for upper address begins with uDSU Module work to achieve efficient 16 Bit data storage. In programming, the ordinary 8 Addressing variable bit address plus 0x2000 Offset to switch to 16 Bit access mode.