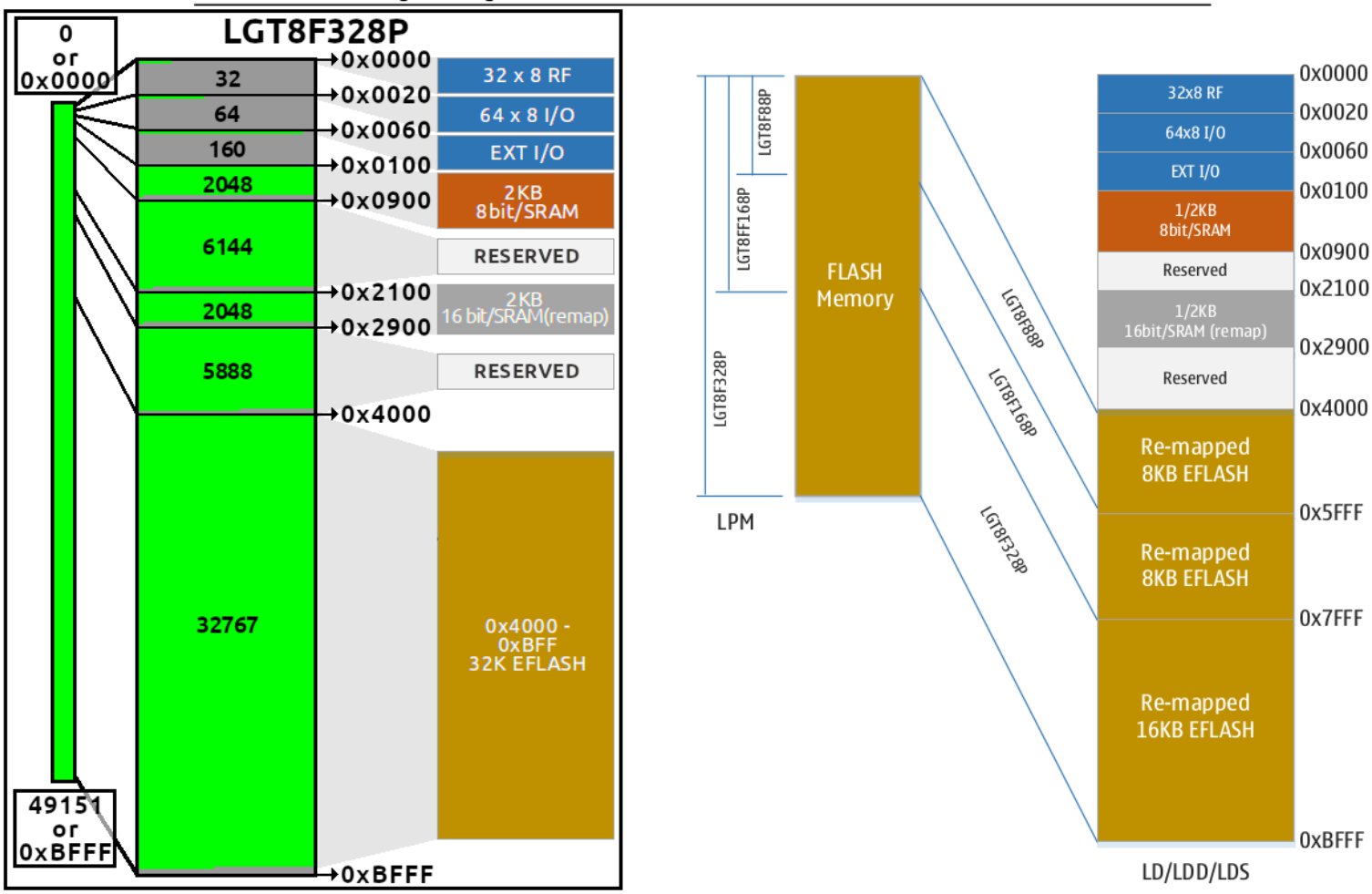

SRAM

The LGT8FX8P series of microcontrollers have 3 sections of address spaces in the first 256 bytes of RAM data memory. The first block section is the Register File. This is the 32 byte Special Function Register, and is addressed from 0x00 to 0x1F. The next 64 addresses, 0x20 to 0x5F, are the Direct I/O Register. The third section is the Extended I/O Register. This occupies from 0x60 to 0xFF. In decimal, this breaks down to addresses 0 to 31, 32 through 95, and 96 through 255. The 32x8 Register File has already been described in the CPU Architecture section beginning on page 11. The 64 Direct I/O Registers can be accessed via the faster IN/OUT instructions. The following 160 Extended I/O Registers from 0x60-0xFF are mapped to the data storage space. These registers are only accessible with the slower data addressing instructions such as ST/STS/STD and LD/LDS/LDD.

The first 256 addresses are directly followed by a maximum of 2K bytes of data SRAM. The portion of the space from 0x4000 to the end of 0xBFFF maps the FLASH program memory location.

The 1KB (LGT8F88P/LGT8F168P) or 2KB (LGT8F328P) of SRAM is mapped to two separate locations. The first space from 0x0100 to 0x0900 is read and written by the CPU in 8-bit bytes. The second SRAM space starting from 0x2100 to 0x2900 is a 16-bit wide access space. The system RAM is mapped to the high-order address starting from 0x2100 and is designed to work with the uDSU module to achieve efficient 16-bit data storage. When programming, the normal 8-bit address is offset by 0x2000 to switch to 16-bit access mode.