		When set DSX01 Bit "0" When, analog comparator 1 As a comparison output signal waveform is off OC0A / OC0B The trigger source is prohibited.
0	DSX00	TC0 Select the trigger source control enables the first 0 Bit. When set DSX00 Bit "1" When, analog comparator 0 As a comparison output signal waveform is off OC0A / OC0B The trigger source is enabled. when DOC0A / DOC0B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC0A / OC0B The waveform output. When set DSX00 Bit "0" When, analog comparator 0 As a comparison output signal waveform is off OC0A / OC0B The trigger source is prohibited.

The following table shows the selection control trigger source waveform output.

shut down OC0A / OC0B Trigger source waveform output from the selection control

DOC0x	DSX0n = 1	Trigger source	description
0	-	-	DOC0x Bit "0" , Trigger source waveform output off function is disabled
1	0	Analog comparator 0	ACIF0 The rising edge will be closed OC0x Waveform output
1	1	Analog comparator 1	ACIF1 The rising edge will be closed OC0x Waveform output
1	4	External Interrupt 0	INTF0 The rising edge will be closed OC0x Waveform output
1	5	Pin Change 0	PCIF0 The rising edge will be closed OC0x Waveform output
1	6	TC2 overflow	TOV2 The rising edge will be closed OC0x Waveform output
1	7	TC1 overflow	TOV1 The rising edge will be closed OC0x Waveform output

note:

1) DSX0n = 1 Show DSX0 The first register n Bit 1 When each register bit may be set simultaneously.

TC0 Count value register - TCNT0

TCNT0 -*TC0 Count value register*								
address: 0x46					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	TCNT07	TCNT06	TCNT05	TCNT04	TCNT03	TCNT02	TCNT01	TCNT00
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name description	
7: 0	TCNT0	TC0 Count value register. by TCNT0 Directly to the counter register 8 Read and write access to the counter value. CPU Correct TCNT0 Write to register on the next timer clock cycle to prevent the occurrence of compare match, even if the timer has stopped. This allows initialization TCNT0 And the value of the register OCR0 The value of the agreement without causing disruption. If you write TCNT0 The value is equal to or bypassed OCR0 Value, compare match will be lost, resulting in incorrect waveform generation. When the timer stops counting the clock source is not selected, but CPU Still access TCNT0 . CPU Write counter is cleared or a higher priority than addition and subtraction operations.