Timer / Counter 3 (TMR3)

- truly 16 Digital design, allowing 16 Bit PWM
- 3 Separate outputs the comparison unit
- Double buffered output compare register
- 1 Input capture unit
- Input Capture Noise Suppressor
- The counter is automatically cleared when compare match and automatically load
- No disturb pulse phase correction PWM
- Variable PWM cycle
- Frequency generator
- External event counter
- 5 Independent interrupt sources
- With dead-time control
- 6 Selectable trigger source automatically shut down PWM Export

Outline

TC3 Is a common 16 Bit timer counter module support PWM Output waveform can be generated accurately. TC3 contain 1 More 16 Bit counter, waveform generation mode control unit, 2 Separate outputs and the comparison unit 1 Input capture unit. Waveform generating mode generates the control unit controls the operation mode of the counter and comparing the output waveform. Depending on the mode of operation, a counter for counting each clock Clkt3 Cleared, incremented or decremented. Clkt3 It may be generated by an internal clock or an external clock source. When the count value of the counter TCNT3 It reached its maximum value (equal to the maximum value 0xFFFF Or a fixed value or output compare register OCR3A Or the input capture register ICR3 ,defined as TOP , The maximum value of the definition MAX When to distinguish), the counter is cleared or decremented. When the count value of the counter TCNT3 Reaches a minimum value (equal to 0x0000 ,defined as BOTTOM), The counter will be incremented by one operation. When the count value of the counter TCNT3 Arrivals OCR3A or OCR3B or OCR3C When, also referred to compare match, set or cleared by the output signal of the comparison OC3A or OC3B or OC3C To produce PWM Waveform. When the input capture function is turned on, i.e. the counter is activated to start or stop counting, ICR3 Register records the captured count values trigger period signal.