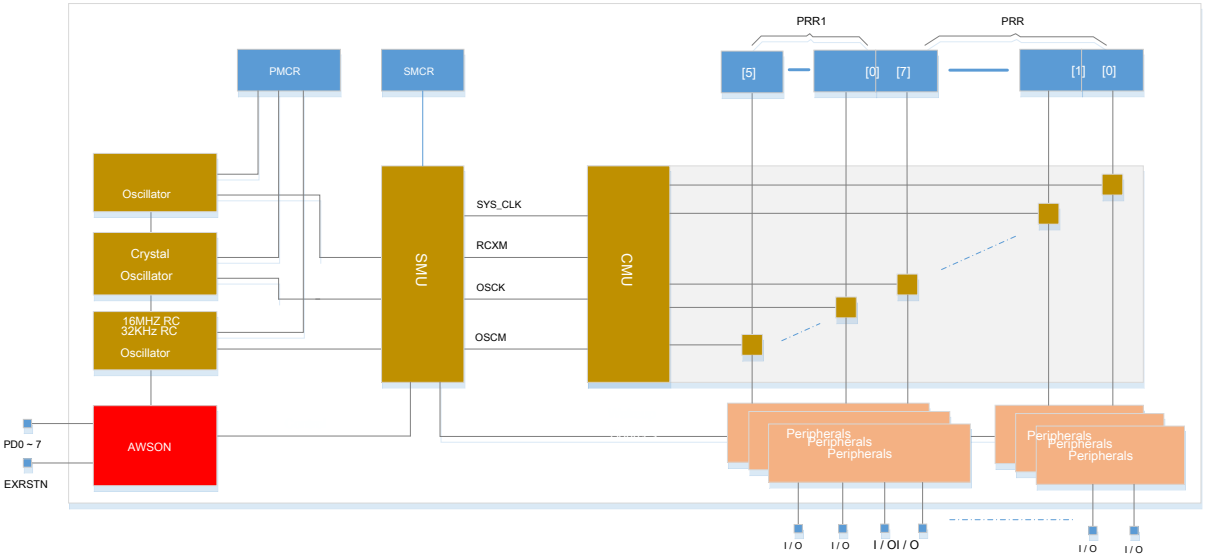
Power management system diagram:



As shown in FIG, LGT8FX8P Mainly through sleep-mode controller (SMU) And a clock management unit (CMU) Control power consumption of the entire system. From the power-saving level, we can put into power 4 Levels:

The first level is by PRR Operation clock control register module, the clock is not used to close the module, power-saving operation of the system dynamics. Under normal circumstances, this level can save power consumption is not obvious.

The second stage is the primary clock source by switching to the low frequency clock, and a clock source module is not closed, and other analog modules used, this mode can be substantially obtained very substantial operating power consumption of the system and sleep power consumption.

The third level is to enter into power-down mode by the system (DPS1) , DPS1 Mode LGT8FX8P Polar standby power consumption can be obtained from the power down mode wake-up, the software can MCUSR Reading the status register before reset.

The fourth level is a power-down mode (DPS2) This kernel mode turns off the power, can achieve the lowest system power consumption. Due to the closure of the core power, All data will be lost in this mode. Immediately perform a power-on reset process after wake-up, the system starts running again from the reset vector.

AWSON Power Management

versus LGT8FX8D Compared to power-down mode DPS2 A new power mode. DPS2 Mode used for applications with higher power requirements of dormancy. enter DPS2 After, the system only maintains a static module (AWSON) In working condition, other circuits are in full power-down state.

AWSON Module is dedicated to the responsible DPS2 Sleep and wake-up control mode, AWSON Modules mainly by IO Wake-up control logic, and a low power consumption LPRC composition. Software can IOCWK Register and DPS2R Register to achieve AWSON control.

IOCWK Register controls PD0 ~ 7 Level change wake-up function. DPS2R Register controls DPS2 Mode and LPRC Function mode. Please refer to the end of this particular section Register Definition section.

use DPS2 Former mode, software settings IOCWK Enable needed wakeup IO Or by DPS2R Register enables LPRC And configure the timed wake-up period, and then by DPS2R Register DPS2EN Enable bit DPS2 mode. After the setup is complete, the software required by SMCR Register Set DPS2 Sleep mode, then execute SLEEP Command goes to sleep.