		0	sampling	Set up
		1	Set up	sampling
1	SPR1 Clock rate select bit 1 . SPR1 with SPR0 Used to select SPI The clock rate of the transmission. See specific control mode SPCK And the system clock of relational tables.			
0	SPR0 Clock rate select bit 0 . SPR1 with SPR0 Used to select SPI The clock rate of the transmission. See specific control mode SPCK And the system clock of relational tables.			

SPSR - SPI Status Register

SPSR - SPI Status Register								
address: 0x4D					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	SPIF	WCOL	-	-	- DUAL		-	SPI2X
R / W	R	R	R	R	R	R / W	R	R / W
Initial	0	0	0	0	0	0	0	0

Bit	Name	description
7	SPIF	SPI Interrupt flag. After serial transfer set SPIF Under the sign, host mode, Configuring SPSS And when the input pin is pulled low, SPIF It will also be set. If at this time SPCR Register SPIE Bit and global interrupt enable bits are set, SPI An interrupt is generated. After entering the interrupt service routine SPIF Bit is automatically cleared by reading first SPSR Register visit again SPDR Register cleared SPIF Bit.
6	WCOL	Write Collision flag. In the process of writing data transmission SPDR The register set WCOL Bit. WCOL Bit by first reading SPSR Register visit again SPDR Register is cleared.
5	-	Reservations.
4	-	Reservations.
3	-	Reservations.
2	DUAL	Wire mode control bit. When set DUAL Bit "1" , Enable SPI Wire transmission mode. When set DUAL Bit "0" Is prohibited SPI Wire transmission mode. Wire transmission mode only SPI Host active mode, MISO with MOSI Are used as host data input, the data transmission wire receiving host, see chapters describe and model data.
1	-	Reservations.
0	SPI2X	SPI Speed control bits. When set SPI2X Bit "1" Time, SPI The transmission speed is doubled. When set SPI2X Bit "0" Time, SPI The transmission speed is not doubled. See specific control mode SPCK And the system clock of relational tables.

The following table SPCK And the relationship between the system clock.

SPCK And the relationship between the system clock