OCR1AH -TC1 Output Compare Register A High Byte

	OCR1AH	7- TC1 Output C	Compare Registe	er A High Byte				
address: 0x89				Defaults: 0x	Defaults: 0x00			
7	6	5	4	3	2	1	0	
Bit OCR1AH7	OCR1AH6 OC	CR1AH5 OCR1A	H4 OCR1AH3 O	CR1AH2 OCR1A	H1		OCR1AH0	
R/W R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Bit Name descrip	otion							
7: 0 OCR1AH	Bit register of When, it shot OCR1A Con an output co double buffe is disabled. It the time synthesis was a simple of the time synthesis of the time synthe	equires two oper uld read OCR1, tinuously with it impare interrupt, red registers. Ti Double buffering chronization, the	rations. write 16 AL . ne counter value , or to the OC1A ne normal opera g may be update ereby preventing	Te composition to a Place OCR1A of a TCNT1 Comparating mode and read OCR1A Regist grasymmetrical F	When, you show are. Compare meation pins. When match clear movester with the ma	atch can be use then PWM When de, double buffe eximum or minin	AH . read 16 Plated to generate in mode, OCR1A ering function num count up rence pulses.	

OCR1BL -TC1 Output Compare Register B Low byte

		OCR1BI	- TC1 Output C	Compare Regis	ter B Low byte				
address: 0x8A				Defaults: 0x00					
Bit 7	7	6	5	4	3	2	1	0	
	OCR1BL7	OCR1BL6 OCR1BL5 OCR1BL4 OCR1BL3 OCR1BL2 OCR1BL1 OCR1BL0							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Bit	Name descrip	otion							
7: 0 O	¢R1BL	Output Compare Register B The low byte. OCR1BL with OCR1BH Incorporated into the composition together 16 Bit OCR1B. Read and write 16 Bit register requires two operations. write 16 Place OCR1B When, you should write OCR1BH. read 16 Place When, it should read OCR1BL. OCR1B Continuously with the counter value TCNT1 Compare. Compare match can be used to generate an output compare interrupt, or to the OC1B Waveform generation pins. When PWM When mode, OCR1B double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR1B Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR1B When the buffer register, double buffering is disabled CPU Access is OCR1B itself.							