Interrupt handler to an end, a new interrupt will occur.

Disabling the Receiver

Compared with the transmitter, the receiver prohibits immediate. Is receiving data will be lost. Disabling the Receiver (RXEN When cleared), the receiver will not take up RxD Pin, the receive buffer will be flushed.

Register Definition

USART Register List

register address		Defaults	description
UCSRA	0xC0	0x20	USPI Control and status registers A
UCSRB	0xC1	0x00	USPI Control and status registers B
UCSRC	0xC2	0x06	USPI Control and status registers C
UBRRL	0xC4	0x0	USPI Baud Rate Register Low Byte
UBRRH	0xC5	0x0	USPI Baud Rate Register High Byte
UDR	0xC6	0x0	USPI Data register

UCSRA - USPI Control and status registers A

UCSRA - USPI Control and status registers A								
address: 0xC0					Defaults: 0x20			
Bit	7	6	5	4	3	2	1	0
Name	RXC	TXC	UDRE	-	-	-	-	-
R / W	R	R / W	R	-	-	-	-	-

Bit	Name	description
7	RXC	Receive Complete flag. when RXC Value "1" , It indicates that there is data in the receive buffer is not read out. when RXC Value "0" , It indicates that there are no data in the receive buffer is read out. When the receiver is disabled, the receive buffer is refreshed, resulting in RXC Is cleared. When the receiving end interrupt enable bit RXCIE for "1" Time, RXC It can be used to generate a Receive Complete interrupt.
6	TXC	Send flag. When the data transmission is sent to the shift register, and the transmit buffer is empty TXC Position. When performing transmission end interrupt TXC Automatically cleared, it can also pair TXC write "1" To be cleared. When sending end interrupt enable bit TXCIE for "1" Time, TXC It can generate a Transmit Complete interrupt.
5	UDRE	Data register empty flag. when UDRE for "1" When the show USPI Transmission data buffer is empty, data can be written. when UDRE for "0" When the show USPI Transmit data buffer is full, you can not write data. When the Data Register Empty Interrupt Enable bit UDRIE for "1" Time, UDRE Used to generate the data register empty interrupt.
4: 0	-	USPI Under Reserved.