

If PORTxn is written logic one when the pin is configured as an output pin, the port pin is driven high (one). If PORTxn is written logic zero when the pin is configured as an output pin, the port pin is driven low (zero).

## 11.2.2 Toggling the Pin

Writing a logic one to PINxn toggles the value of PORTxn, independent on the value of DDRxn. Note that the SBI instruction can be used to toggle one single bit in a port.

## 11.2.3 Switching Between Input and Output

When switching between tri-state ( $\{DDRxn, PORTxn\} = 0b00$ ) and output high ( $\{DDRxn, PORTxn\} = 0b11$ ), an intermediate state with either pull-up enabled ( $\{DDRxn, PORTxn\} = 0b01$ ) or output low ( $\{DDRxn, PORTxn\} = 0b10$ ) must occur. Normally, the pull-up enabled state is fully acceptable, as a high-impedance environment will not notice the difference between a strong high driver and a pull-up. If this is not the case, the PUD bit in the MCUCR Register can be set to disable all pull-ups in all ports.

Switching between input with pull-up and output low generates the same problem. The user must use either the tri-state ( $\{DDRxn, PORTxn\} = 0b00$ ) or the output high state ( $\{DDRxn, PORTxn\} = 0b11$ ) as an intermediate step.

Table 11-1 summarizes the control signals for the pin value.

**Table 11-1.** Port Pin Configurations

DDxn	PORTxn	PUD (in MCUCR)	I/O	Pull-up	Comment
0	0	X	Input	No	Tri-state (Hi-Z)
0	1	0	Input	Yes	Pxn will source current if ext. pulled low.
0	1	1	Input	No	Tri-state (Hi-Z)
1	0	X	Output	No	Output Low (Sink)
1	1	X	Output	No	Output High (Source)

## 11.2.4 Reading the Pin Value

Independent of the setting of Data Direction bit DDRxn, the port pin can be read through the PINxn Register bit. As shown in Figure 11-2, the PINxn Register bit and the preceding latch constitute a synchronizer. This is needed to avoid metastability if the physical pin changes value near the edge of the internal clock, but it also introduces a delay. Figure 11-3 shows a timing diagram of the synchronization when reading an externally applied pin value. The maximum and minimum propagation delays are denoted  $t_{pd,max}$  and  $t_{pd,min}$  respectively.