SPI2X	SPR1	SPR0	SPCK Frequency of
0	0	0	f_{sys} / 4
0	0	1	f_{sys} / 16
0	1	0	f_{sys} / 64
0	1	1	f_{sys} / 128
1	0	0	f_{sys} / 2
1	0	1	f_{sys} / 8
1	1	0	f_{sys} / 32
1	1	1	f_{sys} / 64

SPDR - SPI Data register

SPDR - SPI Data register								
address: 0x4E					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	SPDR7	SPDR6	SPDR5	SPDR4	SPDR3	SPDR2	SPDR1	SPDR0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	SPDR	SPI Transmission and reception of data. **SPI Transmission data and reception data sharing SPI Data register SPDR . The data is written SPDR** **I.e., the transmission data shift register is written, from SPDR I.e., the read data read received data buffer.**

SPFR - SPI Buffer

SPFR - SPI Buffer								
address: 0x39					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	RDFULI	RDEMPT	RDPTR1	RDPTR0	WRFULL	WREMPT	WRPTR1	WRPTR0
R / W	R	R / W	R	R	R	R / W	R	R

Bit	Name	description
7	RDFULL	Receive buffer full flag. **When receiving the data buffer reaches four bytes, RDFULL Bit is high, indicating that the receive buffer is full, and it** will set interrupt flag. If the software is not timely to go read the data in the receive buffer, the data is received again, the receive buffer overflow occurs before the data is overwritten by new data. **When receiving the data buffer is less than four bytes, RDFULL Bit is low, indicating that the receive buffer is non-full, may also receive data. When at the same time RDEMPT Bit and WREMPT When the bit set operation, receive and transmit buffer address and SPI The shift register pointer are zero, RDFULL Bit is low.**
6	RDEMPT	Receive Buffer Empty flag. When data is not received, RDEMPT Bit is high, indicating that the receive buffer is empty. When data is received, it will be stored in the receive buffer, RDEMPT Bit is low, indicating that the receive buffer is non-empty, then MCU You can access SPDR Register reads the reception buffer