4	TWSTO	TWI Stop state control bit. When in master mode, TWSTO Bit "1" Time, TWI The stop state is generated on the bus, and then automatically cleared TWSTO Bit. In the slave mode, the set TWSTO Bit can make TWI Recover from an error condition. Then the state will not stop, will only make TWI Return to a defined unaddressed slave mode, while releasing SCL with SDA A signal line to a high impedance state.
3	TWWC	TWI Write Collision flag. when TWINT Flag is low, write TWDR Register will be set TWWC Flag. when TWINT Flag is high, write TWDR Register will be cleared TWWC Flag.
2	TWEN	TWI Enable control bit. TWEN Enable bit TWI Operation and activate TWI interface. When set TWEN Bit "1" Time, TWI control IO Pin is connected to SCL with SDA Pin. When set TWEN Bit "0" Time, TWI The interface module is turned off, all of the transmission is terminated, including ongoing operations.
1	-	Reservations.
0	TWIE	TWI Interrupt enable control bit. When set TWIE Bit "1" When, and Global Interrupt set, as long as TWINT Flag is high, it activates TWI Interrupt request.

TWAMR - TWI Address mask register

TWAMR - TWI Address mask register								
address: 0xBD						Defaults: 0x00		
Bit	7	6	5	4	3	2	1	0
Name	TWAR6	TWAR5	TWAR4	TWAR3	TWAR2	TWAR1	TWAR0	TWGCE
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 1	TWAM [6: 0]	TWI An address mask control bits. TWAM for 7 Place TWI Slave address mask control. TWAM Each bit is used to shield (prohibited) TWAR The corresponding address bit. When the mask bit address match logic ignores address bit received and TWA A comparison result of the corresponding bit. The following figure shows the details of the address match logic.
0	-	Reservations.

TWI Address match logic

The figure below shows TWI Address match logic diagram: