OCR1BH -TC1 Output Compare Register B High Byte

OCR1BH - TC1 Output Compare Register B High Byte								
address: 0x8B					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR1BH7	OCR1BH6	OCR1BH5	OCR1BH4	OCR1BH3	OCR1BH2	OCR1BH1	OCR1BH0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	OCR1BH	Output Compare Register B The high byte. OCR1BL with OCR1BH Incorporated into the composition together 16 Bit OCR1B . Read and write 16 Bit register requires two operations. write 16 Place OCR1B When, you should write OCR1BH . read 16 Place OCR1B When, it should read OCR1BL . OCR1B Continuously with the counter value TCNT1 Compare. Compare match can be used to generate an output compare interrupt, or to the OC1B Waveform generation pins. When PWM When mode, OCR1B Using double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR1B Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR1B When the buffer register, double buffering is disabled CPU Access is OCR1B itself.

TIMSK1 - TC1 Interrupt mask register

TIMSK1 - TC1 Interrupt mask register								
address: 0x6F					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	-	-	TICIE1	-	-	OCIE1A	OCIE1B	TOIE1
R / W	-	- R / W		-	- R / W		R / W	R / W

Bit	Name	description
7: 6	-	Reservations.
5	TICIE1	TC1 Input Capture interrupt enable control bit. when ICIE1 Bit "1" When, and Global Interrupt set, TC1 Input Capture interrupt is enabled. When the input capture trigger, that is, TIFR1 of ICF1 Flag is set, an interrupt occurs. when ICIE1 Bit "0" Time, TC1 Input capture interrupts are disabled.
4: 3	-	Reservations.
2	OCIE1B	TC1 Output Compare B Match interrupt enable bit. when OCIE1B Bit "1" And Global Interrupt Set, TC1 Output Compare B Match interrupt is enabled. When a compare match occurs, i.e., TIFR in OCF1B When the bit is set, an interrupt is generated. when OCIE1B Bit "0" Time, TC1 Output Compare B Match interrupts are disabled.
1	OCIE1A	TC1 Output Compare A Match interrupt enable bit. when OCIE1A Bit "1" And Global Interrupt Set, TC1 Output Compare A Matching