1	TCR2AUB	TCCR2A Register update flag. When the timer 2 Work in asynchronous mode, for TCCR2A When a write operation, TCR2AUB Bit is set. when TCCR2A After the updated value of the hardware will be cleared TCR2AUB Bit. Only when TCR2AUB Bit 0 When, available for TCCR2A Updated.
0	TCR2BUB	TCCR2B Register update flag. When the timer 2 Work in asynchronous mode, for TCCR2B When a write operation, TCR2BUB Bit is set. when TCCR2B After the updated value of the hardware will be cleared TCR2BUB Bit. Only when TCR2BUB Bit 0 When, available for TCCR2B Updated.