## Pin Description

LGT8FX8P Series package, QFP48L All package lead pin. Other packages are in QFP48 On the basis of multiple internal I / O Bound to produce a pin. Special care configure the pin direction. The following table lists a variety of package pins binding information:

QFP48 QFP	32 SSOP20 Fu	nction Descripti	on
			PD3 / INT1 / OC2B * PD3: Programmable port D3
01	01		INT1: External interrupt input 1 OC2B: Timer 2 Compare
			Match Output B
		03	PD4 / DAO / T0 / XCK PD4: Programmable
			port D4 DAO: internal DAC Export
02	02		
			T0: Timer0 External clock input
			XCK: USART Transmit clock
			PE4 / 0C0A * PE4: Programmable port E4 OC0A: Timer
03	03	-	0 Compare Match Output A
			PF3 / OC3C / OC0B * PF3: Programmable port F3
04	_	_	OC3C: Timer 3 Compare Match Output C OC0B: Timer
			0 Compare Match Output B
			PF4 / OC1B * / ICP3 PF4: Programmable port F4
05	03	03	OC1B: Timer 1 Compare Match Output B ICP3: Timer 3
		03	Capture input
06	04	04	vcc
07	05	<b>05</b> GND	
			PE5 / AC10 / CLK0 * PE5: Programmable
08		_	port E5 C1O: Analog comparator AC1 Export
	06		CLKO: System clock output
			PF5 / OC1A * PF5: Programmable port F5 OC1A: Timer
09		06	1 Compare Match Output A
			PF6 / T3 / OC2A * PF6: Programmable port F6
10	-	-	T3: Timer 3 External clock input
			OCCAL Timer 2 Compare Metch Output A
			OC2A: Timer 2 Compare Match Output A
14	07	06	PB6 / XTALO PB6: Programmable port B6  XTALO: Control IO Output port
11	07	06	XTALO: Crystal IO Output port