

26.6 SPI Timing Characteristics

See [Figure 26-5](#) and [Figure 26-6](#) for details.

Table 26-5. SPI Timing Parameters

	Description	Mode	Min	Typ	Max	
1	SCK period	Master		See Table 16-5		ns
2	SCK high/low	Master		50% duty cycle		
3	Rise/Fall time	Master		3.6		
4	Setup	Master		10		
5	Hold	Master		10		
6	Out to SCK	Master		$0.5 \cdot t_{sck}$		
7	SCK to out	Master		10		
8	SCK to out high	Master		10		
9	\overline{SS} low to out	Slave		15		
10	SCK period	Slave	$4 \cdot t_{ck}$			
11	SCK high/low ⁽¹⁾	Slave	$2 \cdot t_{ck}$			
12	Rise/Fall time	Slave			1600	
13	Setup	Slave	10			
14	Hold	Slave	t_{ck}			
15	SCK to out	Slave		15		
16	SCK to \overline{SS} high	Slave	20			
17	\overline{SS} high to tri-state	Slave		10		
18	\overline{SS} low to SCK	Slave	20			

- Note:
- In SPI Programming mode the minimum SCK high/low period is:
 - $2 t_{CLCL}$ for $f_{CK} < 12$ MHz
 - $3 t_{CLCL}$ for $f_{CK} > 12$ MHz
 - All DC Characteristics contained in this datasheet are based on simulation and characterization of other AVR microcontrollers manufactured in the same process technology. These values are preliminary values representing design targets, and will be updated after characterization of actual silicon.