E2PCTL Read and write FLASH Program Space

by E2PCTL The controller can be achieved on the program FLASH Read and write access to space. And simulation E2PROM The difference is that by E2PCTL The program FLASH Access to space requires full software control. Proceed as follows:

1. Erase the target page, you need to first erase data before updating the target page, the page address EEAR To register Out. Correct FLASH Page erase command and control, please refer to EECR Defined register;
2. programming FLASH Space must be 32 Bit is the smallest unit. by E2PD0 ~ 3 Setting data;
3. By the destination address EEAR Given register, the address EEAR [1: 0] It will be ignored;

by E2PCTL Literacy program FLASH Space, can be achieved online updates (IAP) Function, in some field applications require custom update update application data and the need for the product, very useful.

E2PCTL Interface operation process

E2PCTL The controller works primarily through 4 Registers implemented, respectively, E2PCTL Control Status Register EECR , ECCR ; Data register EEDR (E2PD0 ~ E2PD3) And address register EEAR (EEARL / EEARH) .

ECCR Register sets E2PCTL Working conditions, required in most states E2PCTL Set before the completion of the work, this process is generally implemented in a system initialization. ECCR Register SWM Write bit enables the continuous mode, the control bit needs to be set in a continuous operation during the write.

EECR For controlling the operation type selection register, to select an operation instruction, such as setting the read, erase command.

EEDR Register for 8 Byte mode interface, E2PD0 ~ 3 For 32 Write bit mode operation;

EEAR Register sets read and write target address, page address is also used to set the page erase operations. Page address is the page-bit units have been aligned, the page size is 1K Byte, note EEAR Specified address is a byte address.

by E2PCTL Access Interface FLASH Program space:

by E2PCTL Interface can be achieved on FLASH Read, write and erase program space. Correct FLASH Supports only reading and writing space 32 Bit access width. Page erase operation to position the unit, the size of each page 1K byte(256x32) .

Write FLASH Before the program space, First page erase the destination address is located. E2PCTL write FLASH Space program does not support continuous mode, Users need in order to complete the write operation. The following is a rewritable FLASH Program space process:

1. program FLASH Page Erase

- Set up EEAR [14: 0] To be erased target page address, the program FLASH One size 1K Bytes, EEAR [14:10] The page address, EEAR [9: 0] Set as 0
- Set up EEPM [3: 0] = 1X01 ,among them EEPM [2] Can be set 0 or 1
- Set up EEMPE = 1 , Simultaneously EEPE = 0
- Within four cycles, provided EEPE = 1 ,starting program FLASH Erase Procedure

2. program FLASH Program operation

- write E2PD0 ~ 3 ,ready 32 Bit programming data
- Set up EEAR As the destination address, the address is here 4 Byte alignment
- Set up EEPM [3: 0] = 1X10 , among them EEPM [2] Can be set 0 or 1
- Set up EEMPE = 1 ,Simultaneously EEPE = 0
- Within four cycles, provided EEPE = 1 ,start up FLASH Programming Process