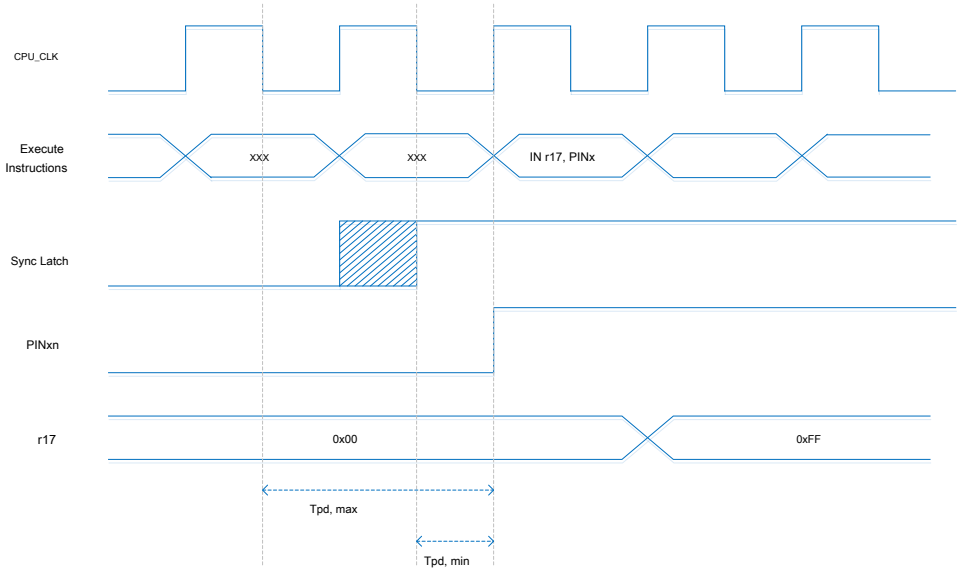

in case PORTxn Bits are written 1 While this port is configured as input port, the port of the pull-up resistor valid. If you want to ban port pull-up resistor, PORTxn It must be written as 0 Or this port is configured as an output port.

Reset initialization state of the port as an input, the pull-up resistor invalid.

PORTxn Set as 1 While this port is configured as an output port, the external port will be driven high. in case PORTxn Set as 0 , The port will be driven low.

Input / Output

when I / O Tristate state ([DDxn, PORTxn]) = 0b00) And output high ([DDxn, PORTxn] = 0b11) When switching between, there will be pulled low or intermediate output port status. Typically, a pull-up resistor can be accepted, because in a high-impedance environment, driven high **and the difference between the pull is not important. If this is not the case, you can MCUCR Register PUD Close the pull-bit port.**

Similarly, when the switching between the pull low energy input and output, the same problem occurs. The user must tri-state ([DDxn, PORTxn] = 0b00) Or high output ([DDxn, PORTxn] = 0b11) As an intermediate state.

Port drive configuration table:

DDxn	PORTxn	PUD	Port Status	Pull-Function
0	0	X	Entry	Prohibit tri-state (High-Z)
0	1	0	Entry	Enable + Internal pull mode input
0	1	1	Entry	Prohibit tri-state (High-Z)
1	0	X	Export	Prohibition low output (fan)
1	1	X	Export	Ban high output (fan-out)

Read port value

Whether the port direction bit DDxn How to set, to pass through PINxn Register bits read current status of the port. To avoid direct read port to produce metastable, PINxn It is through a port register bit synchronizer results. The synchronizer of a latch and a register composed, so PINxn There is a small delay between the value of the current port. This delay is due to the result of the presence of the synchronizer, the delay time of up to 1 Periodic half.

We assume that the system cycle begins with the first falling edge of the system clock, the data latched in the latch clock is low, the clock is high linear data through the latch as shown in the above figure shaded. When the clock is low, data is latched in the port