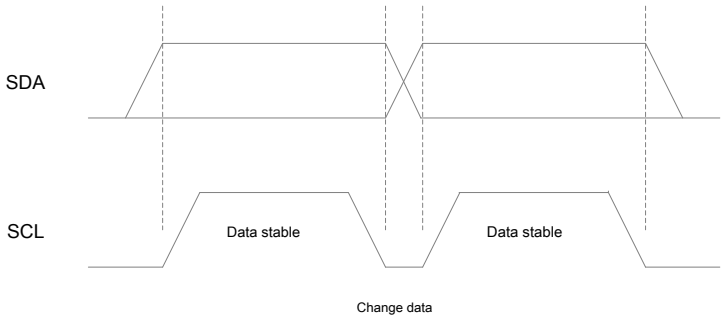
Data transmission and frame structure

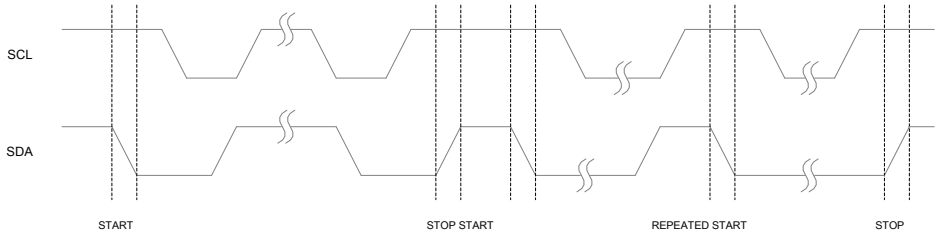
TWI Every data transfer on the bus and the clock are synchronized. While the clock is high, the level of the data line must remain stable, except to start or stop generating state.



TWI Data validation map

Start and stop state

TWI The transmission is started and stopped by the host. Host issues on the bus START Send its data transfer status, issued STOP State to stop the data transmission. in START with STOP Between the state, the bus is considered busy, do not allow other hosts trying to take the control of the bus. There is a special case only allowed to occur in START with STOP Generating a new state between START State, which is called REPEATED START Status for the current host to start a new transfer, without giving up control of the bus. REPEATED START Until next STOP Previously, the bus is still considered busy. This START It is the same, so in this document, unless otherwise stated, are used START To express START with REPEATED START . As shown below, START with STOP Conditions in SCL When the line is high, changes SDA The level of status line.



START , REPEATED START with STOP State diagram

Address Packet Format

all TWI Address packet transmitted on the bus are 9 Bit data length, from the 7 Bit address, 1 Place READ / WRITE And control bits 1 Bit acknowledgment bit. when READ / WRITE Bit "1" , The read operation is performed; when READ / WRITE Bit "0" , The write operation is performed. When a slave is addressed must first 9 More SCL (ACK) By pulling cycle SDA Line to make a response. If the slave is busy or there are other reasons not respond to the host, you should ACK Keep the cycle SDA Line is high. The host can then issue STOP State or REPEATED START State resumes sent.