FWKPEN	Filter Width
0	260us (default)
1	32us

Register Description

Sleep Mode Control Register - SMCR

SMCR - Sleep Mode Control Register							
SMCR: 0x33 (0x53)				Defaults: 0x00			
Bits				SM2	SM1	SM0	SE
R / W	-			R / W	R / W	R / W	R / W
Bit Definitions							
[0]	SE	Sleep mode enable control bit, is set to 1 After execution SLEEP Instructions, the core will enter the sleep mode. SE Bit can protect the system into sleep mode unexpectedly. After the wake, it is recommended immediately clear SE Bit.					
[3: 1]	SM	Sleep Mode Select					
		SM2	SM1	SM0 Mode	Description		
		0	0	0	IDLE mode		
		0	0	1	ADC Noise Reduction		
		0	1	0	Save mode		
		0	1	1	DPS1 mode		
		1	1	0	DPS0 mode		
		1	1	1	DPS2 mode		
		Others			Are reserved		
[7: 4]	-	Are reserved					

Saving Control Register - PRR

PRR - Power control register								
PRR: 0x64					Defaults: 0x00			
PRR	PRTWI	PRTIM2	PRTIM0	-	PRTIM1	PRSPI	PRUART0	PRADC
R / W	R / W	R / W	R / W	-	R / W	R / W	R / W	R / W
Bit Definitions								
[0]	PRADC Set as 1 ,shut down ADC Controller Clock							
[1]	PRUART0 Set as 1 ,shut down USART0 The clock module							
[2]	PRSPI	Set as 1 ,shut down SPI The clock module						
[3]	PRTIM1 Set as 1 Disables the timer / counter 1 Clock							
-	-	Are reserved						
[5]	PRTIM0 Set as 1 Disables the timer / counter 0 Clock							
[6]	PRTIM2 Set as 1 Disables the timer / counter 2 Clock							
[7]	PRTWI	Set as 1 ,shut down TWI The clock module						