And the receiver uses, this process introduces a delay of two system clocks, thus the external XCK The maximum clock frequency is limited by the following equation:

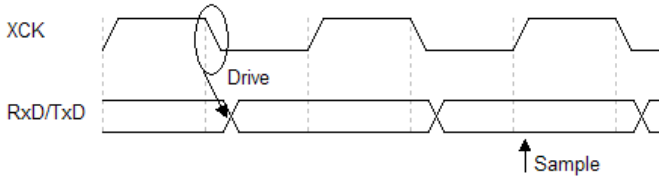
$$f_{XCK} < f_{sys} / 4$$

pay attention fsys Systematic clock stability of the decision, in order to prevent loss of data due to the frequency drift, proposed to retain a sufficient margin.

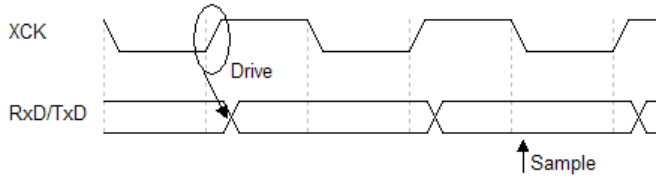
Synchronous Clock Operation

In synchronous mode, XCK A clock input pin is a clock output (master mode) (slave mode). The basic rule of the data sampling clock edge and data changes the relationship is: the data input terminal (RxD) And the clock edge data output clock edge sampling variation used is used contrary.

UCPOL = 1



UCPOL = 0



In synchronous mode XCK Timing

As shown above, when UCPOL Value "1" When, in XCK The falling edge of output data changes in XCK The rising edge of data samples; when UCPOL Value "0" When, in XCK The rising edge of output data changes in XCK The falling edge of the data sampling.

Frame format

A serial data frame synchronization bit (start and stop bits) and a parity bit for error plus a data word.

USART Accept the following 30 Data frame format combination:

- 1 Start bit
- 5 , 6 , 7 , 8 or 9 Data bits
- No parity bit, odd or even parity bit parity bit
- 1 or 2 Stop bit

Data frame begins with a start bit, followed by the least significant bit of the data word, followed by the other data bits, the highest bit data word end, most successful transmission 9 Bit data. If enabled, the parity, parity bit data word will be followed, and finally the stop bit. When a complete data frame transmission, the transmission can be immediately a new frame, or to the transmission line is idle (high) state. Below shows the possible data frame structure, the bits in square brackets are optional.