		Compare output waveform occupies OC0B Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM0B The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
4	COM0B0	TC0 Compare match B Low output mode control. COM0B0 with COM0B1 Together comprise comparison output mode control COM0B [1: 0] To control OC0B The output waveform. in case COM0B of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC0B Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM0B The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
3	DOC0B	TC0 Close control of the high output of the comparator is enabled. when DOC0B Bit "1" It is triggered off the output comparison signal source OC0B It is enabled. When a trigger event occurs, the hardware is automatically cleared COM0B Position, close OC0B The waveform output. By setting software COMB May re-open PWM Output. when DOC0B Bit "0" It is triggered off the output comparison signal source OC0B Prohibited.
2	DOC0A	TC0 Close control of the low output of the comparator is enabled. When set DOC0A Bit "1" It is triggered off the output comparison signal source OC0A It is enabled. When a trigger event occurs, the hardware automatically shut down OC0A The waveform output. When set DOC0A Bit "0" It is triggered off the output comparison signal source OC0A Prohibited. When a trigger event occurs, will not close OC0A The waveform output.
1	WGM01	TC0 Waveform generation mode control bits. WGM01 with WGM00 , WGM02 Together form waveform generation mode control WGM0 [2: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
0	WGM00	TC0 Waveform generation mode control low. WGM00 with WGM01 , WGM02 Together form waveform generation mode control WGM0 [2: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.

TC0 Control register B- TCCR0B

TCCR0B - TC0 Control register B								
address: 0x45						Defaults: 0x00		
Bit	7	6	5	4	3	2	1	0
	FOC0A	FOC0B	OC0AS	DTEN0	WGM02	CS02	CS01	CS00
R / W	W	W	W / R	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	FOC0A	TC0 Force Output Compare A Control bit. In non PWM Mode, the force output by comparing bits FOC0A write "1" The way to compare match. Forcing compare match will not set OCF0A Flag or reload or clear the timer, but the output pin OC0A Will be in accordance with COM0A It sets the appropriate update, just compare match had really happened. Read FOC0A The return value is always zero.
6	FOC0B	TC0 Force Output Compare B Control bit.