System Support 5 Different addressing modes can cover the entire data space: Direct access Indirect access band offset, indirect access, front access to decrement indirect access address, the access address increment indirect access. General purpose working registers R26 To R31 Indirect address pointer for access. Indirect addressing can access the entire data storage space. With indirect access to the offset address can be addressed to Y / Z Near the base address register 63 Address space.

When using the support auto-increment / decrement register indirect access mode, the address register X / Y / Z Will automatically decrement / increment by hardware access occurs before / after. Refer to the instruction set description section.

16 Bit register X / Y / Z And the associated automatic addressing mode (increasing, decreasing), in 16 Lower extended mode also has a very important role. 16 Bit extended mode can be used LD / ST The increment / decrement mode, with automatic variable increment, decrement addressing. This mode when an arithmetic operation of the array, will be very effective. Please refer to the specific implementation " Digital arithmetic accelerator (uDSU) " The relevant sections.

Common I / O register

LGT8FX8P of I / O There are three common space I / O register GPIOR2 / 1/0 , These three registers can be used IN / OUT Access instruction, for storing user-defined data.

Peripheral register space

I / O Detailed definition of space, see LGT8FX8P Data Sheet " Registers Overview " chapter.

LGT8FX8P So peripherals are assigned to I / O space. all I / O Address space can be LD / LDS / LDDD as well as ST / STS / STD Instruction accesses. Data access is through 32 General purpose working registers transfer. in 0x00 ~ 0x1F between I / O Instruction register can be addressed via bit SBI with CBI access. In these registers, a bit value may be used a SBIS with SBIC Instruction detection, process control program to execute. Refer to the instruction set description section.

When IN / OUT Instruction Access I / O When the register must be addressed 0x00 ~ 0x3F Address between. When LD or ST Instruction Access I / O When space must pass I / O Space unified data mapping space in the system memory map address access (plus 0x20 Offset). Some other assignments in the extended I / O Peripheral register space (0x60 ~ 0xFF) , Can only use ST / STS / STD with LD / LDS / LDD Instruction accesses.

For compatibility with future devices, reserved bits must be written in the write operation 0 . You can not be reserved I / O Write operation is performed on the space.

Some registers include a state flag that needs to be written 1 It can be cleared. have to be aware of is, CBI with SBI Command supports only specific bits, CBI / SBI It can only work on registers containing such status flags. In addition, CBI / SBI Command can only work in 0x00 To 0x1F Registers this address range.

FLASH Controller (E2PCTL)

LGT8FX8P Internally integrates a flexible and reliable EFLASH Read-write controller, the system may utilize existing data FLASH Memory, read and write access for byte of storage space, to achieve a similar E2PROM Storage applications; E2PROM Interface using flash analog equalization algorithm, data can be FLASH Life cycle improve 1 Times or so, to ensure 100,000 Or more of erase cycles.

E2PCTL The controller also realized the FLASH Online program space erase operation can be achieved through software online from