TCKCSR - TC Clock control and status registers

TCKSCR - TC Clock control and status registers								
address: 0xEC					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	F2XEN	TC2XF1	TC2XF0	-	AFCKS	TC2XS1	TC2XS0
R / W	-	R / W	R	R	- R / W		R / W	R / W

Bit	Name	description
7	-	Retention
6	F2XEN	RC 32M Output enable control bit multiplier. When set F2XEN Bit "1" Time, 32M RC Output frequency of the oscillator is enabled, the output 64M The high-speed clock. When set F2XEN Bit "1" Time, 32M RC Frequency output of the oscillator is disabled, can not output 64M The high-speed clock.
5	TC2XF1	TC High-speed clock mode flag 1 . See the timing counter 1 Register description.
4	TC2XF0	TC High-speed clock mode flag 0 . When read TC2XF0 Bit "1" , It indicates that the timer counter 0 Work on the high-speed clock mode, as "0" , It indicates that the timer counter 0 Work on the system clock mode.
3: 2	-	Reservations.
1	TC2XS1	TC High speed clock mode selection control bits 1 . See the timing counter 1 Register description.
0	TC2XS0	TC High speed clock mode selection control bits 0 . When set TC2XS0 Bit "1" When selecting the timer counter 0 Work on the high-speed clock mode. When set TC2XS0 Bit "0" When selecting the timer counter 0 Work on the system clock mode.