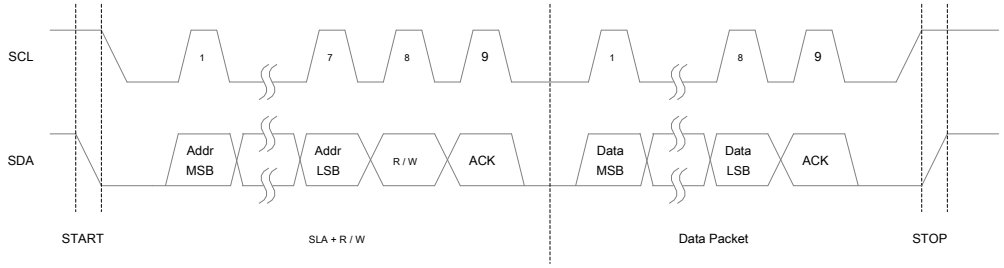
Packet and 1 More STOP composition. only START with STOP Empty information is illegal. can use SCL Wire line and shake hands with the main function to achieve from the machine. Slave down by SCL To extend the line SCL The ground level cycle. When the host is set much faster than the clock slave or slave requires additional time to process the data, this feature is very useful. Slave to extend SCL LOW period does not affect SCL High-level period, it is still determined by the host. It can be seen, by changing the slave SCL To reduce the duty cycle TWI The data transmission speed.

A typical data transfer is shown below. note SLA + R / W versus STOP It can be transferred between a plurality of bytes, depending on the application software to implement the protocols.



typical TWI transmission

Multi-host system and arbitration and synchronization

TWI Bus protocol allows multiple hosts, and the use of special measures to ensure that even if two or more hosts can be simultaneously start the transfer process the same as normal transmission. Multi-host system there will be two questions:

1. The algorithm allows only one host, multiple hosts to complete the transfer. When other hosts find that they will lose the right to choose

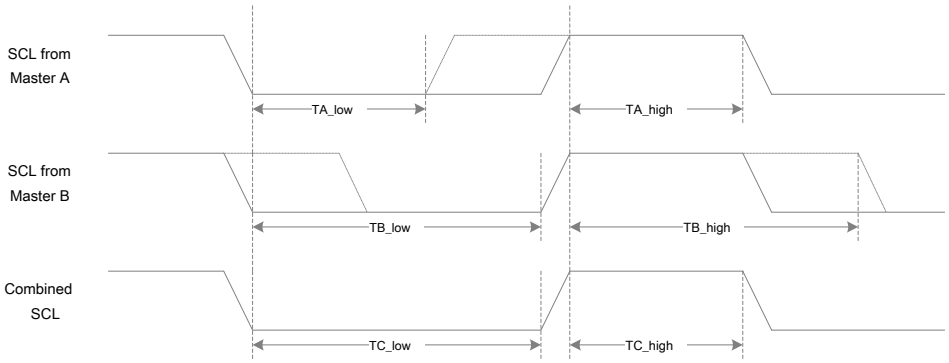
   To cease their transmission. The selection process is called arbitration. When a contending master arbitration found to fail, the address should switch immediately to the host whether it is control of the bus slave mode to detect. Indeed multiple hosts simultaneously should not be detected from the machine at the start of transmission, i.e., destruction of data being transferred is not allowed on the bus.

2. Different hosts may use different SCL frequency. To ensure a consistent transfer, you must design a synchronous serial host

   Line clock program. This will facilitate the arbitration process.

Bus line and the function is to solve the above problems. All hosts are serial clock line to generate a composition with clock, high time which is equal to a master clock in all the shortest, equal to its low level in all the longest of the host clock. All masters listen SCL When combined SCL When the clock goes high or low, respectively, they can be effectively calculate respective start SCL High and low out period.

Multi-host SCL The clock synchronization mechanism as shown below:



Multi-Host SCL Clock synchronization timing chart