Divider reset

Multiplexed mode

When set PSS1 Bit "0" And PSS3 Bit "0" Time, TC0 , TC1 with TC3 Share a prescaler CPS310 .

The prescaler is free running, its operation is independent of the TC The clock selection logic, and which consists of TC0 , TC1 with TC3 shared. Since not affect the control of the clock selection, impact on application status will be divided clock prescaler. When the output is enabled and the **timer prescaler selected as the count clock source (6> CSn [2: 0]> 1 Time), the impact it will have. From the timer is enabled to the first count may take 1 To N + 1 System clock, wherein N To prescale factor (8 ,**

64 , 256 or 1024).

To synchronize the timer and reset program is run by the prescaler is possible. It must be noted, however, whether the other is using the timer prescaler prescaler reset will affect all timers connected to it.

Alone mode

When set PSS1 Bit "1" Time, TC1 Independently prescaler CPS1 , Reset by prescaler PSR1 Bit to control. Respective reset function separately, without affecting other prescaler.

When set PSS3 Bit "1" Time, TC3 Independently prescaler CPS3 , Reset by prescaler PSR3 Bit to control. Respective reset function separately, without affecting other prescaler.

When set PSS1 Bit "1" And PSS3 Bit "1" Time, TC0 Independently prescaler CPS310 , Reset by prescaler PSRSYNC Bit to control, TC1 Independently prescaler CPS1 , TC3 Independently prescaler CPS3 Respective reset function separately, without affecting other prescaler.

External clock source

by T0 / T1 / T3 External clock source pin can be used as the count clock source. T0 / T1 / T3 After the signal pin and the synchronization logic edge detector as counter clock source. Each rising edge (CSn [2: 0] = 7) Or falling edge (CSn [2: 0] = 6) Will produce a count pulse. External clock source will not be sent to the prescaler.

Since the pin is synchronized with the presence of the edge detecting circuit, T0 / T1 / T3 Changes in the level needs to be delayed 2.5 To 3.5 System clock to the counter update.

Enabling and disabling of the clock input must be T0 / T1 / T3 Stable for at least the need for a system clock cycle, otherwise it is likely to have generated error count clock pulses.

In order to ensure correct sampling clock pulse width must be greater than the external system clock cycle, the duty ratio of 50%
When the external clock frequency must be less than half the system clock frequency. Due to differences in the clock oscillator frequency and duty cycle of **the system itself caused the error, recommendations of the external clock frequency is not greater than the maximum f_{sys} / 2.5 .**