2. Set up SPN = 1 ,start up ADC Sampling, recording ADC Sampling results VADC1

3. Set up SPN = 0 ,start up ADC Sampling, recording ADC Sampling results VADC2

4. (VADC1 + VADC2) >> 1 This is the ADC The conversion result

In practice, this algorithm can be combined with the sampling averaging algorithm, even better results can be obtained.

Register Definition

ADC Register List

register	address	Defaults	description
ADCL	0x78	0x00	ADC Low Byte Data Register
ADCH	0x79	0x00	ADC High Byte Data Register
ADCSRA	0x7A	0x00	ADC Control and status registers A
ADCSRB	0x7B	0x00	ADC Control and status registers B
ADMUX	0x7C	0x00	ADC Multiplexer control register
ADCSRC	0x7D	0x01	ADC Control and status registers C
DIDR0	0x7E	0x00	Digital Input Disable Control Register 0
DIDR1	0x7F	0x00	Digital Input Disable Control Register 0
DAPCR	0xDC	0x00	The differential amplifier control register
OFR0	0xA3	0x00	Offset compensation register 0
OFR1	0xA4	0x00	Offset compensation register 1
ADT0L	0xA5	0x00	Automatic monitoring low threshold underflow 8 Place
ADT0H	0xA6	0x00	Automatic monitoring high threshold underflow 8 Place
ADT1L	0xAA	0x00	Automatic monitoring low threshold overflow 8 Place
ADT1H	0xAB	0x00	Automatic monitoring high threshold overflow 8 Place
ADMSC	0xAC	0x01	Automatic monitoring of status and control registers
ADCSRD	0xAD	0x00	ADC Control and status registers D

ADCL - ADC Low Byte Data Register

ADCL - ADC Low Byte Data Register								
address: 0x78					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name0	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Name1	ADC3	ADC2	ADC1	ADC0	-	-	-	-
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Initial	0	0	0	0	0	0	0	0

Bit	Name	description
7: 0	ADC [7: 0] / ADC [3: 0]	ADC Data low byte register. when ADLAR Bit "0" Time, ADC Output data are aligned in the low storage register, i.e., ADCL for ADC [7: 0] ,Such as Name0 Shown; if ADLAR Bit "1" Time, ADC High output data are stored in the register are aligned, i.e., ADCL height of 4 Bit ADC [3: 0] ,low 4 Bit meaningless, as Name1 Fig.