	when DOC3B Bit disables the output is relatively high, hardware B Is enabled, the output after the prohibition condition is satisfied, COM3B Bit is cleared, the output pin OC3B Off the pin becomes universal IO operating. when DOC3B Bit is low,
	the output of the comparator is prohibited hardware B Function is disabled.
4	DOC3A Prohibit output of the comparator A Enable control bit.
	when DOC3A Bit disables the output is relatively high, hardware A Is enabled, the output after the prohibition condition is
	satisfied, COM3A Bit is cleared, the output pin OC3A Off the pin becomes universal IO operating. when DOC3A Bit is low,
	the output of the comparator is prohibited hardware A Function is disabled.
3	DTEN3 Dead time enable control bit.
	when DTEN3 Bit is high, the dead time is enabled, OC3A with OC3B Become complementary output, and press DTR3L
	with DTR3H Set to insert dead time. when DTEN3 Bit is low, the dead time is disabled. OC3A with OC3B Are single
	output.
2	-
1	DOC3C Prohibit output of the comparator C Enable control bit.
	when DOC3C Bit disables the output is relatively high, hardware C Is enabled, the output after the prohibition condition is
	satisfied, COM3C Bit is cleared, the output pin OC3C Off the pin becomes universal IO operating, when DOC3C Bit is low,
	the output of the comparator is prohibited hardware C Function is disabled.
0	FOC3C Force Output Compare C .
	In non PWM Mode, the force output by comparing bits FOC3C write "1" The way to compare match. Forcing compare
	match will not set OCF3C Flag or reload or clear the timer, but the output pin OC3C Will be in accordance with COM3C It
	sets the appropriate update, just compare match had really happened. Work on PWM When mode, write TCCR3A Cleared
	when you want to register. Read FOC3C The return value is always zero.

## TCCR3D-TC3 Control register D

			TCCR3D - 1	C3 Control register [	)				
address: 0x93						Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0	
Name	DSX37	DSX36	DSX35	DSX34	-	- DSX3	1 DSX30		
R/W	R/W	R/W	R/W	R/W	-	-	R/W	R/W	
Bit	Name description								
7	DSX37 TC3 Select the trigger source control enables the first 7 Bit.								
		When set DSX37 Bit "1" Time, TC0 As the output of the comparator is off the overflow signal waveform OC3x							
	1	The trigger source is enabled. when DOC3x Bit "1" Rising edge triggered interrupt source, the selected flag register bits							
		will automatically shut down OC3x The waveform output. When set DSX37 Bit "0" Time, TC0 As the output of the							
		comparator is off the overflow signal waveform OC3x							
	1	The trigger source is prohibited.							
6	DSX36 TC3 Select the trigger source control enables the first 6 Bit.								
	When set DSX36 Bit "1" Time, TC2 As the output of the comparator is off the overflow signal waveform OC3x								
	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	When set DSX36	Bit "1" Time, TC2 /	As the output of the	comparator is off	the overflow signa	I waveform OC	3x	
				As the output of the DOC3x Bit "1" Risi	·	_			
	1	The trigger source	is enabled. when	·	ng edge triggered	interrupt source, th	ne selected flag	register bits	
	1	The trigger source	is enabled. when	DOC3x Bit "1" Risi	ng edge triggered	interrupt source, th	e selected flag	register bits	