Register Definition - SREG

SREG System Status Register								
Address: **0X3F (0X5F)**				Defaults: **0X00**				
Bit	7	6	5	4	3	2	1	0
Name	I	T	H	S	V	N	Z	C
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Definition								

[0]	C	Carry flag, indicating that the arithmetic or logic operation caused the carry. *
[1]	Z	A zero flag indicating that the result of an arithmetic or logical operation is zero. *
[2]	N	A negative flag indicates that an arithmetic or logic operation has produced a negative number. *
[3]	V	The overflow flag indicates that the result of the two's complement operation has overflowed. *
[4]	S	Sign bit, equivalent to the XOR operation result of N and V *
[5]	H	Semi-carry flag, useful in BCD operations, indicating the semi-carry generated by byte operations*
[6]	T	For temporary bits, bit copy (BLD) and bit store (BST) instructions, the T bit is used as a temporary memory bit to temporarily store the value of a bit in the general purpose register. *
[7]	I	The global interrupt enable bit must be set to 1 to enable the CPU to respond to interrupt events. Different interrupt sources are controlled by independent control bits. The global interrupt enable bit is the last barrier that controls the interrupt signal into the CPU. The I bit is automatically cleared in hardware when the CPU responds to the interrupt vector and is automatically set after the interrupt return instruction (RETI) is executed. The I bit can also be changed using the SEI and CLI instructions. *

** Please refer to the instruction description for details.*

General Purpose Register

The General Purpose Registers are optimized for the LGT8XM instruction set. To achieve the efficiency and flexibility required for core execution, the LGT8XM's internal working registers support several access modes:

- Simultaneous 8-bit read and 8-bit write
- Two 8-bit reads simultaneously with 8-bit write
- Two 8-bit reads simultaneously with one 16-bit write
- One 16-bit read simultaneously with one 16-bit write