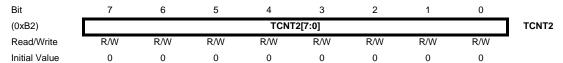
Table 15-9. Clock Select Bit Description

CS22	CS21	CS20	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	clk <sub>T2S</sub> /(No prescaling)
0	1	0	clk <sub>T2S</sub> /8 (From prescaler)
0	1	1	clk <sub>T2S</sub> /32 (From prescaler)
1	0	0	clk <sub>T2S</sub> /64 (From prescaler)
1	0	1	clk <sub>T2S</sub> /128 (From prescaler)
1	1	0	clk <sub>T2S</sub> /256 (From prescaler)
1	1	1	clk <sub>T2S</sub> /1024 (From prescaler)

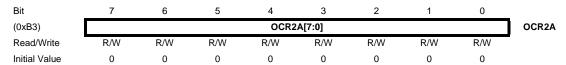
If external pin modes are used for the Timer/Counter0, transitions on the T0 pin will clock the counter even if the pin is configured as an output. This feature allows software control of the counting.

## 15.11.3 TCNT2 – Timer/Counter Register



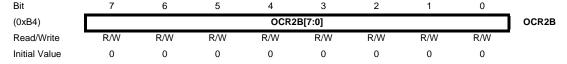
The Timer/Counter Register gives direct access, both for read and write operations, to the Timer/Counter unit 8-bit counter. Writing to the TCNT2 Register blocks (removes) the Compare Match on the following timer clock. Modifying the counter (TCNT2) while the counter is running, introduces a risk of missing a Compare Match between TCNT2 and the OCR2x Registers.

## 15.11.4 OCR2A – Output Compare Register A



The Output Compare Register A contains an 8-bit value that is continuously compared with the counter value (TCNT2). A match can be used to generate an Output Compare interrupt, or to generate a waveform output on the OC2A pin.

## 15.11.5 OCR2B – Output Compare Register B



The Output Compare Register B contains an 8-bit value that is continuously compared with the counter value (TCNT2). A match can be used to generate an Output Compare interrupt, or to generate a waveform output on the OC2B pin.

