TWI - Two-wire serial bus (I2C)

- Simple and powerful and flexible communication interface, only 2 line
- Support master and slave operation
- Device may operate in transmission mode or reception mode
- 7 Bit address space allows 128 Slaves
- It supports multi-master arbitration
- Up 400Kbps Data transfer rate
- Fully programmable slave address and a public address
- You can wake address match in sleep mode

TWI Bus Introduction

Two-wire Serial Interface TWI Well suited for typical microcontroller applications. TWI Protocol allows a system designer using only two bidirectional transmission line can be 128 Different devices interconnected together. These two lines are clock SCL And data SDA . Only external hardware connected to the two lines of each pull-up resistors. All devices connected to the bus has its own address. TWI Agreement to solve the problem of bus arbitration.

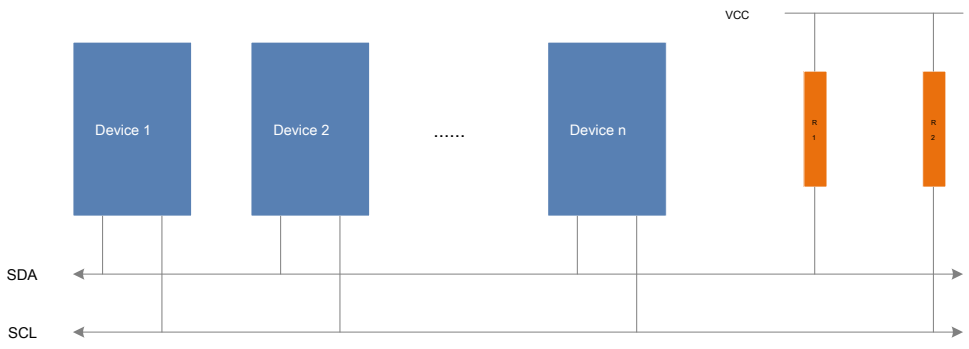
TWI the term

The following defined terms appear frequently in this section.

the term	description
Host computer	Starting and stopping the transmission equipment. Host also responsible for generating SCL clock.
Slave	Addressed by a master device
Transmitter	Device placing data on the bus
receiver	Receiving data from devices on the bus

Electrical connections

As shown below, TWI Two-wire interface through pull-up resistors connected to the positive supply. all TWI The bus driver compliant devices are open-drain or open-collector line and thus achieve the function of the interface operation. when TWI Output devices "0" Time, TWI It generates a low level bus. When all TWI When the tri-state output device, allows pull-up resistor bus voltage high. To ensure that all bus operations, all with TWI Devices connected to the bus must be powered on.



TWI The bus interconnect of FIG.