TCCR3B-TC3 Control register B

TCCR3B - TC3 Control register B								
address: 0x91				Defaults: 0x00				
Bit	7	6	5	4	3	2	1	0
	ICNC3	ICES3	-	WGM33	WGM32	CS32	CS31	CS30
R / W	R / W	R / W	R / W	-	R / W	R / W	R / W	R / W

Bit	Name description	
7	ICNC3	Input Capture noise suppressor enable control bit. When set ICNC3 Bit "1" When the enable input capture noise suppressor, when external pin ICP3 The input is filtered continuously 4 Sampling values of the input signal is valid when equal, the function input capture is delayed 4 Clock cycles. When set ICNC3 Bit "0" When prohibit input capture noise suppressor, this time external pin ICP3 Direct and effective input.
6	ICES3	Input Capture Edge Select control bits. When set ICES3 Bit "1" When the rising edge of selection level input capture trigger; provided when ICES3 Bit "0" When selecting the level of the falling edge of the input capture trigger. When a capture is triggered, the counter value is copied into ICR3 Register, while the set input capture flag ICF3 . If the interrupt is enabled, the input capture interrupt.
5	-	Reservations.
4	WGM33	Waveform generation mode control high. WGM33 with WGM32, WGM31, WGM30 Together form waveform generation mode control WGM3 [3: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
3	WGM32	Second uppermost waveform generation mode control. WGM32 with WGM33, WGM31, WGM30 Together form waveform generation mode control WGM3 [3: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
2	CS32 Clock control high.	For selecting a timing counter 3 The clock source.
1	CS31 Clock selection control bits.	For selecting a timing counter 3 The clock source.
0	CS30 Clock control low.	For selecting a timing counter 3 The clock source.

CS3 [2: 0]	description
0	No clock source, stops counting
1	clk $_{sys}$
2	clk $_{sys}$ / 8 From prescaler
3	clk $_{sys}$ / 64 From prescaler
4	clk $_{sys}$ / 256 From prescaler
5	clk $_{sys}$ / 1024 From prescaler
6	External Clock T3 Pin, falling edge
7	External Clock T3 Pin on the rising edge