2	DORD	Data transfer select bit sequence.	
		DORD	Order data
		0	MSB-first transfer
		1	LSB first transmission
1	UCPHA	Clock phase selection. UCPHA Select data sampling occurs at the start edge or the end edge.	
		UCPHA	Sampling time
		0	Starting along
		1	Trailing Edge
0	UCPOL	Clock polarity selection. UCPOL And changing the selection data sampled on the rising edge or falling edge.	
		UCPOL	Change the transmission of data / Sampling the received data
		0	XCK The rising edge / XCK Of falling
		1	XCK Of falling / XCK The rising edge

UBRRL - USPI Baud Rate Register Low Byte

UBRRL - USPI Baud Rate Register Low Byte								
address: 0xC4				Defaults: 0x00				
Bit	7	6	5	4	3	2	1	0
Name	UBRR7	UBRR6	UBRR5	UBRR4	UBRR3	UBRR2	UBRR1	UBRR0
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name description
7: 0 UBRR [7: 0]	USPI Low byte portion of register baud rate. USPI Baud rate register comprising UBRRL with UBRRH Two parts, joined together to set the baud rate.

UBRRH - USPI Baud Rate Register High Byte

UBRRH - USPI Baud Rate Register High Byte								
address: 0xC5				Defaults: 0x00				
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	UBRR11	UBRR10	UBRR9	UBRR8
	R / W	-	-	-	-	R / W	R / W	R / W	R / W

Bit		Name description
7: 4	-	USPI Under Reserved.
3: 0 UBRR [11: 8]		USPI High byte portion of register baud rate. USPI Baud rate register comprising UBRRL with UBRRH Two parts, joined together to set the baud rate. UBRR = {UBRR [11: 8], UBRRL}