Register Definition

C0SR - AC0 Control and status registers

COSR - ACO Control and status registers									
address: 0x50					Defaults: 0x80				
Bit	7	6	5	4	3	2	1	0	
Name	COD	C0BG	C0O	C0I	C0IE	COIC	C0IS1	C0IS0	
R/WR	/ W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Bit	Name descrip	otion							
7	COD	Analog Comparator Disable bit. When set C0D Bit "1" When the analog comparator is turned off. When set C0D Bit "0" When the analog comparator is							
		turned on.							
	COBG	Analog comparator 0 Positive input source selection. C0BG versus C0XR Register C0PS0 Jointly set AC0 The positive terminal of the input source, { C0BG, C0PS0} = 00 = AC0P As the positive input terminal							
6		01 = ACXP As the positive input terminal 10 = internal DAC As the positive input terminal of the output 11 = shut down AC0 The positive terminal of the input source							
5	C0O	Analog output status bit comparator. The output of the analog comparator is connected directly to the sync after C00 Bit. Software can read C00 Bit value to obtain an output value of the analog comparator.							
4	COI	Analog comparator interrupt flag. When the analog comparator output event triggered by COIS Bits defined interrupt mode, COI Bit is set. When the interrupt enable bit COIE for "1" And the Global Interrupt is set when an interrupt is generated. When performing analog comparator interrupt service routine, COI Will be automatically cleared or COI Write bit "1" Also clears the bit.							
3	COIE	Analog Comparator interrupt enable bit. When set C0IE Bit 1 And enable global interrupt, AC0 The interrupt is enabled. When set C0IE Bit 0 , AC0 Interrupts are disabled.							
2	COIC Analog	og comparator input Capture Enable COIC = 1, Timing counter 1 The input capture source output from the analog comparator. COIC = 0, Timing counter 1 Capture source from an external input pin ICP1.							
1	C0IS1 Analog	g Comparator Interrupt Mode Control high.							
0	C0IS0 Analog	C0IS0 Analog Comparator Interrupt Mode Control low. C0IS0 with C0IS1 Together form C0IS [1: 0],							
	Used to control analog comparator interrupt trigger.								
		COIS	[1: 0]	Interrupt Mo	ode				
		0	0	ACO The	e transition e	dge			
		0	11	Reservation	is.				
		1	0	ACO The	falling edge				
		1	1	ACO The ri	sing edge of the t	rigger			