	Name	Dist	inal list of	Ditto	Bit4	1016/3	DH9	Bit1	BitO				
Addr 0xF6	GUID3	GUID Byte 3							Ditt				
0xF5	GUID2					Byte 2							
0xF4	GUID1					Byte 1							
0xF3	GUID0					Byte 0							
0xF2	PMCR	PMCE	CLKFS	CLKSS	WCLKS	OSCKEN	OSCMEN	RCKEN	RCMEN				
0xF0	PMX2	WCE	STOSC1	STOSC0	(*)		XIEN	E6EN	C6EN				
0xEE	PMX0	PMXCE	C1BF4	C1AF5	C0BF3	C0AC0	SSB1	TXD6	RXD5				
0xED	PMX1		-	-	12	-	C3AC	C2BF7	C2AF6				
0xEC	TCKCSR		F2XEN	TC2XF1	TC2XF0	- 17	AFCKS	TC2XS1	TC2XS0				
0xE2	PSSR	PSS1	PSS3		-			PSR3	PSR1				
0xE1	OCPUE	PUE7	PUE6	PUE5	PUE4	PUE3	PUE2	PUE1	PUE0				
0xE0	HDR		-	HDR5	HDR4	HDR3	HDR2	HDR1	HDR0				
0xDE	DAPTE	DAPTE			-	-	-		-				
0xDD	DAPTR	DAPTP	C41	C 4 0		Trimming	DNICO	0001	DDCO				
0xDC	DAPCR	DAPEN	GA1	GA0	DNS2	DNS1	DNS0	DPS1	DPS0				
0xCF 0xCE	LDOCR VCAL2	WCE	Cal	ibration va	alua for 2	PDEN 048V into	VSEL2	VSEL1	VSEL0				
0xCD	VCAL2			ibration va									
0xCC	VCAL3			ibration va									
0xC8	VCAL			ernal Volta									
0xAF	DPS2R		- 1110	-	-	DPS2E	LPRCE	TOS1	TOS0				
0xAE	IOCWK	IOCD7	IOCD6	IOCD5	IOCD4	IOCD3	IOCD2	IOCD1	IOCDO				
0xAD	ADCSRD	BGEN	REFS2	IVSEL1	IVSEL0	-	VDS2	VDS1	VDS0				
0xAC	ADMSC	AMOF		-	-	AMFC3	AMFC2	AMFC1	AMFCC				
0xAB	ADT1H		ADC	Auto-moi	nitor Over								
0xAA	ADT1L			Auto-mo									
0xA9	PORTE		Por	t Output E	(for com	patible wil	h LGT8FX	8D)					
0xA8	DDRE			Direction									
0xA7	PINE			rt Input E									
0xA6	ADT0H			Auto-mon			- A district the second state of the second						
0xA5	ADT0L		ADC	Auto-mor				byte					
0xA4	OFR1					offset trim		00					
0xA3	OFR0			ADC		offset trim	ming						
0xA1	DALR				DAC dat	a register							
0xA0	DACON	15		-		DACEN	DAOE	DAVS1	DAVSO				
0x9F	OCR3CH			e output r									
0x9E	OCR3CL			re output i									
0x9D	DTR3H			Dead-ban									
0x9C	DTR3L		_		the section is the second of the court of the court	low byte							
0x9B	OCR3BH												
0x9A	OCR3BL				register io	Compare output register high byte of Timer3 B channel Compare output register low byte of Timer3 B channel							
0x99 0x98	OCR3AH OCR3AL		Compare output register high byte of Timer3 A channel										
						gh byte of	Timer3 A	channel					
			Compa	re output i	register lo	gh byte of w byte of	Timer3 A Timer3 A	channel channel					
0x97	ICR3H		Compa	re output i nput captu	register lo ire registe	gh byte of w byte of r high byte	Timer3 A Timer3 A e of Timer	channel channel 3					
0x97 0x96	ICR3H ICR3L		Compa	re output i nput captu nput captu	register lo ire registe ire registe	gh byte of w byte of ir high byte er low byte	Timer3 A Timer3 A e of Timer e of Timer	channel channel 3					
0x97 0x96 0x95	ICR3H ICR3L TCNT3H		Compa	re output i nput captu nput captu Counter	register lo ire registe ire registe register h	gh byte of w byte of er high byte er low byte igh byte o	Timer3 A Timer3 A e of Timer of Timer f Timer3	channel channel 3					
0x97 0x96 0x95 0x94	ICR3H ICR3L TCNT3H TCNT3L		Compa	re output r nput captu nput captu Counter Counter	register lo ire registe ure registe register h register l	gh byte of w byte of r high byte er low byte igh byte o ow byte o	Timer3 A Timer3 A e of Timer of Timer f Timer3 f Timer3	channel channel 3					
0x97 0x96 0x95 0x94 0x93	ICR3H ICR3L TCNT3H		Compa	re output r nput captu nput captu Counter Counter Con	register lo ire registe ire registe register l register l trol regist	gh byte of w byte of ir high byte or low byte igh byte o ow byte o er D of Tir	Timer3 A Timer3 A e of Timer of Timer3 f Timer3 f Timer3 mer3	channel channel 3					
0x97 0x96 0x95 0x94	ICR3H ICR3L TCNT3H TCNT3L TCCR3D		Compa	re output r nput captu nput captu Counter Counter Con	register lo ire registe ire register register l register l trol regist trol regist	gh byte of w byte of r high byte er low byte igh byte o ow byte o	Timer3 A Timer3 A e of Timer e of Timer3 f Timer3 mer3 ner3	channel channel 3					
0x97 0x96 0x95 0x94 0x93 0x92	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C		Compa	re output r nput captu nput captu Counter Counter Con Con	register lo ire registe ire register h register h register l trol regist trol regist	gh byte of w byte of r high byte or low byte ligh byte o ow byte o er D of Tir er C of Tir	Timer3 A Timer3 A e of Timer of Timer f Timer3 f Timer3 mer3 mer3 ner3	channel channel 3					
0x97 0x96 0x95 0x94 0x93 0x92 0x91	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B		Compa li	re output r nput captu nput captu Counter Counter Con Con	register lo ure registe ure register h register l trol regist trol regist trol regist trol regist	gh byte of w byte of er high byte er low byte eigh byte o ow byte o er D of Tin er C of Tin er B of Tin	Timer3 A Timer3 A e of Timer of Timer3 f Timer3 f Timer3 ner3 ner3 ner3 ner3	channel channel 3					
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A		Compa li	re output r nput captu nput captu Counter Counter Con Con Con Con Dead-ban	register lo ure registe ure register h register l trol regist trol regist trol regist trol regist d register	gh byte of w byte of er high byte er low byte eigh byte o ow byte o er D of Tin er C of Tin er B of Tin	Timer3 A Timer3 A e of Timer of Timer3 f Timer3 mer3 mer3 mer3 mer3 ner3 ner3 ner3 ner3 ner3	channel channel 3 3					
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x83	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D	DSX17	Compa li	re output r nput captu nput captu Counter Counter Con Con Con Con Dead-ban Dead-ban	register lo are register register hand register land trol registator land trol registator land trol registator land d register land DAX14	gh byte of w byte of er high byte er low byte igh byte o ow byte o er D of Tin er C of Tin er B of Tin er A of Tin high byte	Timer3 A Timer3 A e of Timer of Timer3 f Timer3 ner3 ner3 ner3 of Timer1 of Timer1	channel channel 3 3					
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x83	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC	OFEN	Compai	re output r nput captu nput captu Counter Counter Con Con Con Con Dead-ban Dead-ban	register lo ure registe ure register h register l trol regist trol regist trol regist trol regist d register d register DAX14 AMEN	gh byte of w byte of er high byte er low byte igh byte o ow byte o er D of Tin er C of Tin er B of Tin er A of Tin high byte	Timer3 A Timer3 A e of Timer of Timer3 f Timer3 mer3 mer3 mer3 mer3 ner3 ner3 ner3 ner3 ner3	channel channel 3 3 3	ADTM				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x83 0x7D	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2		Compai II	re output r nput captu nput captu Counter Counter Con Con Con Con Dead-ban DSX15 SPN	register lo are register register h register l trol regist trol regist trol regist trol register d register d register DAX14 AMEN	gh byte of w byte of ir high byte er low byte igh byte o ow byte o er D of Tir er C of Tir er A of Tir high byte low byte	Timer3 A Timer3 A e of Timer e of Timer f Timer3 f Timer3 ner3 ner3 ner3 of Timer1 - SPD -	channel channel 3 3					
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x83 0x7D 0x76 0x75	ICR3H ICR3L TCNT3H TCNT3H TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE	OFEN	Compai	re output r nput captu nput captu Counter Counter Con Con Con Con Dead-ban DSX15 SPN	register lo are register register h register l trol regist trol regist trol regist trol register d register d register DAX14 AMEN	gh byte of w byte of w byte of or high byte of ow byte of ow byte of or D of Tirer C of Timer A of Tinhigh byte of low byte or byte of the control of the co	Timer3 A Timer3 A e of Timer e of Timer f Timer3 f Timer3 ner3 ner3 ner3 of Timer1 - SPD -	channel channel 3 3 3	ADTM				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x83 0x7D 0x76 0x75 0x74	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4	OFEN	Compai	re output r nput captu nput captu Counter Counter Con Con Con Con Dead-ban DSX15 SPN	register lo re registe register h register h register l register l trol regist trol regist trol regist trol regist d register d register DAX14 AMEN - rupt Vector	gh byte of w byte of w byte of ir high byte or low byte igh byte o ow byte o er D of Tir er B of Tir er B of Tir high byte - or Base Ad	Timer3 A Timer3 A e of Timer e of Timer f Timer3 f Timer3 ner3 ner3 ner3 of Timer1 - SPD -	channel channel 3 3 3	ADTM				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8C 0x7D 0x76 0x75 0x74	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3	OFEN	Compai	re output r nput captu nput captu Counter Counter Com Con Con Dead-ban DEX15 SPN	register lo re registe register h register h register l register l trol regist trol regist trol regist trol regist trol regist d register d register DAX14 AMEN - rupt Vector	gh byte of w byte of re high byte re high byte er low byte igh byte o ow byte o er D of Tir er C of Tir er G of Tir high byte low byte or Base Ad [39:32]	Timer3 A Timer3 A e of Timer e of Timer f Timer3 f Timer3 ner3 ner3 ner3 ner3 ner3 of Timer1 - SPD - dress	channel channel 3 3 3	ADTM -				
0x97 0x96 0x95 0x94 0x93 0x90 0x80 0x80 0x80 0x70 0x75 0x74 0x73	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3	OFEN	Compai	re output r nput captu nput captu Counter Counter Con Con Con Con Dead-ban DSX15 SPN	register lo re registe re register register h register h register l trol regist trol regist trol regist trol regist trol regist trol regist d register d register DAX14 AMEN - rupt Vector	gh byte of w byte of w byte of re high byte er low byte o ow byte o oer D of Tir er C of Tir er B of Tir er A of Tir high byte low byte or Base Ad [39:32] OCIESC	Timer3 A Timer3 A e of Timer e of Timer f Timer3 f Timer3 ner3 ner3 ner3 of Timer1 - SPD -	channel channel 3 3 3	ADTM -				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x80 0x80 0x80 0x70 0x75 0x75 0x74 0x73 0x71 0x67	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 RCKCAL	OFEN	Compai	re output raput captu nput captu nput captu Counter Counter Con Con Con Con Dead-ban Dead-ban DSX15 SPN Inten	register lo re registe re register le register le register le register le trol registe trol registe trol registe trol registe trol registe trol registe de register de register DAX14 AMEN - rupt Vecto PCINT - RC32K C	gh byte of w byte of w byte of re high byte er low byte of ow byte o ow byte o oer D of Tir er C of Tir er B of Tir er A of Tir high byte output out	Timer3 A Timer3 A of Timer of Timer of Timer3 f Timer3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress	channel channel 3 3 3 DSX11 DIFS - OCIE3A	ADTM -				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x7D 0x76 0x75 0x74 0x73 0x71 0x67 0x67	ICR3H ICR3L TCNT3H TCNT3H TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 RCKCAL PRR1	OFEN -	DSX16 PB5D	re output r nput captu nput captu Counter Counter Com Con Con Dead-ban DEX15 SPN	register lo re registe re register register h register h register l trol regist trol regist trol regist trol regist trol regist trol regist d register d register DAX14 AMEN - rupt Vector	gh byte of w byte of w byte of r high byte r low byte igh byte o ow byte o oer D of Tir er C of Tir er B of Tir er A of Tir high byte low byte or Base Ad (39:32] OCIE3C allibration PRTIM3	Timer3 A Timer3 A e of Timer e of Timer f Timer3 f Timer3 ner3 ner3 ner3 ner3 ner3 of Timer1 - SPD - dress	channel channel 3 3 3 3 DSX11 DIFS - OCIE3A PRPCI	TOIE3				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x7D 0x76 0x75 0x74 0x73 0x71 0x67 0x65 0x62	ICR3H ICR3L TCNT3H TCNT3H TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 TIMSK3 RCKCAL PRR1 VDTCR	OFEN	Compai	re output re put captu nput captu nput captu nput captu Counter Counter Com Com Com Com Dead-ban Dead-ban DSX15 SP Inten	register lo re registe register lo re register lo register lo trol regist trol regist trol regist trol regist trol regist trol regist d register d register DAX14 AMEN - rupt Vecto PCINT - RC32K C	gh byte of w byte of w byte of r high byte r low byte igh byte o ow byte o oer D of Tir er C of Tir er A of Tir high byte low byte OCIE3C alibration PRTIM3 VDTS	Timer3 A Timer3 A e of Timer e of Timer f Timer3 f Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress	channel channel 3 3 3 DSX11 DIFS - OCIE3A	TOIE3				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x70 0x76 0x75 0x74 0x73 0x71 0x65 0x62 0x55	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3	OFEN -	DSX16 PB5D	re output re put captu nput captu nput captu nput captu Counter Counter Com Com Com Com Dead-ban Dead-ban DSX15 SP Inten	register lo re registe register h register h register l trol regist trol regist trol regist trol regist trol regist d register d register AMEN - rupt Vecto PCINT - RC32K C - CTL Data	gh byte of w byte of w byte of r high byte r low byte of ow byte of ow byte of or	Timer3 A Timer3 A e of Timer e of Timer f Timer3 f Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress	channel channel 3 3 3 3 DSX11 DIFS - OCIE3A PRPCI	TOIE3				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x76 0x75 0x74 0x73 0x71 0x65 0x65 0x5C	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR	OFEN -	DSX16 PB5D	re output re put captu nput captu nput captu captu nput captu Counter Counter Com Con Com Dead-ban DEAL5 SPN - Intern ICIE3	register lo re registe re register lo re register lo register lo trol regist trol regist trol regist trol regist d register d register d register AMEN - rupt Vector PCINT - RC32K C - CTL Data AC1 trim	gh byte of w byte of w byte of r high byte r high byte r low byte igh byte o ow byte o er D of Tir er C of Tir er C of Tir high byte - or Base Ad (39:32] OCIE3C allibration PRTIM3 VDTS register by ming data	Timer3 A Timer3 A e of Timer e of Timer f Timer3 f Timer3 f Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL	channel channel 3 3 3 3 DSX11 DIFS - OCIE3A PRPCI	TOIE3				
0x97 0x96 0x95 0x94 0x93 0x92 0x80 0x80 0x80 0x76 0x75 0x74 0x73 0x71 0x67 0x67 0x62 0x5C	ICR3H ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR EZPD3 C1TR EZPD1	OFEN -	DSX16 PB5D	re output in put captu nput captu nput captu nput captu Counter Counter Con	register lo re registe re register register h register h register l trol registe trol regist trol regist trol regist trol regist trol regist rol regist ro	gh byte of w byte of w byte of re high byte er low byte o ow byte o oer D of Tir er C of Tir er B of Tir er A of Tir high byte out	Timer3 A Timer3 A e of Timer of Timer of Timer3 f Timer3 f Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 SPD - dress OCIE3B PREFL yte 3	channel channel 3 3 3 3 DSX11 DIFS - OCIE3A PRPCI	DSX10 ADTM - TOIE3				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x80 0x70 0x76 0x75 0x74 0x73 0x71 0x67 0x65 0x5B 0x5B 0x5B	ICR3H ICR3L ICR3L TCNT3H TCNT3H TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK4 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH	OFEN -	DSX16 PB5D	re output re put captu nput captu nput captu nput captu nput captu Counter Counter Con	register lo re registe register lo registe	gh byte of w byte of w byte of re high byte er low byte oigh byte o ow byte o er D of Tir er C of Tir er B of Tir er A of Tir high byte low byte or Base Ad [39:32] OCIE3C alibration PRTIM3 VDTS register by ming data register by ess port of	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer3 f Timer3 ner3 ner3 ner3 ner3 ner3 ner3 ner3 n	channel channel 3 3 3 3 DSX11 DIFS - OCIE3A PRPCI	TOIE3				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x80 0x80 0x70 0x76 0x75 0x74 0x73 0x71 0x67 0x65 0x62 0x5C 0x5B 0x5A 0x59 0x58	ICR3H ICR3L ICR3L TCNT3H TCNT3H TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL	- WCE	DSX16 - PB5D	re output re put captu nput captu nput captu nput captu nput captu Counter Counter Con	register lo re registe register lo re register lo register lo register lo register lo register trol regist trol regist trol regist trol regist rol register d register DAX14 AMEN - ROJANA - RCJANA - CTL Data AC1 trim ACTL Data (1:16] accel 15:0] accel	gh byte of w byte of w byte of r high byte er low byte igh byte o ow byte o er D of Tir er C of Tir er B of Tir er A of Tir high byte low byte or Base Ad (39:32] OCIE3C alibration PRTIM3 VDTS register by ming data register by ess port of	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer3 f Timer3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL rte 3 yte1 fupSC uDSC	channel channel 3 3 3 3 3 5 5 5 5 5 5 5 5 5 5 5 5 5 5	TOIE3				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x80 0x70 0x76 0x75 0x74 0x73 0x71 0x67 0x65 0x5B 0x5B 0x5B	ICR3H ICR3L ICR3L TCNT3H TCNT3H TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK4 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH	OFEN -	DSX16 PB5D	re output riput capturput	register lo re registe register le registe	gh byte of w byte of w byte of r high byte r low byte igh byte o ow byte o oer D of Tir er C of Tir er G of Tir er A of Tir high byte low byte or Base Ad (39:32] OCIE3C alibration PRTIM3 VDTS register by ming data register by ess port of CP1	Timer3 A Timer3 A e of Timer e of Timer of Timer3 f Timer3 f Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL Ate 3 yte1 f UDSC UDSC CP0	channel channel 3 3 3 S S S S S S S S S S S S S S S S	TOIE3				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x7D 0x76 0x75 0x74 0x73 0x71 0x67 0x65 0x62 0x5C 0x5B 0x5A 0x58 0x58 0x58	ICR3H ICR3L ICR3L TCNT3H TCNT3H TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 TIMSK3 TIMSK3 TCK3A TIMSK3 TCR1D TCR	- WCE	DSX16 - PB5D	re output riput capturput	register lo re registe register le registe	gh byte of w byte of w byte of r high byte er low byte igh byte o ow byte o er D of Tir er C of Tir er B of Tir er A of Tir high byte low byte or Base Ad (39:32] OCIE3C alibration PRTIM3 VDTS register by ming data register by ess port of	Timer3 A Timer3 A e of Timer e of Timer of Timer3 f Timer3 f Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL Ate 3 yte1 f UDSC UDSC CP0	channel channel 3 3 3 3 3 5 5 5 5 5 5 5 5 5 5 5 5 5 5	TOIE3				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x75 0x74 0x75 0x75 0x65 0x65 0x62 0x5C 0x5B 0x5A 0x58 0x58 0x58	ICR3H ICR3L ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR COTR	- WCE	DSX16 - PB5D - SWR	re output re put captu nput captu nput captu nput captu nput captu Counter Counter Com Con Con Con Con Con Dead-ban DSX15 SPN International PRWDT - E2PU E2PU DSA[3 DSA[3 ERN A COHYSE	register lo re registe register le registe	gh byte of w byte of w byte of r high byte r high byte r high byte of or Base Ad (39:32] OCIE3C allibration PRTIM VDTS register by ming data register by ess port of CP1 ing register	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer of Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL tte 3 yte1 uDSC uDSC CP0 or COFEN	channel channel 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x76 0x75 0x74 0x73 0x71 0x65 0x65 0x5C 0x5B 0x5A 0x5B 0x5A	ICR3H ICR3L ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR COTR	- WCE	DSX16 - PB5D - SWR	re output re put captu nput captu nput captu nput captu nput captu Counter Counter Com Con Con Con Con Con Dead-ban DSX15 SPN International PRWDT - E2PU E2PU DSA[3 DSA[3 ERN A COHYSE	register lo re registe register le registe	gh byte of w byte of w byte of r high byte er low byte oo ow byte o er D of Tir er C of Tir er C of Tir high byte or Base Ad (39:32] OCIE3C allibration PRTIM3 VDTS register by ming data register by ess port of CP1 ing registe COWKE	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer of Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL tte 3 yte1 uDSC uDSC CP0 or COFEN	channel channel 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 VDTEN ECS0 COFS0				
0x97 0x96 0x95 0x94 0x93 0x92 0x80 0x80 0x70 0x76 0x75 0x74 0x73 0x71 0x65 0x62 0x5C 0x5B 0x5A 0x59 0x58 0x50 0x54 0x54 0x54 0x54 0x54 0x55 0x54 0x55 0x54 0x55 0x54 0x55 0x55 0x56 0x56 0x56 0x56 0x56 0x56 0x56 0x55 0x56	ICR3H ICR3L ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR COTR COXR	- WCE	DSX16 PB5D SWR	re output riput captur put	register loure register register la register la register la troi registe troi registe troi registe troi register la register l	gh byte of w byte of w byte of r high byte er low byte of er low byte oo ow byte of er D of Tir er C of Tir er C of Tir er A of Tir high byte or Base Ad [39:32] OCIE3C alibration PRTIM3 VDTS register by ming data register by ess port of CP1 ing registr COWKE	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer of Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL tte 3 yte1 uDSC uDSC CP0 or COFEN	channel channel 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 TOIE3 VDTEN ECS0 COFS0				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x80 0x80 0x76 0x75 0x74 0x73 0x71 0x67 0x65 0x5B	ICR3H ICR3L ICR3L TCNT3H TCNT3H TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK4 PCMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR COTR COXR DTR0 TCCR0C	OFEN - WCE WEN - DSX07	DSX16 PB5D SWR EEN COOE DSX06	re output riput captur put	register loure register register loure register la register la trol registe trol registe trol register la register	gh byte of w byte of w byte of r high byte r low byte igh byte o ow byte o oer D of Tir er C of Tir er C of Tir er A of Tir high byte low byte or Base Ad (39:32) OCIE3C alibration PRTIM3 VDTS register by ming data register by ess port of CP1 ing registe COWKE ning control	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL vte 3 yte1 fupSC uDSC CP0 or COFEN or cofeen or cofeen or register - C1FEN	channel channel 33 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 TOIE3 VDTEN ECS0 C0FS0 D5X00 C1FS0				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x80 0x80 0x70 0x76 0x75 0x74 0x73 0x71 0x67 0x65 0x62 0x5C 0x5B 0x5A 0x59 0x58 0x54	ICR3H ICR3L ICR3L TCNT3H TCNT3H TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD3 C1TR E2PD1 DSAH DSAL ECCR COTR COTR COTR COTR TCCROC C1XR	OFEN - WCE WEN - DSX07	DSX16 - PB5D - SWR - COOE DSX06 C1OE	re output raptu captu raptu ra	register lo re registe register lo re register le regi	gh byte of w byte of w byte of r high byte r low byte igh byte o ow byte o oer D of Tir er C of Tir er C of Tir er A of Tir high byte low byte or Base Ad (39:32) OCIE3C alibration PRTIM3 VDTS register by ming data register by ess port of CP1 ing registe COWKE ning control	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL vte 3 yte1 fupSC uDSC CP0 or COFEN or cofeen or cofeen or register - C1FEN	channel channel 33 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 - VDTEN ECS0 C0FS0 D5X000 C1FS0 WRPTR				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x83 0x7D 0x76 0x75 0x74 0x73 0x71 0x65 0x62 0x5C 0x5B 0x5A 0x59 0x5A 0x59 0x54 0x59 0x54 0x52 0x51 0x4F 0x49 0x3A 0x34	ICR3H ICR3L ICR3L TCNT3H TCNT3H TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR COTR COXR DTR0 TCCR0C C1XR SPFR	OFEN - WCE WEN - DSX07 - RDFULL	DSX16 - PB5D - SWR - COOE DSX06 C1OE RDEMPT	re output in put captu nput nput nput nput nput nput nput n	register loure register regist	gh byte of w byte of w byte of w byte of r high byte er low byte igh byte o ow byte o er D of Tir er C of Tir er C of Tir high byte or Base Ad [39:32] OCIE3C allibration PRTIM3 VDTS register by ming data register by ess port of CP1 ing registr COWKE hing control wRFULL t of Group	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer of Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL tte 3 yte1 uDSC uDSC CP0 or COFEN ol register - C1FEN WREMPT OCF3B F	channel channel 33 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 - VDTEN ECS0 C0FS0 D5X000 C1FS0 WRPTR				
0x97 0x96 0x95 0x94 0x93 0x90 0x80 0x80 0x70 0x76 0x75 0x71 0x67 0x65 0x52 0x58 0x58 0x51 0x58 0x58 0x58	ICR3H ICR3L ICR3L ICR3L TCNT3H TCNT3H TCNT3CR3C TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK4 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR C0TR COXR DTR0 TCCR0C C1XR SPFR TIFR3 PORTF DDRF	OFEN - WCE WEN - DSX07 - RDFULL	DSX16 - PB5D - SWR - COOE DSX06 C1OE RDEMPT	re output in put captu nput nput nput nput nput nput nput n	register loure register regist	gh byte of w byte of w byte of r high byte er low byte of er low byte ow byte of er D of Tir er C of Tir er B of Tir er A of Tir high byte low byte or Base Ad (39:32) OCIE3C allibration PRTIM3 VDTS register by ming data register by ess port of COWKE hing control COWKE writh tof Group on of Group	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer3 f	channel channel 33 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 - VDTEN ECS0 C0FS0 D5X00 C1FS0 WRPTR				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x76 0x75 0x74 0x73 0x71 0x65 0x65 0x5C 0x5B 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5S 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5A 0x5S 0x5S 0x5A 0x5S 0x5S 0x5A 0x5A	ICR3H ICR3L ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR C0TR C0XR DTR0 TCCR0C C1XR SPFR TIFR3 PORTF	OFEN - WCE WEN - DSX07 - RDFULL	DSX16 - PB5D - SWR - COOE DSX06 C1OE RDEMPT	re output re put captu counter Counter Counter Con	register loure register regist	gh byte of w byte of w byte of r high byte er low byte igh byte o ow byte o er D of Tir er C of Tir er C of Tir er A of Tir high byte low byte or Base Ad (39:32) OCIE3C allibration PRTIM3 VDTS register by ming data register by ess port of CP1 ing register by ess port of CP1 COWKE ing contro C1WKE WRFULL t of Group on of Group of Group	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer3 f Timer3 f Timer3 f Timer3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL Vte 3 Vte1 f UDSC CP0 or COFEN of register - C1FEN WREMPT OCF38 F p F	channel channel 33 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 - VDTEN ECS0 C0FS0 D5X00 C1FS0 WRPTR				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x76 0x75 0x74 0x75 0x67 0x65 0x62 0x5B 0x5C 0x5B 0x5C 0x5B 0x5A 0x59 0x58 0x56 0x52 0x51 0x44 0x33 0x31	ICR3H ICR3L ICR3L ICR3L TCNT3H TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD3 C1TR E2PD1 DSAH DSAL ECCR COTR COXR DTR0 TCCROC C1XR SPFR TIFR3 PORTF DDRF PINF DSDY	OFEN - WCE WEN - DSX07 - RDFULL	DSX16 - PB5D - SWR - COOE DSX06 C1OE RDEMPT	re output raptu captu raptu ra	register lo re registe register lo re register le regi	gh byte of w byte of w byte of r high byte er low byte igh byte o ow byte o oer D of Tir er C of Tir er C of Tir er A of Tir high byte low byte or or Base Ad (39:32) OCIE3C alibration PRTIM3 VDTS register by ming data register by ess port of CP1 ing register COWKE ming control	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer3 f Timer1 of Timer1 of Timer1 of Timer1 clubsc crack c	channel channel 33 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 - VDTEN ECS0 C0FS0 D5X00 C1FS0 WRPTR				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x75 0x74 0x75 0x67 0x65 0x62 0x5C 0x5B 0x5A 0x5B 0x5B 0x5A 0x5B 0x5B 0x5B 0x5B 0x5B 0x5B 0x5B 0x5B	ICR3H ICR3L ICR3L ICR3L TCNT3H TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 TRKSCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR COTR COXR DTR0 TCCROC C1XR SPFR TIFR3 PORTF DDRF PINF DSDY DSDX	VEN - DSX07 - RDFULL	DSX16 - PB5D - SWR - COOE DSX06 C1OE RDEMPT	re output in put captur put	register lo re registe register lo re register le regi	gh byte of w byte of w byte of r high byte er low byte igh byte o ow byte o oer D of Tir er C of Tir er C of Tir er B of Tir high byte low byte or or Base Ad (39:32] OCIE3C alibration PRTIM3 VDTS register by ming data register by ess port of CP1 ing registr COWKE ning control crum crum crum crum crum crum crum crum	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL vte 3 vte 1 uDSC uDSC uDSC uDSC uDSC uDSC uDSC uDSC	channel channel 33 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 - VDTEN ECS0 C0FS0 D5X00 C1FS0 WRPTR TOV3				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x75 0x74 0x75 0x75 0x65 0x65 0x65 0x5C 0x5B 0x5A 0x59 0x58 0x5A 0x59 0x58 0x54 0x52 0x51 0x4F 0x49 0x38 0x34 0x33 0x32 0x31 0x30 0x2F	ICR3H ICR3L ICR3L ICR3L TCNT3H TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR C0TR C0XR DTR0 TCCR0C C1XR SPFR TIFR3 PORTF DDRF PINF DSDY DSDX C1SR	OFEN - WCE WEN - DSX07 - RDFULL	DSX16 - PB5D - SWR - COOE DSX06 C1OE RDEMPT	re output in put captu nput nput nput nput nput nput nput n	register lo re registe register register le register l	gh byte of w byte of w byte of r high byte er low byte igh byte oo ow byte of er D of Tir er C of Tir er C of Tir high byte low byte or Base Ad (39:32] OCIE3C allibration PRTIM3 VDTS register by ming data register by ming contro CP1 ing registe COWKE ing contro control t of Group on of Group on of Group on of Group on of Group of Group t of Ut t port of ut t of LIE	Timer3 A Timer3 A Timer3 A e of Timer of Timer of Timer3 f Timer3 f Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL Ate 3 yte1 uDSC uDSC CP0 er COFEN ol register - C1FEN WREMPT OCF3B F p F = SSC DSC C1IC	channel channel 33 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 - VDTEN ECS0 C0FS0 D5X000 C1FS0 WRPTR				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x83 0x7D 0x76 0x75 0x74 0x73 0x71 0x65 0x62 0x5C 0x5B 0x5A 0x59 0x5A 0x59 0x58 0x54 0x52 0x51 0x4F 0x49 0x3A 0x33 0x32 0x31 0x32 0x31 0x32	ICR3H ICR3L ICR3L ICR3L TCNT3H TCNT3L TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK3 TIMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR C0TR C0XR DTR0 TCCR0C C1XR SPFR TIFR3 PORTF DDRF PINF DSDY DSDX C1SR PORTE	VEN - DSX07 - RDFULL	DSX16 - PB5D - SWR - COOE DSX06 C1OE RDEMPT	re output in put captu nput captu nput captu nput captu nput captu nput captu nput captu Counter Counter Con Com	register loure register regist	gh byte of w byte of w byte of w byte of r high byte er low byte igh byte o ow byte o er D of Tir er C of Tir er C of Tir high byte or Base Ad (39:32] OCIE3C alibration PRTIM3 VDTS register by ming data register by ess port of CP1 ing registr toWKE WRFULL tof Group of Group of Group of Group of Group of Group port of ut colle tof Group colle tof G	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer of Timer3 ner3 ner3 ner3 ner3 of Timer1 of Timer1 - SPD - dress OCIE3B PREFL tte 3 vte1 uDSC uDSC CPO er COFEN ol register - CIFEN ol register - CIFEN ocra SPD ocra COFEN oc	channel channel 33 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 - VDTEN ECS0 C0FS0 D5X00 C1FS0 WRPTR TOV3				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x80 0x85 0x7D 0x76 0x75 0x74 0x73 0x67 0x65 0x52 0x58 0x58 0x58 0x58 0x58 0x58 0x58 0x58	ICR3H ICR3L ICR3L ICR3L ICR3L TCNT3H TCNT3H TCNT3C TCCR3D TCCR3C TCCR3B TCCR3A DTR1H DTR1L TCCR1D ADCSRC DIDR2 IVBASE PCMSK4 PCMSK4 PCMSK3 RCKCAL PRR1 VDTCR E2PD3 C1TR E2PD1 DSAH DSAL ECCR C0TR COTR COTR COTR TCCR0C C1XR SPFR TIFR3 PORTF DDRF PINF DSDY DSDX C1SR PORTE DDRE	VEN - DSX07 - RDFULL	DSX16 - PB5D - SWR - COOE DSX06 C1OE RDEMPT	re output in put captur put	register loss register loss register la register la register la trol register la trol register la trol register la	gh byte of w byte of w byte of w byte of er high byte of er high byte of er high byte of ow byte of ow byte of er D of Tirrer C of Tirrer B of Tirrer	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer3 f	channel channel 33 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 - VDTEN ECS0 C0FS0 D5X00 C1FS0 WRPTR TOV3				
0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x86 0x76 0x76 0x75 0x74 0x73 0x67 0x65 0x62 0x5C 0x5B 0x5A 0x59 0x58 0x56 0x52 0x51 0x4F 0x49 0x3A 0x39 0x38 0x34 0x30 0x2E 0x2D	ICR3H ICR3L ICR3L ICR3L ICR3L ICR3L ICR3H ICR3H ICR3H ICR3H ICCR3C ICCR3B ICCR3C ICCR3B ICCR3C ICR3B ICCR3C ICR3B ICCR3C ICR3C ICR3C ICR3C ICR3C ICR3C IVBASE PCMSK4 PCMSK	VEN - DSX07 - RDFULL	DSX16 - PB5D - SWR - COOE DSX06 C1OE RDEMPT	re output in put captu nput captu nput captu nput captu nput captu nput captu nput captu Counter Counter Con	register loar register loar register loar register la register la register la trol registe trol register la regist	gh byte of w byte of w byte of w byte of or high byte of or high byte of own byte of own byte of own byte of or Both of Timer B of T	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer3 f	channel channel 33 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 - VDTEN ECS0 C0FS0 D5X00 C1FS0 WRPTR TOV3				
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0x97 0x96 0x95 0x94 0x93 0x92 0x91 0x90 0x8D 0x8C 0x76 0x75 0x74 0x73 0x67 0x65 0x62 0x5C 0x5B 0x5A 0x59 0x5A 0x59 0x3A 0x30 0x34 0x33 0x32 0x31 0x30 0x2E 0x2C	ICR3H ICR3L ICR3L ICR3L ICR3L ICR3L ICR3H ICR3H ICR3H ICR3H ICCR3C ICCR3B ICCR3C ICCR3B ICCR3C ICR3B ICCR3C ICR3B ICCR3C ICR3C ICR3C ICR3C ICR3C ICR3C IVBASE PCMSK4 PCMSK	VEN - DSX07 - RDFULL	DSX16 - PB5D - SWR - COOE DSX06 C1OE RDEMPT	re output re put captu counter Counter Counter Con	register loar register registe	gh byte of w byte of w byte of w byte of or high byte of or high byte of own byte of own byte of own byte of or Both of Timer B of T	Timer3 A Timer3 A Timer3 A of Timer of Timer of Timer3 f	channel channel 33 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	TOIE3 - VDTEN ECS0 C0FS0 D5X000 C1FS0 WRPTR TOV3				

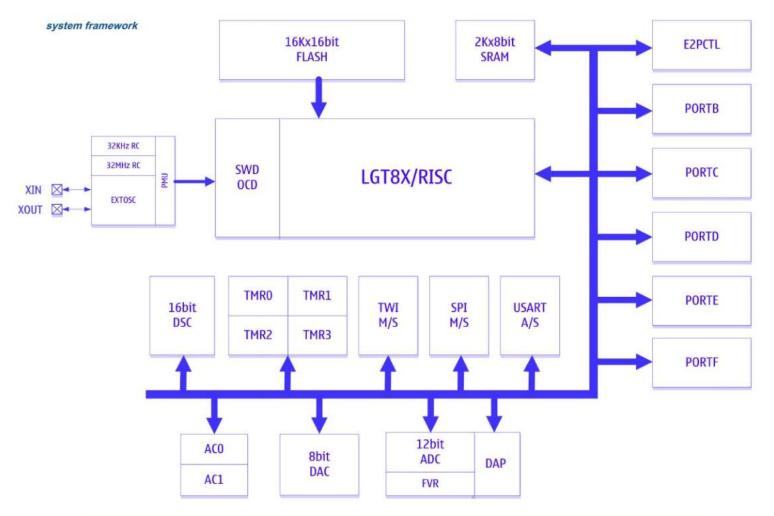
8-bit LGT8XM

RISC Microcontroller with In-System Programmable FLASH Memory

LGT8F88P LGT8F168P LGT8F328P

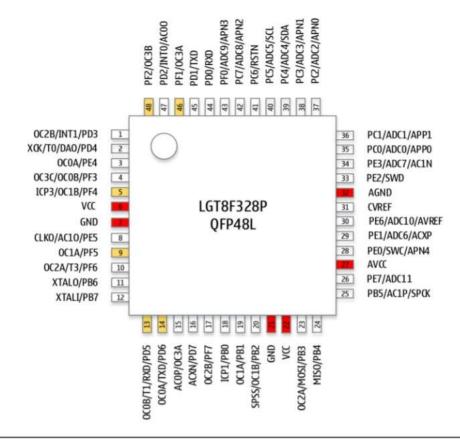
Data book Version 1.0.4(J)

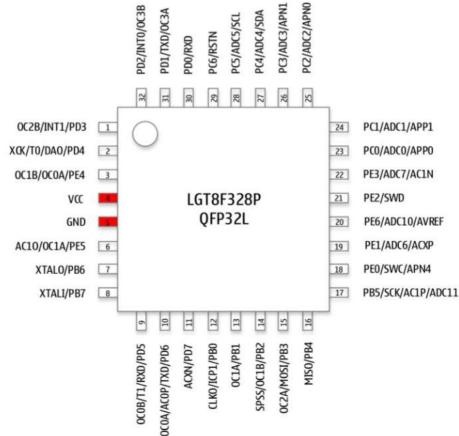
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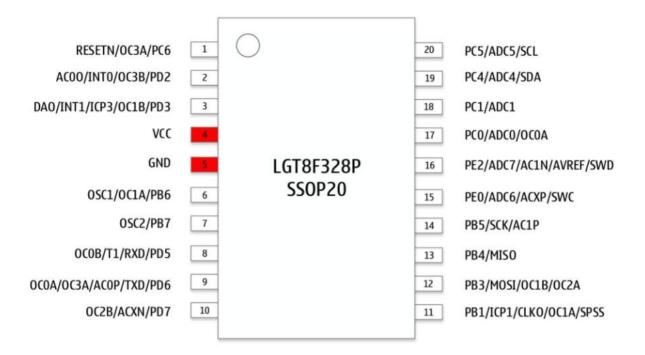


Module Name	Module features
SWD	Debug module, debugging and ISP Features
LGT8X	8Bit high performance RISC Kernel
E2PCTL	FLASH Data Access Interface Controller
PMU	Power management module
PORTB/C/D/E/F	General-purpose programmable input and output ports
DSC	16 Digit arithmetic acceleration unit
ADC	8 Channel 12 Bit ADC with programmable gain
DAP	Differential amplifier
IVREF	1.024V / 2.048V / 4.096V Internal Reference
ACO/1	Analog comparator
TMRO/ 1/2/3	8/16 Bit timer / counter, PWM Controller
WDT	Reset Watchdog module
SPIM/S	Master-slave SPI Controller
TWIM/S	Master-Slave two-wire interface controller, compatible I2C protocol
USART	Synchronous / Asynchronous Serial Transceiver
DAC	8 Bit DAC

Package defined







Pin Description

QFP48	QFP32	SSOP20	
01.10	Q113E	3301 20	PD3/INT1/OC2B*
			PD3: I/O Pin D3
01	01		INT1: External Interrupt 1 Input
			OC2B: Timer/Counter 2 Output Compare Match Output B
		03	PD4/DA0/T0/XCK
			PD4: I/O Pin D4
02	02		DAO: Digital to Analog Converter DAC
			T0: Timer0 Timer/Counter 0
			XCK: USART USART external clock
- 20			PE4/0C0A*
03	03	-	PE4: I/O Pin E4
			OCOA: Timer/Counter 0 Output Compare Match Output A
			PF3/0C3C/0C0B*
04	-	_	PF3: I/O Pin F3
			OC3C: Timer/Counter 3 Output Compare Match Output C
			OCOB: Timer/Counter 0 Output Compare Match Output B
	03	03	PF4/0C1B*/ICP3
05			PF4: I/O Pin F4 OC1B: Timer/Counter 1 Output Compare Match Output B
			ICP3: Timer 3 Capture Input
06	04	04	VCC
07	05	05	GND
01	03	05	PE5/AC10/CLKO*
000,000	06	, <u>=</u>	PE5: I/O Pin E5
80			C10: Comparator AC1 Output
			CLKO: System Clock Output
		06	PF5/0C1A*
09			PF5: I/O Pin F5
0.000			OC1A: Timer/Counter 1 Output Compare Match Output A
	-		PF6/T3/OC2A*
10			PF6: I/O Pin F6
10			T3: Timer 3 External clock input
			OC2A: Timer/Counter 2 Output Compare Match Output A
			PB6/XTALO
11	07	7 06	PB6: I/O Pin B6
			XTALO: Crystal Oscillator Output

QFP48	QFP32	SSOP20	
			PB7/XTALI
12	08	07	PB7: I/O Pin B7
			XTALI: Crystal Oscillator Input
			PD5/RXD*/T1/OC0B
			PD5: I/O Pin D5
13	09	08	RXD: USART Receive Data
			T1: Timer 1 External Clock Input
			OCOB: Timer/Counter 0 Output Compare Match B
			PD6/TXD*/OCOA
14			PD6: I/O Pin D6
14			TXD: USART Transmit Data
	10	09	OCOA: Timer/Counter 0 Output Compare Match A
			ACOP/OC3A
15			ACOP: Analog Comparator 0 Positive Input
			OC3A: Timer/Counter 3 Output Compare Match A
			PD7/ACXN
16	11		PD7: I/O Pin D7
		10	ACXN: Analog Comparator 0/1 Inverting Input
			PF7/OC2B
17	-		PF7: I/O Pin F7
			OC2B: Timer/Counter 2 Output Compare Match B
10	12		PBO/ICP1
18	12		PB0: I/O Pin B0
		11	ICP1: Timer 1 Capture Input
10	12		PB1/OC1A
19	13		PB1: I/O Pin B1 OC1A: Timer/Counter 1 Output Compare Match A
			PB2/OC1B/SPSS
		12	PB2: I/O Pin B2
20	14		OC1B: Timer/Counter 1 Output Compare Match B
			SPSS: SPI Slave Select
21	-	_	GND
22	-	-	VCC
			PB3/MOSI/OC2A
	2	5 12	PB3: I/O Pin B3
23	15		MOSI: SPI Master Output Slave Input
			OC2A: Timer/Counter 2 Output Compare Match A
			PB4/MISO
24	16	13	PB4: I/O Pin B4
27. 5			MISO: SPI Master Input Slave Output
			PB5/SPCK/AC1P
25	17	1.4	PB5: I/O Pin B5
25	17	14	SPCK: SPI Clock
			AC1P: Analog Comparator 1 Noninverting Input
QFP48	QFP32	SSOP20	
	8		-6-

QFP48	QFP32	SSOP20			
			PE7/ADC11		
26	26		PE7: I/O Pin E7		
			ADC11: ADC Input Channel 11		
27	•	-	AVCC: Internal Analog Circuit Positive Power Supply		
			PEO/SWC/APN4		
28	18		PEO: I/O Pin EO		
20	10		SWC: SWD Debug Interface Clock		
		15	APN4: Differential Amplifier Inverting Input Channel 4		
		13	PE1/ADC6/ACXP		
29	19		PE1: I/O Pin E1		
23	19		ADC6: ADC Input Channel 6		
			ACXP: Analog Comparator 0/1 Noninverting Input		
			PE6/ADC10/AVREF		
30	20	16	PE6: I/O Pin E6		
30	20	10	ADC10: ADC Input Channel 10		
			AVREF: ADC External Reference Voltage Input		
31	-	-	CVREF: ADC Reference Voltage External Filter Capacitor (0.1uF)		
32	-	-	AGND: Internal Analog Circuit Power Supply Ground		
			PE2/SWD		
33	21		PE2: I/O Pin E2		
		16	SWD: SWD Debug Interface Data		
		16	PE3/ADC7/AC1N		
34	22		PE3: I/O Pin E3		
			ADC7: ADC Input Channel 7 AC1N: Analog Comparator 1 Inverting Input		
			PCO/ADCO/APPO		
		17	PCO: I/O Pin CO		
35	23		ADC0: ADC Input Channel 0		
			APPO: Differential Amplifier Channel 0 Positive Input		
			PC1/ADC1/APP1		
		100.000.00	PC1: I/O Pin C1		
36	24	18	ADC1: ADC Input Channel 1		
			APP1: Differential Amplifier Channel 1 Positive Input		
			PC2/ADC2/APN0		
27	25	-	PC2: I/O Pin C2		
37	25		ADC2: ADC Input Channel 2		
			APNO: Differential Amplifier Channel 0 Inverting Input		
			PC3/ADC3/APN1		
20	26	5 -	PC3: I/O Pin C3		
38	26		ADC3: ADC Input Channel 3		
			APN1: Differential Amplifier Channel 1 Inverting Input		
QFP48	QFP32	SSOP20			

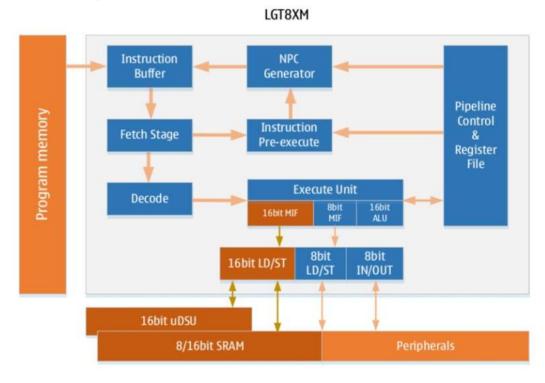
QFP48	QFP32	SSOP20	
			PC4/ADC4/SDA
20	20 27	10	PC4: I/O Pin C4
39 27	19	ADC4: ADC Input Channel 4	
			SDA: I2C Data
			PC5/ADC5/SCL
40	28	20	PC5: I/O Pin C5
40	20		ADC5: ADC Input Channel 5
			SCL: I2C Clock
			PC6/RESETN
41	29	1	PC6: I/O Pin C6
			RESETN: External Reset Input
			PC7/ADC8/APN2
42	_	12	PC7: I/O Pin C7
72			ADC8: ADC Input Channel 8
			APN2: Differential Amplifier Channel 2 Inverting Input
			PF0/ADC9/APN3
43	-	-	PF0: I/O Pin F0
			ADC9: ADC Input Channel 9
			APN3: Differential Amplifier Channel 3 Inverting Input
	20		PDO/RXD
44	30	-	PD0: I/O Pin D0
			RXD: USART Receive
45			PD1/TXD
45		-	PD1: I/O Pin D1
	31		TXD: USART Transmit
16		1	PF1/0C3A PF1: I/O Pin F1
46			0C3A: Timer/Counter 3 Output Compare Match A
			PD2/INTO/ACOO
		32 2	PD2: I/O Pin D2
47			INTO: External Interupt 0 Input
	32		ACOO: Analog Comparator 0 Output
	JL		PF2/OC3B
48			PF2: I/O Pin F2
10			OC3B: Timer/Counter 3 Output Compare Match B
QFP48	QFP32	SSOP20	
Q1140	QITUE	3301 20	

LGT8XM

- Low Power Design
- High Efficency RISC Archatecture
- 16 Bit LD/ST Extension (Dedicated uDSU)
- 130 Instructions, Over 80% execute in a Single Cycle
- Embedded In-Circuit Debugger (OCD)

OVERVIEW

This section discusses the LGT8XM core architecture in general. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.



In order to maximize performance and parallelism, the LGT8XM uses a Harvard architecture – with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is prefetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Reprogrammable Flash memory. The fast-access Register File contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in one clock cycle.

The thirty-two extra working registers are used to Form a combination of three 16-bit registers that can be used to indirectly address the address pointer for accessing external memory and between FLASH programs. The LGT8XM supports single-cycle 16-bit arithmetic, greatly improving the efficiency of indirect addressing. The three special 16-bit registers in the LGT8XM core are named X,Y, Z registers, which are described in more detail later.

The ALU supports arithmetic logic operations between registers and between constants and registers. The operation of a single register can also be performed in the ALU. After the ALU operation is completed, the effect of the operation on the state of the kernal is updated to the status register (SREG). Program Flow control can be addressed to the program area by conditional and unconditional jump/call implementations. Most LGT8XM instructions are 16 bits. Each program address space corresponds to a 16-bit or 32-bit LGT8XM instruction.

After the kernel responds to an interrupt or a subroutine call, the return address (PC) is stored on the stack. The stack is allocated in the system's general data SRAM, so the size of the stack is limited only by the size and usageof the system's SRAM. All applications that support interrupt or subroutine calls must first initialize the Stack Pointer Register (SP), which can be accessed through the IO space. Data SRAM can be accessed in Five different addressing modes. The internal memory of the LGT8XM is linearly mapped to a uniform address space. Please refer to the introduction of the storage memory chapter for further details.

The LGT8XM core includes a Flexible interrupt controller that can be controlled by a global interrupt enable bit in the status register. All interrupts have a separate interrupt vector. The priority of the interrupt has a corresponding relationship with the interrupt vector address. The smaller the interrupt address, the higher the priority of the interrupt. The I/O space contains 64 register spaces that can be directly addressed by IN/OUT instructions. These registers are used for kernel control as well as control Functions For status registers, SPI and other I/O peripherals. This space can be accessed directly by the IN/OUTinstruction or by their address mapped to the data memory space (0x20 - 0x5F). In addition, the LGT8FX8P also includes extended I/O space, which is mapped to data memory space 0x60 — 0xFF, which can only be accessed using ST/STS/STD and LD/LDS/LDD instructions.

To enhance the computing power of the LGT8XM core, a 16-bit LD/ST extension has been added to the instruction set. This 16-bit LD/ST expansion works with the 16-Dimensional Operation Acceleration Unit (UDSU) For efficient 16-bit data operations. At the same time, the kernel also increases the 16-bit access capability to the RAM space. So the 16-bit LD/ST extension can pass 16 bits of data between the uDSU, RAM, and working registers. Please refer to the "Digital Operation Accelerator" section For details.

ARITHMETIC LOGIC UNIT (ALU)

The LGT8XM internally contains a 16-bit arithmetic logic unit that can perform 16 bit arithmetic operations on data in one cycle. The highly efficient ALU is connected to 32 general purpose working registers. The ALU has the ability to perform two arithmetic operations between registers or registers and immediate data in one cycle. There are three types of ALU operations: arithmetic, logic, and bit operations. The ALU also includes a single-cycle hardware multiplier that implements direct signed or unsigned operations on two 8-bit registers in a single cycle. Please refer to the detailed description in the instruction set section.

STATUS REGISTER (SREG)

The status register mainly stores the result information generated by the execution of the most recent ALU operation. This information is used to control the program execution Flow. The status register is updated after the ALU operation has completely ended, thus eliminating the need for separate compare instructions, resulting in a more compact and efficient code implementation. The value of the status register is not automatically saved and restored in response to an interrupt and exit from the interrupt, which requires software to implement.

SREG REGISTER DEFINITION

		egister								
Address:	0X3F (0	X5F)		Defaul	ts: 0X00					
Bit	7	6	5	4	3	2	1	0		
Name	I	T	Н	5	V	N	Z	С		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Bit Defini	tion									
[0]	С	E 100 (100 (100 (100 (100 (100 (100 (100	Carry flag, indicating that the arithmetic or logic operation caused the carry. *							
[1]	Z	A zero flag indicating that the result of an arithmetic or logical operation is zero. *								
[2]	N		A negative flag indicates that an arithmetic or logic operation has produced a negative number. *							
[3]	V	The overflow flag indicates that the result of the two's complement operation has overflowed. *								
[4]	S	Sign bit, equivalent to the XOR operation result of N and V *								
[5]	Н	Semi-carry flag, useful in BCD operations, indicating the semi-carry generated by byte operations*								
[6]	т	For temporary bits, bit copy (BLD) and bit store (BST) instructions, the T bit is used as a temporary memory bit to temporarily store the value of a bit in the general purpose register. *								
[7]	I	The global interrupt enable bit must be set to 1 to enable the core to respond to interrupt events. Different interrupt sources are controlled by independent control bits. The global interrupt enable bit is the last barrier that controls the interrupt signal into the core. The I bit is automatically cleared by the hardware after the core responds to the interrupt vector and is automatically set after the interrupt return instruction (RETI) is executed. The I bit can also be changed using the SEI and CLI instructions. *								

^{*} Please refer to the instruction description for details.

GENERAL WORKING REGISTER

The general purpose working registers are optimized according to the LGT8XM instruction set architecture. To achieve the efficiency and flexibility required for core execution, the LGT8XM's internal working registers support several access modes:

- An 8-bit read and an 8-bit write simultaneously
- Two 8-bit reads simultaneously with an 8-bit write
- Two 8-bit reads simultaneously one 16-bit write
- One 16-bit read and one 16-bit write simultaneously

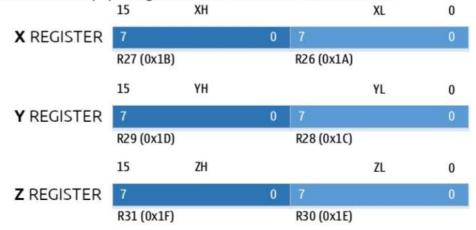
LGT8XM GENERAL WORKING REGISTER



Most of the instructions have direct access to all of the general working registers, and most of them are also single-cycle instructions. As shown in the figure above, each register corresponds to the address of a data storage space, and these general working registers are mapped to the data storage space. These registers only really exist in SRAM, but this unified mapping storage organization gives them a lot of flexibility. The X/Y/Z register can be indexed as a pointer to any general purpose register.

X/Y/Z REGISTER

Registers R26...R31 can be combined in pairs to form three 16-bit registers. These three 16-bit registers are mainly used as address pointers for indirect addressing access. The X/Y/Z registers are structured as follows:



These registers are used as fixed offset, auto-increment, and autodecrement address pointers in different addressing modes. See the Instruction Description section for details.