Figure 26-5. SPI Interface Timing Requirements (Master Mode)

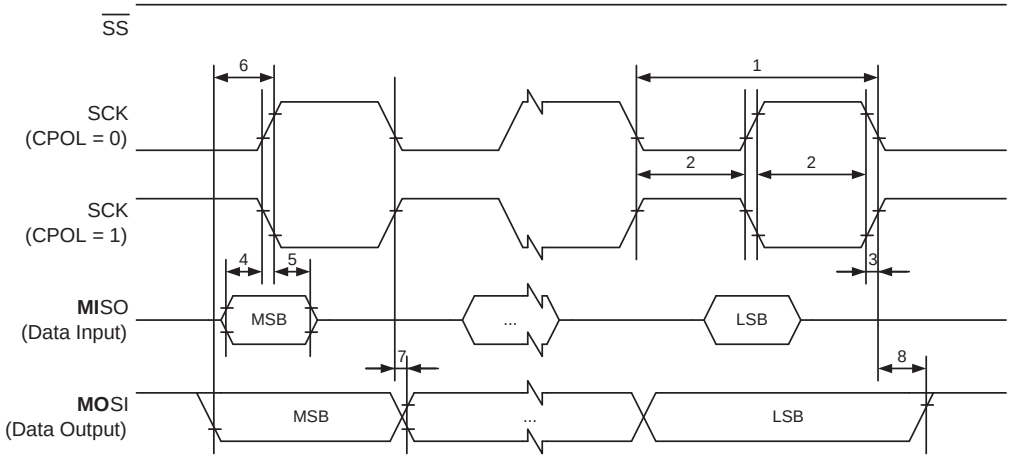

Figure 26-6. SPI Interface Timing Requirements (Slave Mode)