		Any enabled PCn Pin level change will be set PCIF1 . when PCIE1 And Global are set when an interrupt, MCU It will jump to PCI1 Interrupt entry address. PCn Pin interrupts can be independently by the PCMSK1 Control register. Or to execute the interrupt service routine PCIF1 Write bit "1" Will be cleared PCIF1 Bit.
0	PCIF0 Pin change interrupt flag 0 .	Any enabled PBn Pin level change will be set PCIF0 . when PCIE0 And Global are set when an interrupt, MCU It will jump to PCI0 Interrupt entry address. PBn Pin interrupts can be independently by the PCMSK0 Control register. Or to execute the interrupt service routine PCIF0 Write bit "1" Will be cleared PCIF0 Bit.

PCMSK0 - Pin change interrupt mask register 0

PCMSK0 - Pin change mask register 0							
address: 0x6B				Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit Name description		
7	PCINT7	Pin change enable mask 7 . When set PCINT7 Bit "1" Time, PB7 Pin change interrupt is enabled. PB7 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT7 Bit "0" Time, PB7 Pin change interrupts are disabled.
6	PCINT6	Pin change enable mask 6 . When set PCINT6 Bit "1" Time, PB6 Pin change interrupt is enabled. PB6 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT6 Bit "0" Time, PB6 Pin change interrupts are disabled.
5	PCINT5	Pin change enable mask 5 . When set PCINT5 Bit "1" Time, PB5 Pin change interrupt is enabled. PB5 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT5 Bit "0" Time, PB5 Pin change interrupts are disabled.
4	PCINT4	Pin change enable mask 4 . When set PCINT4 Bit "1" Time, PB4 Pin change interrupt is enabled. PB4 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT4 Bit "0" Time, PB4 Pin change interrupts are disabled.
3	PCINT3	Pin change enable mask 3 . When set PCINT3 Bit "1" Time, PB3 Pin change interrupt is enabled. PB3 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT3 Bit "0" Time, PB3 Pin change interrupts are disabled.
2	PCINT2	Pin change enable mask 2 . When set PCINT2 Bit "1" Time, PB2 Pin change interrupt is enabled. PB2 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT2 Bit "0" Time, PB2 Pin change interrupts are disabled.
1	PCINT1	Pin change enable mask 1 . When set PCINT1 Bit "1" Time, PB1 Pin change interrupt is enabled. PB1 Pin