USART Mainly includes three parts: a clock generator, a transmitter and a receiver. Control and status registers are shared by these three portions. The clock generator and a synchronous baud rate generator operating mode from the external input clock synchronization logic components.

XCK Pin is only used for asynchronous transfer mode. Transmitting the write data buffer comprises a serial shift register, Parity Generator and Control logic for different frame formats. A write data buffer allows continuous transmission of data without delay between the data frames. The receiver having a clock and data recovery unit, for receiving asynchronous data. In addition to restoring unit, the receiver further comprising a parity, the control logic, two serial shift register and a receive buffer UDR . The receiver and the transmitter supports the same frame format, and can detect frame error, overrun data and parity errors.

Clock Generation

Clock generating logic generates the base clock for the transmitter and receiver. USART stand by 4 Clock modes: Normal asynchronous mode, double-speed asynchronous mode, the synchronous mode host, and a synchronization pattern from the machine. USCRC of UMSEL Bits select the synchronous or asynchronous mode. USCRA of U2X Position control speed asynchronous mode enabled. It is only valid in the synchronous mode XCK Pin data direction register (with IO Multiplexing) determines the source is produced (master mode) or externally generated (slave mode) from the inside.

Baud Rate Generator

Baud Rate Register UBRR And a down counter connected together as USART The programmable prescaler or baud rate generator. Descending counters work in the system clock (f_{sys}) Next, when it counts down to zero, or UBRRL When the register is written, it will automatically load UBRR Register. When the count reaches zero generating a clock, which clock baud rate generator output, the frequency of f_{sys} / (UBRR + 1) .

The following table shows the various operating modes computing the baud rate (bits / sec) and UBRR Formula values.

Operating mode	The baud rate is calculated (1)	UBRR Value calculation formula
Asynchronous Normal mode	BAUD = f_{sys} / (16 * (UBRR + 1))	UBRR = f_{sys} / (16 * BAUD) - 1
Asynchronous speed mode	BAUD = f_{sys} / (8 * (UBRR + 1))	UBRR = f_{sys} / (8 * BAUD) - 1
Synchronous Master Mode	BAUD = f_{sys} / (2 * (UBRR + 1))	UBRR = f_{sys} / (2 * BAUD) - 1

Description:

1. The baud rate is defined as the transfer rate in bit per second (bps);

2. BUAD Baud rate, f_{sys} As the system clock, UBRR Baud rate register UBRRH with UBRRL The combined value.

Speed Operation

By setting UCSRA Register U2X Bit transfer rate can be doubled, this bit is valid only in asynchronous mode, this bit is set to the synchronous operation mode, "0" .

This bit will be set to divide by half the baud rate divider, effectively doubles the transfer rate for asynchronous communication. In this case, the receiver uses only half the number of samples to the data sampling and clock recovery, and therefore more accurate baud rate setting and the system clock. The transmitter did not change.

External Clock

Synchronous drive slave modes of operation by an external clock. After synchronizing the external clock register and the edge detector was only transmitter