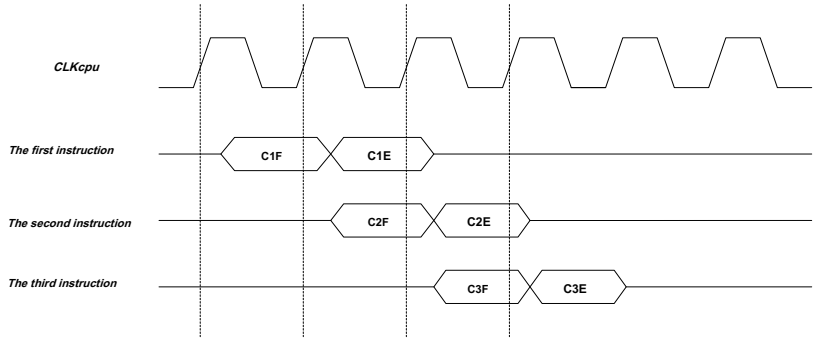
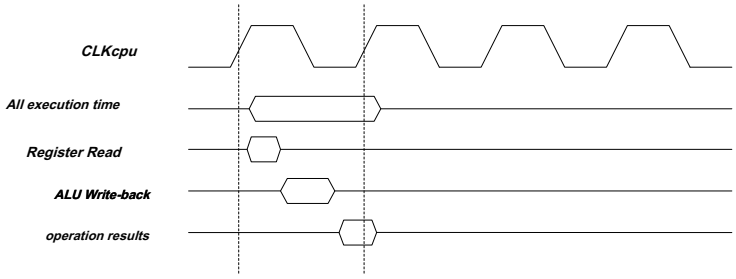
Have access to the kernel 1MIPS / MHz Guarantee the physical execution efficiency.

As can be seen from the figure, while the second instruction will read out during execution of the first instruction. When entering the second instruction execution



During the row, while the third will read instructions. So throughout the implementation period, you do not need to spend extra period of reading instruction, the pipeline from the point of view, to achieve efficiency every Monday execute an instruction.

The following figure shows the access sequence of general purpose working registers, in one cycle, ALU Operation uses two registers as operands, and during this period the ALU Execution result into the destination register.



Reset and Interrupt Handling

LGT8XM Support for multiple interrupt sources. These and a reset interrupt vector corresponding to a single program space vector entry program. In general, all the interrupts have a separate control bits. When the control bit is set and enabled kernel after the global interrupt enable bit kernel in order to respond to the interrupt.

The lowest default program space reserved for the reset and interrupt vector area. LGT8FX8P A complete list of supported interrupts refer to interrupts introduce chapters. This list also determines the priority levels of the different interrupts. The lower the interrupt vector address, the corresponding interrupt priority is higher. Reset (RESET) It has the highest priority, followed by INT0 - External Interrupt Request 0.
Interrupts can be redefined to any of the start address of the vector table (except for the reset vector) 256 Starting at byte aligned, need MCU Control Register (MCUCR) middle IVSEL Bits and IVBASE Vector base register achieve.

When the kernel response, the global interrupt enable flag I Hardware will be automatically cleared. Users can be I Bit enables the realization of nested interrupts. So any disruption that ensued will interrupt the current interrupt service routine. I Bit in the interrupt return instruction (RETI) After automatically set, the normal interrupt response can be followed.

A kind of basic types of interrupts. The first type is triggered by an event, the event interrupt set interrupt flag. After interruption for this, the kernel interrupt request, the current PC Value is a direct replacement for the actual interrupt vector address, perform the corresponding interrupt service routine, while the hardware interrupt flag is automatically cleared. Interrupt flag can also write to the location of the interrupt flag 1 Clear. If the interrupt occurs, the interrupt enable bit is cleared, the interrupt flag will still be set to record interrupt events. Wait until after the interrupt is enabled, the record interrupt event will be an immediate response. Similarly, if an interrupt occurs, the Global Interrupt Enable bit (SERG.I) Is cleared, the corresponding interrupt flag will be set to record interrupt events, etc.