		Any enabled PEn Pin level change will have PCI3 Interrupted. PEn Pin interrupts can be independently by the PCMSK3 Control register. When set PCIE3 Bit "0" When, pin change interrupt 3 Prohibited.
2	PCIE2 Pin change interrupt enable control bit 2 .	When set PCIE2 Bit "1" And when the global interrupt enable pin change interrupt 2 It is enabled. Any enabled PDn Pin level change will have PCI2 Interrupted. PDn Pin interrupts can be independently by the PCMSK2 Control register. When set PCIE2 Bit "0" When, pin change interrupt 2 Prohibited.
1	PCIE1 Pin change interrupt enable control bit 1 .	When set PCIE1 Bit "1" And when the global interrupt enable pin change interrupt 1 It is enabled. Any enabled PCn Pin level change will have PCI1 Interrupted. PCn Pin interrupts can be independently by the PCMSK1 Control register. When set PCIE1 Bit "0" When, pin change interrupt 1 Prohibited.
0	PCIE0 Pin change interrupt enable control bit 0 .	When set PCIE0 Bit "1" And when the global interrupt enable pin change interrupt 0 It is enabled. Any enabled PBn Pin level change will have PCI0 Interrupted. PBn Pin interrupts can be independently by the PCMSK0 Control register. When set PCIE0 Bit "0" When, pin change interrupt 0 Prohibited.

PCIFR - Pin change interrupt flag register

PCIFR - Pin change interrupt flag register								
address: 0x3B						Defaults: 0x00		
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	PCIF4	PCIF3	PCIF2	PCIF1	PCIF0
R / W	-	-	-	R / W	R / W	R / W	R / W	R / W

Bit	Name description	
7: 5	-	Reservations.
4	PCIF4 Pin change interrupt flag 4 .	Any enabled PFn Pin level change will be set PCIF4 . when PCIE4 And Global are set when an interrupt, MCU It will jump to PCI4 Interrupt entry address. PFn Pin interrupts can be independently by the PCMSK4 Control register. Or to execute the interrupt service routine PCIF4 Write bit "1" Will be cleared PCIF4 Bit.
3	PCIF3 Pin change interrupt flag 3 .	Any enabled PEn Pin level change will be set PCIF3 . when PCIE3 And Global are set when an interrupt, MCU It will jump to PCI3 Interrupt entry address. PEn Pin interrupts can be independently by the PCMSK3 Control register. Or to execute the interrupt service routine PCIF3 Write bit "1" Will be cleared PCIF3 Bit.
2	PCIF2 Pin change interrupt flag 2 .	Any enabled PDn Pin level change will be set PCIF2 . when PCIE2 And Global are set when an interrupt, MCU It will jump to PCI2 Interrupt entry address. PDn Pin interrupts can be independently by the PCMSK2 Control register. Or to execute the interrupt service routine PCIF2 Write bit "1" Will be cleared PCIF2 Bit.
1	PCIF1 Pin change interrupt flag 1 .	