FLASH Protection operation

in case VCC Voltage is low, FLASH The erase operation may occur error because the voltage is too low.

FLASH / Data erase operation error at low pressure may be provided by two reasons. First, the normal FLASH Erase operation requires a minimum operating voltage, this voltage is lower than the operation will fail and result in data errors. The second reason is the kernel operating at a certain frequency, it requires a minimum voltage requirement, when this voltage is below, the instruction execution error will result, so that FLASH Operating errors occur.

By following simple ways to avoid similar problems:

When the supply voltage is low, the system enters the reset state. This low-voltage detection circuit can be arranged inside (VDT) achieve. in case VDT Detecting the current operating voltage is lower than the set threshold, VDT Will output a reset signal. in case VDT Threshold can not meet the needs of the application, can be considered an additional external reset circuit.

Register Description

FLASH Address Register - EEARH / EEARL

EEARH / EEARL		
EEARH: 0x22 (0x42) EEARL: 0x21 (0x41)		Defaults: 0x0000
bits	EEAR [15: 0]	
R / W	R / W	
Bit Definitions		
[7: 0]	EEARL EFLASH / E2PROM Access address low 8 Bit.	
[14: 8]	EEARH EFLASH / E2PROM Access Address High 7 Place	
[15]	-	Are reserved

When E2PCTL Controller Access Program FLASH When the region, EEAR [14: 2] Used to access 4 Byte aligned entire program space. EEAR [1: 0] Only access to the data register EEDR Use. For details, please refer to the following on EEDR Description data register. E2PCTL Controller Support 8/16/32 Bit mode, no matter what kind of model, here EEAR Are byte aligned address.

FLASH Data Register - EEDR / E2PD0

EEDR / E2PD0 - FLASH / E2PROM Data register 0		
EEDR / E2PD0: 0x20 (0x40)		Defaults: 0x00
bits	EEDR [7: 0]	
R / W	R / W	
Bit Definitions		
[7: 0]	EEDR E2PD0	E2PCTL Data register 16/32 When the bit pattern, used to access the least significant byte

FLASH Data Register - E2PD1

E2PD1 - E2PCTL Data register 1	
E2PD1: 0x5A	Defaults: 0x00
bits	E2PD1 [7: 0]