Transmission states to control operation of the transmitter and receiver. The transmitter consists of a shift register and transmit control logic components. The receiver consists of a shift register, four reception buffers and control logic receiving the composition.

Clock Generation

Clock generation logic into the master clock and slave clock prescaler detector, respectively, in Master mode of operation and the slave operation. Clock speed prescaler control bits and control bits by the bit rate selected division factor, to produce the corresponding frequency-divided clock (Total 7 Selectable division factor, details see Register description), the output SPCK Pin provides a communication clock to provide simultaneous transmission and reception shift clock for the shift register internal. Clock Detector Clock input SPCK The edge detection, according to SPI Data transmission mode the transmitter and receiver shift operation. In order to ensure proper sampling of the clock signal, SPCK High and low levels shall be greater than the width of the clock 2 System clock cycles.

Transmission and reception

SPI Module supports simultaneous transmission and reception in the single-wire mode, the host support wire received in the wire mode only.

Single line to send and receive

SPI Host will need to communicate slave select signal SPSS Down, you can start a transfer process. Master and slave data will be ready to be transmitted, the master clock signal SPCK Generating clock pulses the data exchange of data, from the host MOSI Removed from MISO Moved, from the data from the machine MISO Removed from MOSI Moved, after exchanging data host pulled finish SPSS Signal to complete the communication.

When configured as a master, SPI Does not control module SPSS Pin, must be handled by user software. Software down SPSS Pin, the slave select, initiate transmission of communication. The software will write data to be transmitted SPDR Register is initiated clock generator, the clock generated by the hardware communication, and the 8 Bits are shifted to the slave, while the data is moved from the machine. After shifting one byte of data, stopping the clock generator, and the transfer completion flag is set SPIF . Software data can be written to once again SPDR To continue the transmission registers a byte, may be pulled SPSS It signals the end of the current transmission. Finally, the incoming data will be saved in a receive buffer.

When configured as a slave, as long as SPSS Signal remains high, SPI Module will maintain sleep and keep MISO Pin is tri-state. Then the software can be updated SPDR Contents of the register. Even at this time SPCK A clock pulse input pin, SPDR The data is not removed until SPSS Signal is pulled low. When one byte of data transfer is completed, the transfer completion flag set hardware SPIF . At this time, before reading the data into the software may continue to SPDR Write data register, the last incoming data will be saved in a receive buffer.

SPI Module in the transmit direction only four buffers in the receive direction have four buffers. When data is transmitted, when the transmission buffer is not full (i.e., transmit buffer full flag WRFULL When the bit is low), to be SPDR Register is written. When receiving the data, when the receive buffer is non-empty state (i.e., the reception buffer empty flag RDEMPT When the bit is low), can be accessed by SPDR Register read character that has been received.

Host double reception

SPI Module wire mode only effective in the master mode of operation, and in that a different wire mode MOSI with MISO They are used for the host to receive data, each SPCK Simultaneously receiving a clock pulse 2 Bits of the data (MISO On the data line