

26.9 Parallel Programming Characteristics

Table 26-8. Parallel Programming Characteristics, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min	Typ	Max	Units
V_{PP}	Programming Enable Voltage	11.5		12.5	V
I_{PP}	Programming Enable Current			250	μA
t_{DVXH}	Data and Control Valid before XTAL1 High	67			ns
t_{XLXH}	XTAL1 Low to XTAL1 High	200			ns
t_{XHXL}	XTAL1 Pulse Width High	150			ns
t_{XLDX}	Data and Control Hold after XTAL1 Low	67			ns
t_{XLWL}	XTAL1 Low to \overline{WR} Low	0			ns
t_{XLPH}	XTAL1 Low to PAgEL high	0			ns
t_{PLXH}	PAgEL low to XTAL1 high	150			ns
t_{BVPH}	BS1 Valid before PAgEL High	67			ns
t_{PHPL}	PAgEL Pulse Width High	150			ns
t_{PLBX}	BS1 Hold after PAgEL Low	67			ns
t_{WLBX}	BS2/1 Hold after \overline{WR} Low	67			ns
t_{PLWL}	PAgEL Low to \overline{WR} Low	67			ns
t_{BVWL}	BS1 Valid to \overline{WR} Low	67			ns
t_{WLWH}	\overline{WR} Pulse Width Low	150			ns
t_{WLRL}	\overline{WR} Low to RDY/ \overline{BSY} Low	0		1	μs
t_{WLRH}	\overline{WR} Low to RDY/ \overline{BSY} High ⁽¹⁾	3.7		4.5	ms
t_{WLRH_CE}	\overline{WR} Low to RDY/ \overline{BSY} High for Chip Erase ⁽²⁾	7.5		9	ms
t_{XLOL}	XTAL1 Low to \overline{OE} Low	0			ns
t_{BVDV}	BS1 Valid to DATA valid	0		250	ns
t_{OLDV}	\overline{OE} Low to DATA Valid			250	ns
t_{OHDZ}	\overline{OE} High to DATA Tri-stated			250	ns

- Notes:
1. t_{WLRH} is valid for the Write Flash, Write EEPROM, Write Fuse bits and Write Lock bits commands.
 2. t_{WLRH_CE} is valid for the Chip Erase command.