	DTR1L										
R/WR	/ W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Bit	Name descri	Name description									
7: 0	DTR1L		High byte deed time register. when DTEN1 Bit is high, OC1A with OC1B Complementary output, OC1A The output from the dead time inserted DTR1L Count clock determined.								

DTR1H -TC1 High byte dead time register

0	1	x00 2	Defaults: 0:	4			(8D	addraga: Ov		
0	1	2	3	4	address: 0x8D Defaults: 0x00					
				4	5	6	7	Bit		
	DTR1H									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	/ W	R/WR		
	Name descr	Bit								
put, OC1B The	High byte dead time register. when DTEN1 Bit is high, OC1A with OC1B Complementary output, OC1B TO OUTPUT from the dead time inserted DTR1H Count clock determined.						DTR1H	7: 0		
pu	nplementary ou				•	High byte o				

TCKCSR -TC Clock Control Status Register

		:	TCKCSR - TC CI	lock Control Stat	us Register					
address: 0x	ÆC			Defaults: 0x00						
Bit	7	6	5	4	3	2	1	0		
	-	F2XEN	TC2XF1	TC2XF0	-	AFCKS	TC2XS1	TC2XS0		
R/W	-	R/W	R/O	R/O	-	R/W	R/W	R/W		
Bit	Name descri	ption								
7	-	Retention								
6	F2XEN	oscillator is enabled, the output 64M When the high-speed clock provided F2XEN Bit "1" Time, 32M RC Frequence output of the oscillator is disabled, can not output 64M The high-speed clock								
5	TC2XF1	When read To	TC High-speed clock mode flag 1 When read TC2XF1 Bit "1", It indicates that the timer counter 1 Work on the high-speed clock mode, as "0", It indicates that the timer counter 1 Work on the system clock mode							
4	TC2XF0 TC I	ligh-speed clock mode flag 0 , The reference timing counter 0 Register Description								
3: 2	-	Retention								
1	TC2XS1	TC High speed clock mode selection control bits 1 When set TC2XS1 Bit "1" When selecting the timer counter 1 Clock Mode When operating in the high-speed setting TC2XS1 Bit "0" When selecting the timer counter 1 Work on the system clock mode								
0	TC2XS0 TC I	High speed cloc	k mode selectio	n control bits 0,	The reference ti	ming counter 0	Register Descri	ption		