Down until the TWINT Is cleared;

- when TWINT Flag is set, the user must update all TWI The next value of the register TWI Bus cycle correlation values. E.g, TWDR Value register must be loaded next bus cycle be sent.
- After completion of updating all registers, and perform other necessary operations, the application writes TWCR register. Write TWCR Time, TWINT Bit must be set for clearing TWINT Mark. TWINT After being cleared, TWI Started by a TWCR Set operation.

### *Transfer mode*

TWI You can work in the following 4 The main species: master transmitter ( MT ), Host receiver ( MR ), Transmitted from the machine ( ST ) And slave receivers ( SR ). Under the same application you can use a variety of modes. E.g, TWI can use MT Mode to TWI EEPROM Writing data, with MR Mode from EEPROM Read the data. If there are other hosts on the system, some may go TWI Transmitting data, will be used SR mode. This is determined by the application software which mode is used.

Below these modes will be described in detail. In the data transmission in each mode, the image will be described in conjunction with the possible status codes. These images contain the following abbreviations:

S : Start status

Rs : REPEATED START status

R : Read flag ( SDA HIGH)

W : Write flag ( SDA LOW)

A: Acknowledge bit ( SDA LOW)

NA : No acknowledge bit ( SDA HIGH)

Data : 8 Bit data byte

P : STOP status

SLA : Slave address

Picture used to represent the circle TWINT Flag is set, the digital circle shows TWSR Register status code, wherein the pre-division control bits are masked as "0" . In these places, the application must perform the appropriate actions to continue or complete TWI transmission. TWI Transmission will be suspended until TWINT Flag is cleared.

when TWINT Flag is set, TWSR The status code is used to determine the proper software operation. Each table shows details of the software operation and the subsequent serial transfer of code required for each state. Note that the form TWSR Prescaler bits are masked as "0" .

## *Host mode*

In the master transmission mode, TWI It will send a certain number of data bytes to a slave-receiver. To enter host mode, you must send START signal. The next decision to address packet format TWI Mode is the master transmitter or receiver mode host. If you send SLA + W , Then enter the master transmitter mode. If you send SLA + R , The master receiver mode. The status code section referred to assume control bit prescaler "0" .

Go through TWCR Register write to emit following values START signal:

| TWINT | TWEA | TWSTA | TWSTO | TWWC | TWEN | - | TWIE |
|---|---|---|---|---|---|---|---|
| 1 | x | 1 | 0 | x | 1 | 0 | x |

TWEN Bit must be set "1" To enable TWI interface, TWSTA Put "1" To send START signal, TWINT Put "1" Cleared