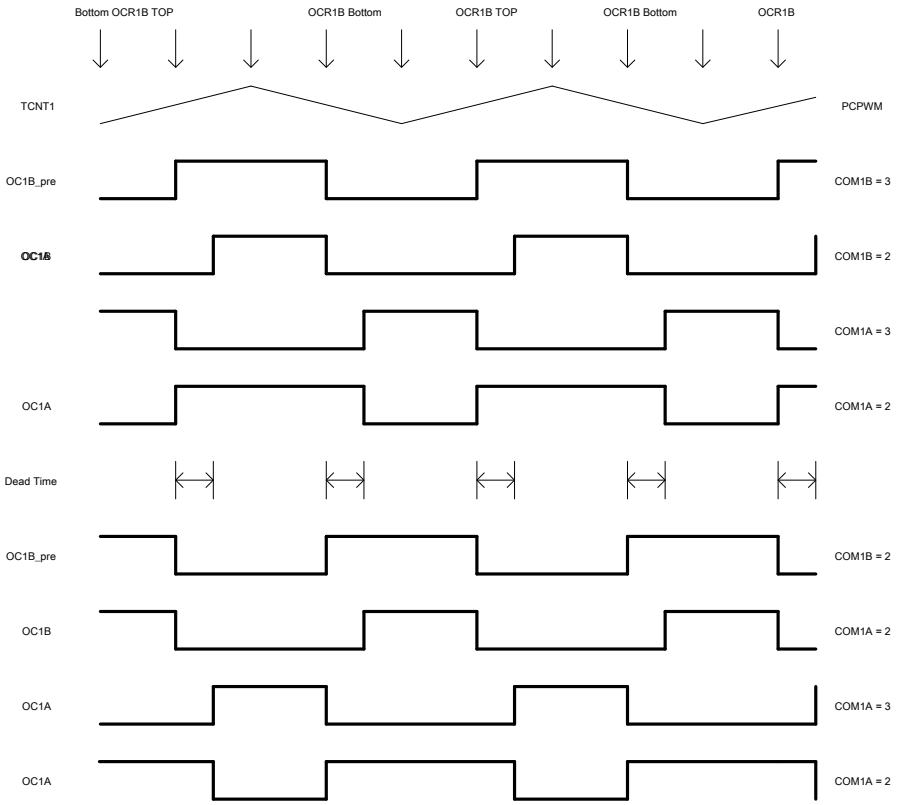

Figure 4 PCPWM Mode TC1 Dead-time control

Set up DTEN1 Bit "0" When inserting the dead time function is disabled, OC1A with OC1B The waveform of the output waveform generated by each comparator output.

High-speed counting mode

The high-speed clock mode using a higher frequency clock count as the clock source for generating higher speed and higher resolution PWM Waveform. This is achieved by the internal clock frequency 32M RC Oscillator output clock rc32m get on 2 Frequency doubling to produce a. Thus, before entering the high-frequency mode, the need to enable the internal 32M RC Oscillator frequency function, i.e. set TCKCSR Register F2XEN Position, and wait for a certain time until the output frequency of the clock signal stable. May then be set TCKCSR of TC2XS1 Timer counter bit to enter the high-speed clock mode.

In this mode, the system clocks are asynchronous with the high-speed clock, and some register (see TC1 Register list) working in the high-speed clock domain, and therefore, such a configuration register and reading is asynchronous, note operation.

No special requirements of high speed clock domain registers in read and write non-continuous, and continuous read and write operations, wait for a system clock, according to the following steps:

5) Write register A ;

6) Waiting for a system clock (NOP Clock register operating system or under);

7) Read or write register A or B .

8) Waiting for a system clock (NOP Registers in the clock or operating system).

When the high-speed clock domain register read operation, a width 8 Bit registers are directly readable, and to read 16 Bit value of the register (OCR1A , OCR1B, ICR1, TCNT1), The low value of the first register is read, the system waits for a clock