Multi-processor communication mode that allows a plurality of receiving data from the host processor from the processor. Determining a first decoded address addressed by a frame which is from the processor. Addressed normal receive the subsequent data from the processor, while the other processor from the data frames until the next frame address is ignored.

As for a host processor, it may be used 9 Bit data frame format, with the first and 9 It identifies the frame bit data format. In this communication mode, the processor must operate in the 9 Bit data frame format. The following steps shall be carried out in the data exchange multiprocessor communication mode:

1 . All work in a multi-processor communication mode (set from the processor MPCM);

2 . The main processor sends an address frame, all the frame received from the processors. From the processor UCSRA Register RXC Place Normal set;

3 . Each processor reads from UDR The contents of the register, decodes the address to determine whether the frame is selected. If selected, It clears UCSRA Register MPCM Bit, not selected, will remain MPCM for "1" And waits for the next address of the frame;

4 . The new address until it receives a frame addressed receiving all data frames from the processor. From the unaddressed Ignore the data frame processor;

5 . It addressed after the last received data frame from the processor, set MPCM Position, and wait for the next frame address arrival. From the second step is then repeated.

use 5 To 8 Bit data frame format is possible, but impractical because the receiver must use n with n + 1 Switching between frame formats. Since the receiver and transmitter use the same character size settings, which makes full-duplex operation becomes difficult. If you use 5 To 8 Bit data frame format, the transmitter should be provided two stop bits, wherein the first stop bit is used for the frame type.

Register Definition

UCSRA - USART Control and status registers A

UCSRA **- USART Control and status registers A**								
address: 0xC0					Defaults: 0x20			
Bit	7	6	5	4	3	2	1	0
Name	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPME
R / W	R	R / W	R	R	R	R	R / W	R / W
Bit	Name	description						
7	RXC	Receive Complete flag. when RXC Value "1" , It indicates that there is data in the receive buffer is not read out. when RXC Value "0" , It indicates that there are no data in the receive buffer is read out. When the receiver is disabled, the receive buffer is refreshed, resulting in RXC Is cleared. When the receiving end interrupt enable bit RXCIE for "1" Time, RXC It can be used to generate a Receive Complete interrupt.						
6	TXC	Send flag. When the data transmission is sent to the shift register, and the transmit buffer is empty TXC Position. When performing transmission end interrupt TXC Automatically cleared, it can also pair TXC write "1" To be cleared. When sending end interrupt enable bit TXCIE for "1" Time, TXC It can generate a Transmit Complete interrupt.						