<table>
<tr><td></td><td></td><td>In non PWM Mode, the force output by comparing bits FOC0B write
"1" The way to compare match. Forcing compare match will not set OCF0B Flag or reload or clear the timer, but the output pin OC0B Will be in accordance with
COM0B It sets the appropriate update, just compare match had really happened. Read FOC0B The return value is always zero.</td></tr>
<tr><td>5</td><td>OC0AS</td><td>OC0A Output port selection control bits. When set OC0AS Bit "0" Time, OC0A The waveform from the pin PD6 Output; when set OC0AS Bit "1" Time, OC0A The waveform from the pin PE4 Output (QFP32 Package valid).</td></tr>
<tr><td>4</td><td>DTEN0</td><td>TC0 Dead time enable control bit. When set DTEN0 Bit "1" When, enabling dead-time insertion. OC0A with OC0B They are in B Insertion of dead time waveform of the comparison output is generated based on the channel, inserted by the dead time interval DTR0 Register corresponding to the count time determined. OC0A The polarity of the output waveform COM0 with COM0B The correspondence between the decision, see OC0A

After insertion of dead time waveform table shown polarity. When set DTEN0 Bit "0" Is prohibited dead-time insertion, OC0A with OC0B Comparing each of the generated output waveforms.</td></tr>
<tr><td>3</td><td>WGM02</td><td>TC0 Waveform generation mode control high.
WGM02 with WGM00 , WGM01 Together form waveform generation mode control
WGM0 [2: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.</td></tr>
<tr><td>2</td><td>CS02</td><td>TC0 Clock control high. For selecting a timing counter 0
The clock source.</td></tr>
<tr><td>1</td><td>CS01</td><td>TC0 Clock selection control bits. For selecting a timing
counter 0 The clock source.</td></tr>
<tr><td rowspan="10">0</td><td rowspan="10">CS00</td><td>TC0 Clock control low. For selecting a timing counter 0
The clock source.</td></tr>
<tr><td>CS0 [2: 0]</td><td>description</td></tr>
<tr><td>0</td><td>No clock source, stops counting</td></tr>
<tr><td>1</td><td>clk sys</td></tr>
<tr><td>2</td><td>clk sys / 8 From prescaler</td></tr>
<tr><td>3</td><td>clk sys / 64 From prescaler</td></tr>
<tr><td>4</td><td>clk sys / 256 From prescaler</td></tr>
<tr><td>5</td><td>clk sys / 1024 From prescaler</td></tr>
<tr><td>6</td><td>External Clock T0 Pin, falling edge</td></tr>
<tr><td>7</td><td>External Clock T0 Pin on the rising edge</td></tr>
</table>

The following table non PWM Mode (ie, normal mode and CTC Mode), the comparison output of the comparator mode control output waveform.

COM0x [1: 0]	description
0	OC0x Disconnect, GM IO Port operations
1	Flip compare match OC0x signal
2	Clear compare match OC0x signal
3	When set compare match OC0x signal