

TC0 Interrupt Mask Register - TIMSK0

| <i>TIMSK0</i> - TC0 Interrupt mask register | | | | | | | | |
|---------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---|----------------|--------|------------|-------|
| address: 0x6E | | | | | Defaults: 0x00 | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | - | - | - | - | - | OCIE0B | OCIE0A | TOIE0 |
| R / W | - | - | - | - | - R / W | | R / WR / W | |
| Bit | Name | description | | | | | | |
| 7: 3 | | Reservations. | | | | | | |
| 2 | OCIE0B | TC0 Output Compare B Match interrupt enable bit. when OCIE0B Bit "1" And Global Interrupt Set, TC0 Output Compare B Match interrupt is enabled. When a compare match occurs, i.e., TIFR0 in OCF0B When the bit is set, an interrupt is generated. when OCIE0B Bit "0" Time, TC0 Output Compare B Match interrupts are disabled. | | | | | | |
| 1 | OCIE0A | TC0 Output Compare A Match interrupt enable bit. when OCIE0A Bit "1" And Global Interrupt Set, TC0 Output Compare A Match interrupt is enabled. When a compare match occurs, i.e., TIFR0 in OCF0A When the bit is set, an interrupt is generated. when OCIE0A Bit "0" Time, TC0 Output Compare A Match interrupts are disabled. | | | | | | |
| 0 | TOIE0 | TC0 Overflow interrupt enable bit. when TOIE0 Bit "1" And Global Interrupt Set, TC0 Overflow interrupt is enabled. when TC0 Overflow occurs, that is, TIFR middle TOV0 When the bit is set, an interrupt is generated. when TOIE0 Bit "0" Time, TC0 Overflow interrupts are disabled. | | | | | | |

TC0 Interrupt Flag Register - TIFR0

| <i>TIFR0</i> - TC0 Interrupt Flag Register | | | | | | | | |
|--------------------------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---|----------------|-------|-------|-------|
| address: 0x35 | | | | | Defaults: 0x00 | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | OC0A | OC0B | - | - | - | OCF0B | OCF0A | TOV0 |
| R / W | R / O | R / O | - | - | - | R / W | R / W | R / W |
| Bit | Name | description | | | | | | |
| 7 | OC0A | Compare output waveform signal OC0A . Compare output waveform signal OC0A Software read but not write. Software can not enable OC0A Signal to its respective IO Before the pin, can first reading OC0A The polarity of the value of the bit to be acquired waveform signal output from the comparator, and by configuring COM0A Bit and set FOC0A Bits to change its polarity, enabling to avoid OC0A Signal to its respective IO Unwanted disturb pulse produced after the pin. | | | | | | |
| 6 | OC0B | Compare output waveform signal OC0B . Compare output waveform signal OC0B Software read but not write. Software can not enable OC0B Signal to its respective IO Before the pin, can first reading OC0B Bit | | | | | | |