OCR1AH -TC1 Output Compare Register A High Byte

OCR1AH - TC1 Output Compare Register A High Byte								
address: 0x89					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR1AH7	OCR1AH6	OCR1AH5	OCR1AH4	OCR1AH3	OCR1AH2	OCR1AH1	OCR1AH0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name description	
7: 0	OCR1AH	Output Compare Register A The high byte. **OCR1AL with OCR1AH Incorporated into the composition together 16 Bit OCR1A . Read and write 16 Bit register requires two operations. write 16 Place OCR1A When, you should write OCR1AH . read 16 Place OCR1A When, it should read OCR1AL .** **OCR1A Continuously with the counter value TCNT1 Compare. Compare match can be used to generate an output compare interrupt, or to the OC1A Waveform generation pins. When PWM When mode, OCR1A Using** double buffered registers. The normal operating mode and match clear mode, double buffering function **is disabled. Double buffering may be updated OCR1A Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses.** **When using the double buffering feature CPU Access is OCR1A When the buffer register, double buffering is disabled CPU Access is OCR1A itself.**

OCR1BL -TC1 Output Compare Register B Low byte

OCR1BL - TC1 Output Compare Register B Low byte								
address: 0x8A					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR1BL7	OCR1BL6	OCR1BL5	OCR1BL4	OCR1BL3	OCR1BL2	OCR1BL1	OCR1BL0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name description	
7: 0	OCR1BL	Output Compare Register B The low byte. **OCR1BL with OCR1BH Incorporated into the composition together 16 Bit OCR1B . Read and write 16 Bit register requires two operations. write 16 Place OCR1B When, you should write OCR1BH . read 16 Place OCR1B When, it should read OCR1BL .** **OCR1B Continuously with the counter value TCNT1 Compare. Compare match can be used to generate an output compare interrupt, or to the OC1B Waveform generation pins. When PWM When mode, OCR1B Using** double buffered registers. The normal operating mode and match clear mode, double buffering function is **disabled. Double buffering may be updated OCR1B Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR1B When the buffer register, double buffering is disabled CPU Access is OCR1B itself.**