

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
\$B9	<a href="#">TWSR</a>	TWI Status bits					-	TWPS	
\$B8	<a href="#">TWBR</a>	TWI Bit Rate register							
\$B6	<a href="#">ASSR</a>	INTCK	-	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB
\$B4	<a href="#">OCR2B</a>	Timer 2 Output Compare Register B							
\$B3	<a href="#">OCR2A</a>	Timer 2 Output Compare Register A							
\$B2	<a href="#">TCNT2</a>	Timer 2 Counter Register							
\$B1	<a href="#">TCCR2B</a>	FOC2A	FOC2B	-	-	WGM22	CS2		
\$B0	<a href="#">TCCR2A</a>	COM2A1	COM2A0	COM2B1	COM2B0	-	-	WGM21	WGM20
\$AF	<a href="#">DPS2R</a>	-	-	-	-	DPS2E	LPRCE	TOS1	TOS0
\$AE	<a href="#">IOCWK</a>	IOCD7	IOCD6	IOCD5	IOCD4	IOCD3	IOCD2	IOCD1	IOCD0
\$AD	<a href="#">ADCSR</a>	BGEN	REFS2	IVSEL1	IVSEL0	-	VDS2	VDS1	VDS0
\$AC	<a href="#">ADMSC</a>	AMOF	-	-	-	AMFC3	AMFC2	AMFC1	AMFC0
\$AB	<a href="#">ADT1H</a>	ADC Auto-monitor Overflow threshold high byte							
\$AA	<a href="#">ADT1L</a>	ADC Auto-monitor Overflow threshold low byte							
\$A9	<a href="#">PORTE</a>	Port Output E (for compatible with LGT8FX8D)							
\$A8	<a href="#">DDRE</a>	Data Direction E (for compatible with LGT8FX8D)							
\$A7	<a href="#">PINE</a>	Port Input E (for compatible with LGT8FX8D)							
\$A6	<a href="#">ADTOH</a>	ADC Auto-monitor Underflow threshold high byte							
\$A5	<a href="#">ADTOL</a>	ADC Auto-monitor Underflow threshold low byte							
\$A4	<a href="#">QFR1</a>	ADC positive offset trimming							
\$A3	<a href="#">QFR0</a>	ADC negative offset trimming							
\$A1	<a href="#">DALR</a>	DAC data register							
\$A0	<a href="#">DACON</a>	-	-	-	-	DACEN	DAOE	DAVS1	DAVS0
\$9F	<a href="#">OCR3CH</a>	Compare output register high byte of Timer3 C channel							
\$9E	<a href="#">OCR3CL</a>	Compare output register low byte of Timer3 C channel							
\$9D	<a href="#">DTR3H</a>	Dead-band register high byte of Timer3							
\$9C	<a href="#">DTR3L</a>	Dead-band register low byte of Timer3							
\$9B	<a href="#">OCR3BH</a>	Compare output register high byte of Timer3 B channel							
\$9A	<a href="#">OCR3BL</a>	Compare output register low byte of Timer3 B channel							
\$99	<a href="#">OCR3AH</a>	Compare output register high byte of Timer3 A channel							
\$98	<a href="#">OCR3AL</a>	Compare output register low byte of Timer3 A channel							
\$97	<a href="#">ICR3H</a>	Input capture register high byte of Timer3							
\$96	<a href="#">ICR3L</a>	Input capture register low byte of Timer3							
\$95	<a href="#">TCNT3H</a>	Counter register high byte of Timer3							
\$94	<a href="#">TCNT3L</a>	Counter register low byte of Timer3							
\$93	<a href="#">TCCR3D</a>	Control register D of Timer3							
\$92	<a href="#">TCCR3C</a>	Control register C of Timer3							
\$91	<a href="#">TCCR3B</a>	Control register B of Timer3							
\$90	<a href="#">TCCR3A</a>	Control register A of Timer3							
\$8D	<a href="#">DTR1H</a>	Dead-band register high byte of Timer1							
\$8C	<a href="#">DTR1L</a>	Dead-band register low byte of Timer1							
\$8B	<a href="#">OCR1BH</a>	Timer 1 Output Compare B High							