		2	External Interrupt 0
		3	Timing counter 0 Compare match
		4	Timing counter 0 overflow
		5	Timing counter 1 Compare match B
		6	Timing counter 1 overflow
		7	Timing counter 1 Input capture event

ADMUX - ADC Multiplexer control register

ADMUX - ADC Multiplexer control register								
address: 0x7C					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	REFS1	REFS0	ADLAR	CHMUX4	CHMUX3	CHMUX2	CHMUX1	CHMUX0
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Initial	0	0	0	0	0	0	0	0

Bit	Name	description	
7: 6	REFS [1: 0]	versus ADCSRD Register REFS2 Fit for selection ADC By providing a reference voltage source REFS Reference voltage control bit, if the change in the conversion process REFS Settings, change will work only until the end of the current conversion.	
		REFS2, REFS [1: 0]	Reference voltage selection
		0_00	AREF
		0_01	AVCC
		0_10	Chip 2.048V The reference voltage source
		0_11	Chip 1.024V The reference voltage source
		1_00	Chip 4.096V The reference voltage source
5	ADLAR	The result is left-aligned enable control bit. When set ADLAR Bit "1" When the conversion result in ADC Align left data register. When set ADLAR Bit "0" When the conversion result in ADC Data registers are right-justified.	
4: 0	CHMUX [4: 0]	ADC Input source selection control bits.	
		CHMUX [4: 0]	Single-ended input source / description
		0_0000	PC0
		0_0001	PC1
		0_0010	PC2
		0_0011	PC3
		0_0100	PC4
		0_0101	PC5
		0_0110	PE1
		0_0111	PE3
		0_1001	PC7
			External input port