0	INT0 External pin 0 Interrupt enable control bit. When set INT0 Bit "1" When, and Global Interrupt set, external pin 0 Interrupts are enabled, wake-up function is enabled. even if INT0 Pin is configured as an output pin corresponding change in level occurs, an interrupt will be generated. When set INT0 Bit "0" When the external pin 0 Interrupts are disabled, wake-up function is also disabled.	

External Interrupt Flag Register - EIFR

EIFR - External Interrupt Flag Register								
address: 0x3C						Defaults: 0x00		
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	INTF1	INTF0
R / W	-	-	-	-	-	- R / W		R / W

Bit	Name description	
7: 2	-	Reservations.
1	INTF1 External pin 1 Interrupt flag. When the edge-triggered external pin 1 Interrupted, INTF1 It is set. When the low level triggered external pins 1 When the interrupt is not set INTF1 Bit. If the external pin at this time 1 Interrupt Enable INT1EN Bit "1" And the Global interrupt flag is set, it will produce an external pin 1 Interrupted. When you do this the interrupt service routine INTF1 Will be automatically cleared or INTF1 Write bit "1" Also clears the bit.	
0	INTF0 External pin 0 Interrupt flag. When the edge-triggered external pin 0 Interrupted, INTF0 It is set. When the low level triggered external pins 0 When the interrupt is not set INTF0 Bit. If the external pin at this time 0 Interrupt Enable INT0EN Bit "1" And the Global interrupt flag is set, it will produce an external pin 0 Interrupted. When you do this the interrupt service routine INTF0 Will be automatically cleared or INTF0 Write bit "1" Also clears the bit.	