SECTION 3
MEMORY

Overview

The LGT8XM architecture has two main memory spaces, Data and Program Memory space. The LGT8FX8P contains internal FLASH that can emulate EEPROM data storage. There is also a special space for storing system configuration information and the chip's global ID number (GUID).

The LGT8FX8P series includes three different models: LGT8F88P/168P/328P. These three models are fully compatible. The differences are the size of FLASH and SRAM available. The following table describes the LGT8FX8P memory configuration options by model:

Table 3. LGT8FX8P Memory Configurations

DEVICE	FLASH	SRAM	EEPROM	INTERRUPTS
LGT8F88P	8KB	1KB	2KB	1 inst. words
LGT8F168P	16KB	1KB	4KB	2 inst. words
LGT8F328P	32KB	2KB	Can be configured as 0K/1K/2K/4K/8K (shared with FLASH)	2 inst. words

The emulated E2PROM Memory of the LGT8F328P is not stored in a separate location from FLASH Memory. The emulated E2PROM system is integrated into FLASH Memory. The user selects the appropriate FLASH partition configuration according to their requirements.

Due to the user configured emulated E2PROM, the system requires twice the program FLASH space to simulate an E2PROM memory space. For example, if the user configures a 1KB E2PROM, 2KB of FLASH memory will be reserved, leaving 30KB for program memory.

Table 4. LGT8F328P FLASH & E2PROM Configuration

DEVICE	FLASH	E2PROM
LGT8F328P	32KB	0KB
	30KB	1KB
	28KB	2KB
	24KB	4KB
	16KB	8KB

FLASH Program Memory

The LGT8FX8P series of microcontrollers each include 8K/16K/32K bytes of on-chip programmable FLASH memory. The FLASH memory is designed for at least 100,000 erase cycles. The LGT8FX8P integrates a FLASH interface controller that includes an in circuit programming feature. For specific implementation details, please see the information on page 23.

Program Memory can be directly read via the LPM instruction. This feature enables application-dependent constant lookup tables. The FLASH program memory is address mapped as a single monolithic block along with the system data storage memory (SRAM). FLASH Memory can also be accessed using the LD/LDD/LDS instructions. The program memory is mapped to the address range directly following the 16-bit data memory (0x4000). This is illustrated in Figure 6. on page 17.