Register Definition

C1SR - AC1 Control and status registers

| C1SR - AC1 Control and status registers | | | | | | | | | |
|---|--|--|-----|--------------|-------------------|--------|--------|---------|--|
| address: 0x2F | | | | | Defaults: 0x80 | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Name | C1D | C1BG | C10 | C1I | C1IE | C1IC | C1IS1 | C1IS0 | |
| R/WR | / W | R/W | R | R/W | R/W | R/W | R/W | R/W | |
| Bit | Name descrip | escription | | | | | | | |
| | C1D | Analog Comparator Disable bit. When set C1D Bit "1" When the analog | | | | | | | |
| 7 | | comparator is turned off. When set C1D Bit "0" When the analog comparator is | | | | | | | |
| | | turned on. | | | | | | | |
| | C1BG | Analog comparator 1 Positive input source selection. C1BG versus C1XR Register C1PS0 Jointly set AC1 The | | | | | | | |
| | | positive terminal of the input source, { C1BG, C1PS0} = 00 = AC1P As the positive input terminal | | | | | | | |
| 6 | | | | | | | | | |
| | | 01 = ACXP As the positive input terminal | | | | | | | |
| | | 10 = internal DAC As the positive input terminal of the output | | | | | | | |
| | | 11 = shut down AC1 The positive terminal of the input source Analog output status bit comparator. The output of the analog comparator is connected directly to the sync after C10 | | | | | | | |
| 5 | C10 | Analog output status bit comparator. The output of the analog comparator is connected directly to the sync after C10 Bit. Software can read C10 | | | | | | | |
| | | Bit value to obtain an output value of the analog comparator. | | | | | | | |
| | Analog comparator interrupt flag. When the analog comparator output event triggered by C1IS Bits d | | | | | | | defined | |
| | C1I | interrupt mode, C1I | | | | | | | |
| 4 | | Bit is set. When the interrupt enable bit C1IE for "1" And the Global Interrupt is set when an interrupt is generated. | | | | | | | |
| | | When performing analog comparator interrupt service routine, C1I Will be automatically cleared or C1I Write bit "1" | | | | | | | |
| | | Also clears the bit. | | | | | | | |
| | | Analog Comparator interrupt enable bit. When set C1IE Bit 1 And enable global interrupt, AC1 The | | | | | | | |
| 3 | 3 C1IE interrupt is enabled. When set C1IE Bit 0 , AC1 Interrupts are disabled. | | | | | | | | |
| | | | | | | | | | |
| 2 | C1IC Analog comparator input Capture Enable | | | | | | | | |
| C1IC = 1, Timing counter 1 The input capture source output from the analog co | | | | | | | rator. | | |
| | | C1IC = 0, Timing counter 1 Capture source from an external input pin ICP1 . | | | | | | | |
| 1 | C1IS1 Analog | g Comparator Interrupt Mode Control high. | | | | | | | |
| 0 | C1IS0 Analog Comparator Interrupt Mode Control low. C1IS0 with C1IS1 Together form C1PS [1: 0] , Used to control analog comparator interrupt trigger. | | | | | | | | |
| | | | | | | | | | |
| | | C1IS | - | Interrupt Mo | | | | | |
| | - | | | | transition ed | lge | | | |
| | - | | 11 | Reservation | | | | | |
| | - | | 0 | | alling edge | | | | |
| | | 1 | 1 | AC1 The ris | ing edge of the t | rigger | | | |