before, MOSI After the data line) set by hardware after two bytes of data transmission after receiving the completion flag SPIF , Save the data in the receive buffer and the shift register. At this point the software to be read SPDR Register twice to obtain two bytes of the received data. Note that, although not to the host computer sends data from the software still needs to wire mode SPDR

Register write clock generator generates data to initiate communication clock, write once SPDR Register to receive two bytes of data.

Data Mode

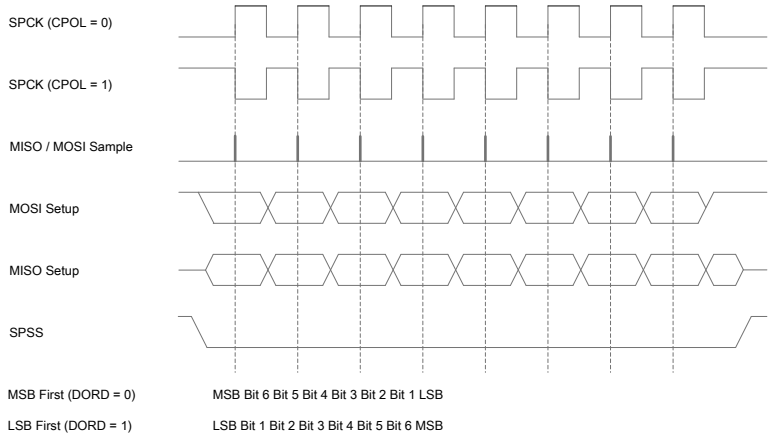
The single-wire mode, with respect to serial data, SPI Have 4 Kind SPCK Combination of phase and polarity, the CPHA with CPOL

To control, as shown in the following table.

CPHA with CPOL Selection data transmission mode

CPOL	CPHA	Starting along	Trailing Edge	SPI mode
0	0	Sampling (rising)	Setting (falling edge)	0
0	1	Setting (rising)	Sampling (falling edge)	1
1	0	Sampling (falling edge)	Setting (rising)	2
1	1	Setting (falling edge)	Sampling (rising)	3

when CPHA = 0 , The data sampling clock and disposed along as shown below:



CPHA for "0" Time SPI Data transmission mode

when CPHA = 1 , The data sampling clock and disposed along as shown below: