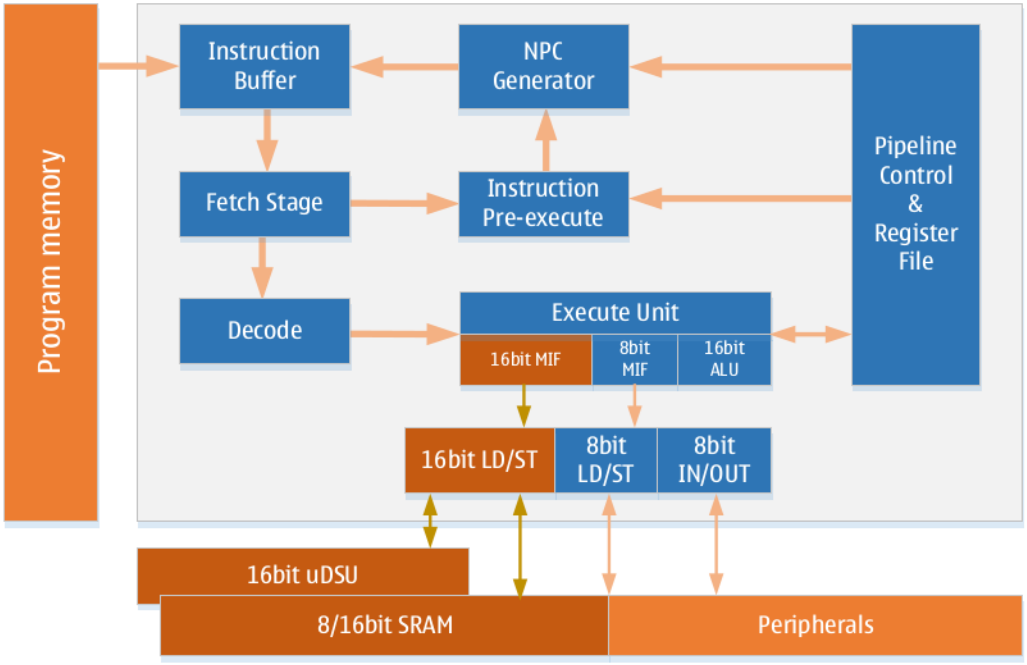
LGT8XM

- Low Power Design
- High Efficency RISC Archatecture
- 16 Bit LD/ST Extension (Dedicated uDSU)
- 130 Instructions, Over 80% execute in a Single Cycle
- Embedded In-Circuit Debugger (OCD)

OVERVIEW

This chapter describes LGT8XM Core architecture and it's function. The core is responsible for ensuring the correct implementation of programs, it must be able to perform accurate calculations, control peripherals and handle a variety of interrupts.

LGT8XM



In order to achieve greater accuracy and efficiency, the LGT8XM Core uses a Harvard architecture - Separate program and data buses. Through an optimized, two instruction execution pipeline, it is possible to reduce the number of unused instruction cycles. This reduces the number of times the FLASH and program memory are read, thus reducing power consumption during core operation. Simultaneously the LGT8XM core has been designed with an improved instruction fetch cycle that can store 2 instructions each cycle. This extra pre-fetched instruction enables a further reduction in FLASH memory access frequency. These improvements to the architecture enable the LGT8XM Core to perform 50% faster than similar core architectures at the same frequency while also consuming less power.