status 0x00 It represents a serial bus error has occurred during transmission. When illegal START or STOP Error occurs when a bus appeared. For example, the address and data, address and ACK Occurs between the START or STOP . Bus error will be set

TWINT . To recover from the error, must be set TWSTO And by writing "1" To clear TWINT . This will TWI Interface enters not addressed slave mode without generating STOP And the release of SCL with SDA And cleared TWSTO Bit. Combined mode

In some cases, in order to complete the desired action must be several TWI Mode combined. For example, from the serial EEPROM

Read data transmission typically comprises the steps of:

1. Transfer must be initiated;

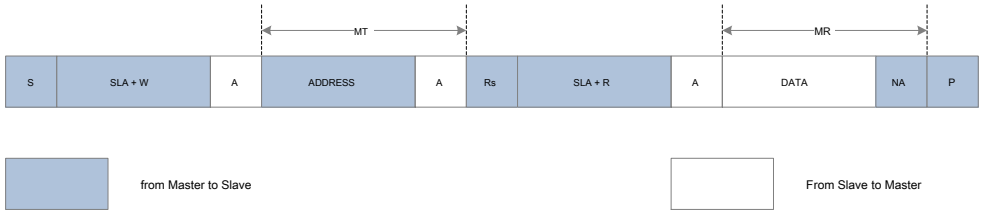
2. You must tell EEPROM You should read position data;

3. Reading must be performed;

4. Transport must end.

Note that data can be transmitted from the master to the slave, and vice versa. It tells the host to read data from confidential position, using the master transmission mode. Next, from the data read from the machine, using the master receive mode. It will change the direction of transmission. The host must maintain control of the bus at all stages, all the steps are uninterrupted operation. If a multi-master system, at step 2 with 3 Another main change between the position of the read data, is to break this principle, the host reads the position data will be wrong. Changing the direction of data transfer between the transfer by sending and receiving data byte address REPEATED START To achieve. send REPEATED START After that, the host still has control of the bus.

The following diagram describes the transmission process:



A combination of a variety of TWI Mode to access the serial EEPROM Map

Multi-host system and arbitration

If there are multiple host connections in the same TWI On the bus, the one or more of them may be simultaneously start data transfer.

TWI Agreement to ensure that in this case, through an arbitration process, which allows a host to transmit data will not be lost. In the following two main processes attempt to send data from the machine will be described as an example of bus arbitration.

There are several different scenarios may arise during arbitration:

- Two or more hosts to communicate with a slave. In this case, either a master or slave do not know there is competition on the bus;

- Two or more masters on the same or a different data access operations from the machine direction. Arbitration takes place in this case, READ / WRITE Bits or data bits. When other hosts to SDA Send online "0" When, to SDA Send online "1" The host arbitration will fail. Failed host switches to a new transmission not addressed slave mode, or idle waiting for the bus from START Signal, which depends on the operation of the application software.
- Two or more masters are different from the machine. In this case, the arbitration will occur in SLA stage. When other hosts to SDA Send online "0" When, to SDA Send online "1" The host arbitration will fail. in SLA It failed master arbitration when the bus switches to slave mode, and checks whether it is addressed to obtain control of the bus master. If addressed, it will enter SR or ST Mode, depending on the SLA Back READ / WRITE Bit. If not look for