TCNT2 -TC2 Count value register

TCNT2 - TC2 Count value register								
address: 0xB2					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	TCNT27	TCNT26	TCNT25	TCNT24	TCNT23	TCNT22	TCNT21	TCNT20
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name description	
7: 0	TCNT2	**TC2 Count value register. by TCNT2 Directly to the counter register 8 Read and write access to the** counter value. **CPU Correct TCNT2 Write to register on the next timer clock cycle to prevent the occurrence of compare match, even if the timer has stopped. This allows initialization TCNT2 And the value of the register OCR2 The value of the agreement without causing disruption. If you write TCNT2 The value is equal to or bypassed OCR2 Value, compare** match will be lost, resulting in incorrect waveform generation. When the timer stops counting the clock source is not **selected, but CPU Still access TCNT2 . CPU** Write counter is cleared or a higher priority than addition and subtraction operations.

OCR2A - TC2 Output Compare Register A

OCR2A - TC2 Output Compare Register A								
address: 0xB3					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR2A7	OCR2A6	OCR2A5	OCR2A4	OCR2A3	OCR2A2	OCR2A1	OCR2A0
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit Name		description
7: 0	OCR2A	**TC2 Output Compare Register A .** **OCR2A It contains a 8 Bit data, with the counter value continuously TCNT2 Compare. Compare match can be used to generate an output compare interrupt, or to the OC2A Waveform generation pins. When PWM When mode, OCR2A Using** double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated **OCR2A Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR2A When the buffer register, double buffering is disabled CPU Access is OCR2A itself.**

OCR2B - TC2 Output Compare Register B

OCR2B - TC2 Output Compare Register B								
address: 0xB4					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR2B7	OCR2B6	OCR2B5	OCR2B4	OCR2B3	OCR2B2	OCR2B1	OCR2B0
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W