		After 6 Clock cycles, change IOCR The value of the other bits. After four cycles WCE Automatically cleared of IOCR Register update operation is invalid.

MCU Status Register - MCUSR

MCUSR - IO Special Function Registers Control								
MCUSR: 0x34 (0x54)				Defaults: 0x00				
Bits	SWDD	-	PDRF	OCDRF	WDRF	BORF	EXTRF	PORF
R / W	R / W	-	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[0]	PORF	Power-on reset flag, write 0 Clear						
[1]	EXTRF	External reset flag, power-on reset automatically cleared, or write 0 Clear						
[2]	BORF	Detection reset, power-on reset automatically cleared, or write 0 Clear						
[3]	WDRF	Watchdog reset flag, power-on reset automatically cleared, or write 0 Clear						
[4]	OCDRF	OCD Debugger reset flag, power-on reset automatically cleared, or write 0 Clear						
[5]	PDRF	From Power / off Wake-up signs, detailed description please refer to the power management section.						
[6]	-	Are reserved						
[7]	SWDD	SWD Interface disable bit. write 1 Will be closed SWD interface. SWD After the interface is down, and will not be able to debug ISP operating. If the user program closed SWD Interface, power down process by RESET Way as to prohibit the operation of internal procedures, and then debug ISP operating. SWD After closing the interface, SWD Occupied by two I / O Interface can be used as general-purpose I / O use. To avoid SWDD Misuse, users need to first update in SWDD Within four cycles after a write bit SWDD To take effect.						

[Use suggestions]:

To be more accurate and effective use of the reset flag information, it is recommended that users try to read the pre-reset flag in the initialization process and then cleared.

Watchdog Control Status Register - WDTCSR

WDTCSR - WDT Control and status registers								
address: 0x60					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	WDIF	WDIE	WDP3	WDTOE	WDE	WDP2	WDP1	WDP0
	R / W	R / W		R / W	R / W	R / W	R / W	

Bit	Name description	
[7]	WDIF	WDT Interrupt flag. when WDT Work in the interrupt mode and an overflow occurs will set WDIF Bit. when WDT Interrupt enable bit WDIE for "1" And the Global Interrupt When set, WDT An interrupt is generated. carried out WDT Will be cleared when the interrupt WDIF Bit of WDIF Write bit "1" Also clears the bit.
[6]	WDIE	WDT Interrupt enable control bit. When set WDIE Bit "1" When, and Global Interrupt set, WDT Interrupt is enabled.