Register Definition

MCU Control Register - MCUCR

MCUCR - MCU Control register								
MCUCR: 0x35 (0x55)				Defaults: 0x00				
MCUCR	FWKEN	FPDEN	EXRFD		PUD	IRLD	IFAIL	IVSEL	WCE
R / W	R / W	R / W	R / W		R / WW / O		R / O	R / W	R / W

Bit Definitions		
[0]	WCE	MCUCR Update Enable bit, update MCUCR Before, you first need to set this bit, and then 6 Completed within a period MCUCR Update registers
[1]	IVSEL	Interrupt Vector Select bit, this location 1 After the interrupt vector address will be based IVBASE Mapped to the new value of the register address
[2]	IFAIL	The system failed to load configuration bits flag, 0 = By checking the configuration information 1 = Failed to load configuration information
[3]	IRLD	write 1 The reload the system configuration information
[4]	PUD	Pull on the global disable bit 0 = Pull-up control to enable global 1 = Close all IO The pull-up resistor
[5]	EXRFD	External reset filtering disable bit 0 = Enable External reset (190us) The digital filter 1 = Disable external reset of the digital filter circuit
[6]	FPDEN	Flash Power / down Enable Control 0 :system SLEEP Rear FLASH Remain powered 1 :system SLEEP Rear FLASH Power outage
[7]	FWKEN	Fast wake-up mode enable control, only Power / Off Mode is active 0 : 260us Filter delay 1 : 32us Filter delay

Interrupt Vector Address Register - IVBASE

IVBASE - Interrupt Vector Address Register		
IVBASE: 0x75		Defaults: 0x00
IVBASE	IVBASE [7: 0]	
R / W	R / W	

Bit Definitions		
[7: 0]	IVBASE	in case IVSEL for 1 Interrupt vector (except for the reset vector) will IVBASE Base address 512 Remapping bytes on a page. Interrupt vector base address is mapped to: (IVBASE << 8) + table 1 Corresponding vector address