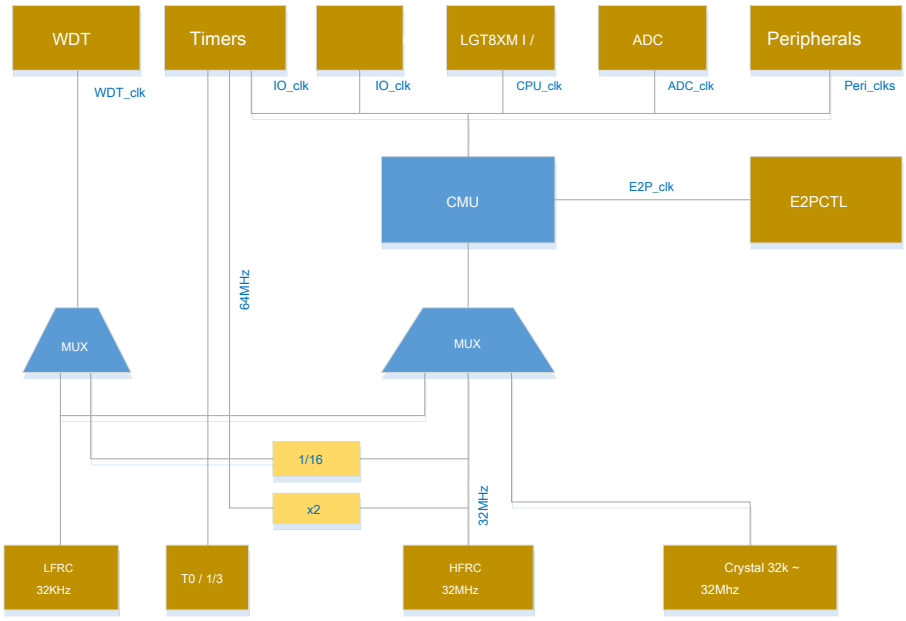
System Clock and Configuration

System Clock Distribution

LGT8FX8P Support for multiple clock input. The system can operate in three main clock sources, each of the internal 32KHz Can be calibrated RC Oscillator, internal 32MHz Can be calibrated RC And an external oscillator 400KHz ~ 32MHz Crystal input. The figure below shows LGT8FX8P Clock distribution system, CMU The center of the clock management is responsible for dividing the system clock, the clocks generated independently for different clock control module and the like. General applications, not all of the clocks do not operate simultaneously, in order to reduce power consumption, depending on the power management system of the sleep mode, the clock is not used to close the module. Specific operation details, please refer to the relevant sections of power management.



CPU_clk

For driving LGT8XM Kernel and SRAM Operation. Such drive general purpose working registers, status registers, etc.

CPU After the clock is stopped, the kernel will not continue to execute instructions and calculation. Execution system SLEEP After the instruction into the sleep mode the core clock will be turned off.

Peri_clk

Most peripheral modules for driving, such as timer / counter, SPI , USART Wait. IO Clock is also used to drive an external interrupt module. When the peripheral clock is stopped due to sleep, some peripherals may be part of the work in the wake of the system clock or a separate asynchronous mode. such as TWI The address recognition can wake up most of the sleep mode, when the address recognition part of the work in asynchronous mode.

E2P_clk

E2P_clk A clock for generating FLASH Interface access timing. E2P_clk Generating access E2PCTL access FLASH The timing of the interface. E2P_clk Fixed from the inside 32MHz HFRC Oscillator 32 Divider (1MHz) . If you need to use E2PCTL Internal program module to read and write FLASH Or data FLASH Space, need to be able to advance inside 32MHz Oscillator.