32KHz RC Oscillator Calibration Register - RCKCAL

| RCKCAL - 32MHz RC Calibration Registers | | | | | | | | |
|---|--|--|--|--|--|--|--|--|
| RCKCAL: 0x67 | 7 Default: factory settings | | | | | | | |
| Bits | RCKCAL [7: 0] | | | | | | | |
| R/W | R/W | | | | | | | |
| Bit Definitions | | | | | | | | |
| [7: 0] | RCKCAL The calibration values is written RCKCAL Register completed 32KHz RC Oscillator Calibration | | | | | | | |

Clock Source Register Management - PMCR

| | | PMC | R - Clock So | urce reç | jister management | | | | | | |
|---------------------------|-----------|---|---|----------|-------------------|-----|-----|--|--|--|--|
| PMCR: 0xF2 Defaults: 0x03 | | | | | | | | | | | |
| Bits | PMCE | PMCE CLKFS / CLKSS WCLKS OSCKEN OSCMEN RCKEN RCMEN | | | | | | | | | |
| R/W | R/W | R/W | R/W | ' | R/W | R/W | R/W | | | | |
| Bit Definitions | 5 | | | | | | | | | | |
| [0] | RCMEN in | RCMEN internal 32MHz RC Oscillator Enable Control, 1 Enable, 0 Ban | | | | | | | | | |
| [1] | RCKEN int | RCKEN internal 32KHz RC Oscillator Enable Control, 1 Enable, 0 Ban | | | | | | | | | |
| [2] | OSCMEN EX | OSCMEN External high frequency crystal oscillator enable control, 1 Enable, 0 Ban | | | | | | | | | |
| [3] | OSCKEN E | OSCKEN External enable control low frequency oscillator, 1 Enable, 0 Ban | | | | | | | | | |
| [4] | WCLKS | WDT Clock source selection, WCLKS 0 - Select the internal 32MHz HFRC Oscillator 16 Divide 1 - internal 32KHz LFRC Oscillator | | | | | | | | | |
| [5] | CLKSS | | Master clock source selection control to select the clock source type, the reference clock source selection portion | | | | | | | | |
| [6] | CLKFS | | Master clock source frequency controlled clock frequency selection type, a reference clock source selection portion | | | | | | | | |
| [7] | PMCE | | PMCR Change enable control register bits. Change PMCR Position before the other, this bit must first be set, and then set the value of the other bits in the four cycles. | | | | | | | | |

Master clock prescaler register - CLKPR

| CLKPR - Master clock prescaler register | | | | | | | | | | | | | | |
|---|-------|-------|----------------------------|-----|-------|--|----|-----|-----|-----|------------------------|------------------------------|-----|--|
| CLKPR: 0x61 Defaults: 0x03 | | | | | | | | | | | | | | |
| Bits | WCE | СКС | EN1 | СКО | KOEN0 | | - | PS3 | | P | S2 | PS1 | PS0 | |
| R/W | R/W | R | / W | R | - w | | - | R | R/W | | / W | R/W | R/W | |
| Bit Definitions | | | | | | | | | | | | | | |
| [3: 0] | CLKPS | | Clock select bit prescaler | | | | | | | | | | | |
| | | | PS3 | 3 | PS2 | | PS | 1 | PS | PS0 | | Frequency division parameter | | |
| | | | 0 | | 0 | | 0 | | 0 | | 1 | | | |
| | | CLKPS | | | 0 | | 0 | | 1 | | 2 | | | |
| | | | | | 0 | | 1 | | 0 | 0 | | 4 | | |
| | | | 0 | | 0 | | 1 | | 1 | | 8(default allocation) | | | |