

• Bit 0 - PCIF0: Pin Change Interrupt Flag 0

When a logic change on any PCINT7..0 pin triggers an interrupt request, PCIF0 becomes set (one). If the I-bit in SREG and the PCIE0 bit in PCICR are set (one), the MCU will jump to the corresponding Interrupt Vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical one to it.

10.2.6 PCMSK2 – Pin Change Mask Register 2

Bit	7	6	5	4	3	2	1	0									
(0x6D)	<table><tr><td>PCINT23</td><td>PCINT22</td><td>PCINT21</td><td>PCINT20</td><td>PCINT19</td><td>PCINT18</td><td>PCINT17</td><td>PCINT16</td></tr></table>								PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	PCMSK2
PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16										
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W									
Initial Value	0	0	0	0	0	0	0	0									

• Bit 7..0 – PCINT23..16: Pin Change Enable Mask 23..16

Each PCINT23..16-bit selects whether pin change interrupt is enabled on the corresponding I/O pin. If PCINT23..16 is set and the PCIE2 bit in PCICR is set, pin change interrupt is enabled on the corresponding I/O pin. If PCINT23..16 is cleared, pin change interrupt on the corresponding I/O pin is disabled.

10.2.7 PCMSK1 – Pin Change Mask Register 1

Bit	7	6	5	4	3	2	1	0									
(0x6C)	<table><tr><td>–</td><td>PCINT14</td><td>PCINT13</td><td>PCINT12</td><td>PCINT11</td><td>PCINT10</td><td>PCINT9</td><td>PCINT8</td></tr></table>								–	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	PCMSK1
–	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8										
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W									
Initial Value	0	0	0	0	0	0	0	0									

• Bit 7 – Res: Reserved Bit

This bit is an unused bit in the ATmega48P/88P/168P/328P, and will always read as zero.

• Bit 6..0 – PCINT14..8: Pin Change Enable Mask 14..8

Each PCINT14..8-bit selects whether pin change interrupt is enabled on the corresponding I/O pin. If PCINT14..8 is set and the PCIE1 bit in PCICR is set, pin change interrupt is enabled on the corresponding I/O pin. If PCINT14..8 is cleared, pin change interrupt on the corresponding I/O pin is disabled.

10.2.8 PCMSK0 – Pin Change Mask Register 0

Bit	7	6	5	4	3	2	1	0									
(0x6B)	<table><tr><td>PCINT7</td><td>PCINT6</td><td>PCINT5</td><td>PCINT4</td><td>PCINT3</td><td>PCINT2</td><td>PCINT1</td><td>PCINT0</td></tr></table>								PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	PCMSK0
PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0										
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W									
Initial Value	0	0	0	0	0	0	0	0									

• Bit 7..0 – PCINT7..0: Pin Change Enable Mask 7..0

Each PCINT7..0 bit selects whether pin change interrupt is enabled on the corresponding I/O pin. If PCINT7..0 is set and the PCIE0 bit in PCICR is set, pin change interrupt is enabled on the corresponding I/O pin. If PCINT7..0 is cleared, pin change interrupt on the corresponding I/O pin is disabled.