Bit	7	6	5	4	3	2	1	0
Name	DTR3L7	DTR3L6	DTR3L5	DTR3L4	DTR3L3	DTR3L2	DTR3L1	DTR3L0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	DTR3L	Low byte dead time register. **when DTEN3 Bit is high, OC3A with OC3B Complementary output, OC3A The output from the dead time inserted DTR3L** Count clock determined.						

DTR3H-TC3 High byte dead time register

DTR3H **- TC3 High byte dead time register**								
address: 0x9D					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	DTR3H7	DTR3H6	DTR3H5	DTR3H4	DTR3H3	DTR3H2	DTR3H1	DTR3H0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	DTR3H	High byte dead time register. **when DTEN3 Bit is high, OC3A with OC3B Complementary output, OC3B The output from the dead time inserted DTR3H** Count clock determined.						

TIMSK3-TC3 Interrupt mask register

TIMSK3 **- TC3 Interrupt mask register**								
address: 0x71					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	-	ICIE3	-	OCIE3C	OCIE3B	OCIE3A	TOIE3
R / W	-	-	R / W	-	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 6	-	Reservations.						
5	ICIE3	TC3 Input Capture interrupt enable control bit. **when ICIE3 Bit "1" When, and Global Interrupt set, TC3 Input Capture interrupt is enabled. When the input capture trigger,** **which is TIFR3 of ICF3 Flag is set, an interrupt occurs.** **when ICIE3 Bit "0" Time, TC3 Input capture interrupts are disabled.**						
4	-	Reservations.						
3	OCIE3C	**TC3 Output Compare C Match interrupt enable bit.** **when OCIE3C Bit "1" And Global Interrupt Set, TC3 Output Compare C Match interrupt is enabled. When compare match occurs** **When, that is, TIFR3 in OCF3C When the bit is set, an interrupt is generated.** **when OCIE3C Bit "0" Time, TC3 Output Compare C Match interrupts are disabled.**						
2	OCIE3B	**TC3 Output Compare B Match interrupt enable bit.** **when OCIE3B Bit "1" And Global Interrupt Set, TC3 Output Compare B Match interrupt is enabled. When compare match occurs** **When, that is, TIFR3 in OCF3B When the bit is set, an interrupt is generated.** **when OCIE3B Bit "0" Time, TC3 Output Compare B Match interrupts are disabled.**						
1	OCIE3A	**TC3 Output Compare A Match interrupt enable bit.** **when OCIE3A Bit "1" And Global Interrupt Set, TC3 Output Compare A Match interrupt is enabled. When compare match occurs**						