		TCNT1H with TCNT1L Incorporated into the composition together TCNT1 ,by TCNT1 Directly to the counter register 16 Count value read and write access. Read and write 16 Bit register requires two operations. write 16 Place TCNT1 When, you should write TCNT1H . read 16 Place TCNT1 When, it should read TCNT1L . CPU Correct TCNT1 Write to register on the next timer clock cycle to prevent the occurrence of compare match, even if the timer has stopped. This allows initialization TCNT1 And the value of the register OCR1x The value of the agreement without causing disruption. If you write TCNT1 The value is equal to or bypassed OCR1x Value, compare match will be lost, resulting in incorrect waveform generation. When the timer stops counting the clock source is not selected, but CPU Still access TCNT1 . CPU Write counter is cleared or a higher priority than addition and subtraction operations.

TCNT1H -TC1 High byte count value register

TCNT1H - TC1 High byte count value register								
address: 0x85					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	TCNT1H7	TCNT1H6	TCNT1H5	TCNT1H4	TCNT1H3	TCNT1H2	TCNT1H1	TCNT1H0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name description	
7: 0	TCNT1H	TC1 The count value of the high byte. TCNT1H with TCNT1L Incorporated into the composition together TCNT1 ,by TCNT1 Directly to the counter register 16 Count value read and write access. Read and write 16 Bit register requires two operations. write 16 Place TCNT1 When, you should write TCNT1H . read 16 Place TCNT1 When, it should read TCNT1L . CPU Correct TCNT1 Write to register on the next timer clock cycle to prevent the occurrence of compare match, even if the timer has stopped. This allows initialization TCNT1 And the value of the register OCR1x The value of the agreement without causing disruption. If you write TCNT1 The value is equal to or bypassed OCR1x Value, compare match will be lost, resulting in incorrect waveform generation. When the timer stops counting the clock source is not selected, but CPU Still access TCNT1 . CPU Write counter is cleared or a higher priority than addition and subtraction operations.

ICR1L -TC1 Input Capture Register Low Byte

ICR1L - TC1 Input Capture Register Low Byte								
address: 0x86					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	ICR1L7	ICR1L6	ICR1L5	ICR1L4	ICR1L3	ICR1L2	ICR1L1	ICR1L0
		R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name description	
7: 0	ICR1L	TC1 Input capture the low byte value. ICR1H with ICR1L Incorporated into the composition together 16 Bit ICR1 . Read and write 16 Bit register requires two operations. write 16 Place ICR1 When, you should write ICR1H . read 16 Place