Address matching means

Address matching means for checking whether the received address byte and TWI Address register 7 Bit address match. when TWAR Register TWI Broadcast Enable bit call identification (TWGCE) Is set, the address received from the bus to the broadcast address will be compared. Upon an address match, the control unit will execute the correct action. TWI Response, or module does not respond to its address, depending on the TWCR Register is set. Even in the sleep mode, the address matching unit may compare the address, if they are addressed by a master on the bus, then MCU Wake-up from sleep mode.

control unit

The control unit is responsible for monitoring the bus and in accordance with TWCR Setting produces a corresponding response. when TWI When an event occurs it requires applications to participate on the bus, TWI Interrupt flag TWINT It will be set. In the next clock cycle, TWI Status Register TWSR It will be updated to show the status code of the event. in TWINT When set, TWSR It contains the exact status information. At other times, TWSR For a special status code indicating that there is no exact status information. once TWINT Flag is set, SCL Line has been kept low, pause on the bus TWI Transmission, so that the application process events.

Under the following circumstances, TWINT Flag will be set:

- TWI End transmission START / REPEATED START After the state
- TWI End transmission SLA + R / W Rear
- TWI After transmitting an address byte
- TWI Bus after arbitration loss
- TWI After being addressed by the master (or slave address match broadcast)
- It addressed as work from the machine, receive STOP or REPEATED START Rear
- The illegal START or STOP When the state caused by the bus error

TWI usage of

TWI The interface is byte-oriented and interrupt based. All bus event, such as a byte received or transmitted an START Signal, will have a TWI Interrupted. due to TWI Is interrupt-based, so TWI Byte transfer process, the application software can perform other operations freely. TWCR Register TWI Interrupt enable bit TWIE And global interrupt enable bit in the control together TWINT Whether generated when the flag is set TWI Interrupted. in case TWIE Bit is cleared, the application must query TWINT Way to detect flag TWI Action on the bus.

when TWINT When the flag is set, it indicates TWI Interface to complete the current operation, wait for the response from the application. under these circumstances, TWI Status Register TWSR It contains reflect the current state of the bus status code. Applications can set TWCR with TWDR Register, to decide in the next TWI Bus cycle TWI How the interfaces work.

The following figure shows the applications and TWI Examples of connection interface. In this embodiment, the host desires to transmit one byte of data to the slave. Described here is very simple, the next chapter will have a more detailed presentation.