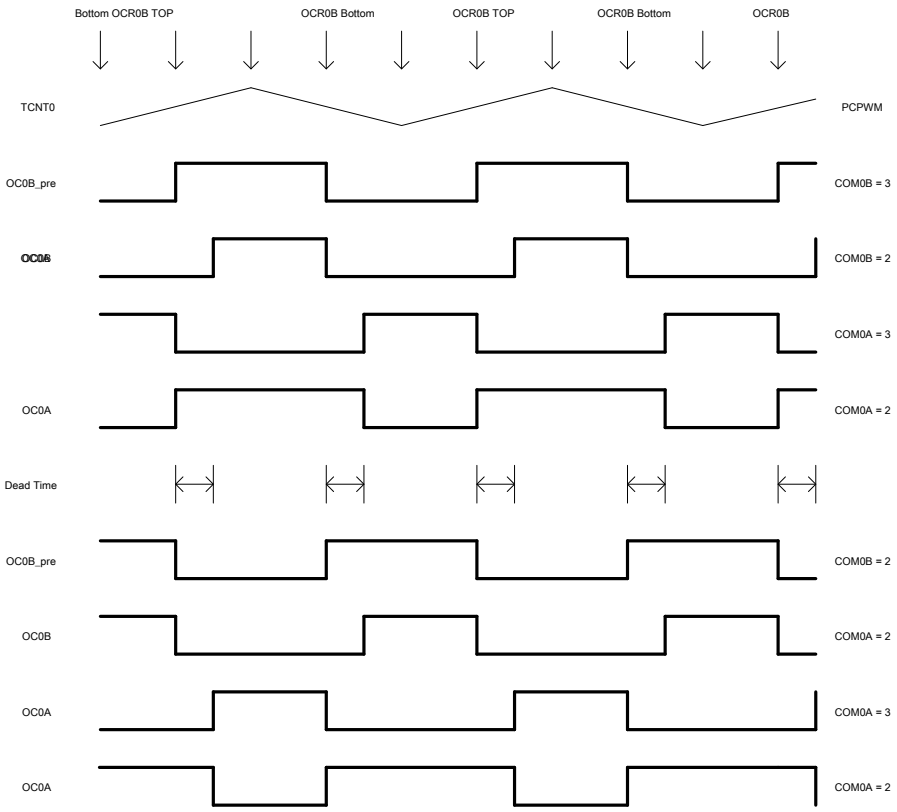

Figure 2 PCPWM Mode TC0 Dead-time control

Set up DTEN0 Bit "0" When inserting the dead time function is disabled, OC0A with OC0B The waveform of the output waveform generated by each comparator output.

High-speed clock mode

The high-speed clock mode using a higher frequency clock count as the clock source for generating higher speed and higher resolution PWM Waveform. This is achieved by the internal clock frequency 32M RC Oscillator output clock rc32m get on 2 Frequency doubling to produce a. Thus, before entering the high-frequency mode, the need to enable the internal 32M RC Oscillator frequency function, i.e. set TCKCSR

Register F2XEN Position, and wait for a certain time until the output frequency of the clock signal stable. May then be set TCKCSR of TC2XS0 Timer counter bit to enter the high-speed clock mode.

In this mode, the system clocks are asynchronous with the high-speed clock, and some register (see TC0 Register list) working in the high-speed clock domain, and therefore, such a configuration register and reading is asynchronous, note operation.

No special requirements of high speed clock domain registers in read and write non-continuous, and continuous read and write operations, wait for a system clock, according to the following steps:

1) Write register A ;

2) Waiting for a system clock (NOP Clock register operating system or under);

3) Read or write register A or B .

4) Waiting for a system clock (NOP Registers in the clock or operating system).

When the high-speed clock domain register read operation, in addition to TCNT0 The registers are directly readable outside, when the counter is still counting, TCNT0 The value changes with a high speed clock, pause counter (provided CS0 Zero) then read TCNT0

Value.