Timer / Counter 0 (TMR0)

- 8 Bit counter
- Two independent comparing unit
- The counter is automatically cleared when compare match occurs and automatically loads
- No disturb pulse phase correction PWM Export
- Frequency generator
- External event counter
- 10 Bit clock prescaler
- Overflow and Compare Match Interrupt
- With dead-time control
- 6 Selectable trigger source automatically shut down PWM Export
- Generating a high-resolution high-speed (high-speed clock mode 500KHz @ 7Bit) PWM

Outline

TC0 Is a common 8 Bit timer counter module support PWM Output waveform can be generated accurately. TC0 contain 1 Count clock generation unit, 1 More 8 Bit counter, and a waveform generation mode control unit 2 Output comparison unit. Simultaneously, TC0 With TC1 Common 10 Bit prescaler, can be used independently 10 Bit prescaler. The system clock prescaler clkio Or high-speed clock rcm2x (internal 32M RC Clock oscillator output rc32m of 2 Frequency) for frequency-dividing the count clock Clkt0 . Waveform generating mode generates the control unit controls the operation mode of the counter and comparing the output waveform. Depending on the mode of operation, a counter for counting each clock Clkt0 Cleared, incremented or decremented. Clkt0 It may be generated by an internal clock or an external clock source. When the count value of the counter TCNT0 It reached its maximum value (equal to the maximum value 0xFF Or output compare register OCR0A ,defined as TOP , The maximum value of the definition MAX When to distinguish), the counter is cleared or decremented. When the count value of the counter TCNT0 Reaches a minimum value (equal to

0x00 ,defined as BOTTOM), The counter will be incremented by one operation. When the count value of the counter TCNT0 Arrivals OCR0A / OCR0B When, also referred to compare match, set or cleared by the output signal of the comparison OC0A / OC0B To produce PWM Waveform. When the enable insertion of dead time, the dead time is set (DTR0 Count clock number corresponding to the register) will be inserted into the generated PWM Waveform. Software by clearing COM0A / COM0B Bit close to zero OC0A / OC0B The waveform output, or set the respective trigger source, when a triggering event occurs automatically cleared by hardware COM0A / COM0B Bit to close OC0A / OC0B The waveform output.

Count clock can be internal or external clock source to generate, select, and divided by the selected frequency clock source located TCCR0B Register CS0 Control bits, see the detailed description TC0 with TC1 Prescaler section.

Length counter is 8 Bit, supporting bi-directional counter. I.e., Waveform generating mode by the operation mode counter is located TCCR0A with TCCR0B Register WGM0 Bit to control. Depending on the mode of operation, a counter for counting each clock Clkt0 Cleared, incremented or decremented. When an overflow occurs count Located TIFR0 Counter register overflow flag TOV0 Bit is set. When the interrupt is enabled may produce TC0 Counter overflow interrupt.

Count value output of the comparison unit TCNT0 And output compare register OCR0A with OCR0B The value, when TCNT0 equal OCR0A or OCR0B When referred to as Comparative match occurs, it is located TIFR0 Output compare flag register OCF0A or OCF0B Bit is set. When the interrupt is enabled may produce TC0 Output Compare match interrupt. It should be noted that, in the PWM Under work mode, OCR0A with OCR0B Register is double buffered. In the normal mode and