CE232 DIGITAL SYSTEM

Topic 11. Design of Sequential Circuit

Prepared by Nabila Husna Shabrina

Contact : nabila.husna@umn.ac.id

Subtopic

11. 1 Asynchronous Up/Down Counter

11.2 Synchronous Up/Down Counter

11.3 Basic Register

11.1 Asynchronous Up/Down Counter

11.1 Asynchronous Up/Down Counter

- **Counter** is a digital device used **to count number of pulses**
- Counter is a sequential circuit for **counting purpose**
- Counter can count in 2 ways
  - Up count (0,1,2,…,n)
  - Down count (N, N-1, …., 1,0)

11.1 Asynchronous Up/Down Counter

- Present count of the counter represent state of the counter
- Counter contains set of flip flops, A n-bit counter require N flip flops and 2^n states
- Counter classification (according to clock cycle)
  - Asynchronous counter
  - Synchronous counter

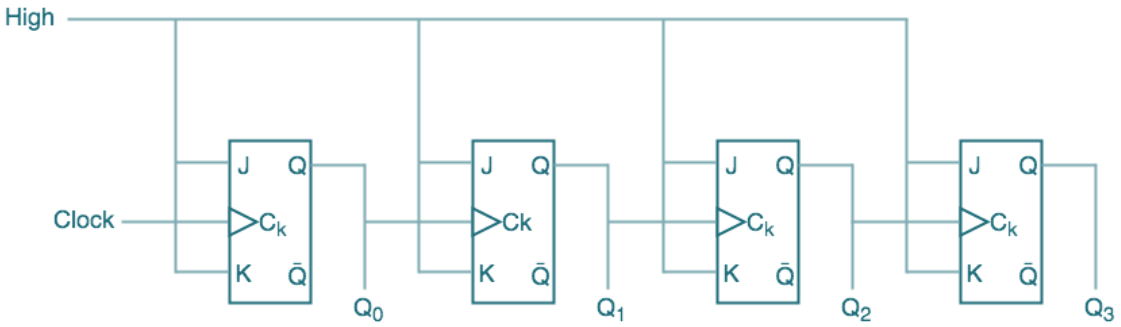
11.1 Asynchronous Up/Down Counter

Asynchronous Counter

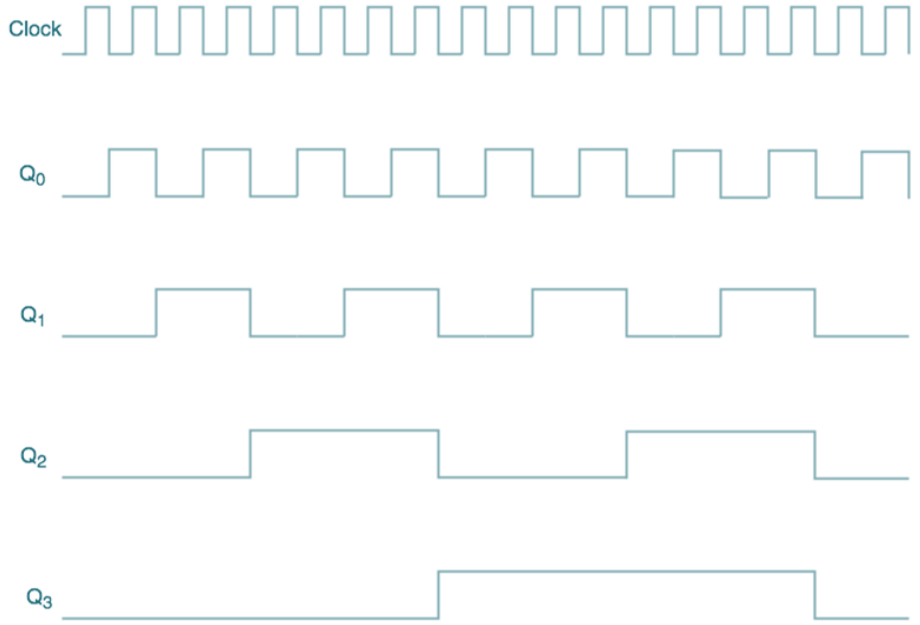
- Asynchronous refers to states that does not have a fixed time relationship with each other
- In asynchronous counter flip flops does not have a common clock pulse, so their state doesn’t change exactly at same time
- First flip flop is driven by main clock and the clock input
- The rest flip flop is driven by output of previous flip flops

11.1 Asynchronous Up/Down Counter

Example of asynchronous counters



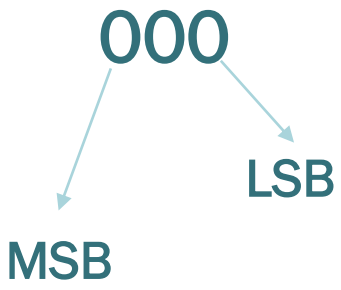
(a) Asynchronous counter

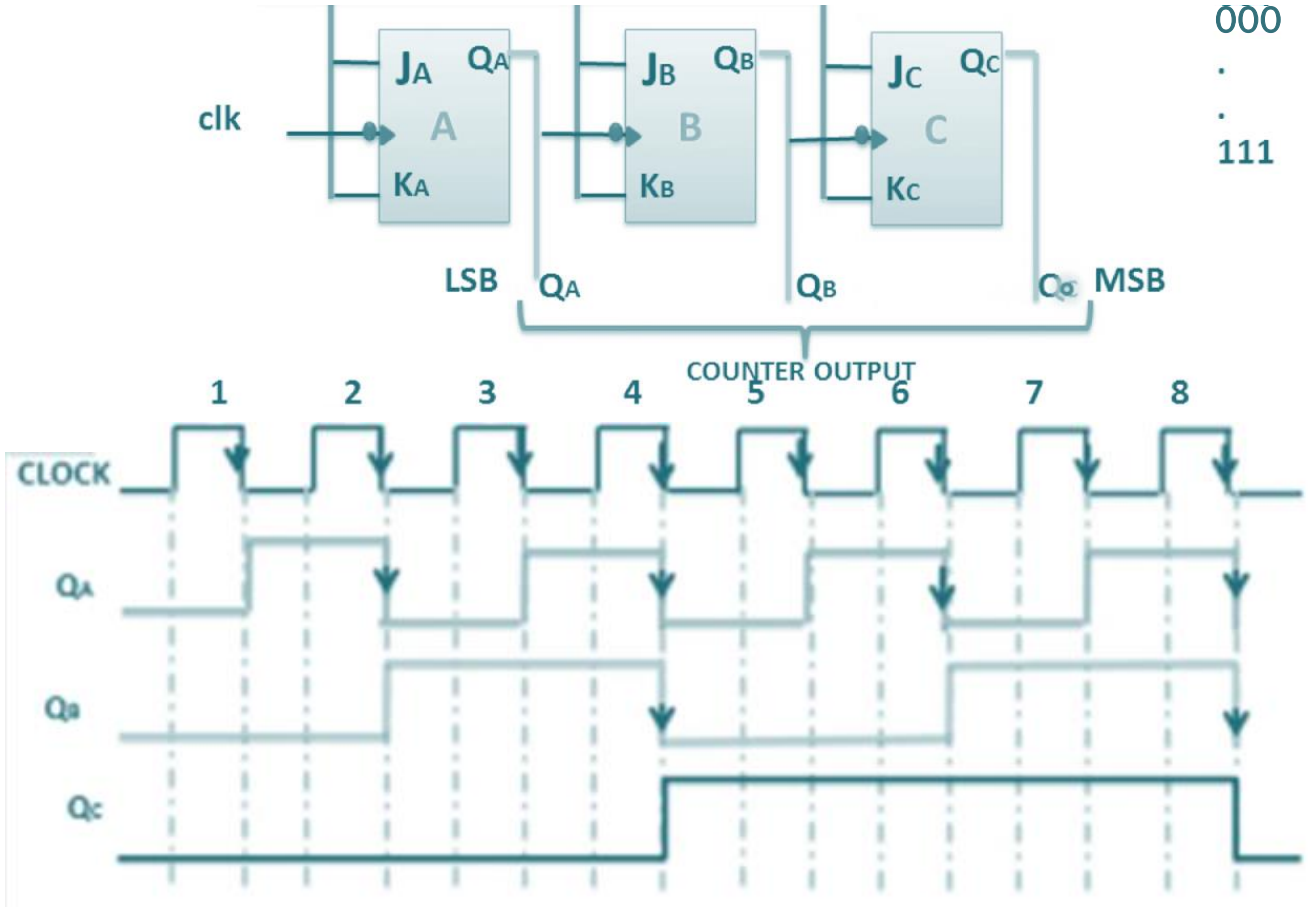


(b) Timing Diagram

11.1 Asynchronous Up/Down Counter

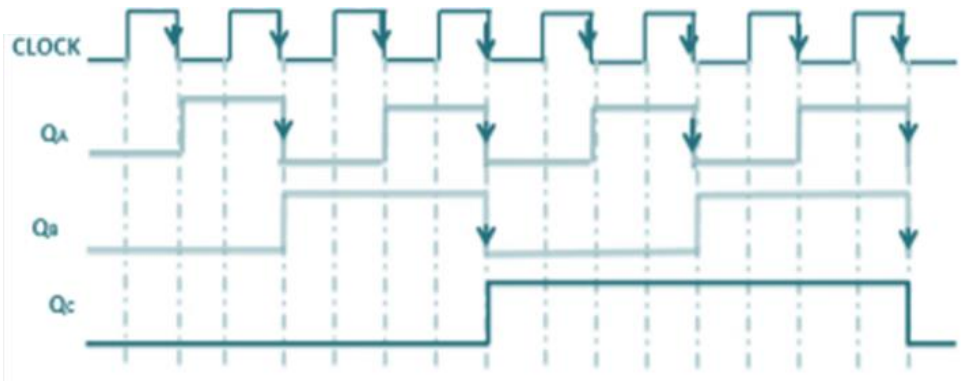
3-bit asynchronous up counter

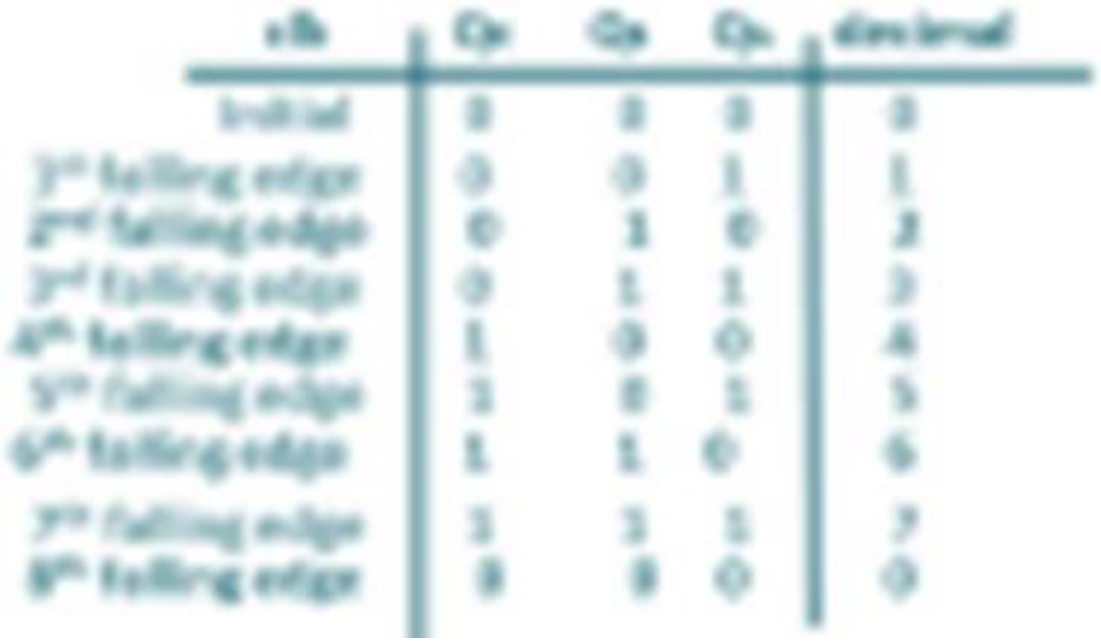




11.1 Asynchronous Up/Down Counter

3-bit asynchronous up counter

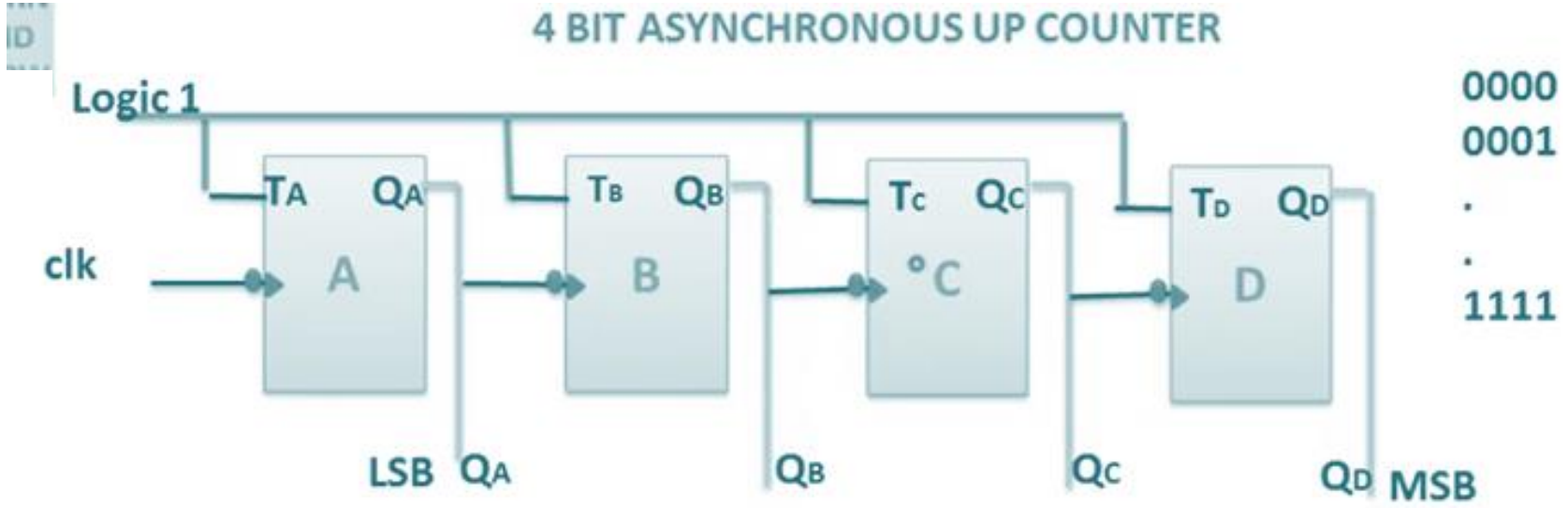




Maximum count = $2^n - 1$,
n = number of ff

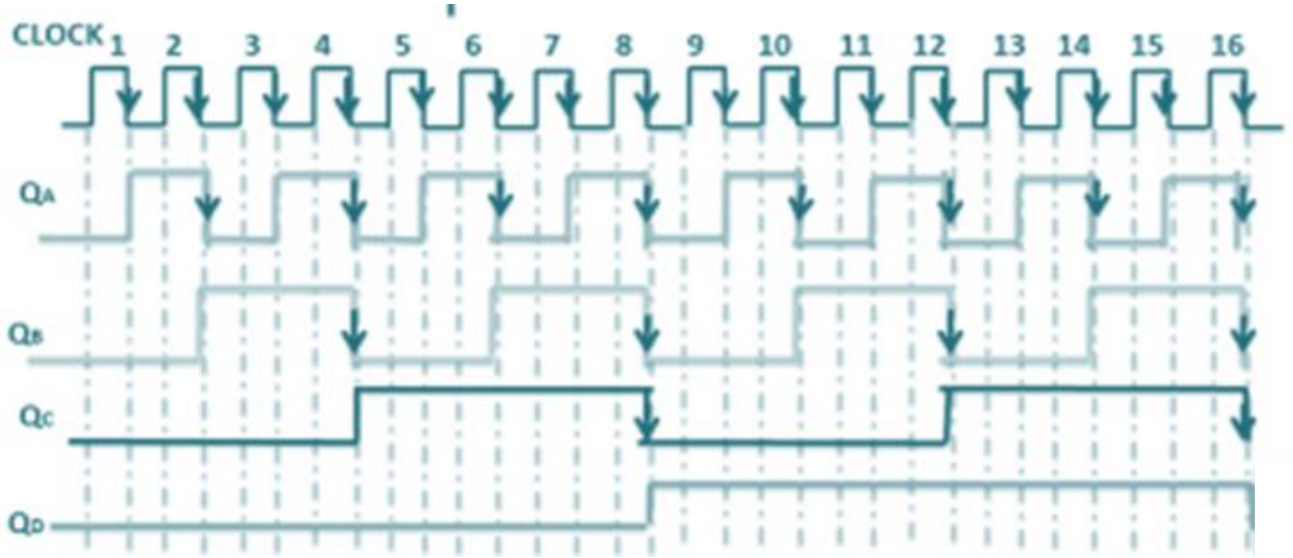
11.1 Asynchronous Up/Down Counter

4-bit asynchronous up counter



11.1 Asynchronous Up/Down Counter

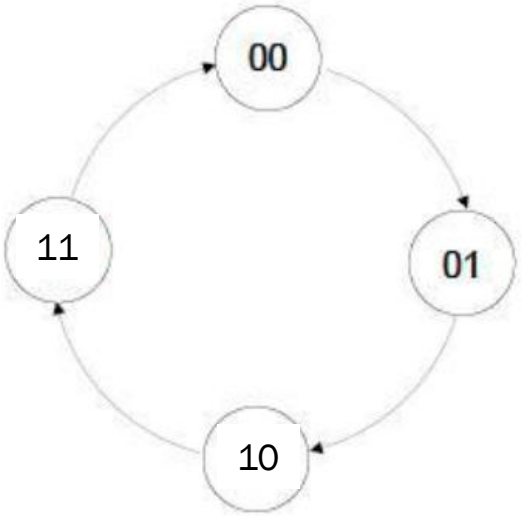
4-bit asynchronous up counter

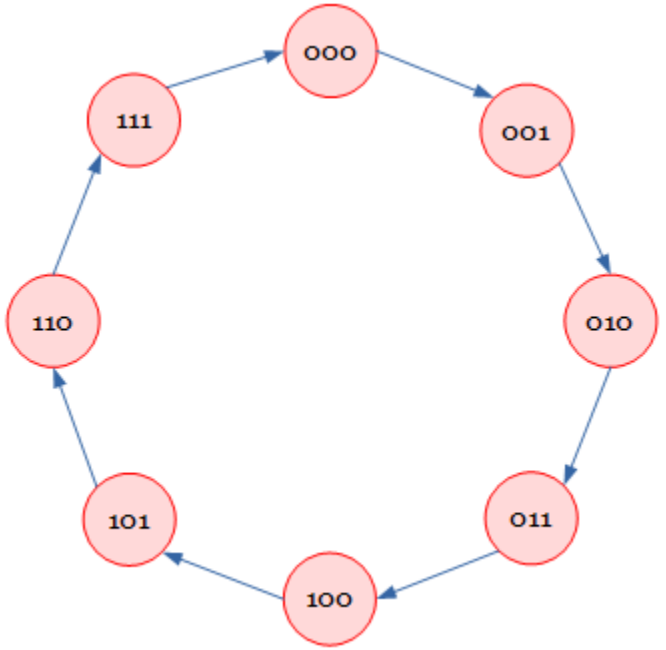


clk	Q_D	Q_C	Q_B	Q_A	decimal
Initial	0	0	0	0	0
1st falling edge	0	0	0	1	1
2nd falling edge	0	0	1	0	2
9th falling edge	1	0	0	1	9
14th falling edge	1	1	1	0	14
15th falling edge	1	1	1	1	15

11.1 Asynchronous Up/Down Counter

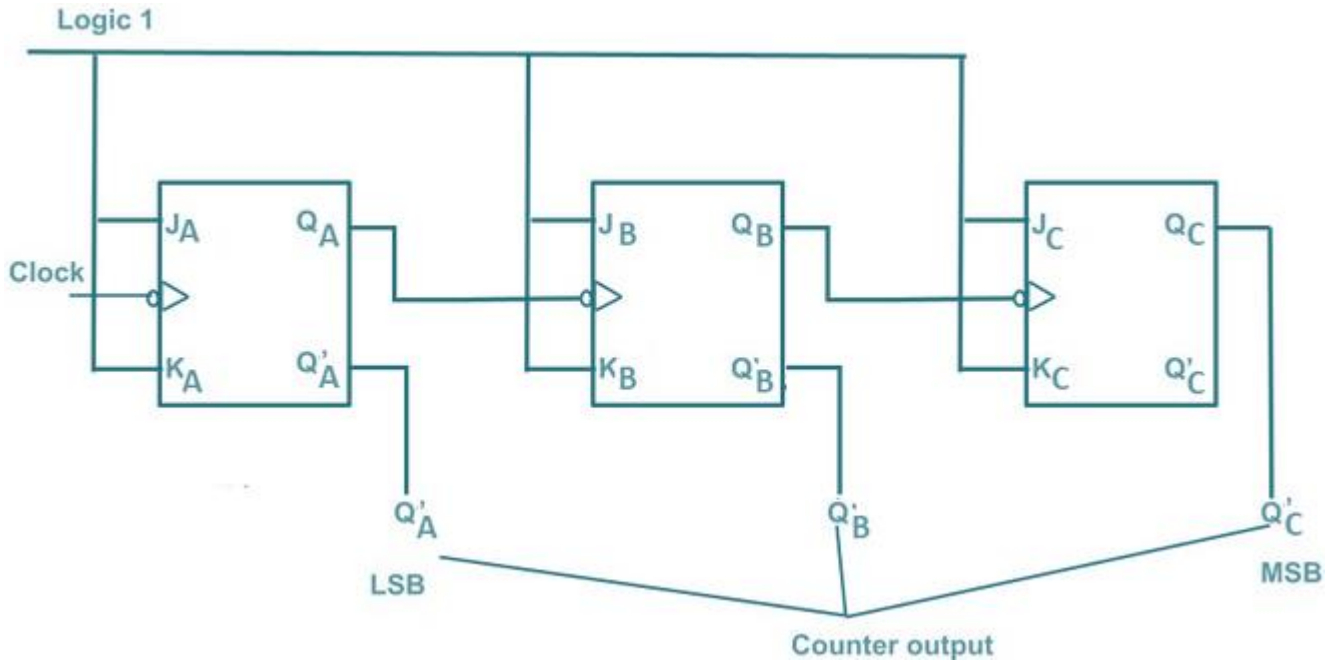
State diagram 2-bit and 3-bit up counter





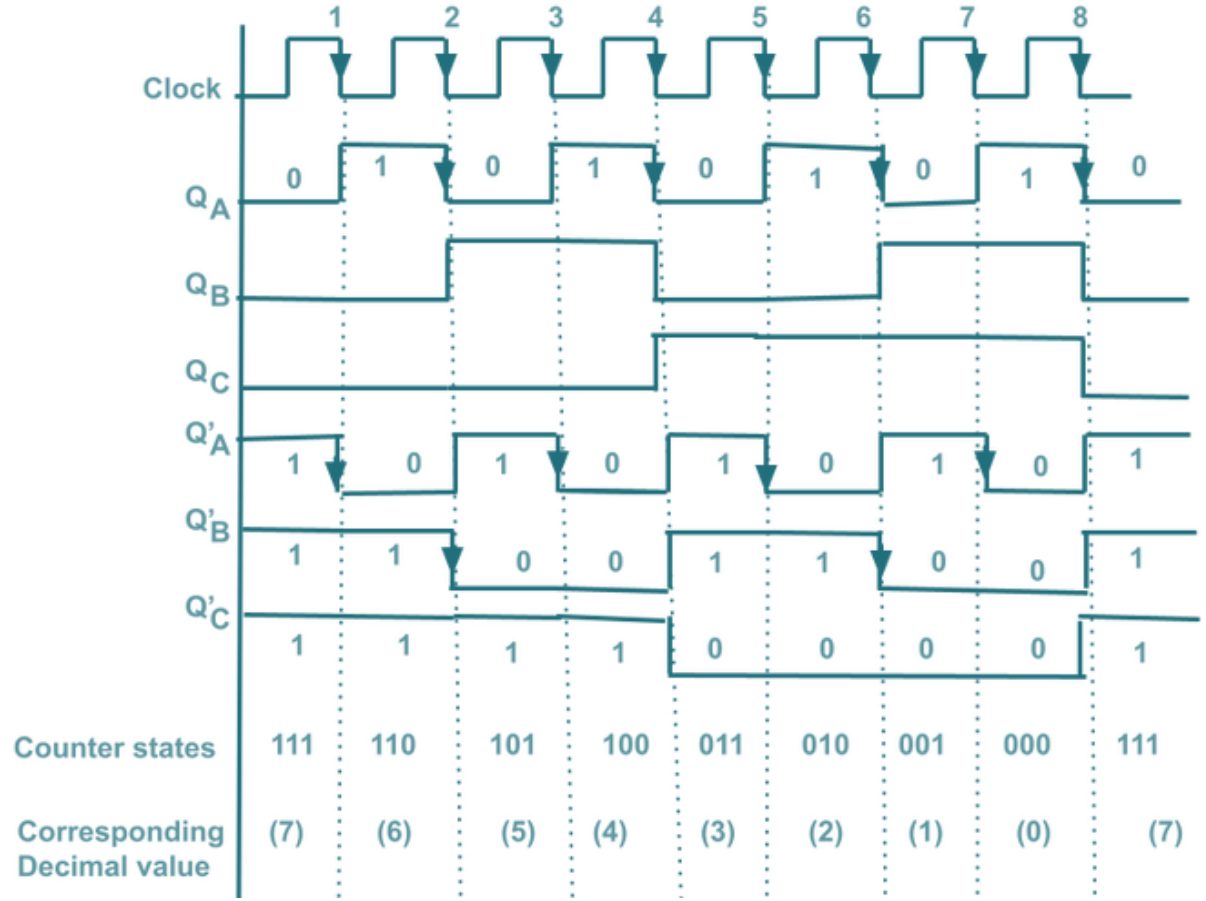
11.1 Asynchronous Up/Down Counter

3-bit Asynchronous down Counter



11.1 Asynchronous Up/Down Counter

3-bit Asynchronous down Counter



11.1 Asynchronous Up/Down Counter

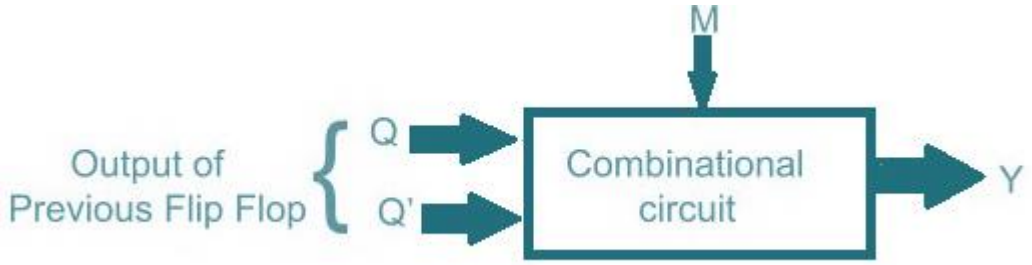
3-bit Asynchronous down Counter

Clock	Q_C	Q_B	Q_A	Q'_C	Q'_B	Q'_A
Initially	0	0	0	1	1	1
1st	0	0	1	1	1	0
2nd	0	1	0	1	0	1
3rd	0	1	1	1	0	0
4th	1	0	0	0	1	1
5th	1	0	1	0	1	0
6th	1	1	0	0	0	1
7th	1	1	1	0	0	0

11.1 Asynchronous Up/Down Counter

Asynchronous Up/Down Counter

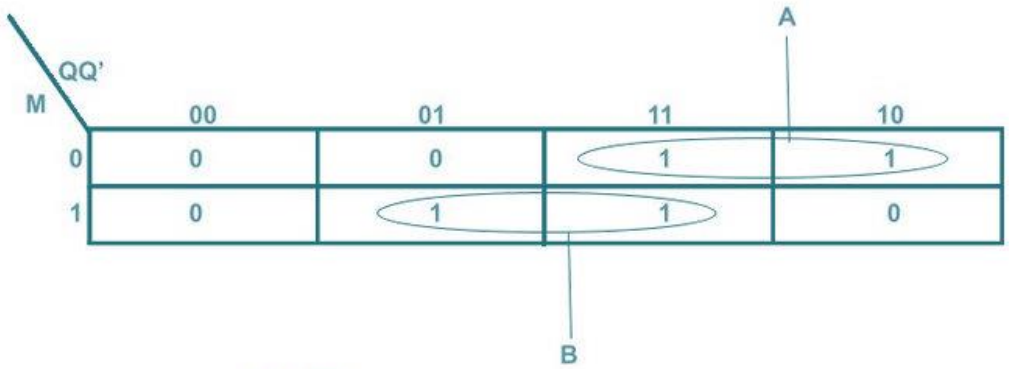
- In practice, both up and down counters are combined
- A mode control input is used to select either up or down mode
- A combinational circuit is required between each pair of flip flops



When M = 0, then Y= Q, therefore it will perform Up counting
When M = 1, then Y= Q’ therefore it will perform Down counting

11.1 Asynchronous Up/Down Counter

M	Q	Q'	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

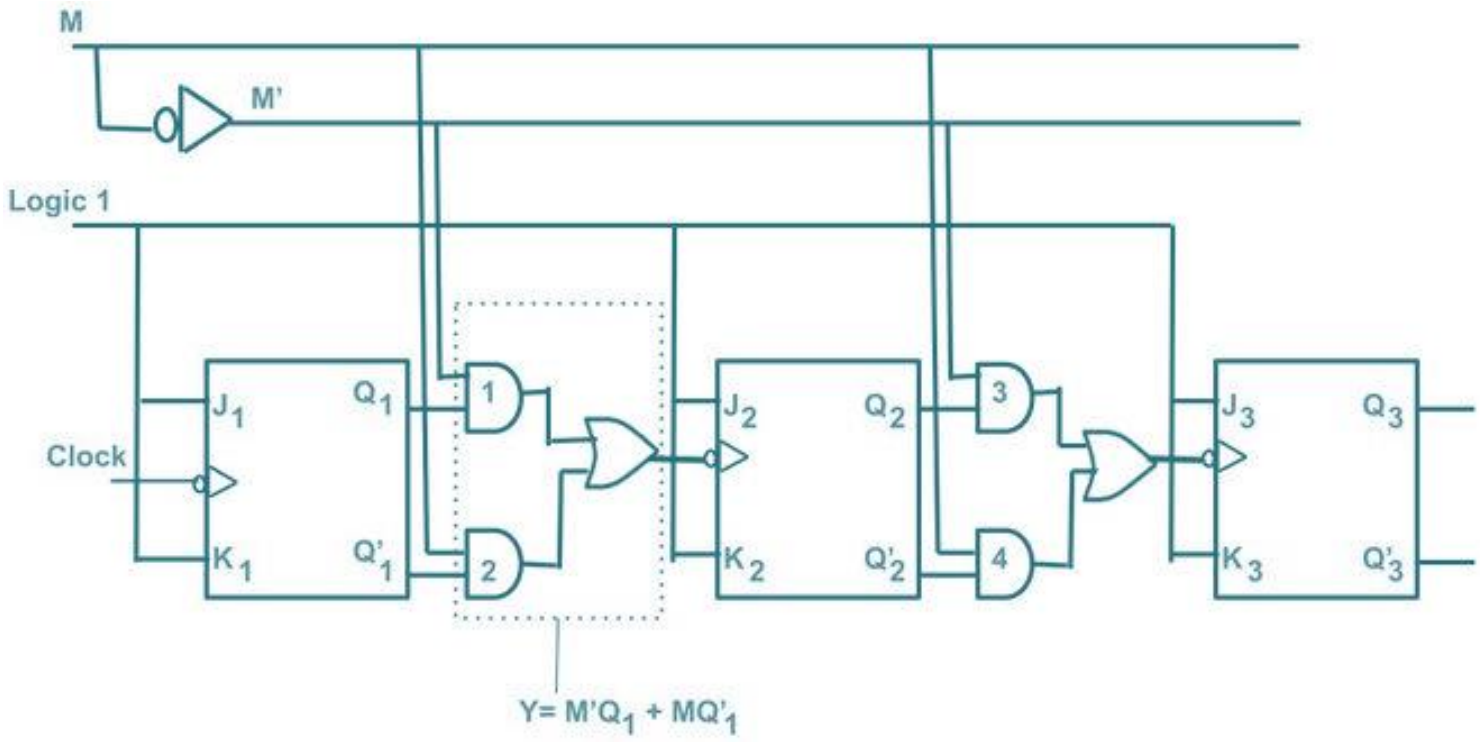


Y = A+B

Y= M'Q + MQ'

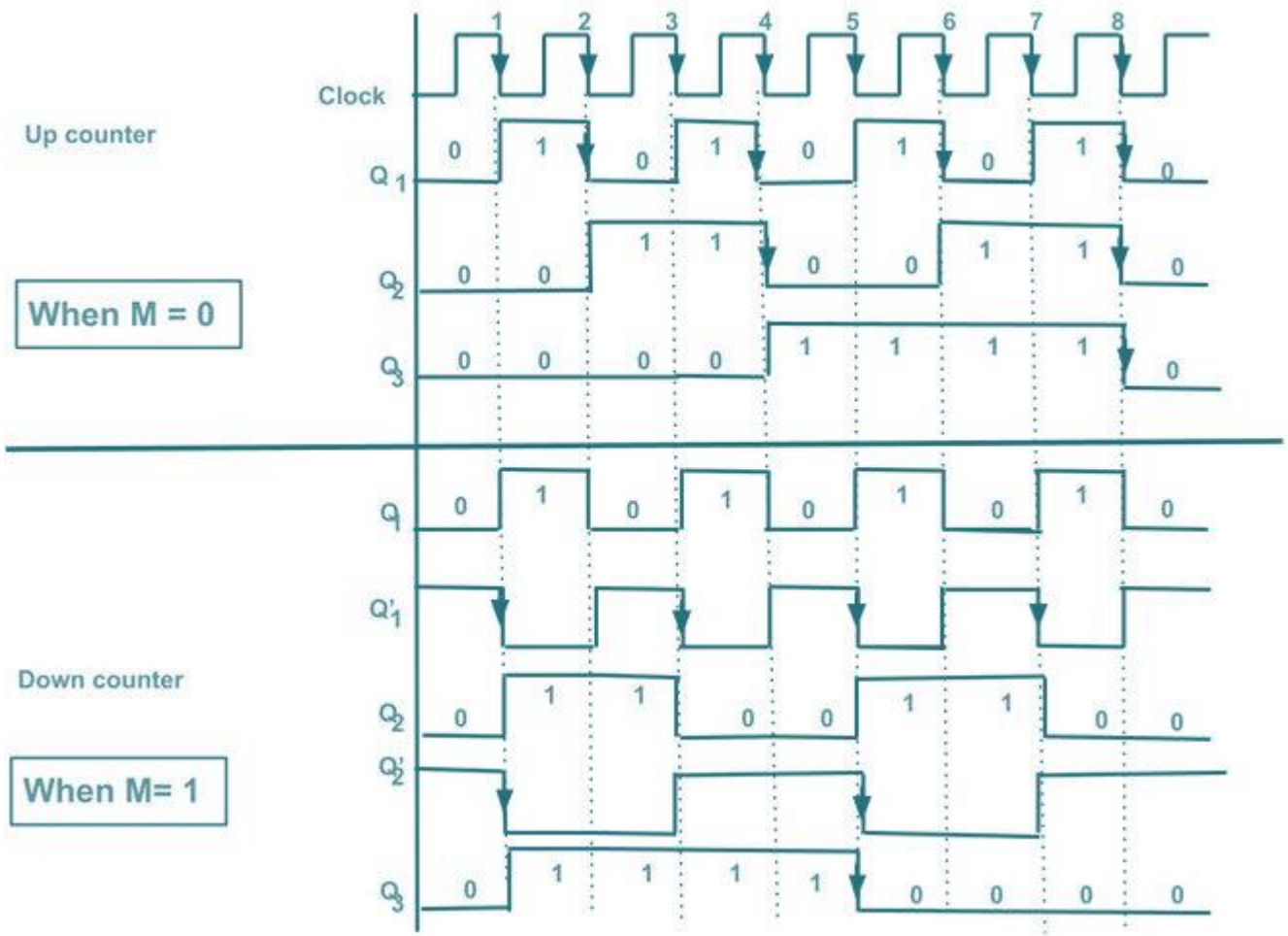
11.1 Asynchronous Up/Down Counter

Implementation of asynchronous up/down counter



11.1 Asynchronous Up/Down Counter

Timing diagram of asynchronous up/down counter



11.2 Synchronous Up/Down Counter

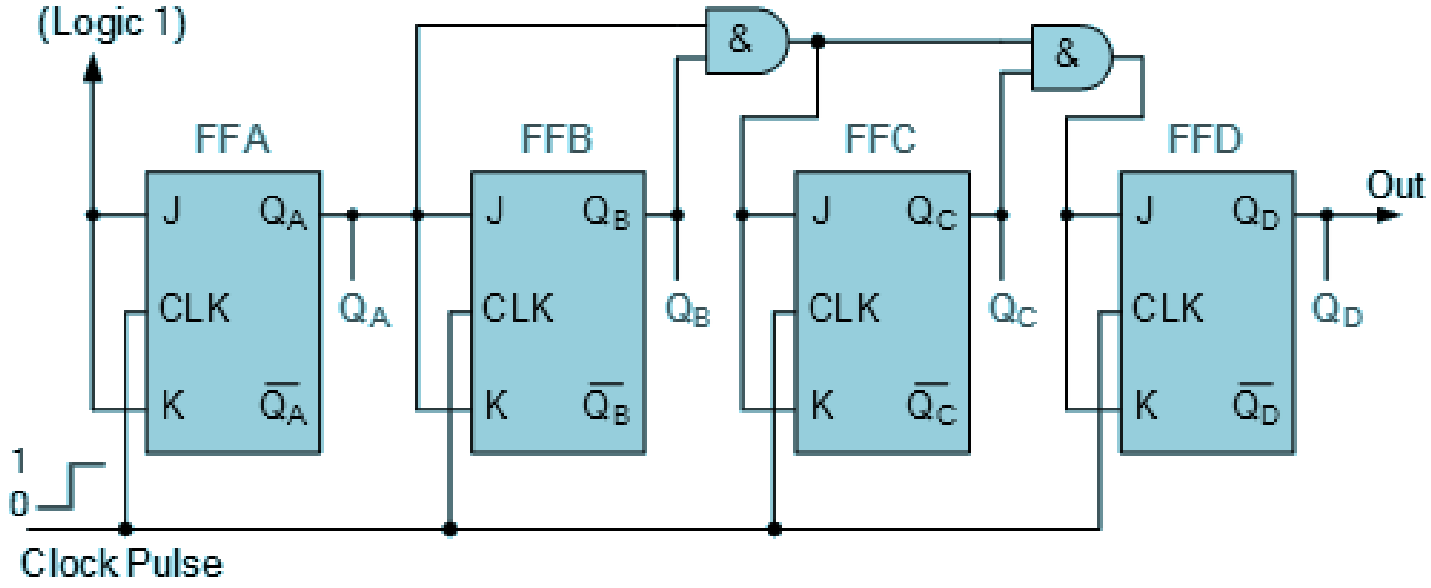
11.2 Synchronous Up/Down Counter

Synchronous counter

- There is no connection between output of first flip flops and clock of next flip flops
- Flip flops are clocked simultaneously

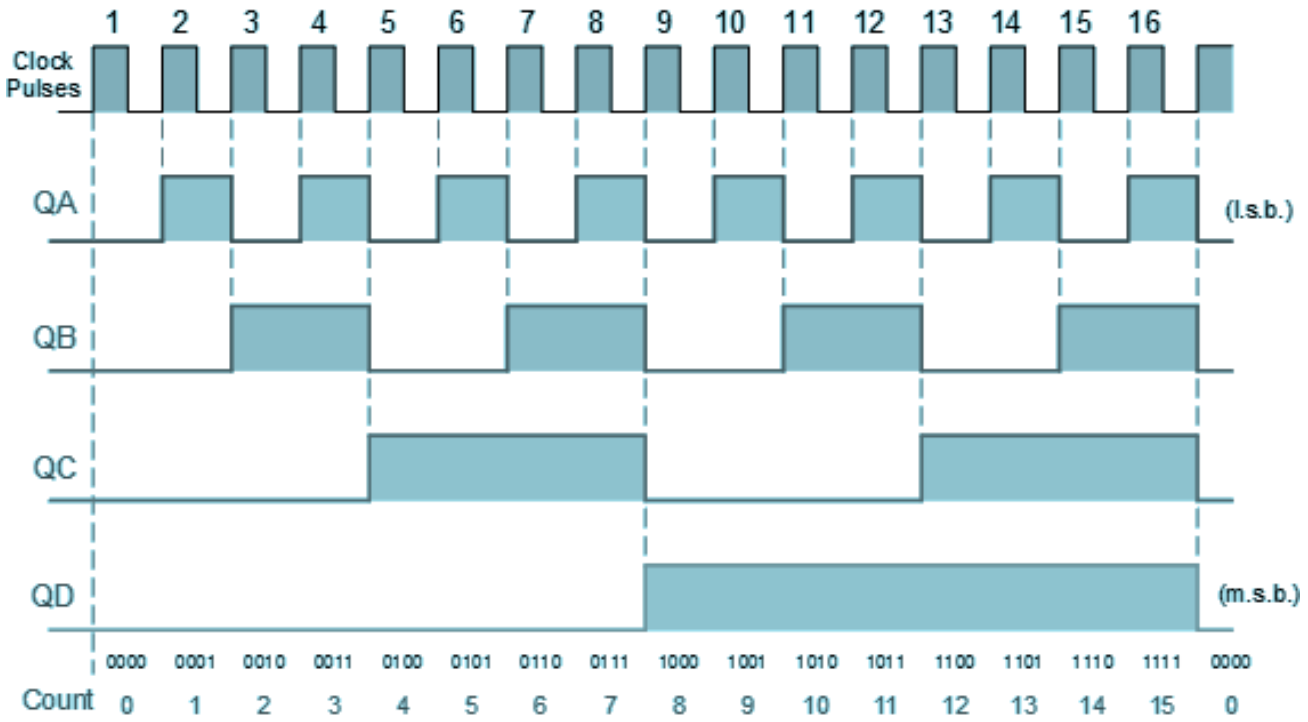
11.2 Synchronous Up/Down Counter

Example of 4-bit synchronous up counter



11.2 Synchronous Up/Down Counter

Example of 4-bit synchronous up counter



11.2 Synchronous Up/Down Counter

How to design synchronous counters

1. Decide the number of flip flops
2. Make excitation table of FF
3. Make state diagram and circuit excitation table
4. Obtain simplifies equations using K-map
5. Draw the logic diagram

11.2 Synchronous Up/Down Counter

Example.

Design 2-bit synchronous up counter using JK flip flop

Step 1. Decide the number of flip flops

2-bit → 2 flip flops

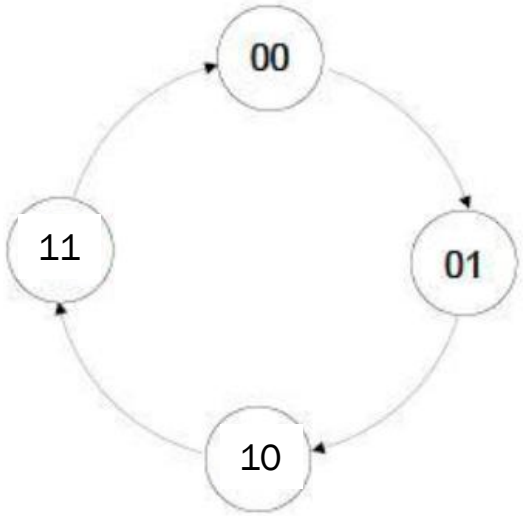
11.2 Synchronous Up/Down Counter

Step 2. Make excitation table of FF

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

11.2 Synchronous Up/Down Counter

Step 3. Make state diagram and circuit excitation table

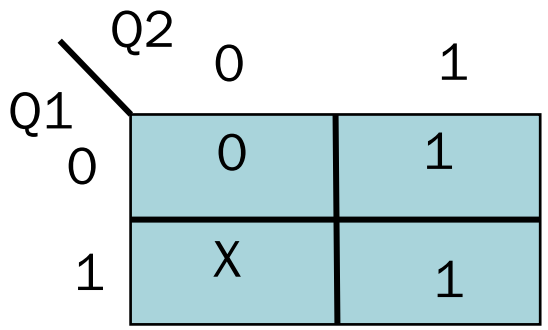


PS		NS					
Q1	Q2	Q1*	Q2*	J1	K1	J2	K2
0	0	0	0	0	X	1	X
0	1	0	1	1	X	X	1
1	0	1	0	X	0	1	X
1	1	1	1	X	1	X	1

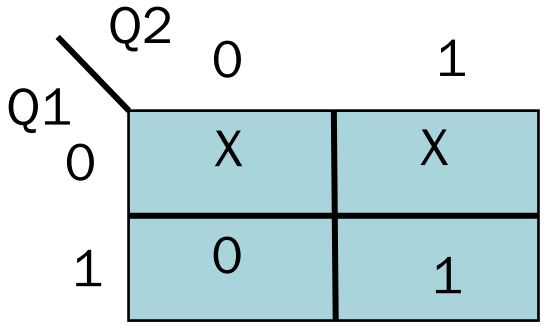
Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

11.2 Synchronous Up/Down Counter

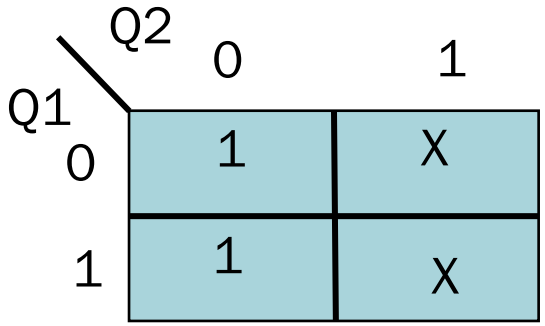
Step 4. Obtain simplifies equations using K-map



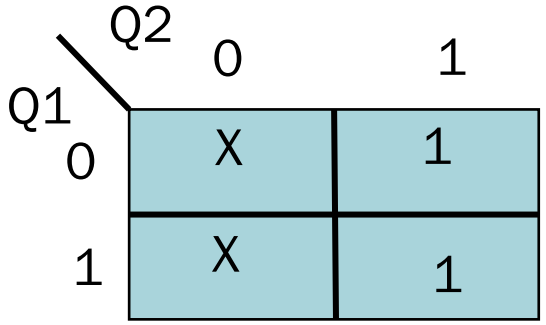
J1=Q2



K1=Q2



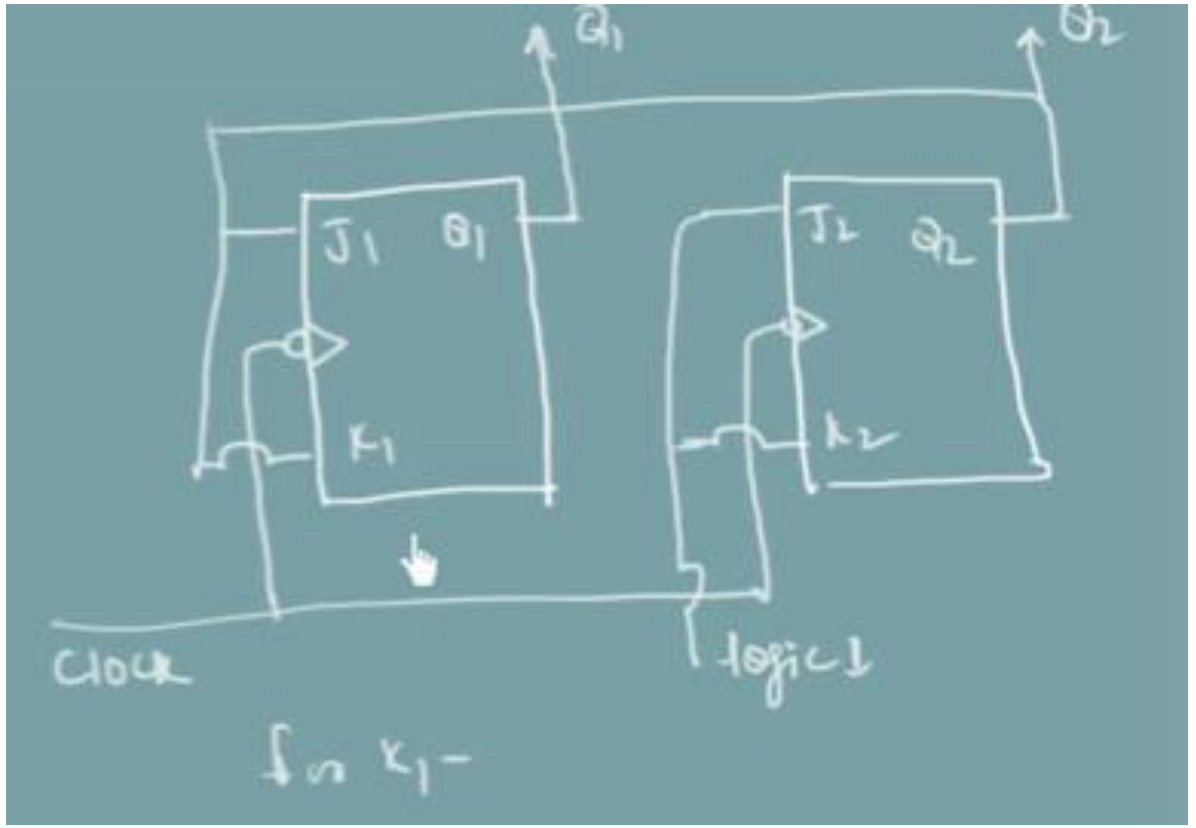
J2=1



K2=1

11.2 Synchronous Up/Down Counter

Step 5. Draw the logic diagram



11.2 Synchronous Up/Down Counter

Example.

Design 3-bit synchronous up counter using T flip flop

Step 1. Decide the number of flip flops

3-bit → 3 flip flops

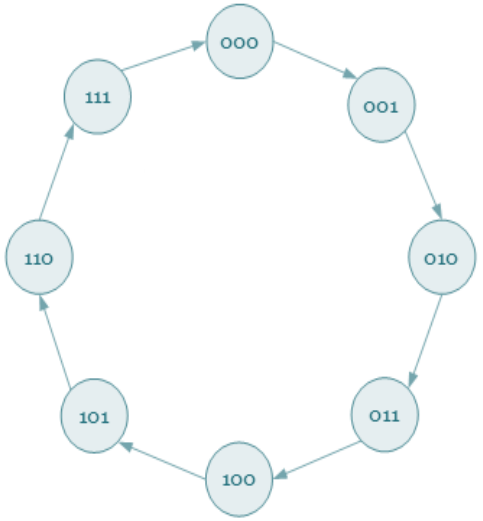
11.2 Synchronous Up/Down Counter

Step 2. Make excitation table of FF

Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0

11.2 Synchronous Up/Down Counter

Step 3. Make state diagram and circuit excitation table

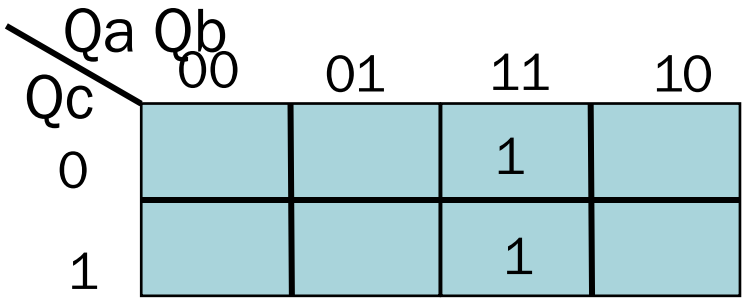


Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0

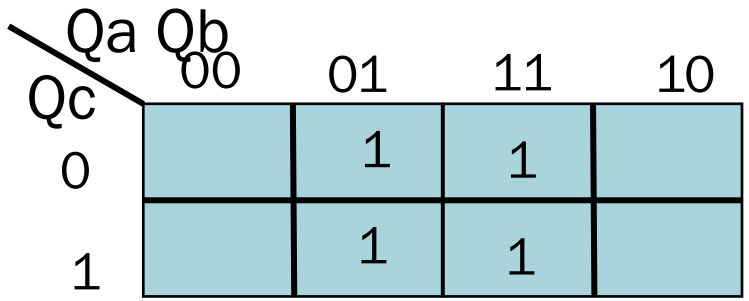
PS			NS					
Qc	Qb	Qc	Qc*	Qb*	Qa*	Tc	Tb	Ta
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

11.2 Synchronous Up/Down Counter

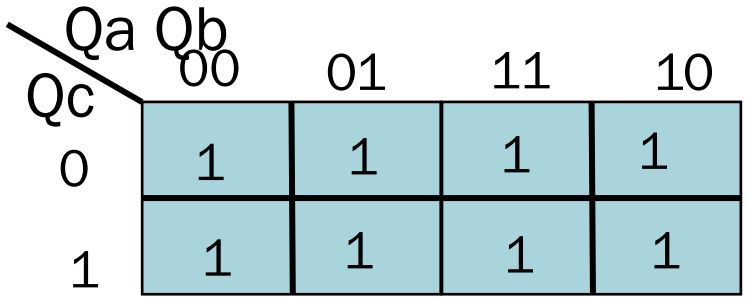
Step 4. Obtain simplifies equations using K-map



Tc = Qb Qa



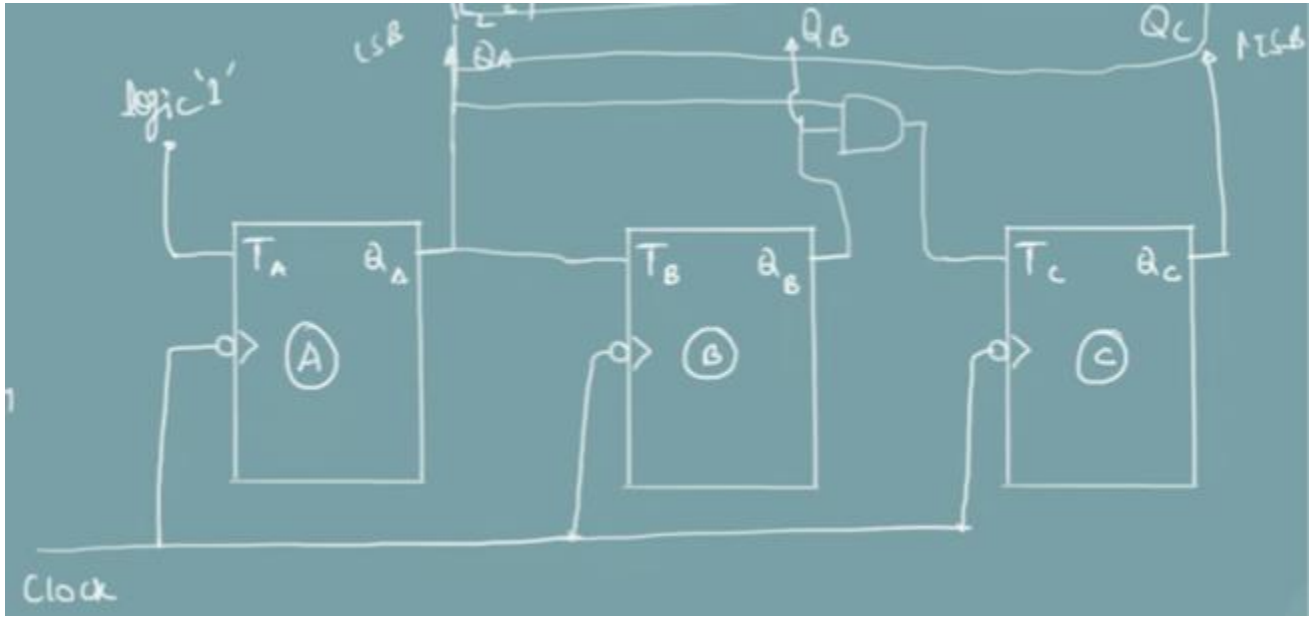
Tb = Qa



Ta = 1

11.2 Synchronous Up/Down Counter

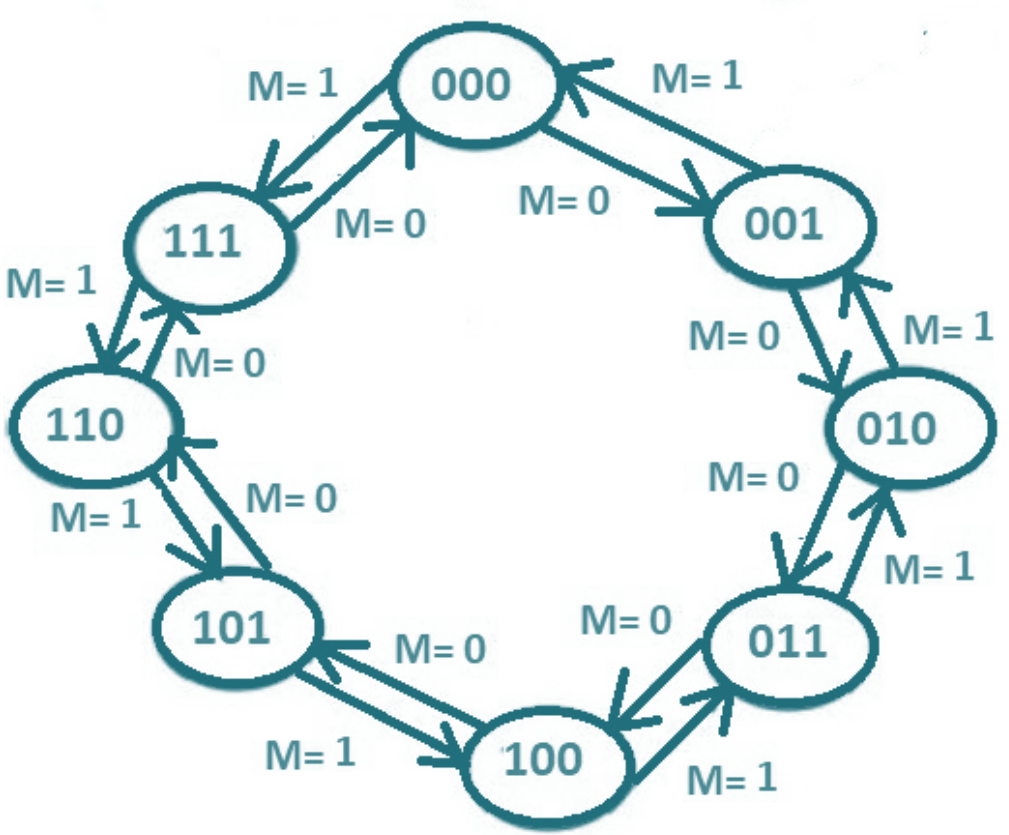
Step 5. Draw the logic diagram



11.2 Synchronous Up/Down Counter

3-bit synchronous up/down counter

- When M=0 ,then the counter will perform up counting
- When M=1 ,then the counter will perform down counting



11.2 Synchronous Up/Down Counter

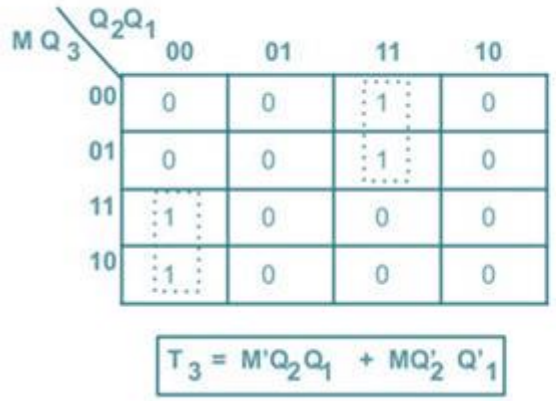
Circuit excitation table for 3-bit synchronous up/down counter

M	Q_3	Q_2	Q_1	Q_3^*	Q_2^*	Q_1^*	T_3	T_2	T_1
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1

M	Q_3	Q_2	Q_1	Q_3^*	Q_2^*	Q_1^*	T_3	T_2	T_1
1	0	0	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	0	1	0	0	0	1

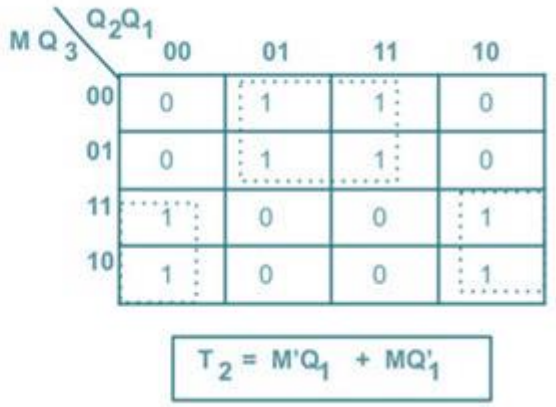
11.2 Synchronous Up/Down Counter

Simplified equation



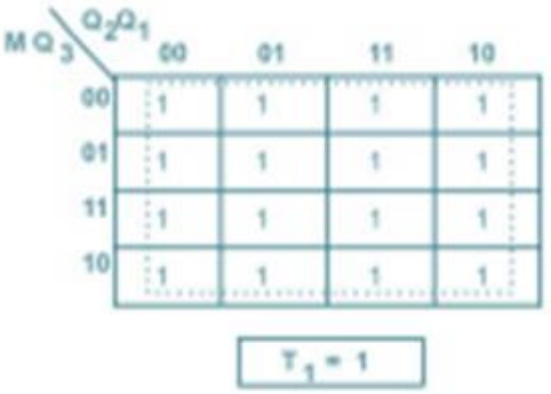
MQ_3 \ Q_2Q_1	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	1	0	0	0
10	1	0	0	0

$T_3 = M'Q_2Q_1 + MQ'_2Q'_1$



MQ_3 \ Q_2Q_1	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

$T_2 = M'Q_1 + MQ'_1$

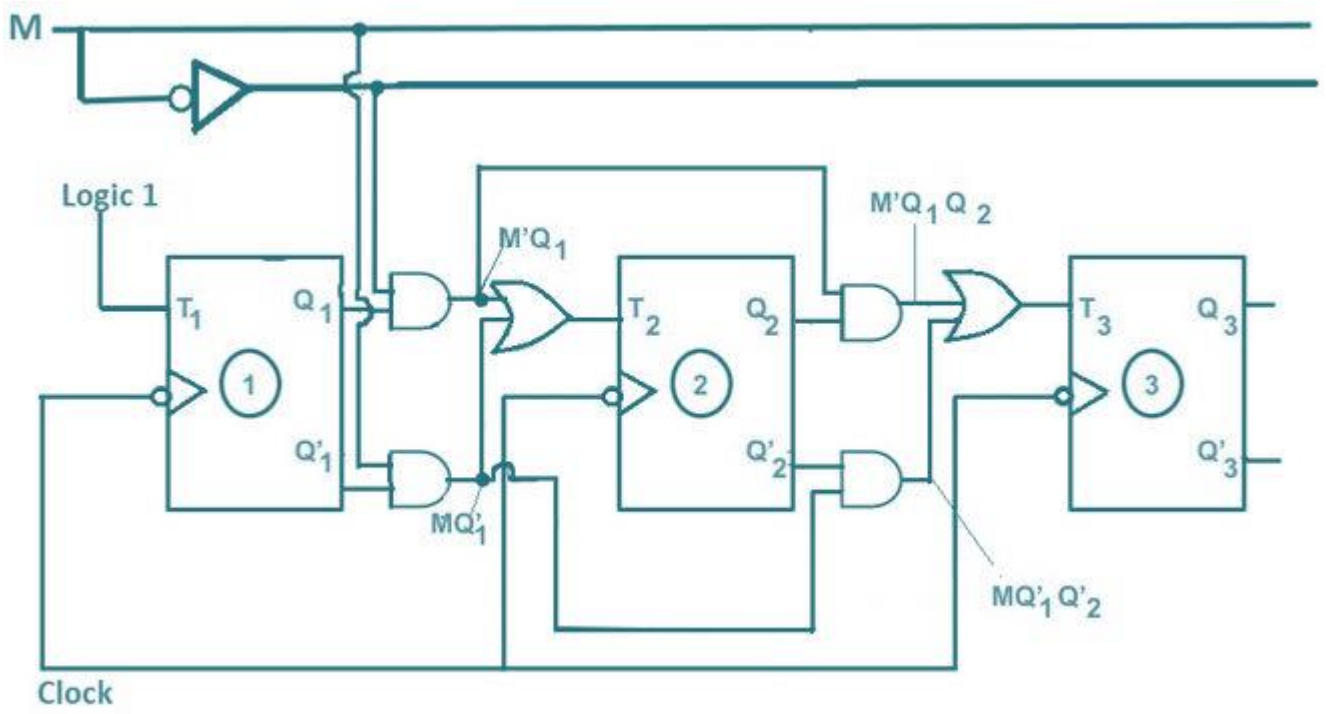


MQ_3 \ Q_2Q_1	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$T_1 = 1$

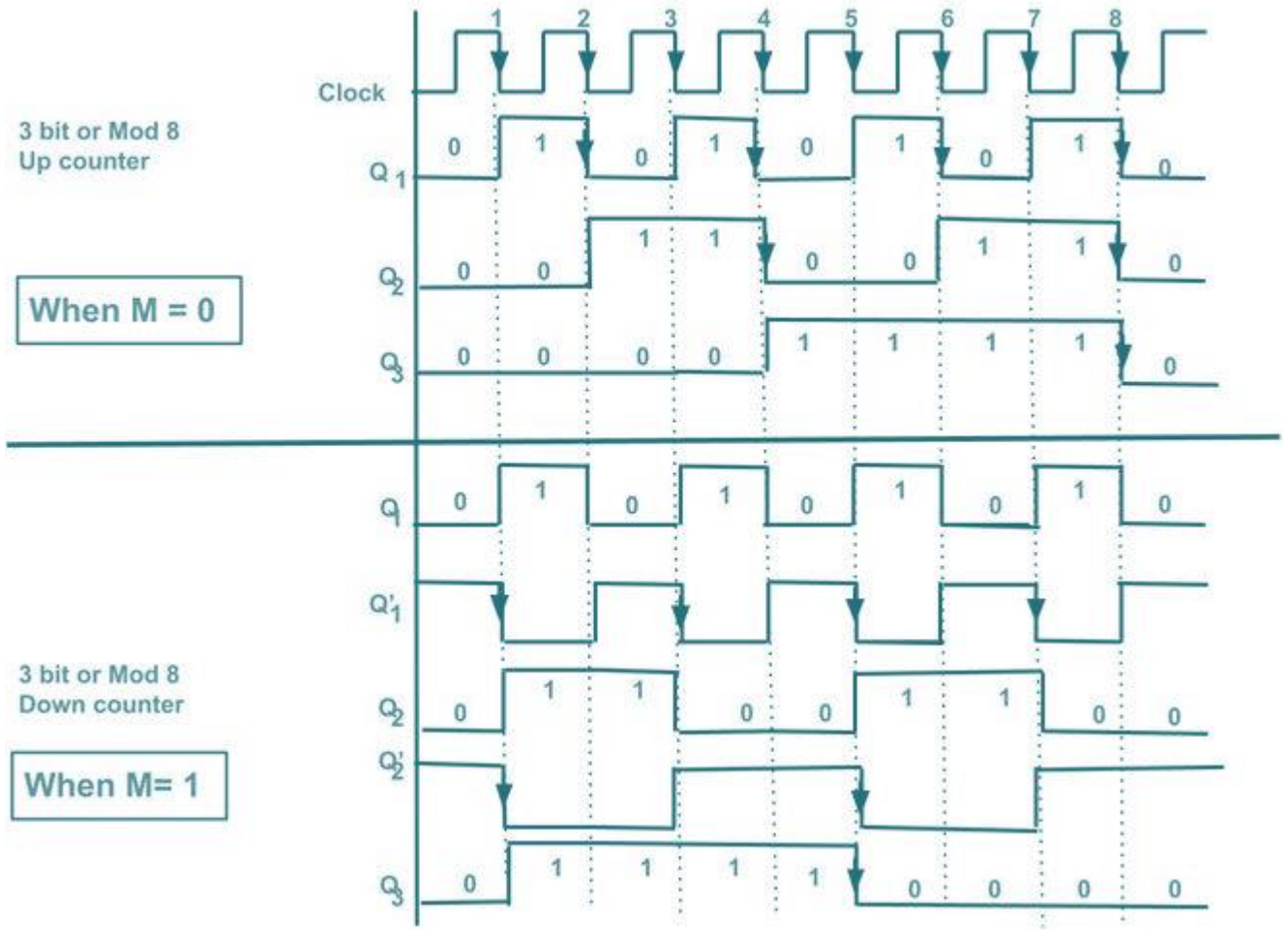
11.2 Synchronous Up/Down Counter

Circuit diagram for 3-bit synchronous up/down counter



11.2 Synchronous Up/Down Counter

Timing diagram for 3-bit synchronous up/down counter



11.2 Synchronous Up/Down Counter

Modulus of counter

- 2-bit ripple counter is called as MOD-4 or modulus 4 counter
- 3-bit ripple counter is called as MOD-8 counter
- Modulus → represent the number of state
- MOD also can be used to counting to particular values

11.2 Synchronous Up/Down Counter

Example.

Design MOD-5 counter using JK Flip flops

Number of States : 5

maximum count : 5 - 1 = 4 (0-4)

11.2 Synchronous Up/Down Counter

Step 1. Decide the number of flip flops

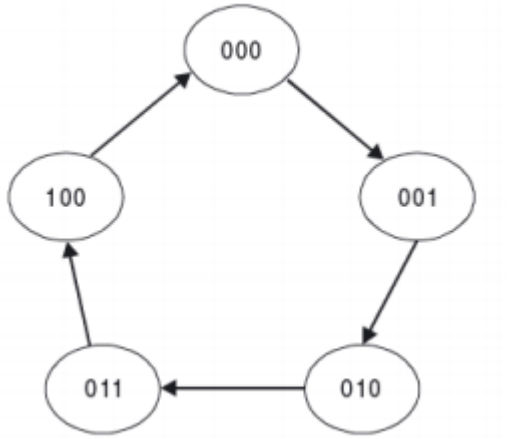
5 state → 3-bit → 3 flip flops

Step 2. Make excitation table of FF

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

11.2 Synchronous Up/Down Counter

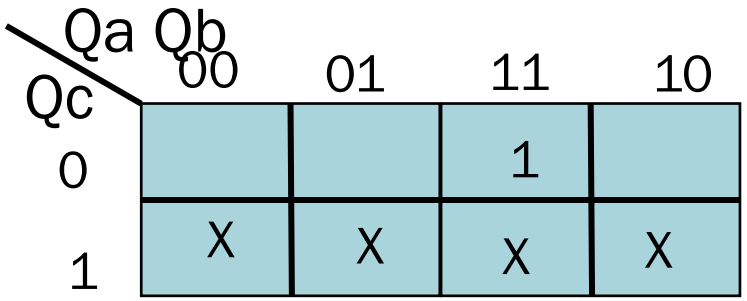
Step 3. Make state diagram and circuit excitation table



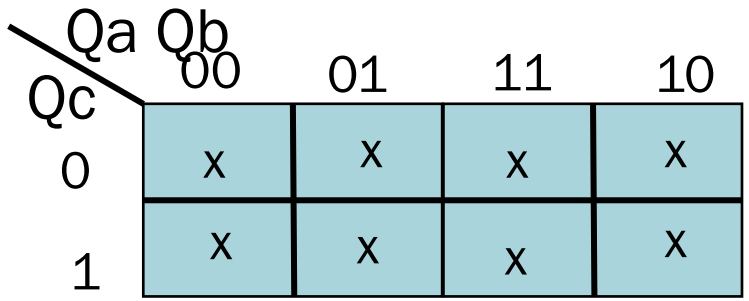
PS			NS								
Qc	Qb	Qa	Qc*	Qb*	Qa*	Jc	Kc	Jb	Kb	Ja	Ka
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	x	1	0	X	0	X
1	0	1	x	x	x	x	x	x	X	X	X
1	1	0	x	x	x	x	x	x	X	X	X
1	1	1	x	x	x	x	x	x	X	X	X

11.2 Synchronous Up/Down Counter

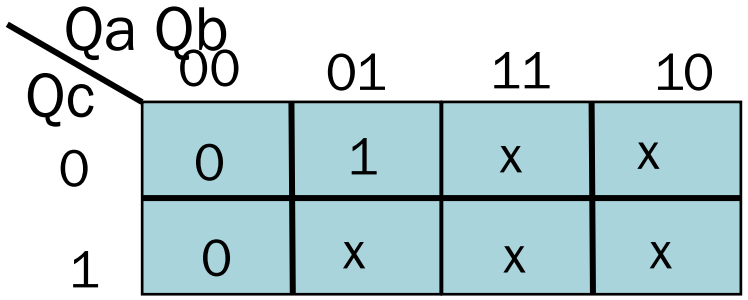
Step 4. Obtain simplifies equations using K-map



Jc = Qb Qa



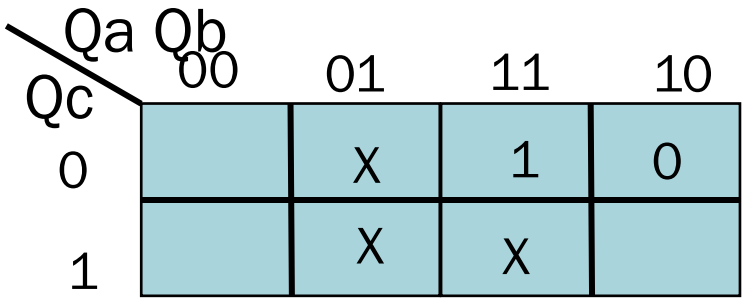
Kc = 1



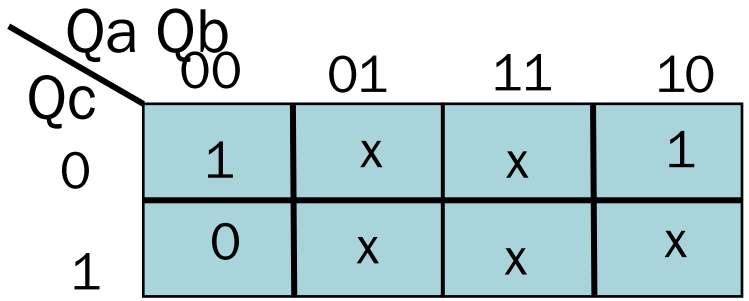
Jb = Qa

11.2 Synchronous Up/Down Counter

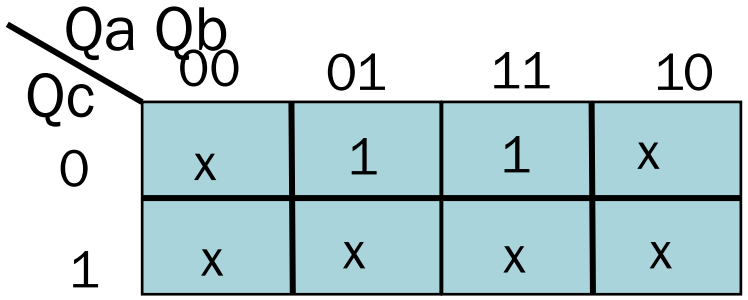
Step 4. Obtain simplifies equations using K-map



Kb = Qa



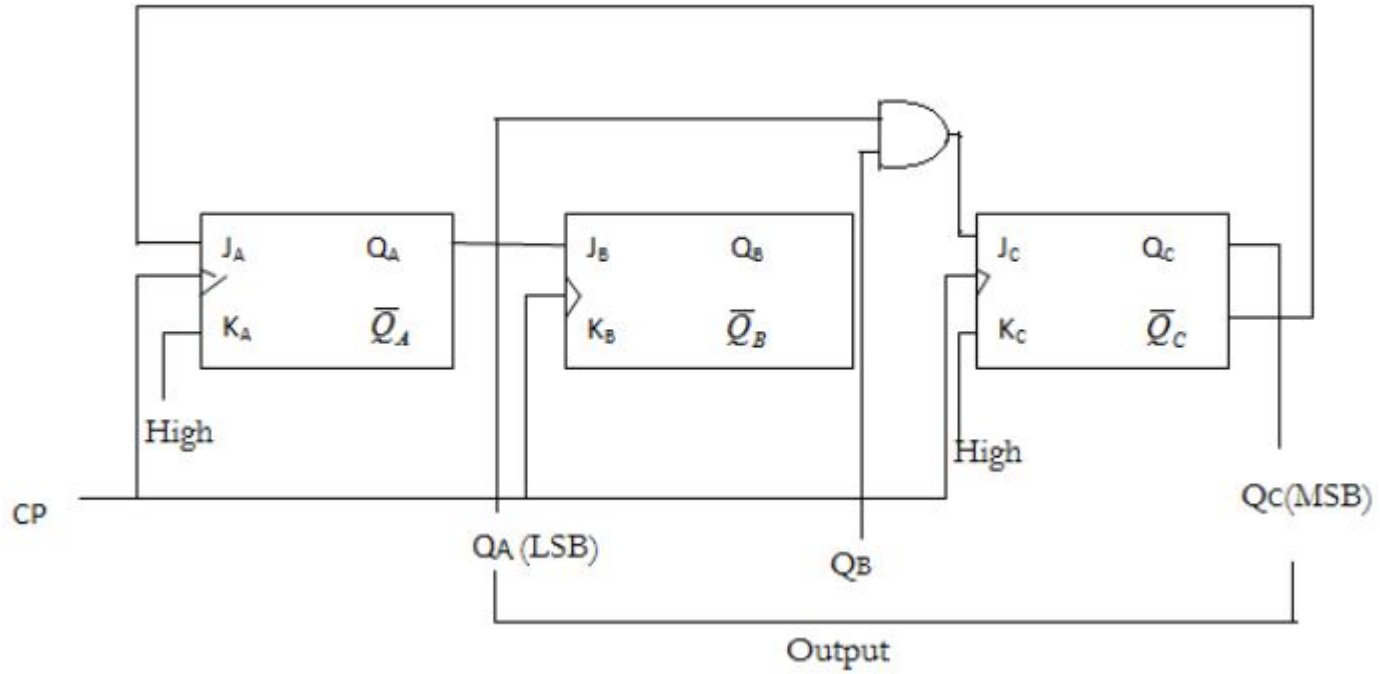
Ja =Qc'



Ka = 1

11.2 Synchronous Up/Down Counter

Step 5. Draw the logic diagram



11.3 Basic Register

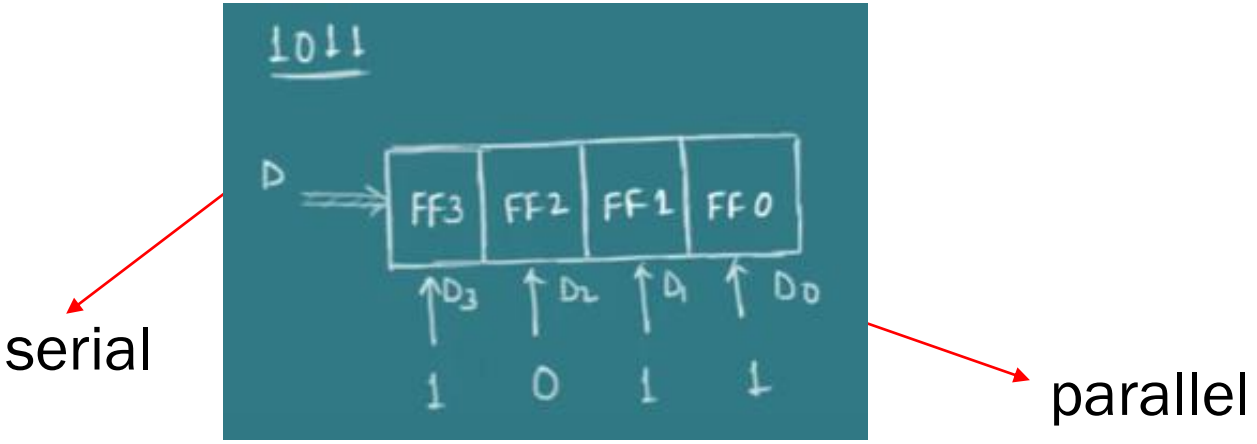
11.3 Basic Register

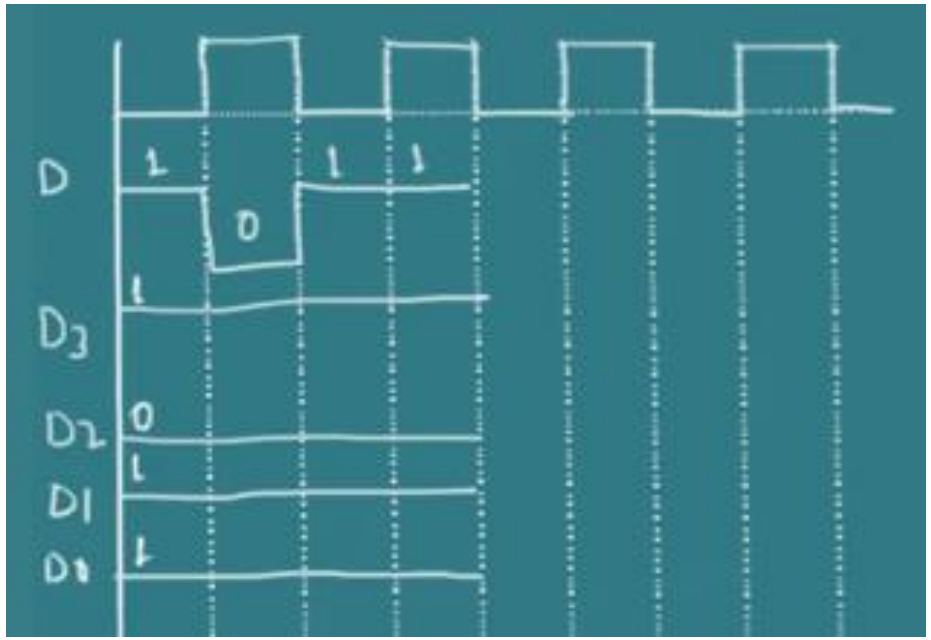
- A Register is a collection of flip flops.
- A flip flop is used to store single bit digital data
- For storing a large number of bits, the storage capacity is increased by grouping more than one flip flops.
- If we want to store an n-bit word, we have to use an n-bit register containing n number of flip flops.

11.3 Basic Register

DATA FORMAT

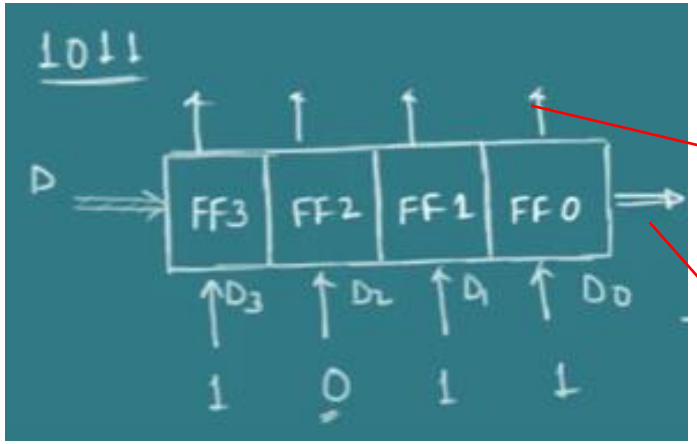
- Data in register can be entered in serial (one bit at a time) or in parallel form (all bits at a time)





11.3 Basic Register

- Data can also be extracted in serial (temporal code) or in parallel (special code) form



parallel

serial

11.3 Basic Register

CLASSIFICATION

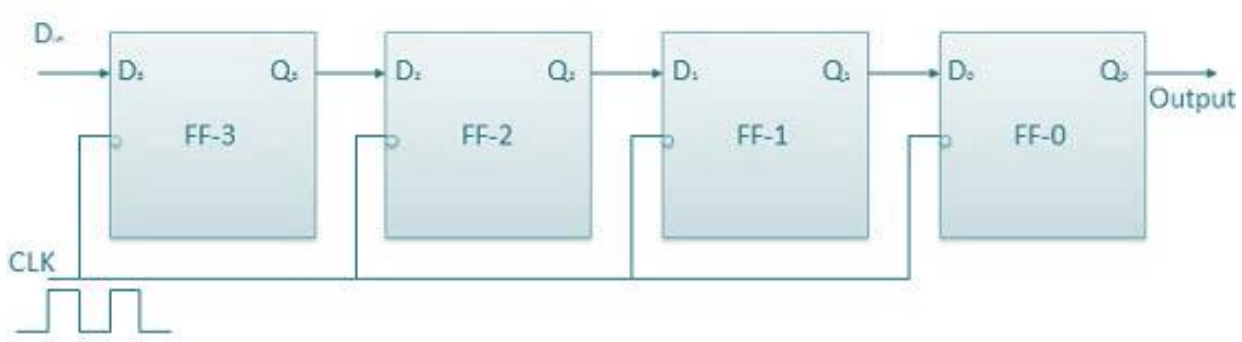
- Depending on Application the classification are
  - Shift Register
  - Storage Register
- Depending on Input and Output, the classification are
  - Serial In Serial Out Register (SISO)
  - Serial In Parallel Out Register (SIPO)
  - Parallel In Serial Out Register (PISO)
  - Parallel In parallel Out Register (PIPO)

11.3 Basic Register

SHIFT REGISTER

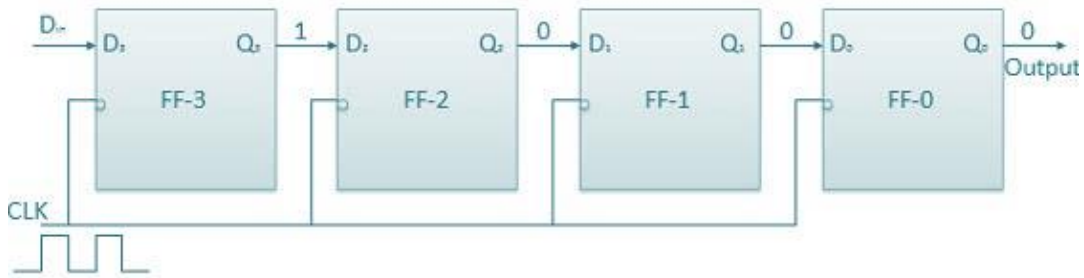
- A sequential circuit which used to data storage, data transfer and certain of arithmetic and logic operation

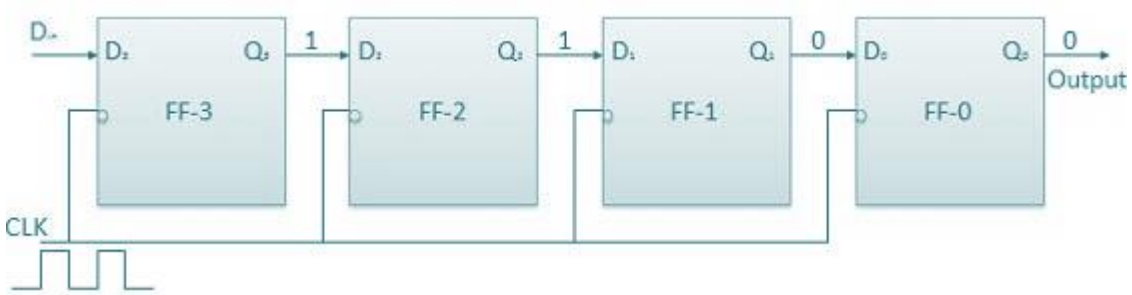
SISO

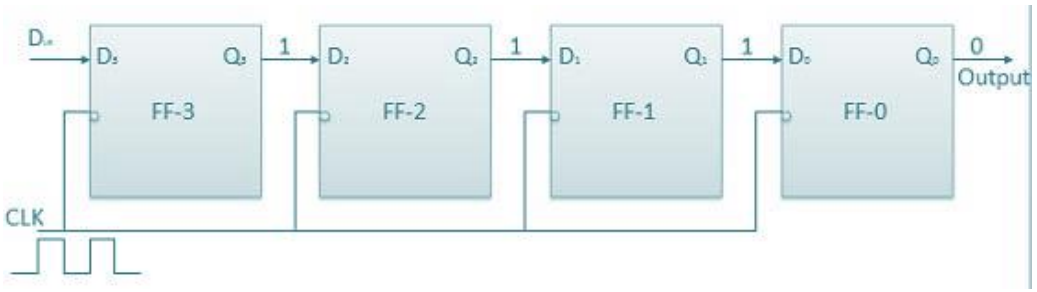


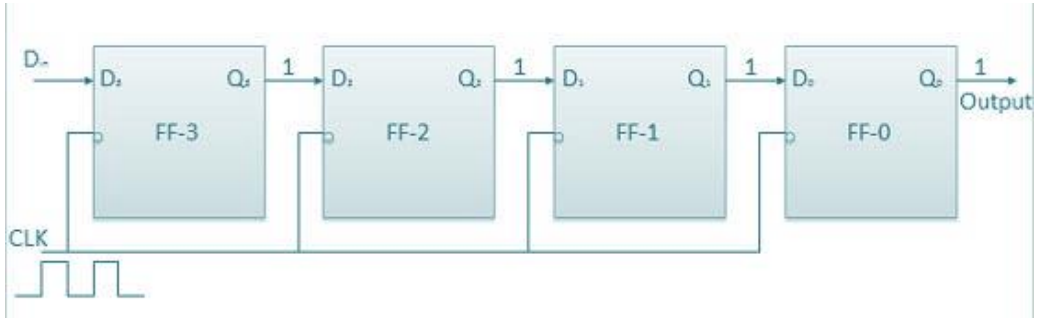
11.3 Basic Register

SISO OPERATION







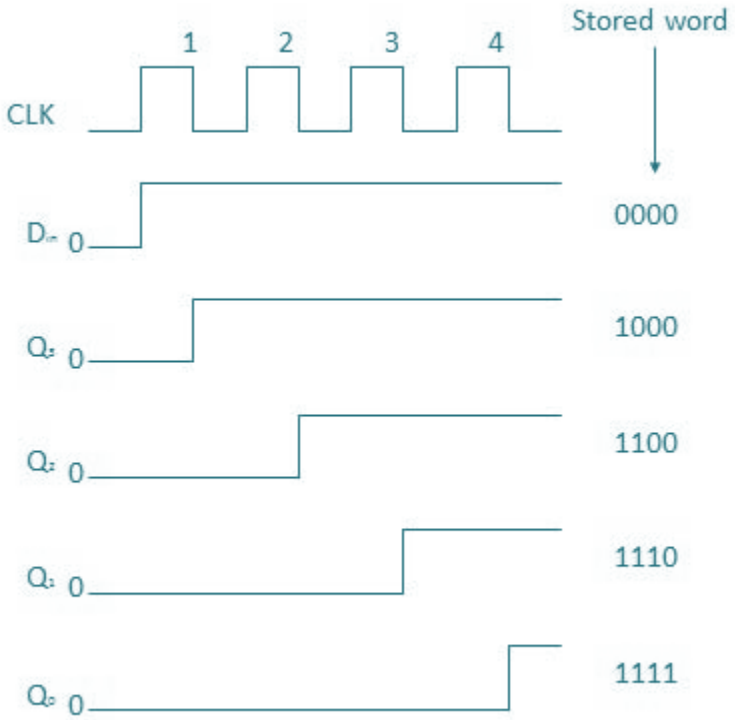


11.3 Basic Register

SISO Truth table and waveform

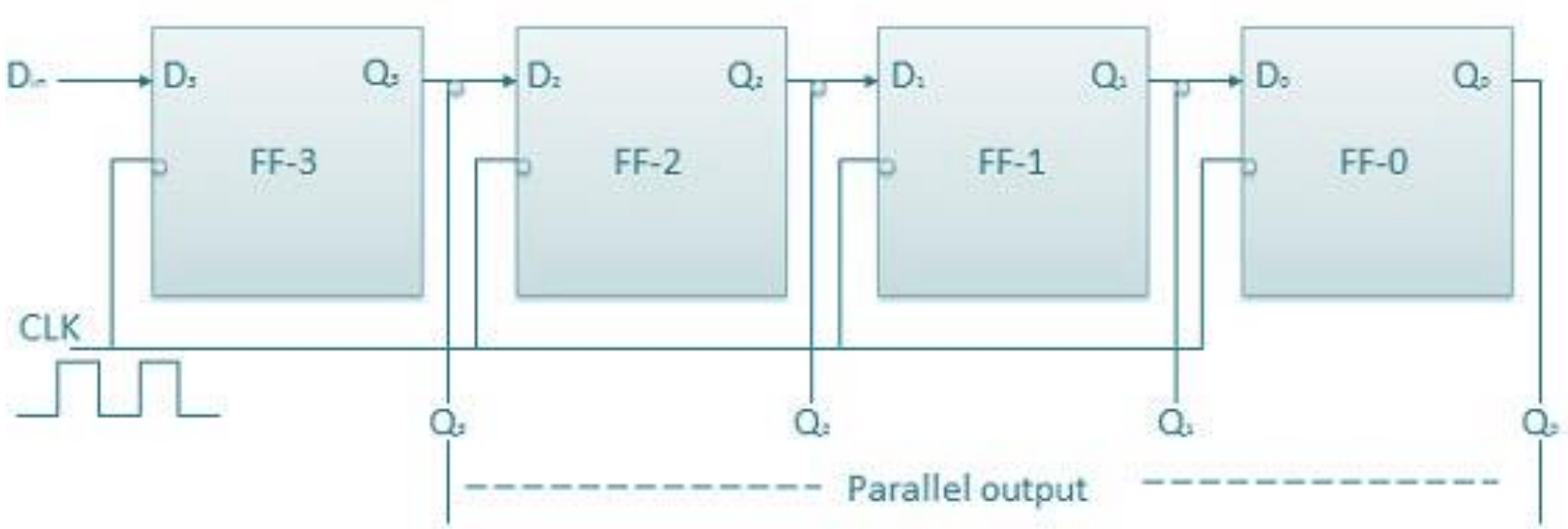
	CLK	$D_{in} = Q_3$	$Q_3 = D_2$	$Q_2 = D_1$	$Q_1 = D_0$	Q_0
Initially			0	0	0	0
(i)	↓	1	1	0	0	0
(ii)	↓	1	1	1	0	0
(iii)	↓	1	1	1	1	0
(iv)	↓	1	1	1	1	1

→ Direction of data travel



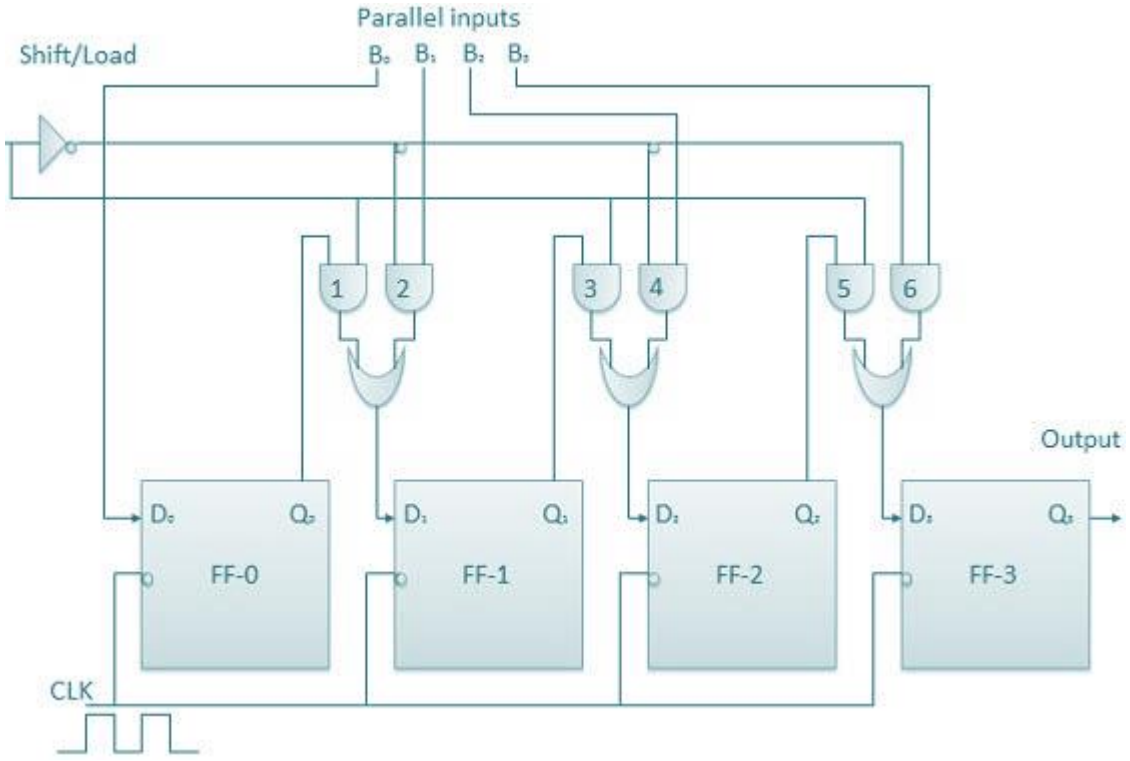
11.3 Basic Register

SIPO



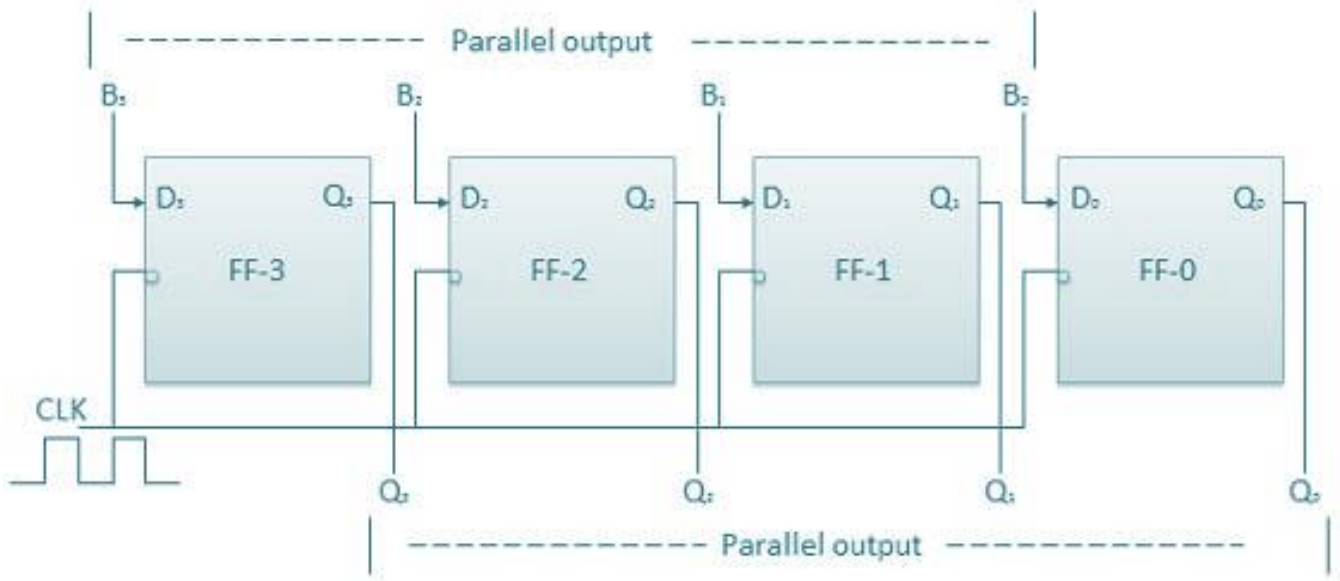
11.3 Basic Register

PISO



11.3 Basic Register

PIPO



References

M. Morris Mano, Digital Design, 5th ed, Prentice Hall, 2012, **Chapter 5**

Next Topic : Implementation of Combinational Circuit