CE232 DIGITAL SYSTEM

Topic 8. Basic Sequential Circuit and Flip-Flop

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Subtopic

8.1 Block Diagram Sequential Circuit

8.2 Basic Latch

8.3 Flip Flop Circuit

8.4 RS Flip Flop

8.5 Clock SR Flip Flop

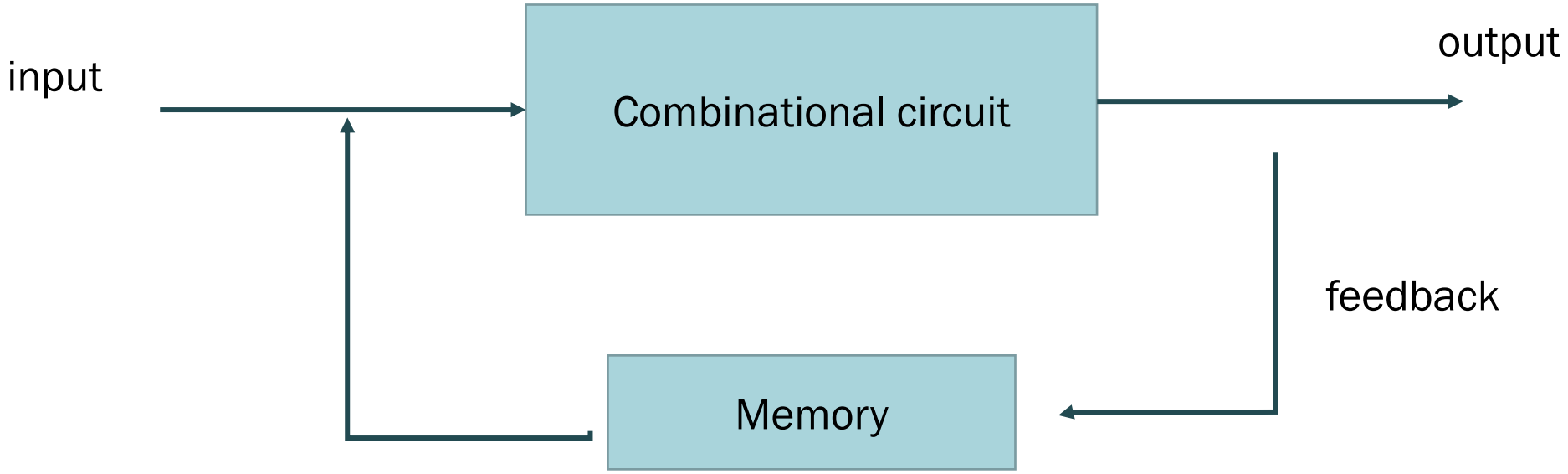
8.1 Block Diagram Sequential Circuit

8.1 Block Diagram Sequential Circuit

- **Sequential circuit** is a combinational circuit with memory
- The output of sequential circuit depends upon present inputs and present state (past output)
- The information stored in sequential circuit represents present state
- The present state and present inputs will define output and next state

8.1 Block Diagram Sequential Circuit

Block Diagram



8.2 Basic Latch

8.2 Basic Latch

- There are two types of memory elements based on the type of triggering that is suitable to operate it.
  - Latches
  - Flip-flops
- Latches are basic storage elements that operate with signal levels (rather than signal transitions)
- Flip flop operate with signal transition

8.2 Basic Latch

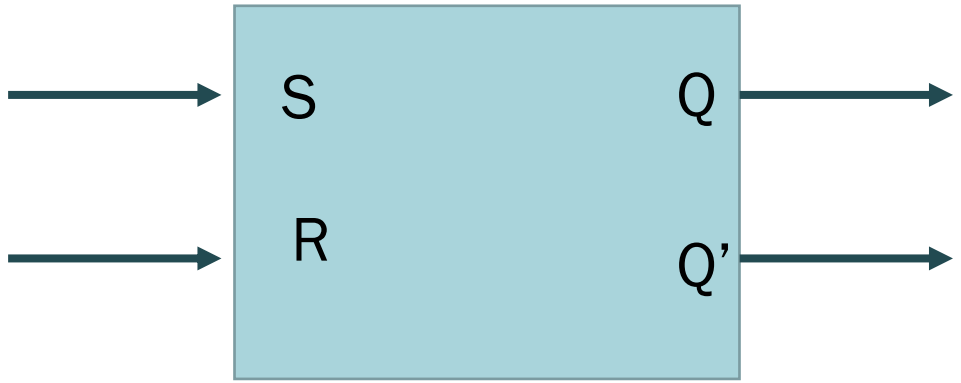
S-R Latch

- Also called as Set Reset Latch
- Can store 1 bit at a time
- SR Latch is a circuit with:
  - 2 cross coupled NOR gate, or 2 cross coupled NAND gate
  - 2 inputs : S for SET and R for RESET
  - 2 output Q and Q’

Q	Q’	STATE
1	0	Set
0	1	Reset

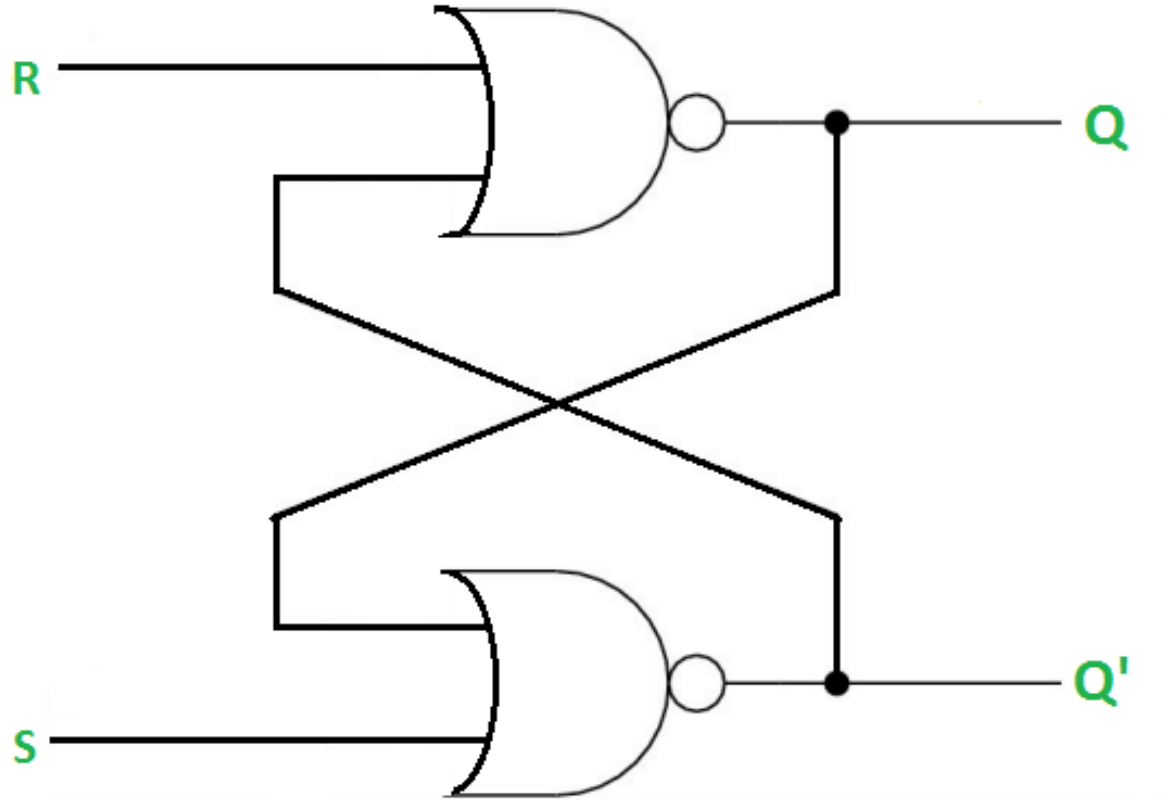
8.2 Basic Latch

SR Latch Logic Symbol



8.2 Basic Latch

SR Latch with NOR Gate



8.2 Basic Latch

Truth table (NOR gate)

S	R	Q	$\bar{Q}$
0	0	MEMORY	
0	1	0	1
1	0	1	0
1	1	Not used	

S : 0, R : 1

$Q = 0, \bar{Q} = \bar{0} = 1$

S : 0, R : 0

$Q = 0, \quad \bar{Q} = \bar{0} = 1$

S : 1, R : 0

$Q = 1, \quad \bar{Q} = \bar{1} = 0$

S : 0, R : 0

$Q = 1, \quad \bar{Q} = \bar{0} = 0$

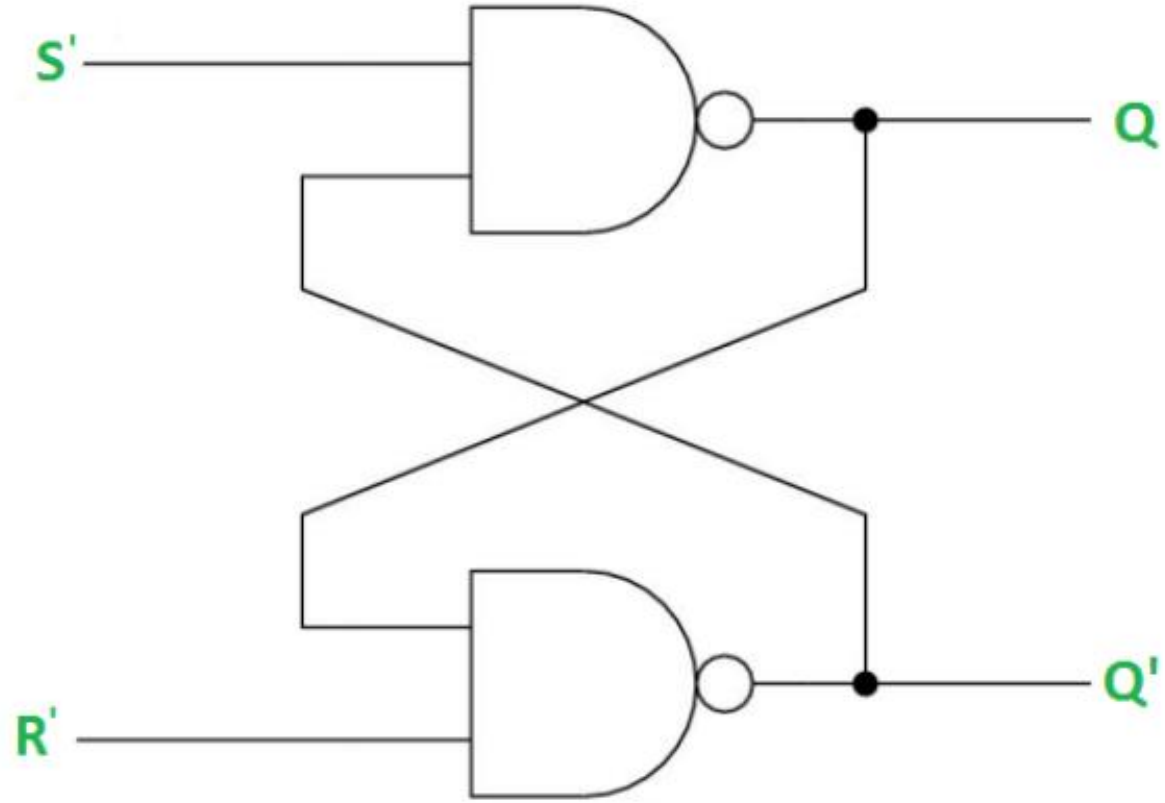
MEMORY

S : 1, R : 1

$Q = 0, \quad \bar{Q} = 0$ → NOT USED

8.2 Basic Latch

SR Latch with NAND Gate



8.2 Basic Latch

Truth table (NAND Gate)

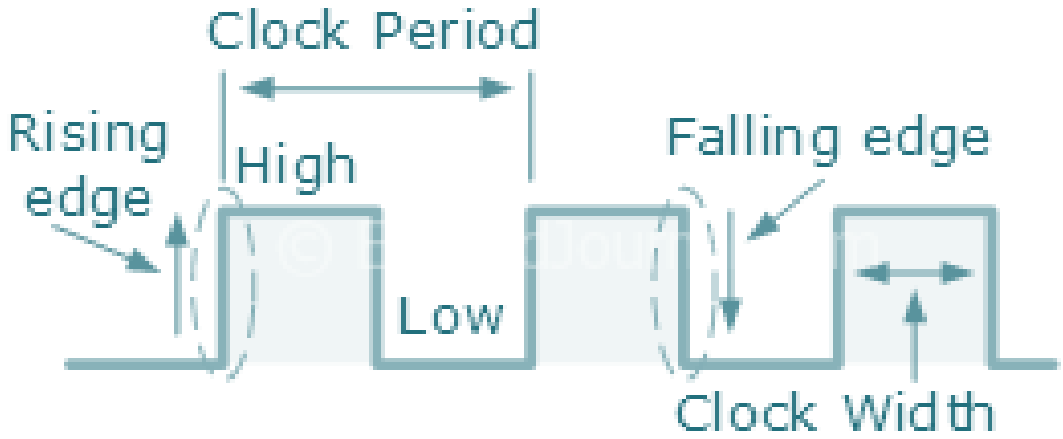
S	R	Q	$\overline{Q}$
0	0	NOT USED	
0	1	1	0
1	0	0	1
1	1	MEMORY	

8.3 Flip-Flop Circuit

8.3 Flip-Flop Circuit

Clock

- Clock or a clock signal is particular type of signal that oscillates between a high and a low state
- Clock can be used to activate the Flip Flops



8.3 Flip-Flop Circuit

Latch vs Flip Flops

- Latch is a level-triggered type, means that the output changes when the input changes
- A flip-flop is edge-triggered and only changes state when a control signal goes from high to low or low to high

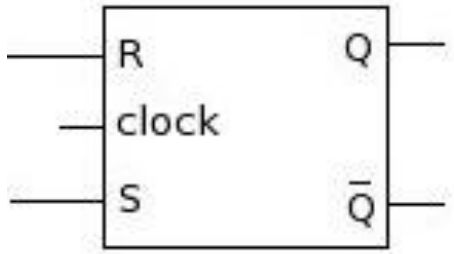
8.3 Flip-Flop Circuit

- Flip-flop is a circuit that maintains a state until **directed by input to change the state**
- A basic flip-flop can be constructed using four-NAND or four-NOR gates
- Types of flip-flops:
  - SR Flip Flop
  - JK Flip Flop
  - D Flip Flop
  - T Flip Flop

8.3 Flip-Flop Circuit

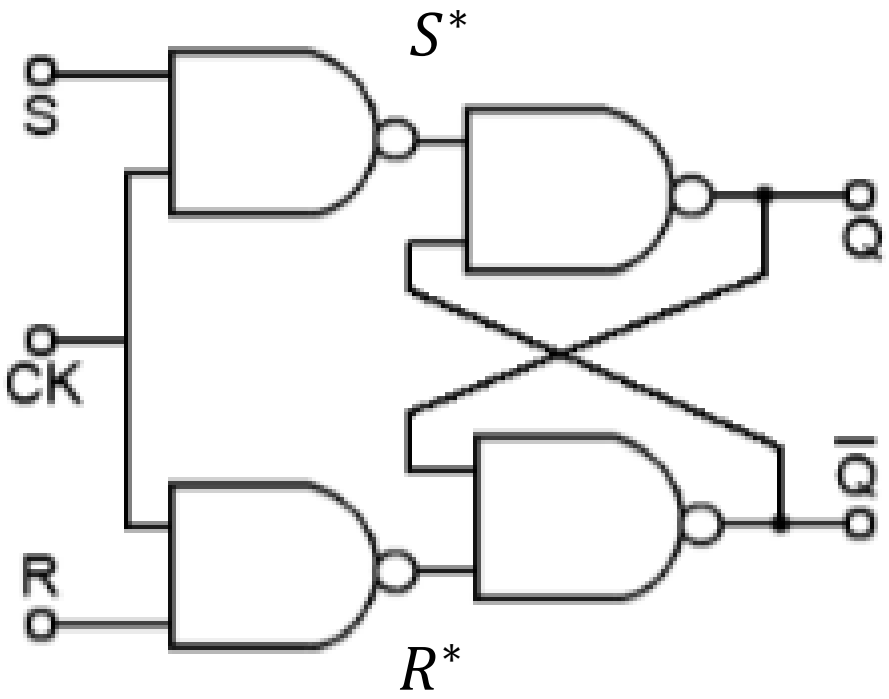
SR Flip Flop

- SR Flip flop stands for SET-RESET Flip flop



Symbol

$$S^* = \overline{(S\,.\,Clk)} = \bar{S} + \overline{Clk}$$



$$R^* = \overline{(R\,.\,Clk)} = \bar{R} + \overline{Clk}$$

8.3 Flip-Flop Circuit

Truth table for SR Flip Flop

S^*	R^*	Q	$\overline{Q}$
0	0	NOT USED	
0	1	1	0
1	0	0	1
1	1	MEMORY	

8.3 Flip-Flop Circuit

Truth table for SR Flip Flop

Clk	S	R	Q	$\bar{Q}$
0	x	x	MEMORY	
1	0	0	MEMORY	
1	0	1	0	1
1	1	0	1	0
1	1	1	NOT USED	

Clk	S	R	Qn+1
0	x	x	Qn
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	Invalid

8.3 Flip-Flop Circuit

Characteristic Table
(when Clk =1)

Qn	S	R	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

8.3 Flip-Flop Circuit

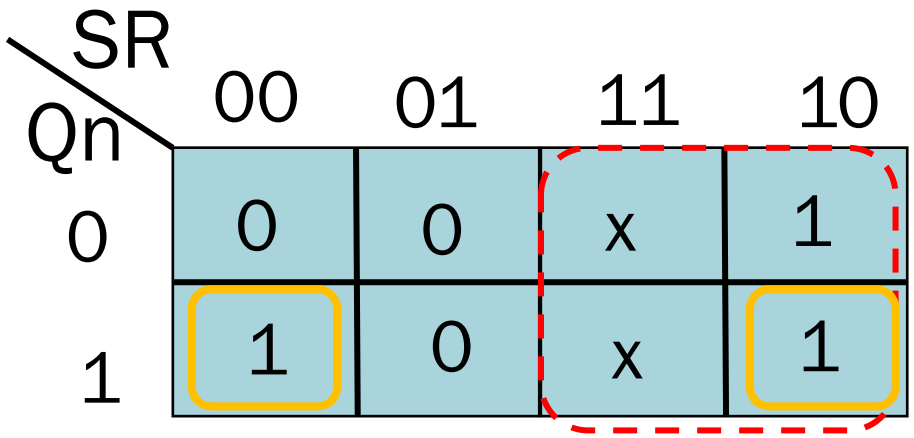
Excitation table

Input : Qn and Qn+1

Qn	Qn+1	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

8.3 Flip-Flop Circuit

Equation for RS Flip Flop

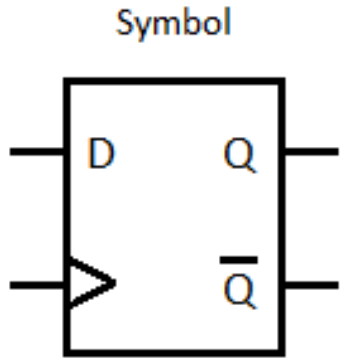


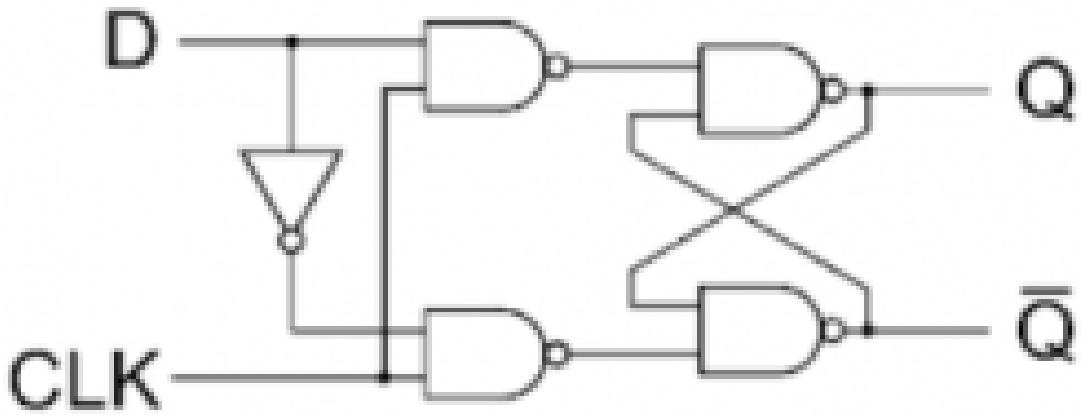
$$Q_{n+1} = S + Q_n\mathrm{R}$$

8.3 Flip-Flop Circuit

D Flip Flop

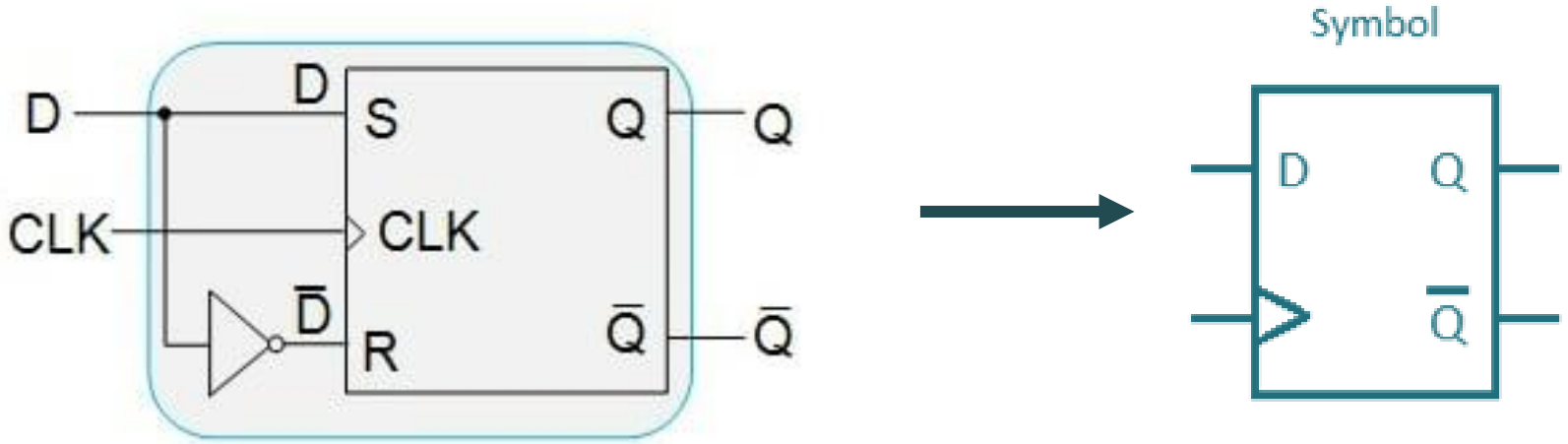
- D Flip flop stands for Data or Delay Flip Flop
- D Flip flop is a type of flip flop that tracks the input, making transitions with match those of the input D





8.3 Flip-Flop Circuit

SR to D Flip Flop



8.3 Flip-Flop Circuit

Truth table for D Flip Flop

D : 0
S = 0, R = 1

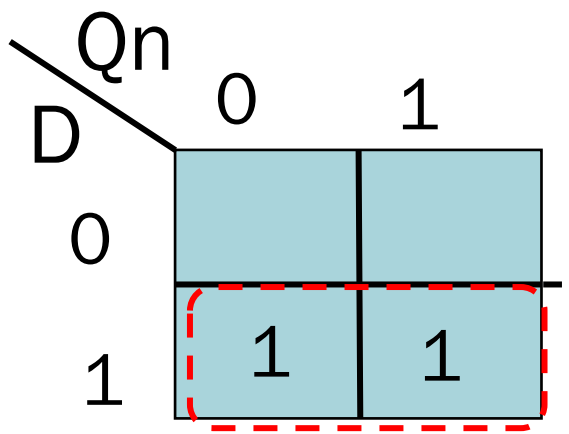
D : 1
$S = 1\ R = 1$

Clk	D	Qn+1
0	x	Qn
1	0	0
1	1	1

8.3 Flip-Flop Circuit

Characteristic Table for D Flip Flops

Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1



$$Q_{n+1} = D$$

8.3 Flip-Flop Circuit

Excitation Table

Qn	Qn+1	D
0	0	0
0	1	1
1	0	0
1	1	1

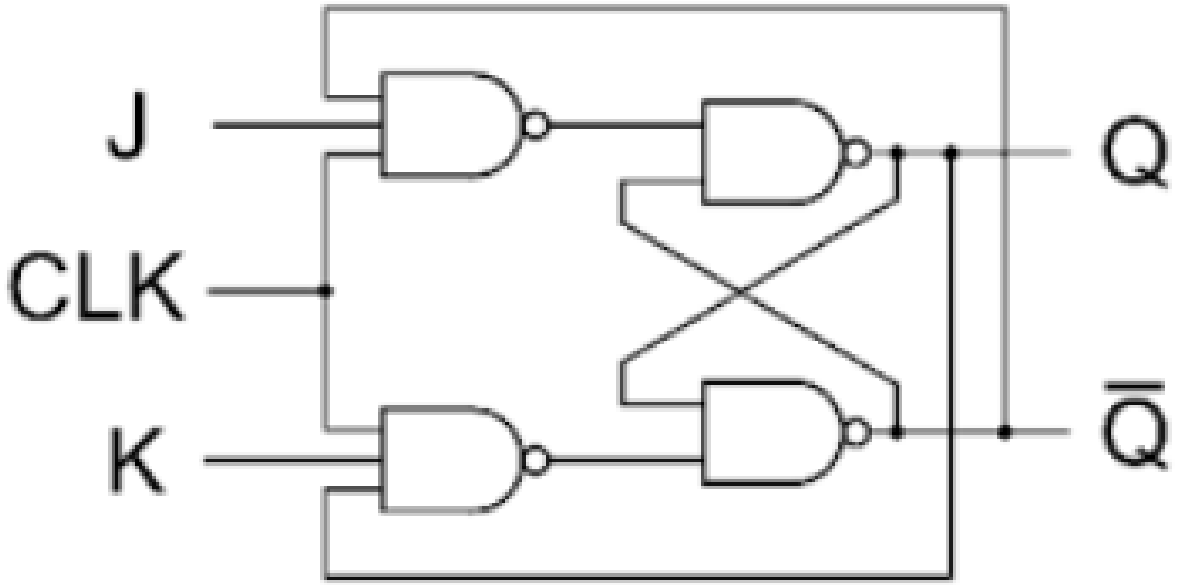
8.3 Flip-Flop Circuit

JK Flip Flop

- JK flip flop is one of the most used flip flops in digital circuits
- The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuit that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”

8.3 Flip-Flop Circuit

JK flip flop logic circuit



8.3 Flip-Flop Circuit

Truth table for JK Flip Flop

Clk	J	K	Qn+1
0	x	x	Qn (Memory)
1	0	0	Qn (Memory)
1	0	1	0
1	1	0	1
1	1	1	$\overline{Qn}$ (toggle)

8.3 Flip-Flop Circuit

Characteristic table for JK Flip Flop

Qn	J	K	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

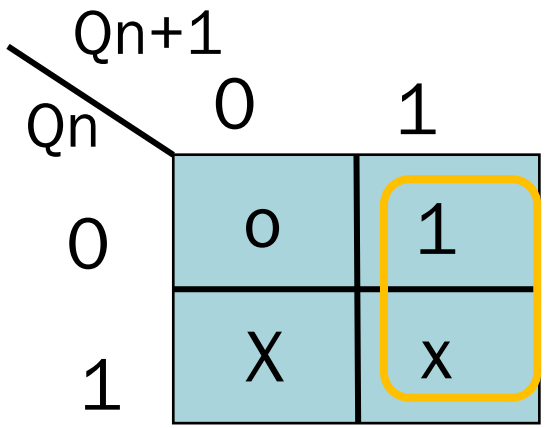
8.3 Flip-Flop Circuit

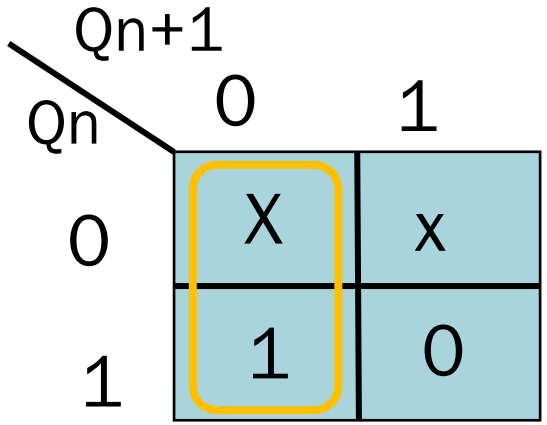
Excitation table for JK Flip Flop

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

8.3 Flip-Flop Circuit

Equation for JK Flip Flop



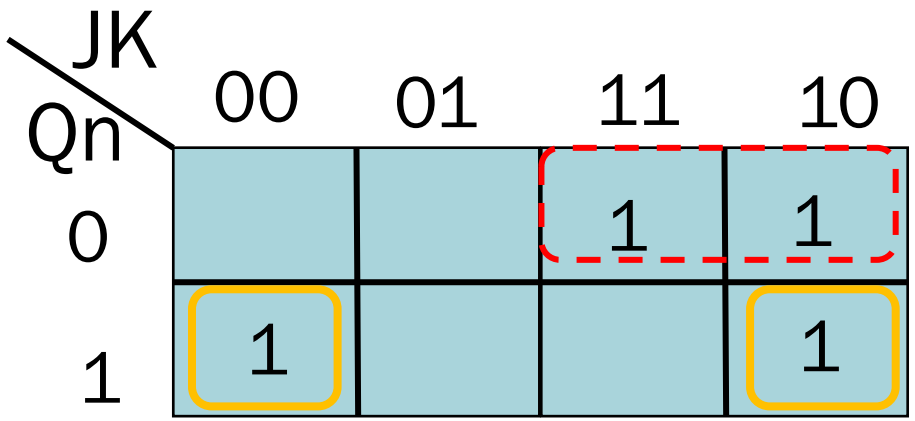


$$J = Q_{n+1}$$

$$K = \overline{Q_{n+1}}$$

8.3 Flip-Flop Circuit

Equation for JK Flip Flop



$$Q_{n+1} = \overline{Q_n}J + Q_n\overline{K}$$

8.3 Flip-Flop Circuit

T Flip Flop

- T flip flop is a single input flip flop
- T flip flop only works when a clock signal is high
- When the T signal is set low (0), it will not affect the present state of the output and the response will not change

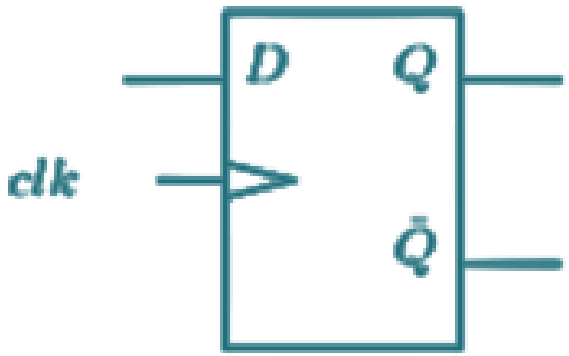
8.3 Flip-Flop Circuit

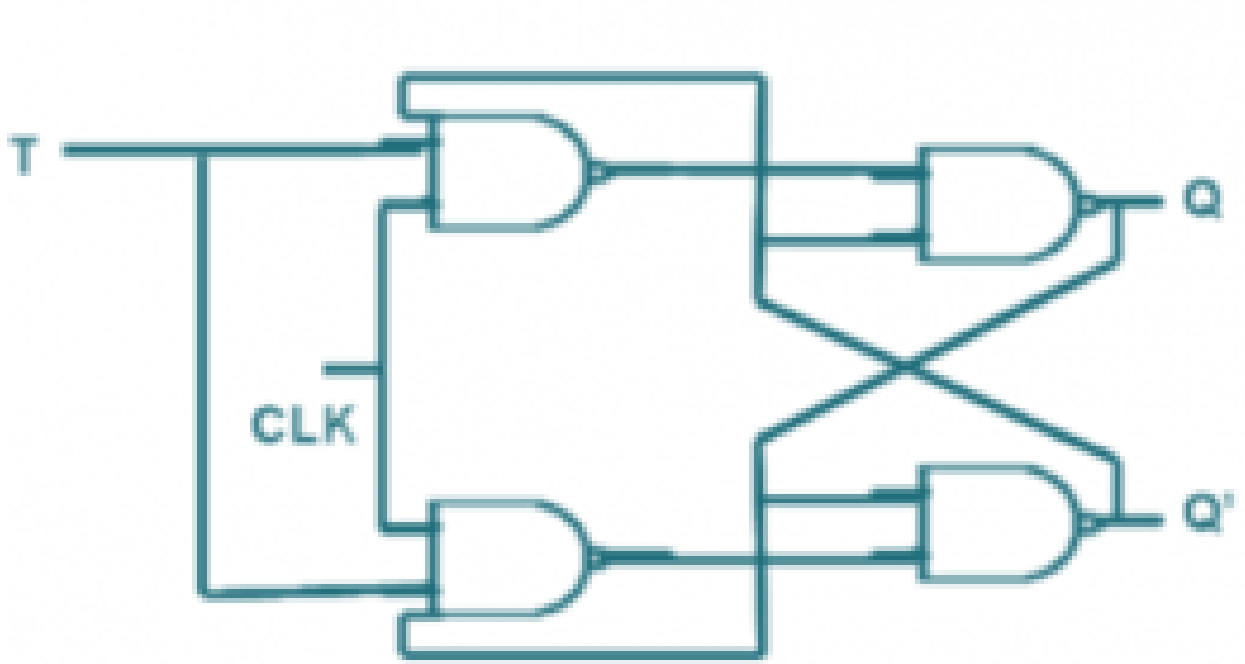
Truth table for T Flip Flop

Clk	T	Qn+1
0	X	Qn
1	0	Qn
1	1	$\overline{Qn}$

8.3 Flip-Flop Circuit

T flip flop logic circuit





8.3 Flip-Flop Circuit

Characteristic Table

Qn	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_{n+1} = Q_n \; XOR \; T$$

8.3 Flip-Flop Circuit

Excitation Table

Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0

References

M. Morris Mano, Digital Design, 5th ed, Prentice Hall, 2012, **Chapter 4**

Next Topic : Sequential Circuit Analysis