CE232 DIGITAL SYSTEM

Topic 7. Combinational Logic Circuit (2)

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Subtopic

7.6 Universal Gate

7.7 Decoder, Encoder

7.8 Multiplexer, Demultiplexer

7.9 Programmable Logic Array

7.6 Universal Gate

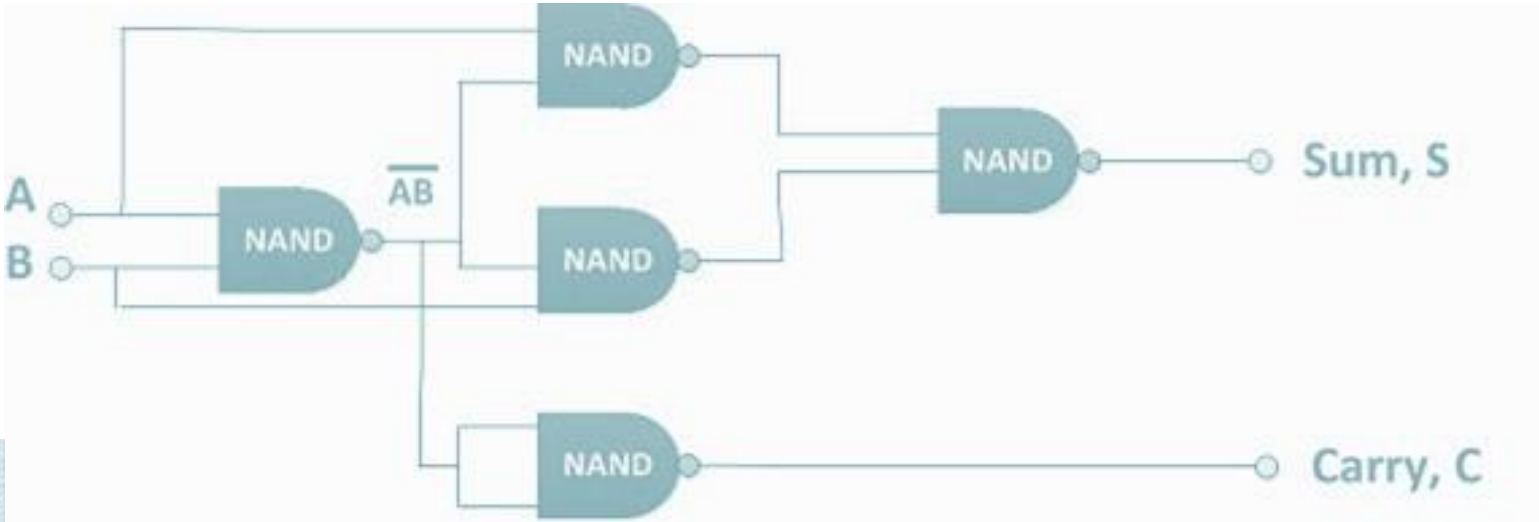
7.6 Universal Gate

- **Universal Gate :** NAND & NOR
- Adder dan Subtractor can be represented by universal gate

7.6 Universal Gate

Half Adder using NAND Gate

- Sum = A XOR B
- Carry = AB



$$\text{SUM, } S = \overline{A.\overline{AB}} \; . \; \overline{B.\overline{AB}}$$

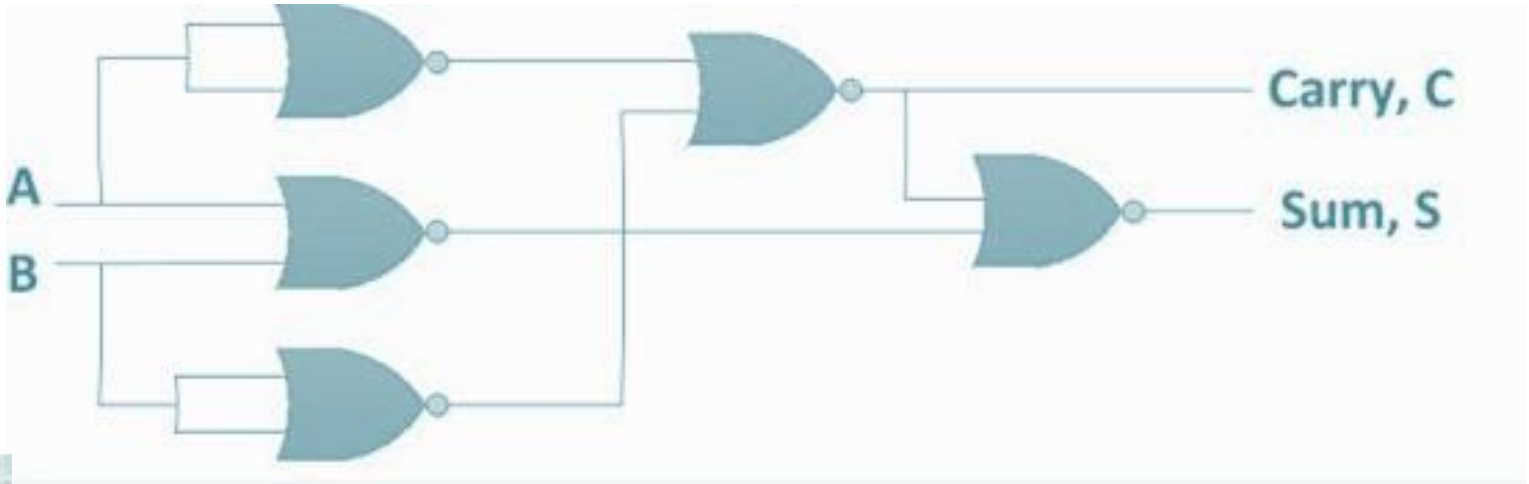
$$\text{SUM, } S = A\overline{B} + \overline{A}B$$

$$\text{Carry, } C = AB = \overline{\overline{AB}}$$

7.6 Universal Gate

Half Adder using NOR Gate

- Sum = A XOR B
- Carry = AB



$$\text{SUM, } S = \overline{\overline{A+B} + \overline{A+B}}$$

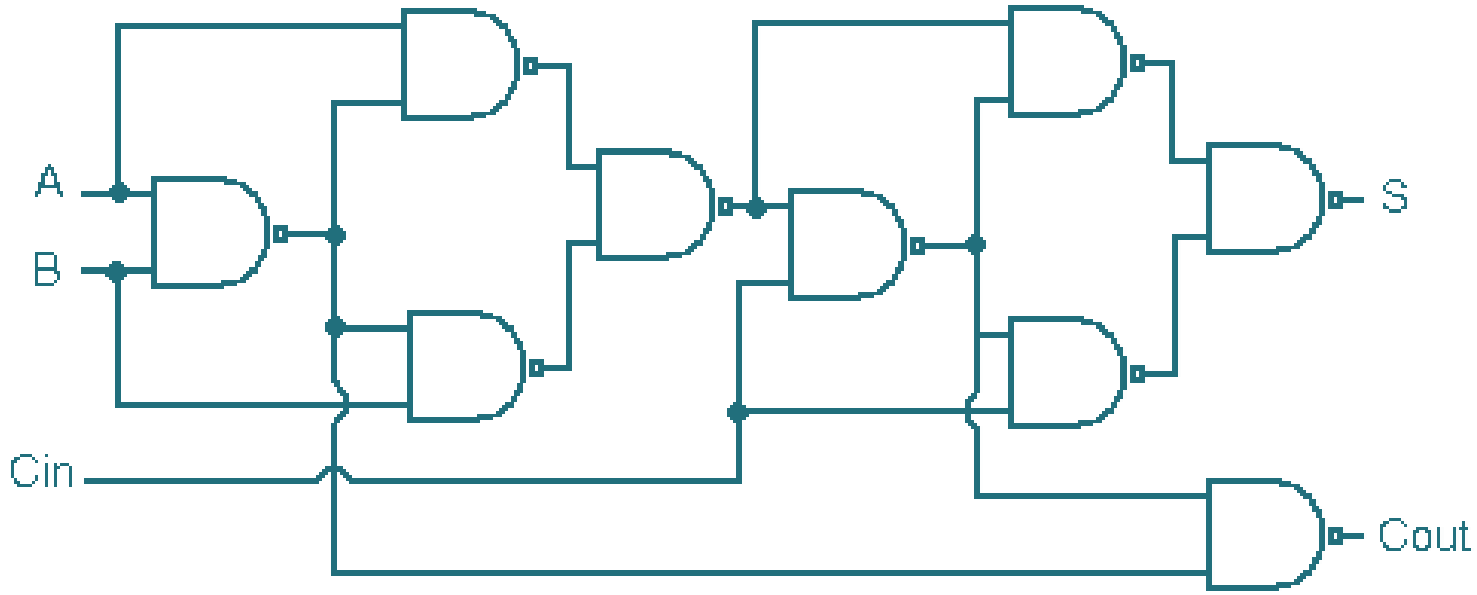
$$\text{SUM, } S = A\overline{B} + \overline{A}B$$

$$\text{Carry, } C = \overline{\overline{A}+\overline{B}}$$

7.6 Universal Gate

Full Adder using NAND Gate

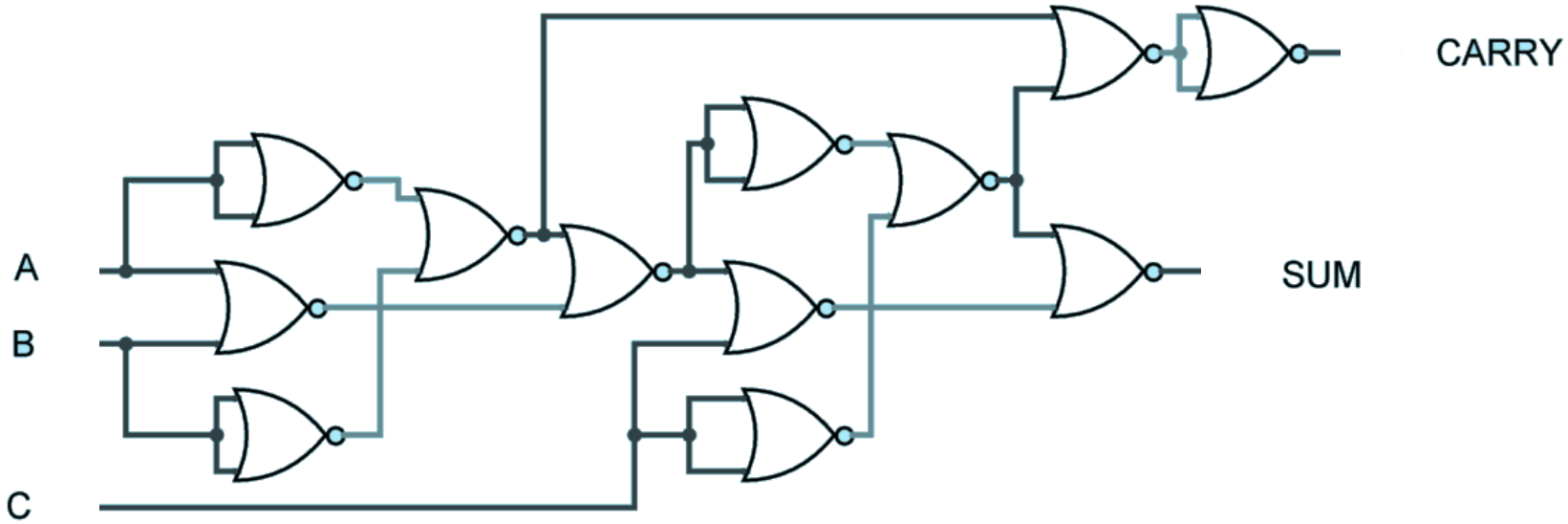
- Sum = A XOR B XOR Cin
- Carry = A Cin + B Cin +AB



7.6 Universal Gate

Full Adder using NOR Gate

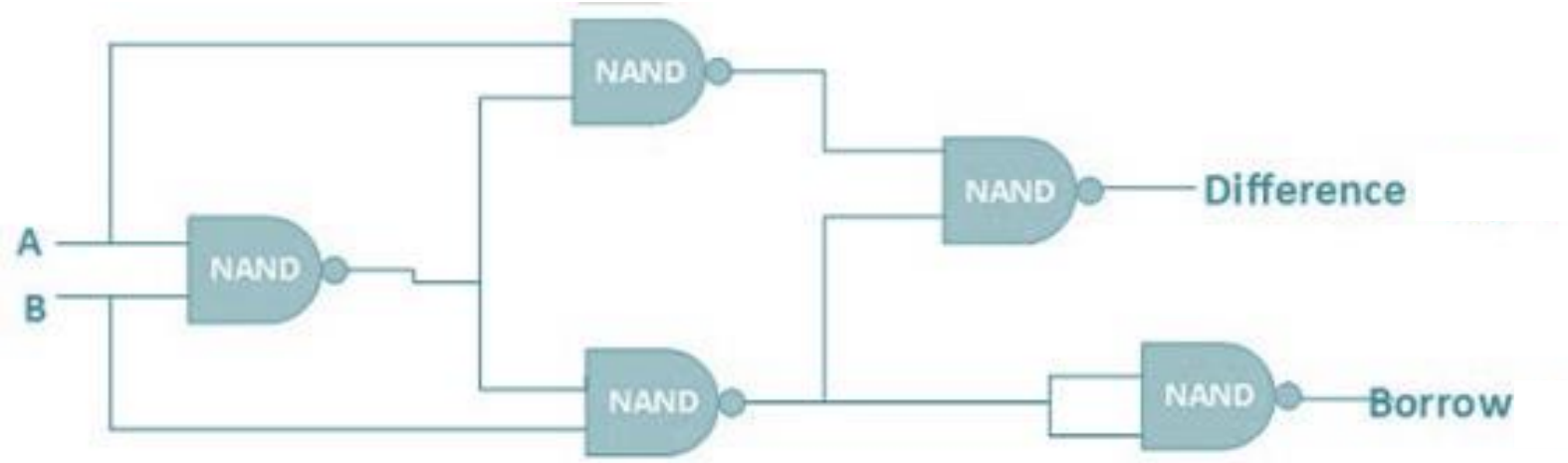
- Sum = A XOR B XOR Cin
- Carry = A Cin + B Cin +AB



7.6 Universal Gate

Half Subtractor using NAND Gate

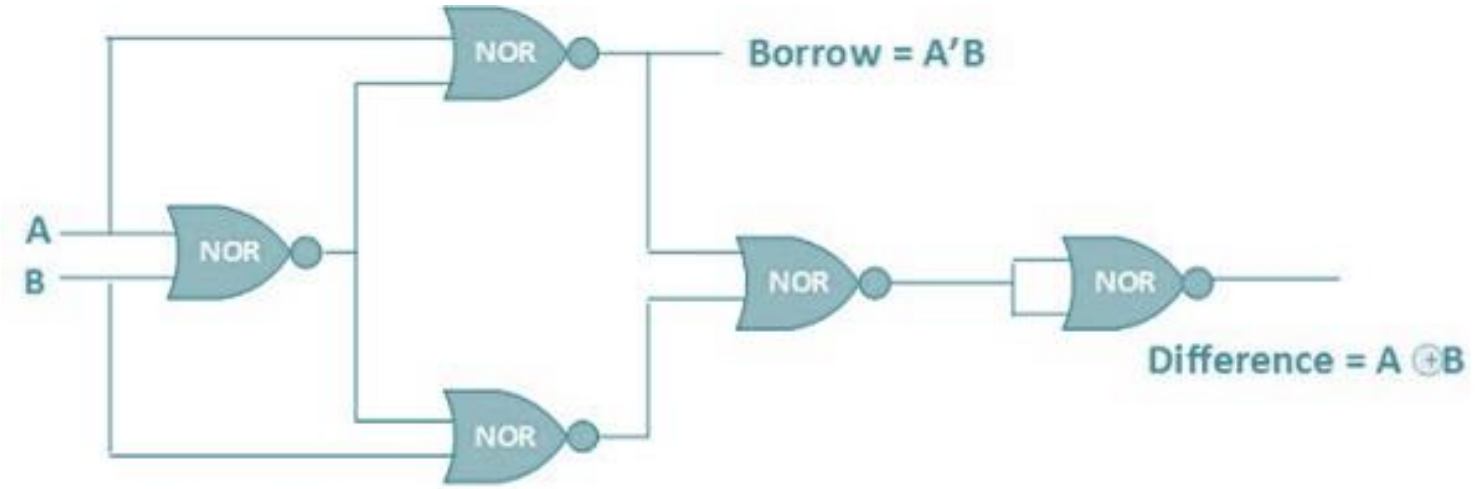
- Difference = A XOR B
- Borrow = A'B



7.6 Universal Gate

Half Subtractor using NOR Gate

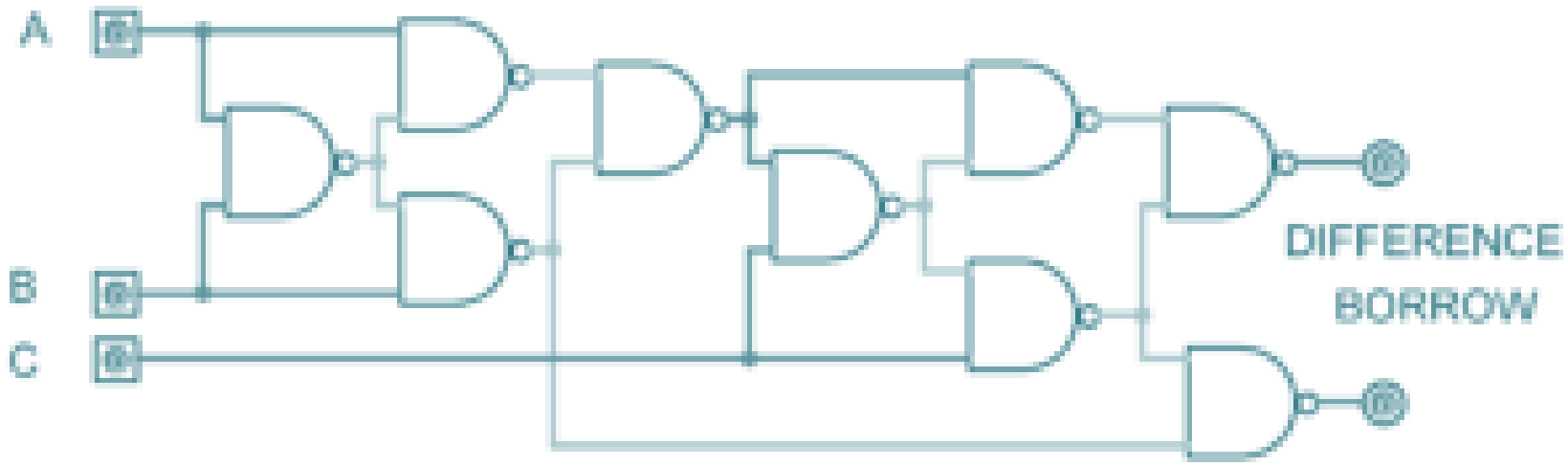
- Difference = A XOR B
- Borrow = A'B



7.6 Universal Gate

Full Subtractor using NAND Gate

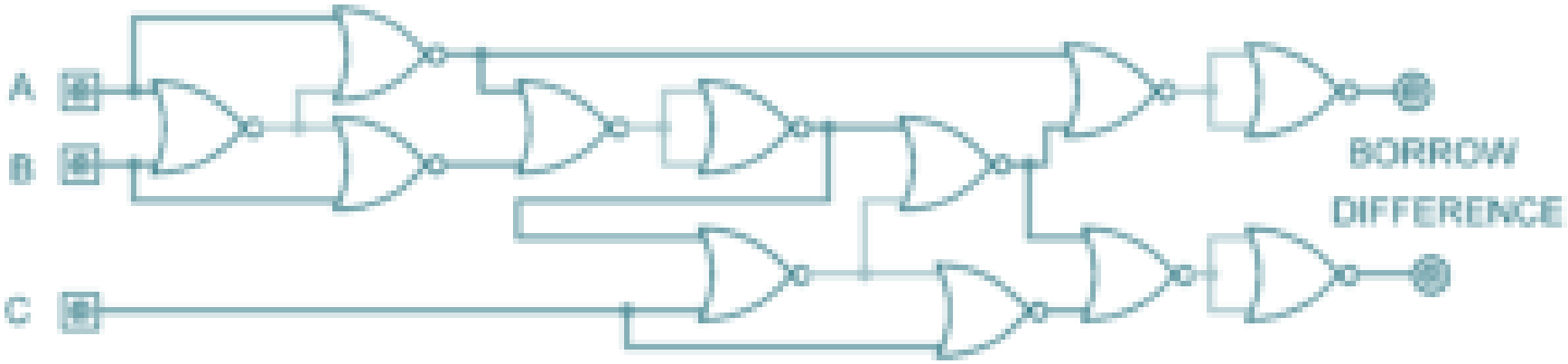
- Sum = A XOR B XOR Cin
- Carry = A Cin + B Cin +AB



7.6 Universal Gate

Full Subtractor using NOR Gate

- Difference = A XOR B XOR Cin
- Borrow = A Cin + B Cin +AB



7.7 Decoder, Encoder

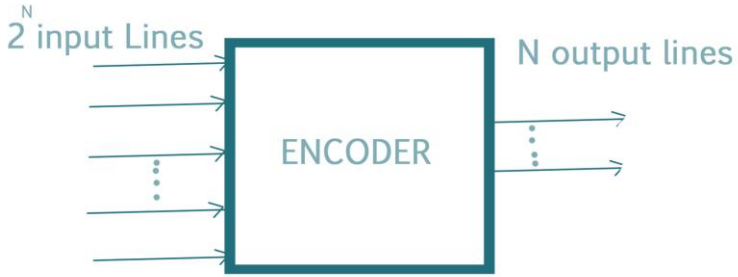
7.7 Decoder, Encoder

- Binary code of N digits can be used to store 2^N distinct elements of coded information
- Encoders convert 2^N lines of input into a code of N bits
- Decoders decode the N bits into 2^N lines.

7.7 Decoder, Encoder

Encoder

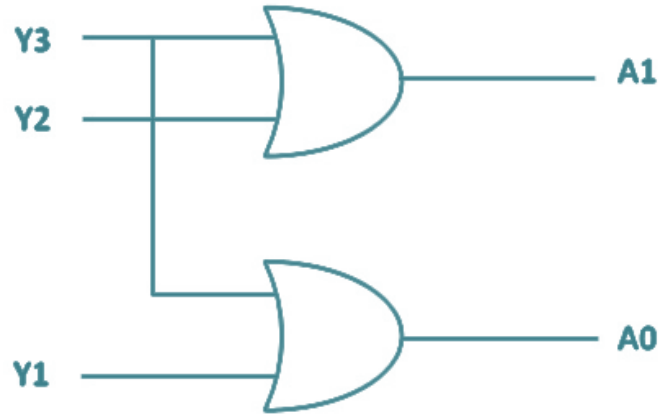
- An encoder is a combinational circuit that converts binary information in the form of a 2^N input lines into N output lines, which



7.7 Decoder, Encoder

4 to 2 binary encoderthe

INPUTS				OUTPUTS	
Y3	Y2	Y1	Y0	A1	A0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



A1 = Y3 + Y2
A0 = Y3 + Y1

7.7 Decoder, Encoder

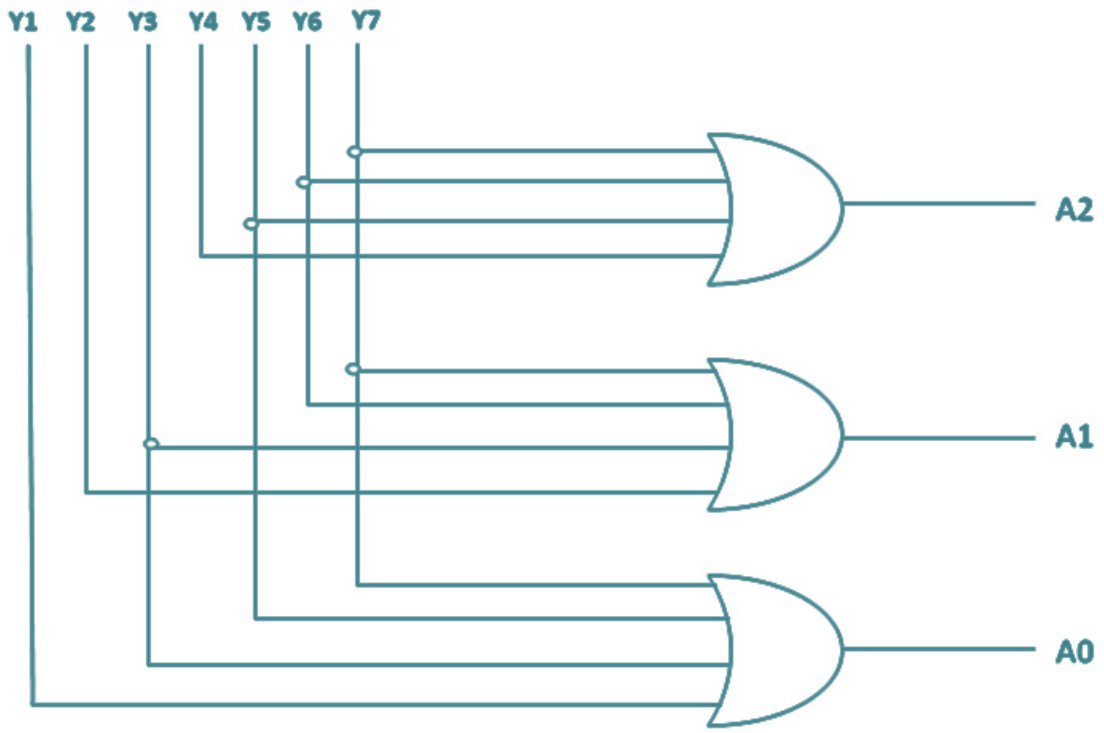
8-to-3-bit Encoder

INPUTS								OUTPUTS		
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	A2	A1	A0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

7.7 Decoder, Encoder

8-to-3-bit Encoder Output Expression

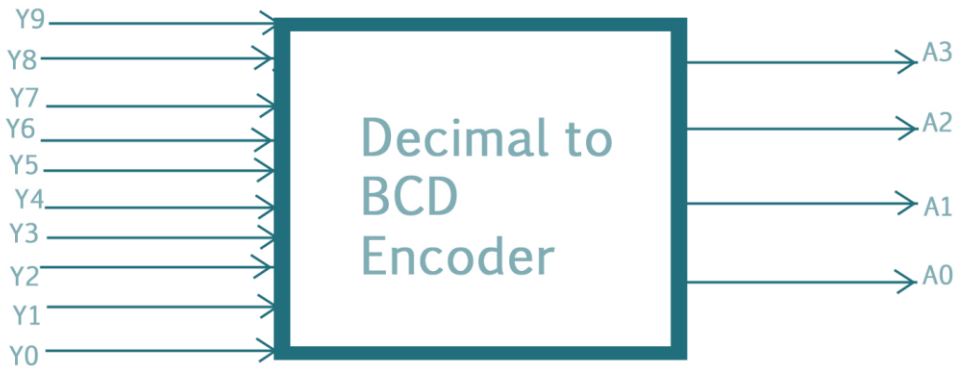
$$A2 = Y7 + Y6 + Y5 + Y4$$
$$A1 = Y7 + Y6 + Y3 + Y2$$
$$A0 = Y7 + Y5 + Y3 + Y1$$



7.7 Decoder, Encoder

Decimal to BCD Encoder

- The decimal to binary encoder usually consists of 10 input lines and 4 output lines
- This encoder accepts the decoded decimal data as an input and encodes it to the BCD output which is available on the output lines



7.7 Decoder, Encoder

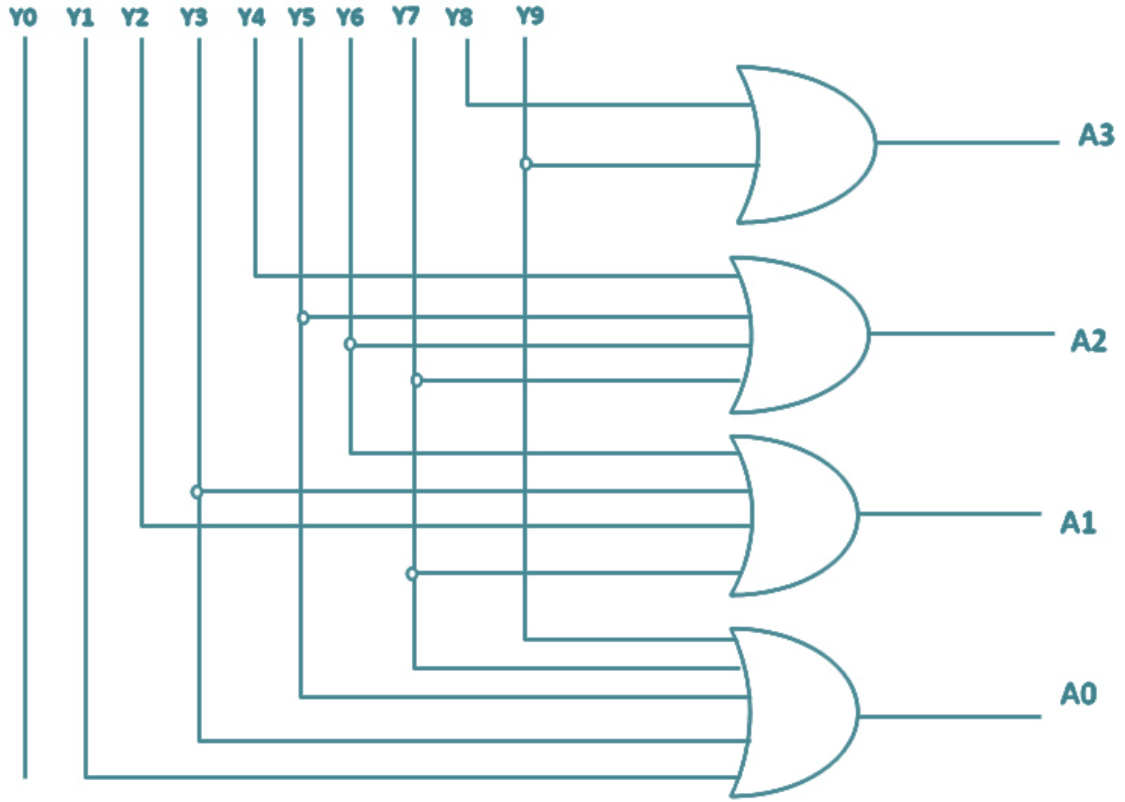
Decimal to BCD Encoder Output

$$A3 = Y9 + Y8$$
$$A2 = Y7 + Y6 + Y5 + Y4$$
$$A1 = Y7 + Y6 + Y3 + Y2$$
$$A0 = Y9 + Y7 + Y5 + Y3 + Y1$$

INPUTS										OUTPUTS			
Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	A3	A2	A1	A0
0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0	0	1

7.7 Decoder, Encoder

Decimal to BCD Encoder Circuit



7.7 Decoder, Encoder

Main disadvantages of standard digital encoders :

- It can generate the wrong output code when there is more than one input present at logic level “1”
- One simple way to overcome this problem is to “Priorities” the level of each input pin
- This type of digital encoder is known commonly as a Priority Encoder or P-encoder for short
- The priority encoders output corresponds to the currently active input which has the highest priority → when an input with a higher priority is present, all other inputs with a lower priority will be ignored

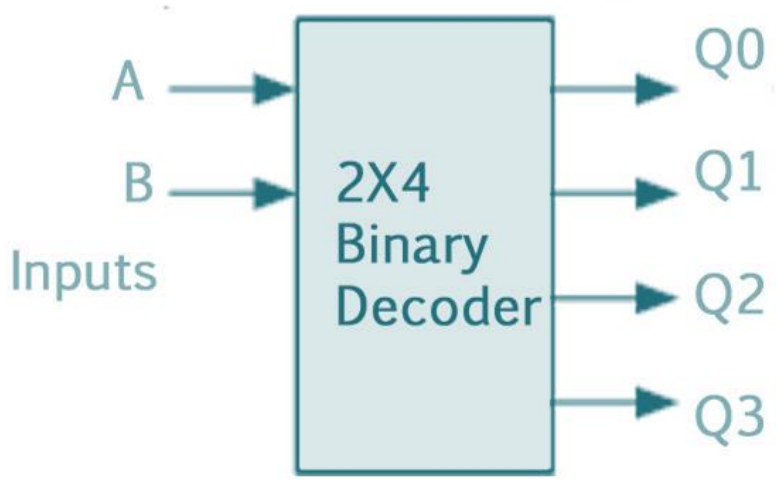
7.7 Decoder, Encoder

Decoder

- Decoder is multi-input multi output logic circuit which decodes n input into 2^N possible outputs

7.7 Decoder, Encoder

2 to 4 Binary Decoders



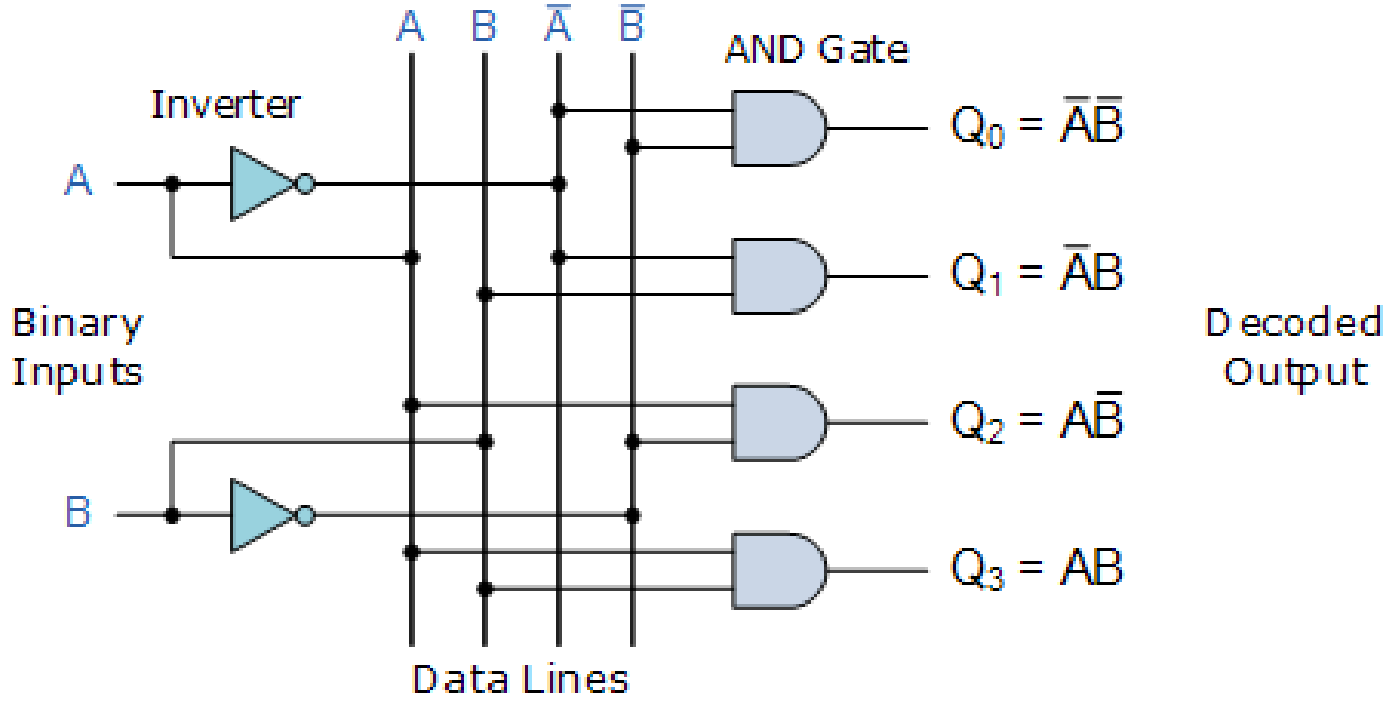
Output

A	B	Q0	Q1	Q2	Q3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

7.7 Decoder, Encoder

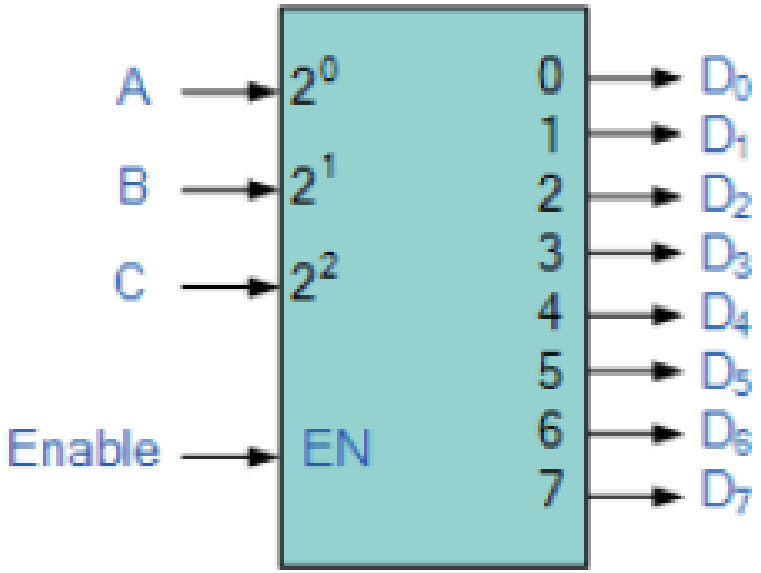
2 to 4 Binary Decoders

Qo=A'B'
Q1=A'B
Q2=AB'
Q3=AB



7.7 Decoder, Encoder

3 to 8 Binary Decoders



A	B	C	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

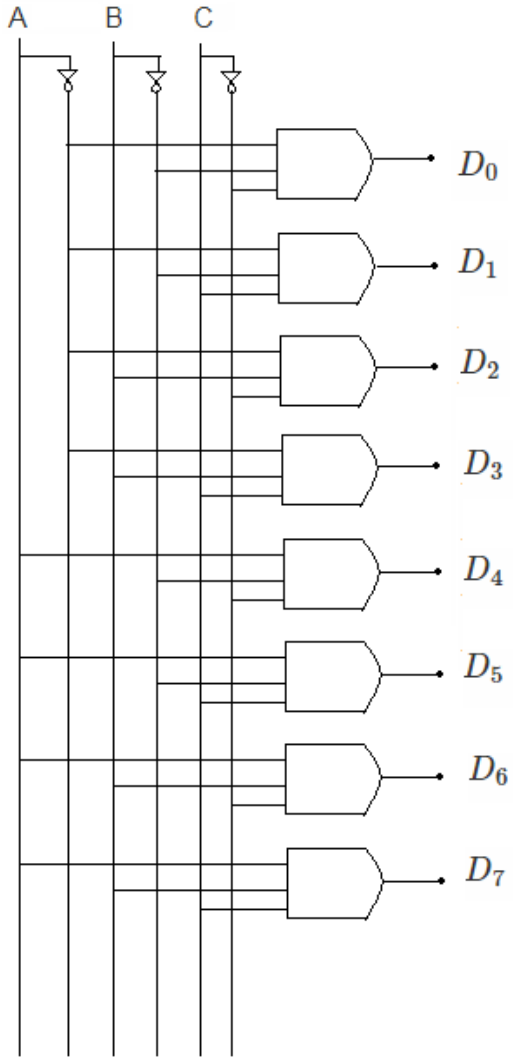
7.7 Decoder, Encoder

3 to 8 Binary Decoders

$$D_0 = \bar{A}\bar{B}\bar{C}, \quad D_1 = \bar{A}\bar{B}C, \quad D_2 = \bar{A}B\bar{C},$$

$$D_3 = \bar{A}BC, \quad D_4 = A\bar{B}\bar{C}, \quad D_5 = A\bar{B}C,$$

$$D_6 = AB\bar{C}, \quad D_7 = ABC$$



7.8 Multiplexer, Demultiplexer

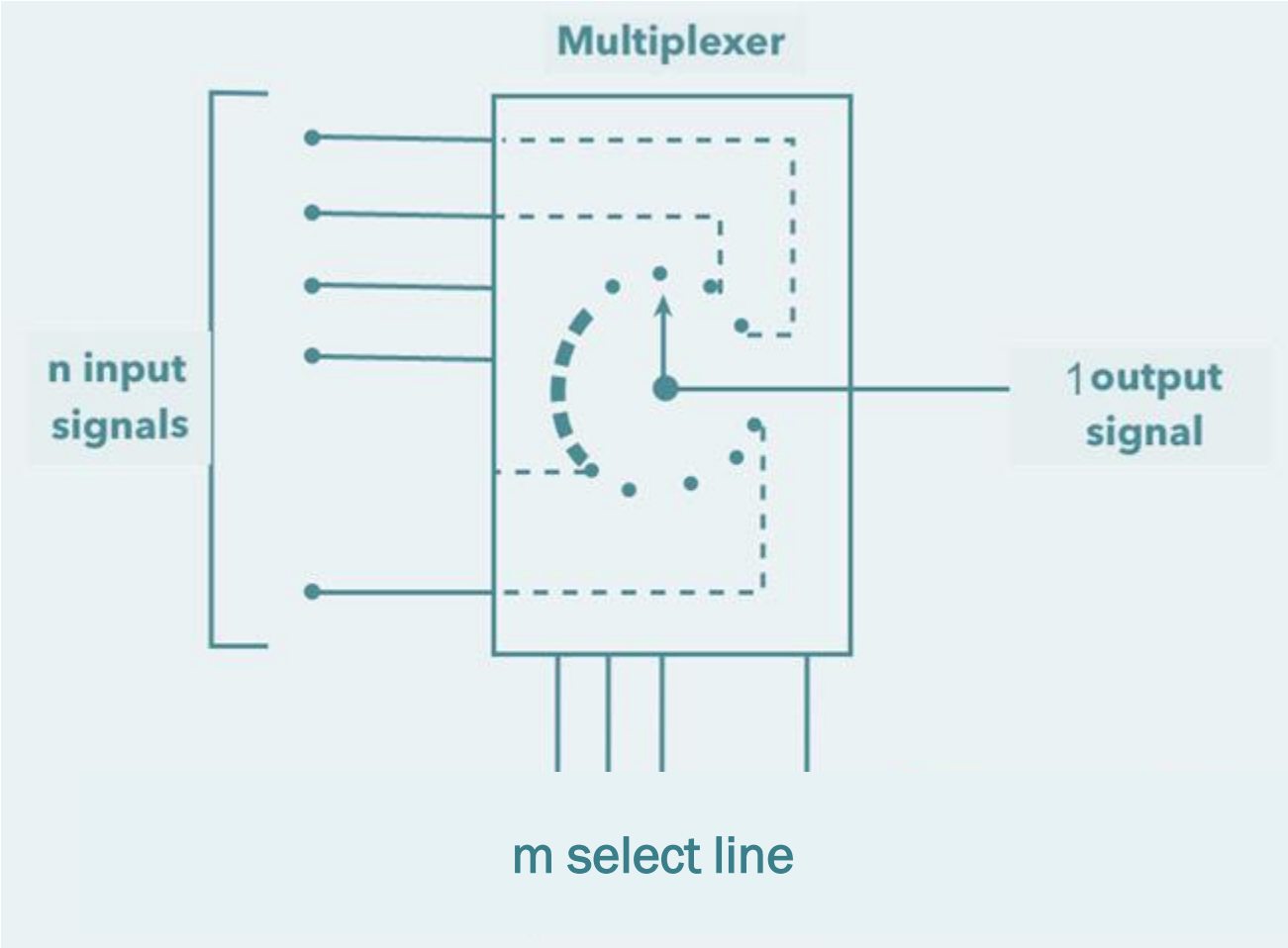
7.8 Multiplexer, Demultiplexer

Multiplexer

- Multiplexer is a combinational logic circuit used to select only one input among several input based on selection lines
- Multiplexer can act as digital switch
- For a MUX there can be 2^n input, n selection lines and only one output
- Multiplexers are also known as “Data n selector, parallel to serial convertor, many to one circuit, universal logic circuit”

7.8 Multiplexer, Demultiplexer

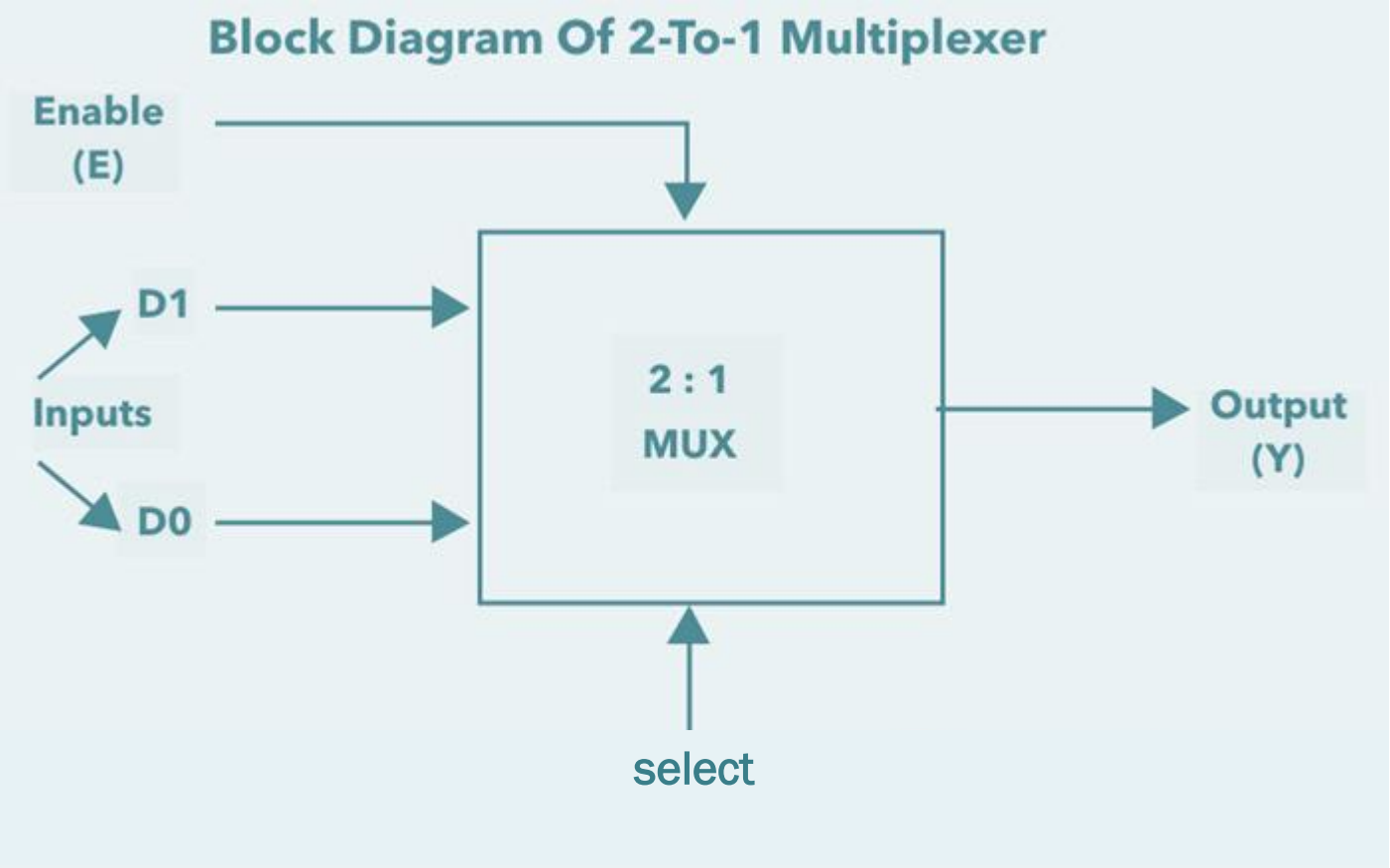
Multiplexer



7.8 Multiplexer, Demultiplexer

2 x 1 MUX

- Consists of two inputs D0 and D1, one select input S and one output Y



7.8 Multiplexer, Demultiplexer

2 x 1 MUX

- If the select line is low, then the output will be switched to D0 input, whereas if select line is high, then the output will be switched to D1 input.

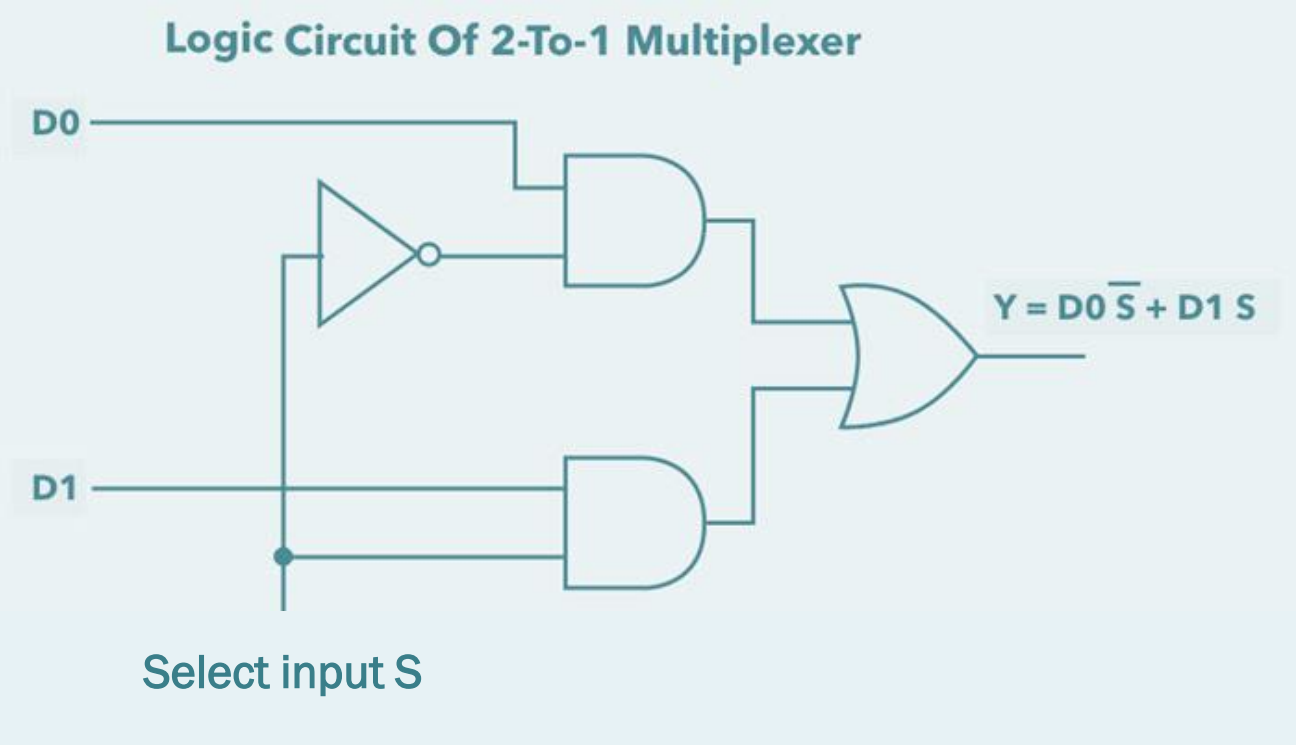
$$Y = \bar{S}D0 + SD1$$

Truth Table

S	D0	D1	Y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

7.8 Multiplexer, Demultiplexer

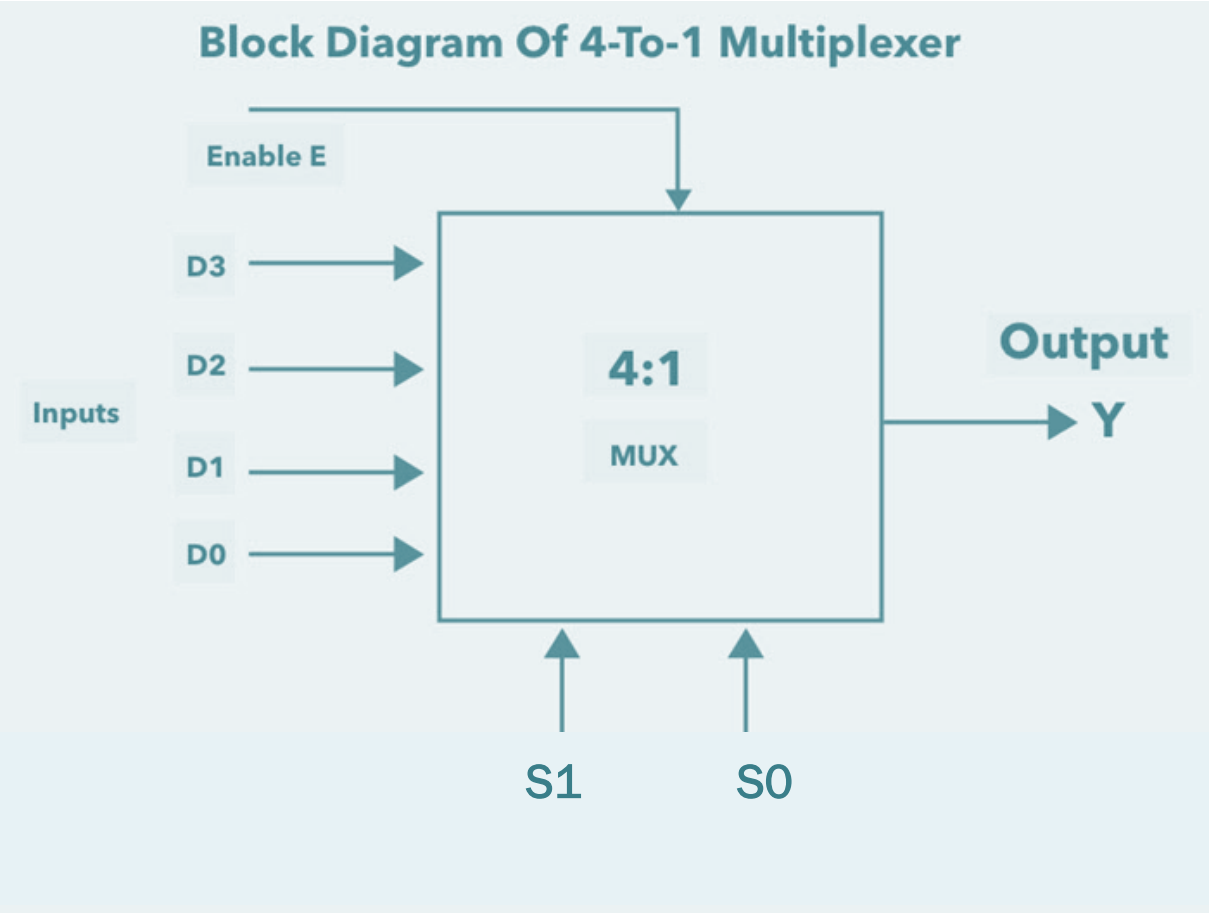
2 x 1 MUX Logic Circuit



7.8 Multiplexer, Demultiplexer

4 x 1 MUX

- Consists four data input lines as D0 to D3, two select lines as S0 and S1 and a single output line Y



7.8 Multiplexer, Demultiplexer

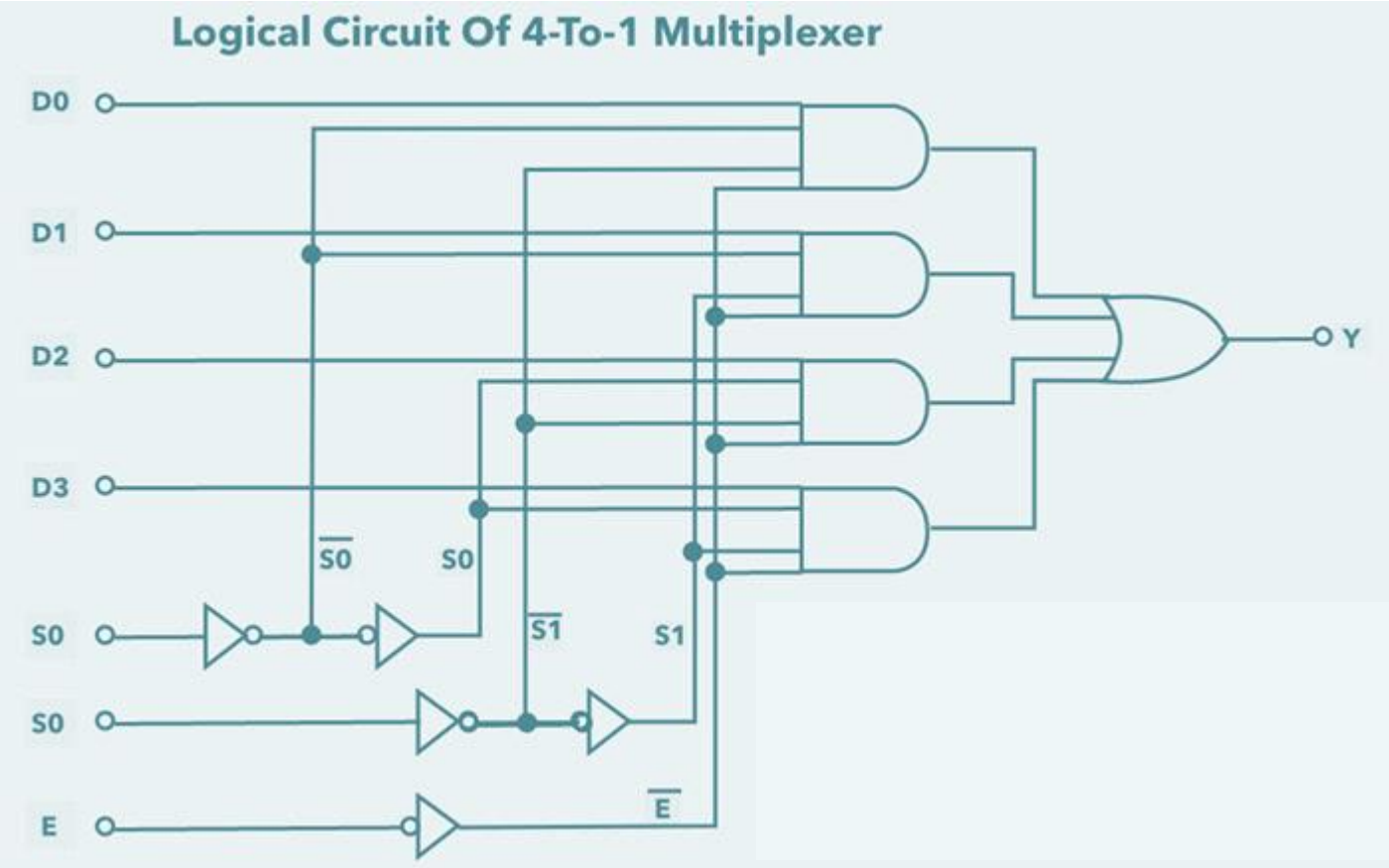
4 X 1 MUX

$$Y = \overline{S0}\ \overline{S1}\ D0 + \overline{S0}\ S1\ D1 + S0\ \overline{S1}\ D2 + S0\ S1\ D3$$

S0	S1	D0	D1	D2	D3	Y
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

7.8 Multiplexer, Demultiplexer

4 x 1 MUX Logic Circuit



7.8 Multiplexer, Demultiplexer

Example

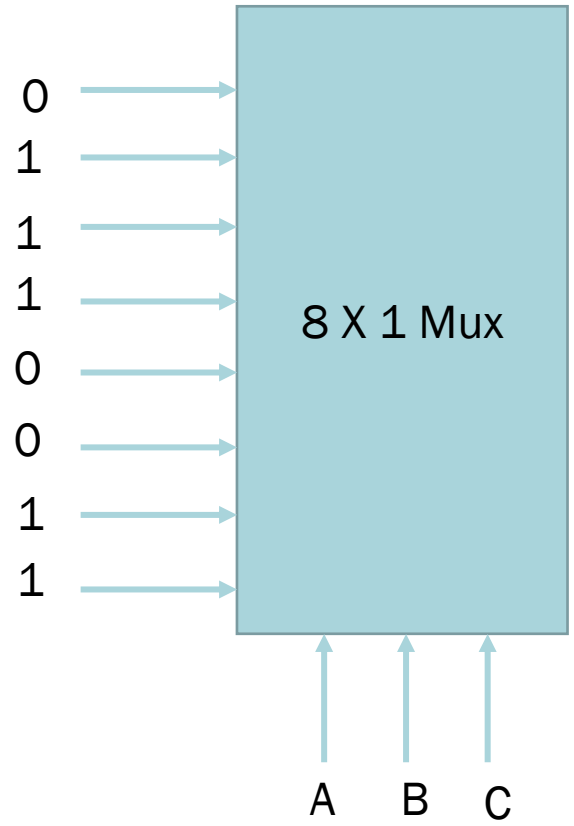
Implement $\sum m(1,2,3,6,7)$ using multiplexer

N variable function 2^n → to satisfy the problem, set n =3

A	B	C	Output
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

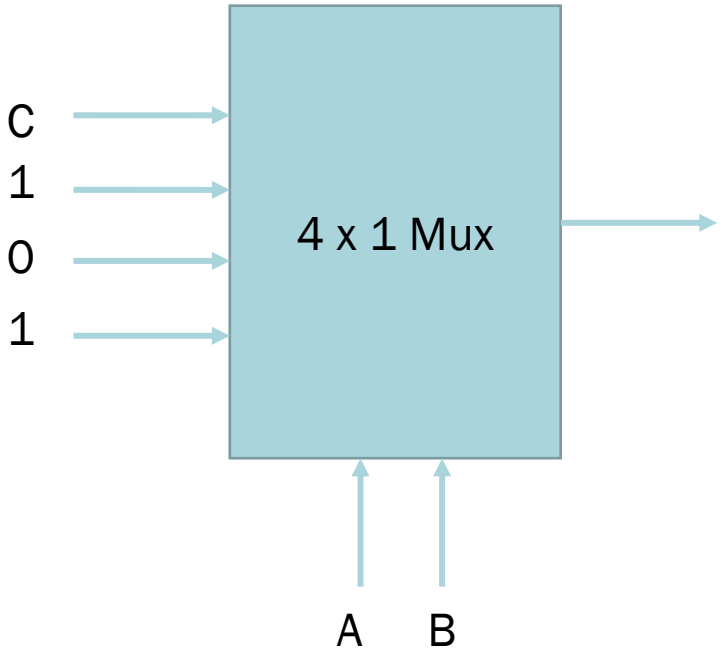
7.8 Multiplexer, Demultiplexer

A	B	C	Ouput	
0	0	0	0	C
0	0	1	1	
0	1	0	1	1
0	1	1	1	
1	0	0	0	0
1	0	1	0	
1	1	0	1	1
1	1	1	1	



7.8 Multiplexer, Demultiplexer

There is only 4 possible output, therefore the result can also be represented as given



7.9 Programmable Logic Array

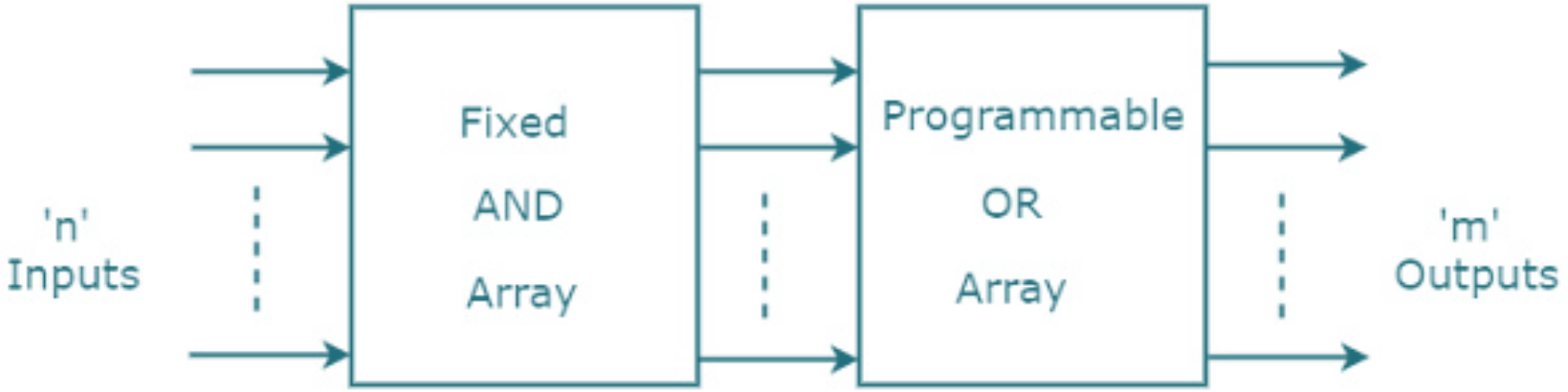
7.9 Programmable Logic Array

- Programmable Logic Devices (PLDs) are the integrated circuits
- They contain an array of AND gates & another array of OR gates.
- The process of entering the information into these devices is known as programming
- There are three kinds of PLDs :
  - Programmable Read Only Memory : has fixed AND array & Programmable OR array
  - Programmable Array Logic : has Programmable AND array & fixed OR array
  - Programmable Logic Array : has both Programmable AND array & Programmable OR array

7.9 Programmable Logic Array

Programmable Read Only Memory (PROM)

- PROM is a programmable logic device that has fixed AND array & Programmable OR array



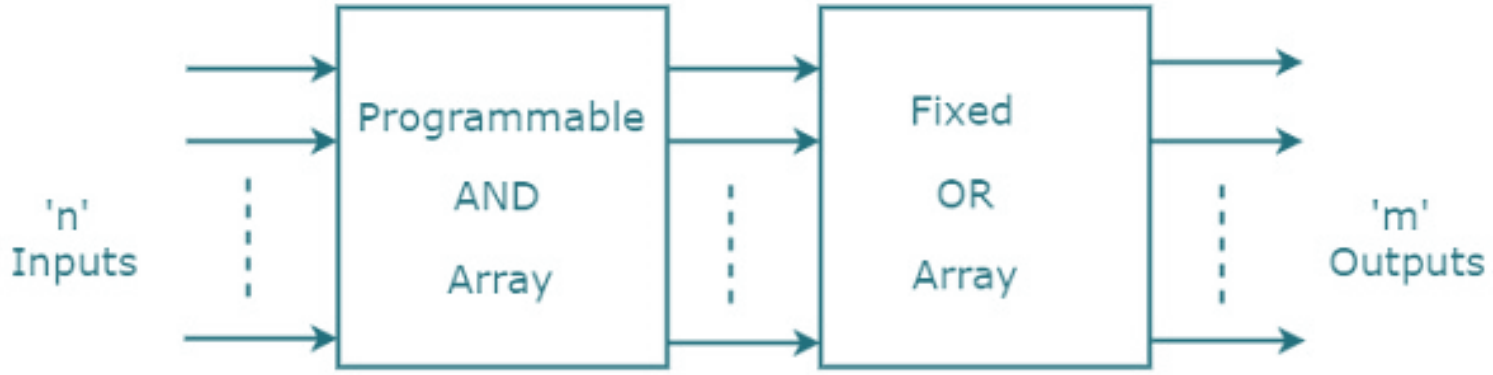
7.9 Programmable Logic Array

- The inputs of AND are not programmable, so we generate 2^n product terms by using 2^n AND gates having n inputs each (can be implemented using nx 2^n decoder)
- The outputs of PROM will be in the form of sum of min terms

7.9 Programmable Logic Array

Programmable Array Logic (PAL)

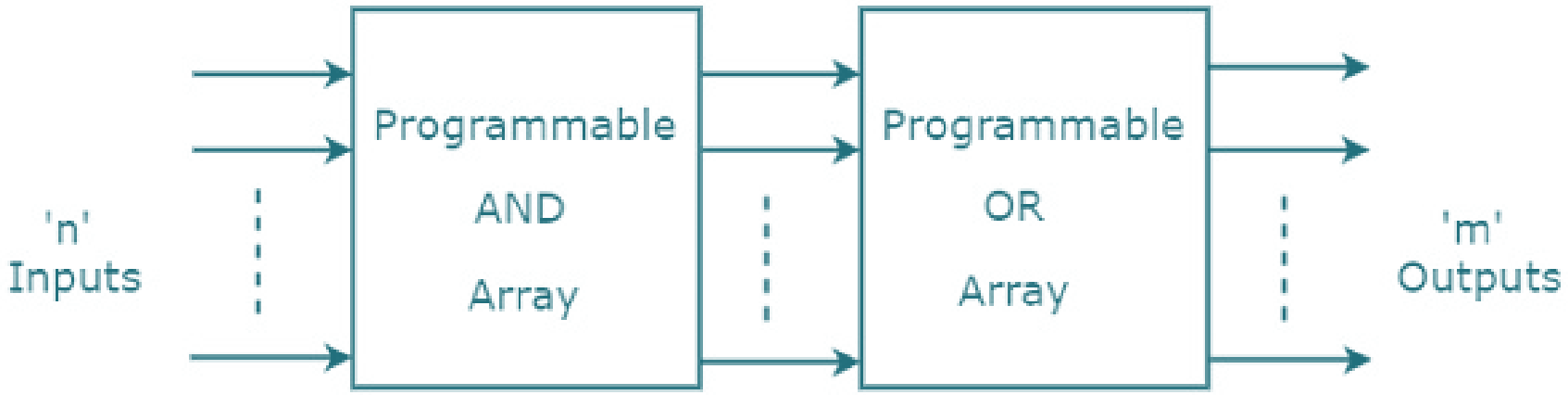
- PAL is a programmable logic device that has Programmable AND array & fixed OR array.
- In PAL, we can generate only the required product terms of Boolean function instead of generating all the min terms by using programmable AND gates



7.9 Programmable Logic Array

Programmable Logic Array

- PLA is a programmable logic device that has both Programmable AND array & Programmable OR array → most flexible PLD



7.9 Programmable Logic Array

- The inputs of AND gates are programmable, we can generate only the required product terms by using these AND gates
- The inputs of OR gates are also programmable, therefore the outputs of PAL will be in the form of sum of products form

7.9 Programmable Logic Array

Example.

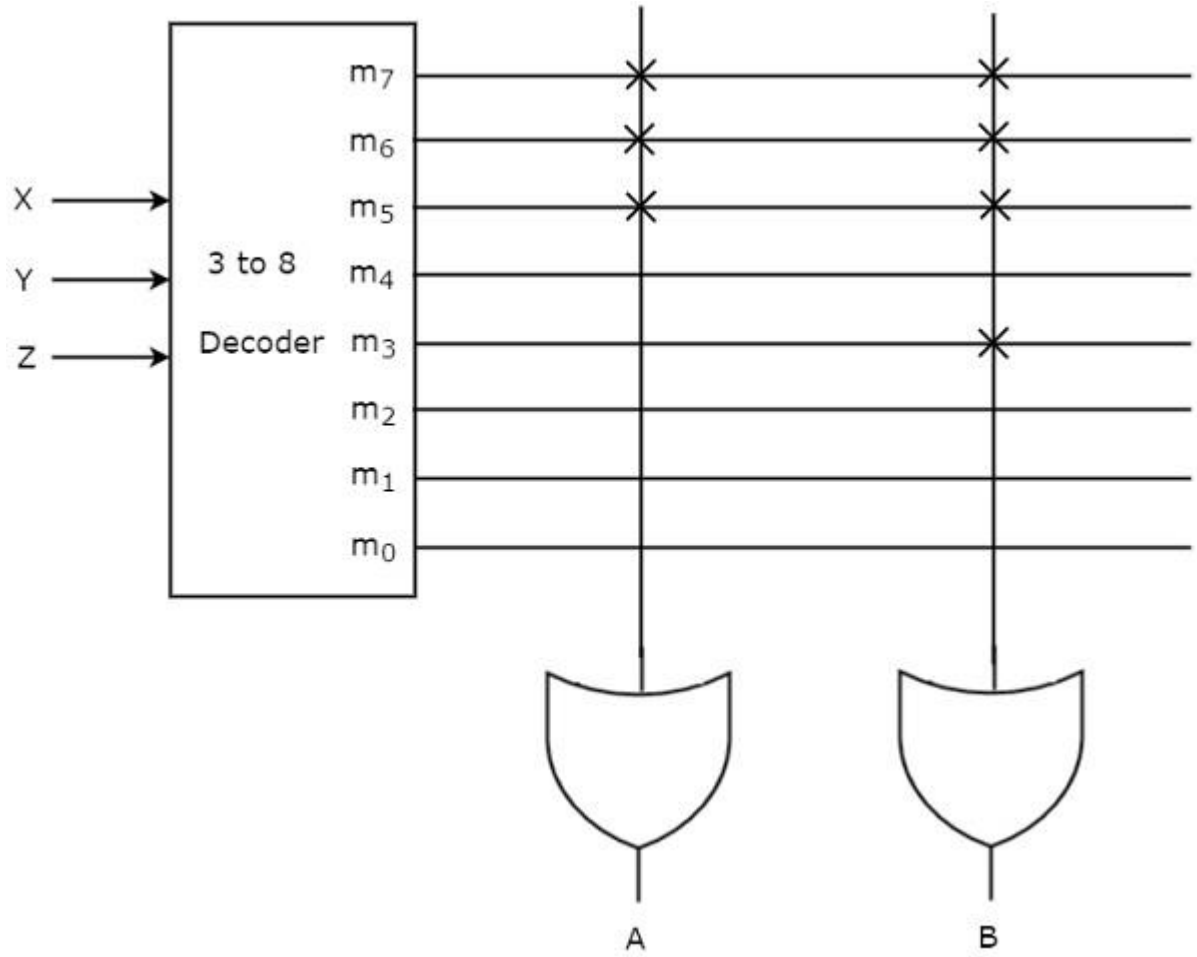
Implement the following Boolean functions using PROM

$$A(X, Y, Z) = \sum m(5, 6, 7)$$

$$B(X, Y, Z) = \sum m(3, 5, 6, 7)$$

7.9 Programmable Logic Array

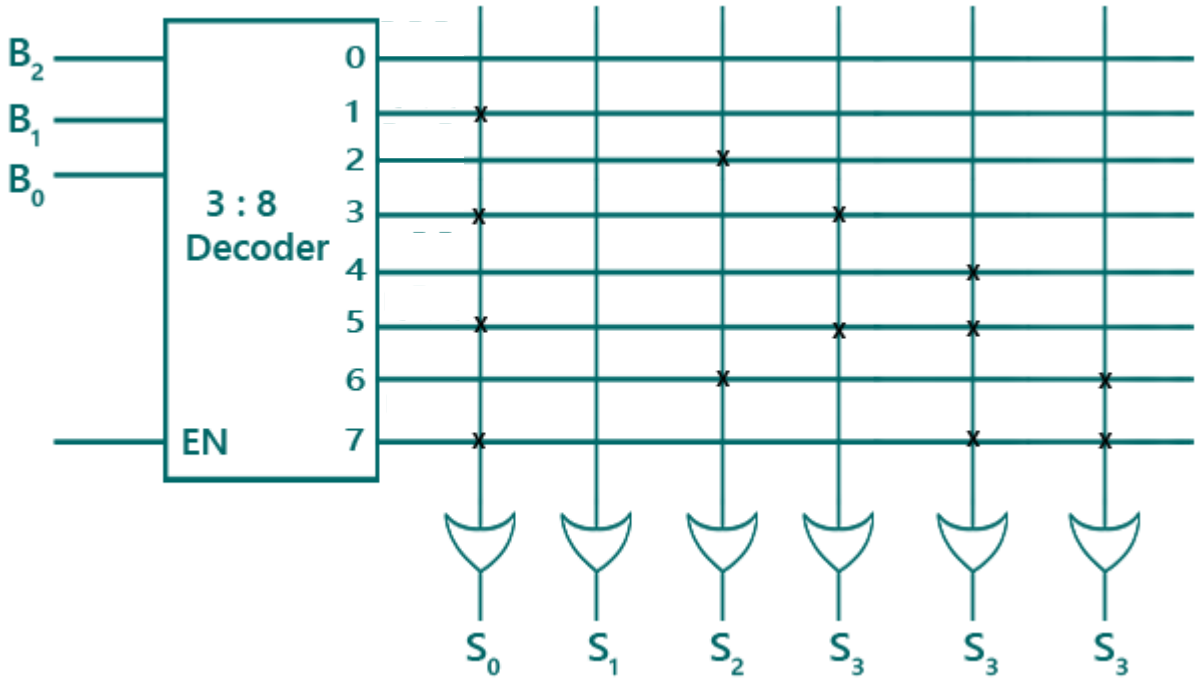
The given two functions are in sum of min terms form and each function is having three variables X, Y & Z → require a 3 to 8 decoder and 2 programmable OR



7.9 Programmable Logic Array

Example.

Find the output of S_1 and S_4

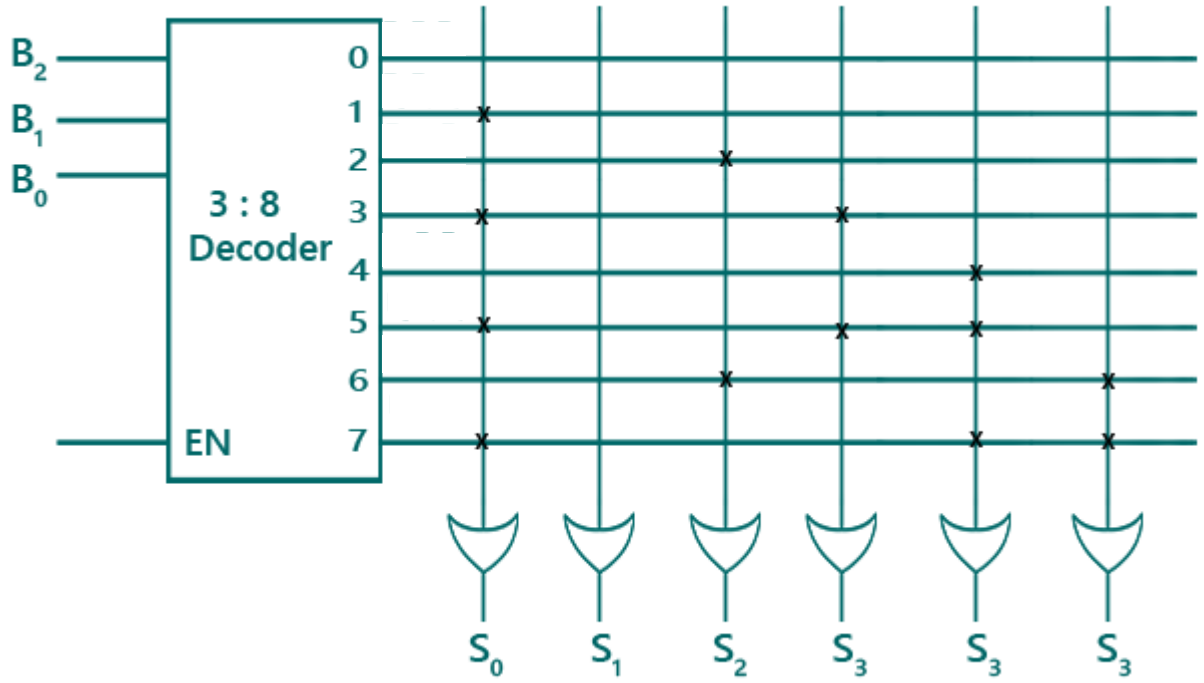


7.9 Programmable Logic Array

Solutions.

$S_1 (B_2, B_1, B_0)$ has no min-terms

$S_4 (B_2, B_1, B_0) = \sum \mathbf{m\ (4,5,7)}$



7.9 Programmable Logic Array

Example.

Implement the following Boolean functions using PLA

$$A = XY + XZ'$$

$$B = XY' + YZ + XZ'$$

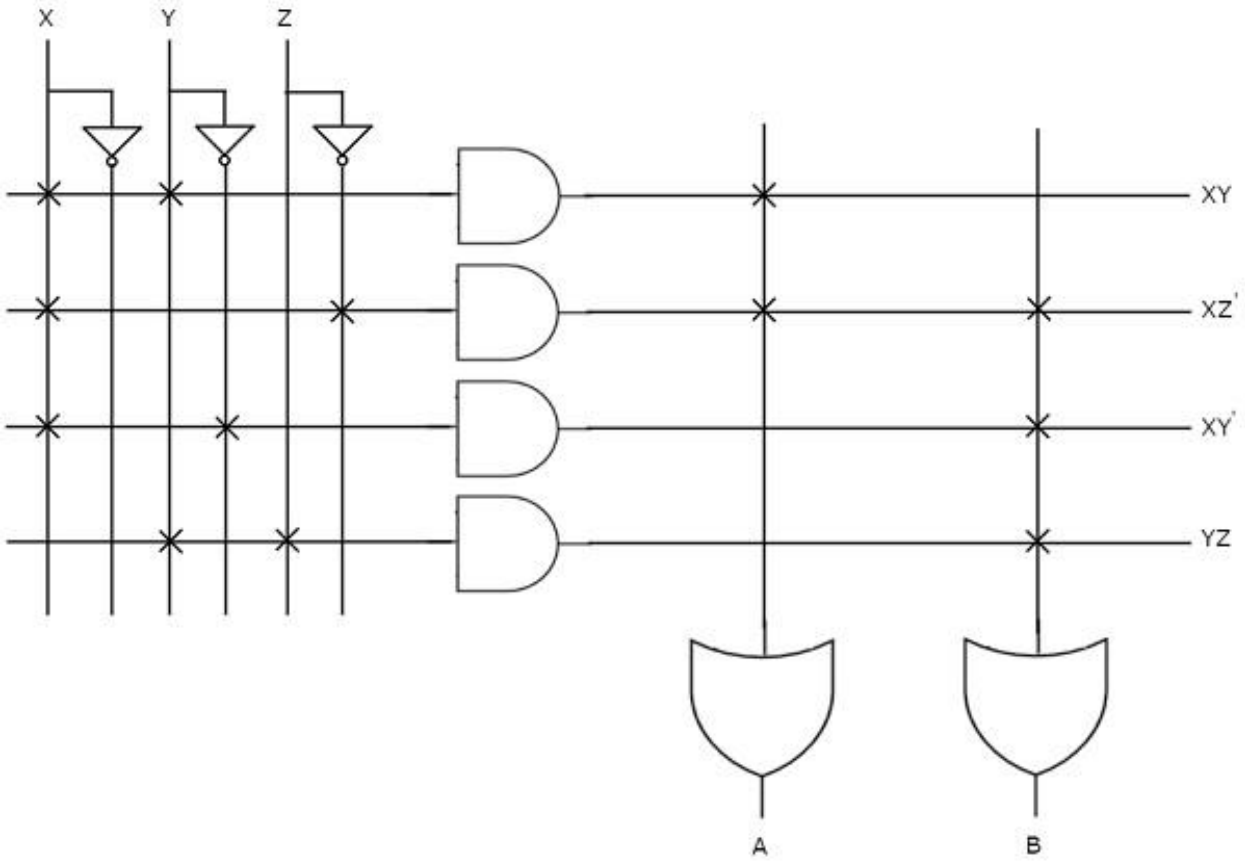
7.9 Programmable Logic Array

Solutions,

The corresponding PLA

$$A = XY + XZ'$$

$$B = XY' + YZ + XZ'$$



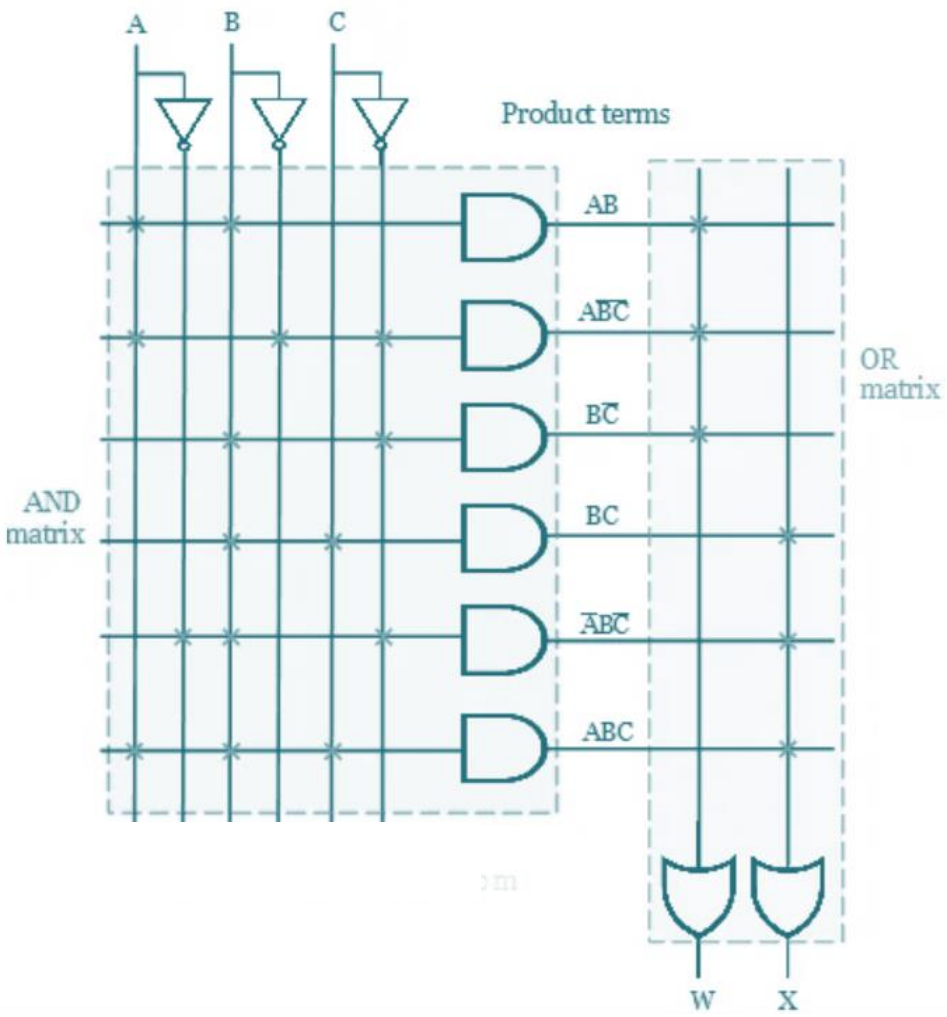
7.9 Programmable Logic Array

Example.

Implement

X = AB + AB'C' + BC' and

Y = BC + A'BC' + ABC using PLA



References

M. Morris Mano, Digital Design, 5th ed, Prentice Hall, 2012, **Chapter 5**

Next Topic : Sequential Circuit and Flip-Flop