

## Topic 3. Logic Gates

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## Subtopic

3.1 Basic Logic Gates

3.2 Type of Logic Gates





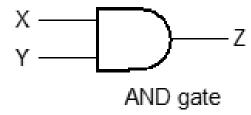


- Logic Gates are used to perform logic function
- Logic Gates also used to design logic circuit
- Logic Gates perform operation on one or more logic function and provide single output
- There are 3 Basic Gates, 2 Universal Gates, and 2 Special Gates

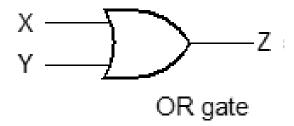
- Basic gates: AND, OR, NOT
- Universal gates: NAND, NOR (by using those gates we can implement all other gates
- Special gate: EX-OR, EX-NOR (XOR, NOR)

#### **BASIC GATES**

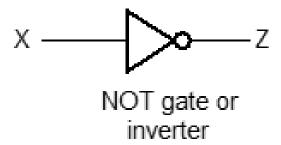
AND = multiplication functionality



• OR = addition functionality



• NOT = complement functionality



where 
$$Z = \bar{X}$$

#### **UNIVERSAL GATES**

• NAND: AND + NOT

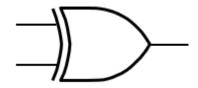
• NOR : OR + NOT

$$\begin{array}{c|c}
x \\
Y \\
Z
\end{array}$$

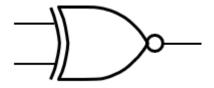
$$F(X,Y,Z) = \overline{X} + \overline{Y} + \overline{Z}$$

#### **SPECIAL GATES**

• XOR: eXclusive OR



• XNOR: eXclusive NOR (complement of XOR)



There are other concepts that will be used in this topic

Truth table

Has **one column for each input variable** (for example, A and B), and **one final column showing all of the possible results** of the logical operation that the table represents

Timing diagram

Representation of a set of signals in the time domain

For example

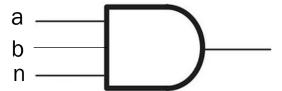


#### **BASIC GATES**

**AND GATE:** Logical multiplication

2 input AND gate
a
b

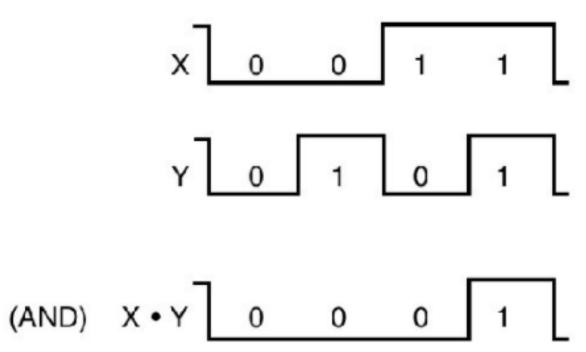
n input AND gate



#### Truth table

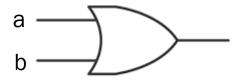
Inputs		Output	
A	В	Y=A.B	
0	0	0	
0	1	0	
1	0	0	
1	1	1	

Timing diagram AND GATE

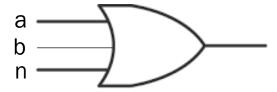


**OR GATE:** Logical addition

2 input OR gate



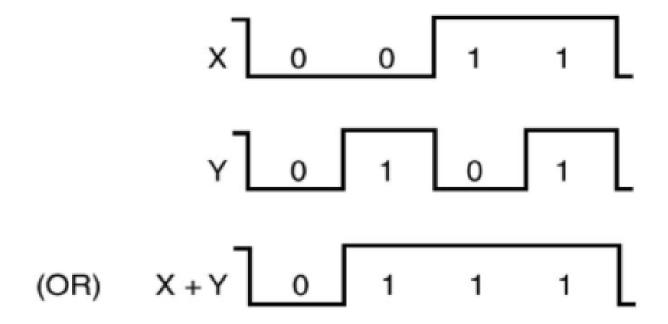
n input OR gate



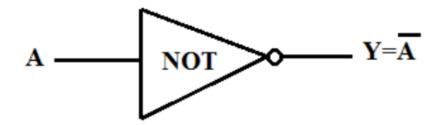
Truth table

Inputs		Output	
A	В	Y=A+B	
0	0	0	
0	1	1	
1	0	1	
1	1	1	

Timing diagram OR GATE



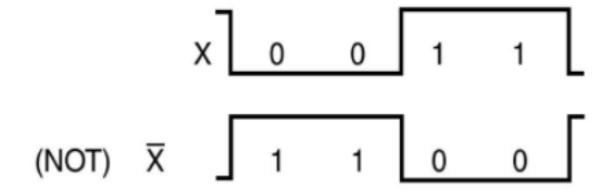
**NOT GATE:** complement



Truth table

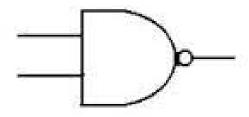
Input	Output	
A	$Y = \overline{A}$	
0	1	
1	0	

Timing diagram NOT GATE

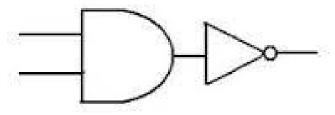


#### **UNIVERSAL GATE**

NAND GATE: AND + NOT



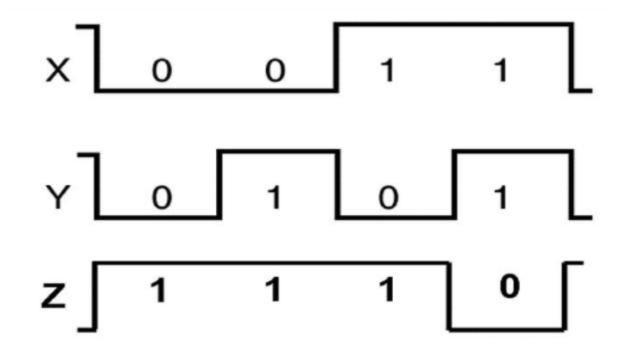
The symbol can also be represented as



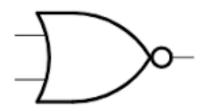
Truth table

Inputs		Output	
A	В	Y= <u>A. B</u>	
0	0	1	
0	1	1	
1	0	1	
1	1	0	

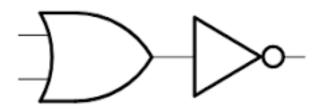
Timing diagram NAND GATE



NOR GATE: OR + NOT



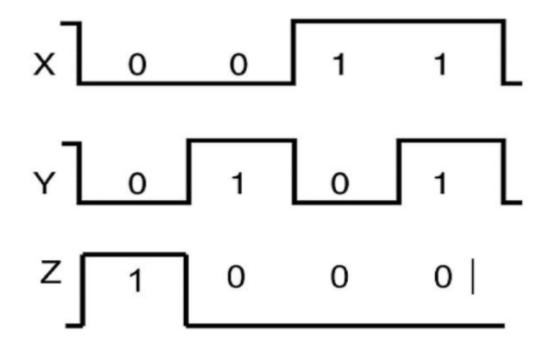
The symbol can also be represented as



Truth table

Inputs		Output	
A	В	$Y = \overline{A + B}$	
0	0	1	
0	1	0	
1	0	0	
1	1	0	

Timing diagram NOR GATE



#### **SPECIAL GATE**

**EX-OR GATE**: Exclusive OR

has the output only high when an odd number of inputs are high

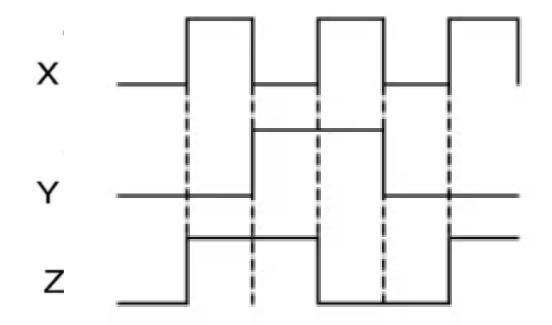
he output is low when both the inputs are low, and both the inputs are high



#### Truth table

Inputs		Output	
A	В	Y=А⊕В	
0	0	0	
0	1	1	
1	0	1	
1	1	0	

Timing diagram EX-OR GATE



#### **EX-NOR GATE:** Exclusive NOR

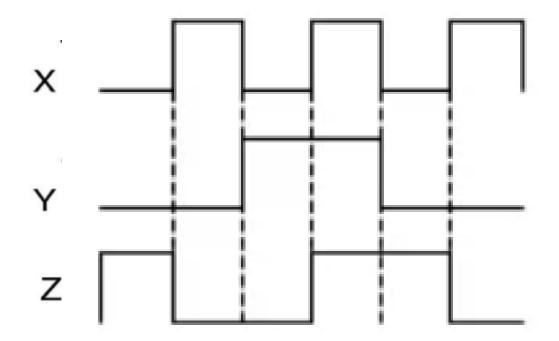
has the output only high when both the inputs have the same values either high or low



#### Truth table

Inputs		Output	
A	В	Y=A ⊕ B	
0	0	1	
0	1	0	
1	0	0	
1	1	1	

• Timing diagram EX-NOR GATE



#### Properties of XOR and XNOR GATE

X	0	0	=	X
	147	U	_	/\

• 
$$X \oplus Y' = X' \oplus Y = (X \oplus Y)' = X \otimes Y$$

- X ⊕ Y = X' ⊕ Y' (same with XNOR)
- X ⊕ Y = Y ⊕ X (commutative, same with XNOR)
- X ⊕ (Y ⊕ Z) = (X ⊕ Y) ⊕ Z (associative, same with XNOR)

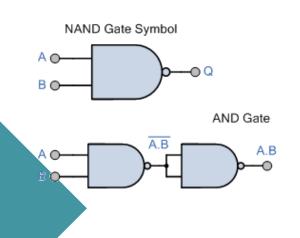
 $X \otimes 0 = X'$ 

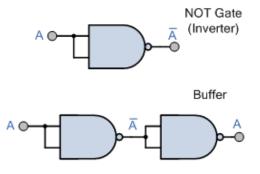
 $X \otimes 1 = X$ 

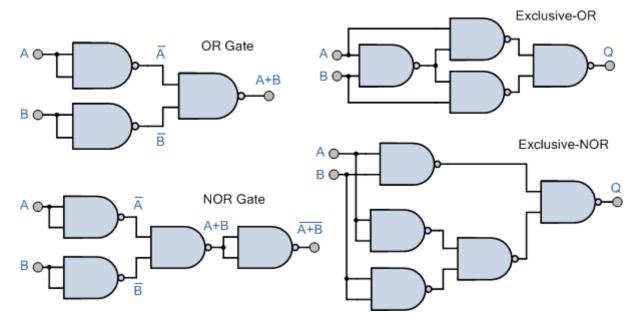
 $X \otimes X = 1$ 

 $X \otimes X' = 0$ 

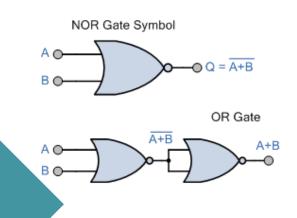
#### **NAND** Realization

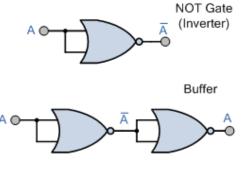


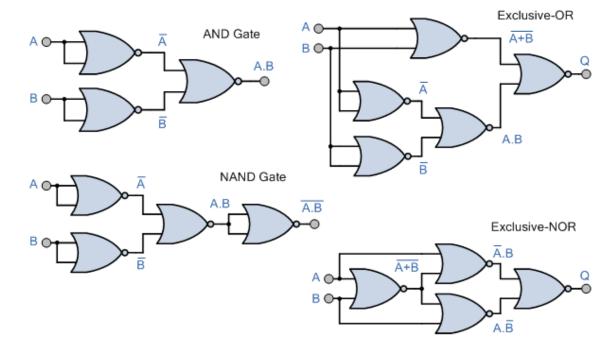




#### **NOR Realization**



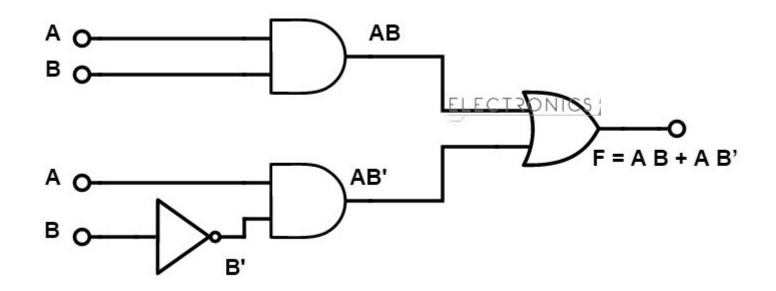






Example.

Implement  $AB + A\overline{B}$  using logic gate



Example.

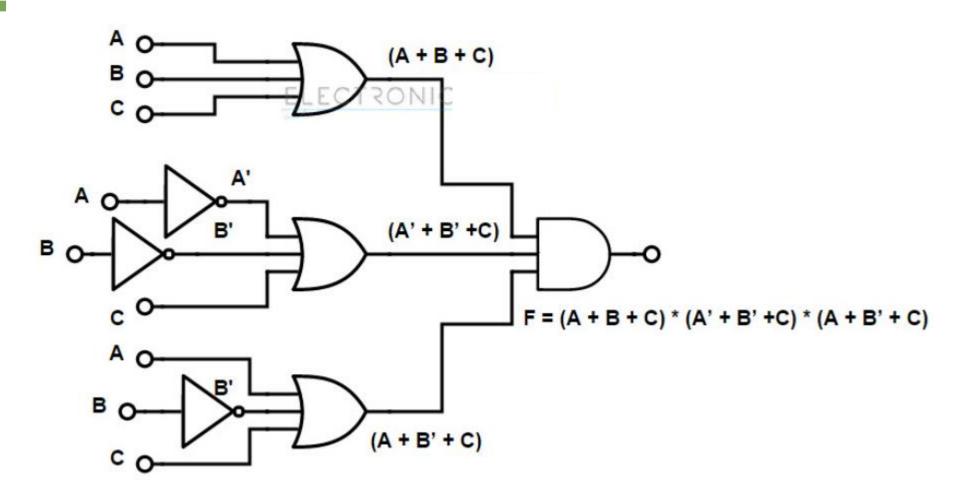
Implement

$$(A+B+C)$$
.

$$(\bar{A} + \bar{B} + C)$$
.

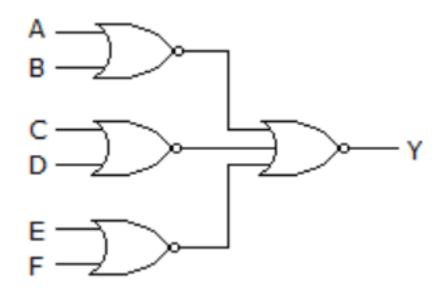
$$(A + \overline{B} + C)$$

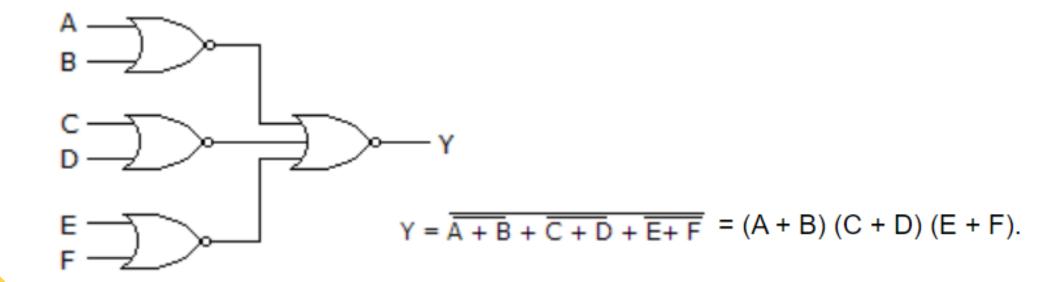
using logic gate



Example.

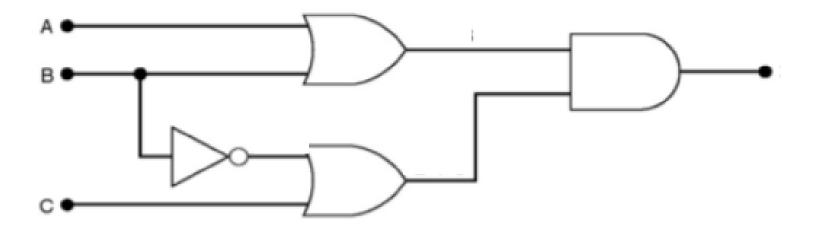
Find the Boolean equation of the following logic circuit

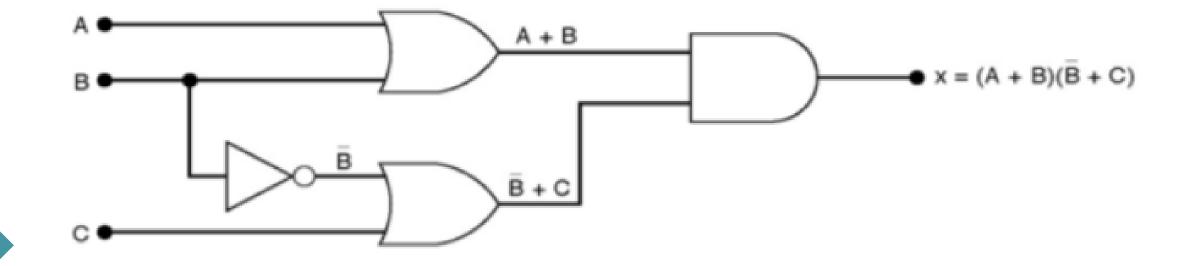




Example.

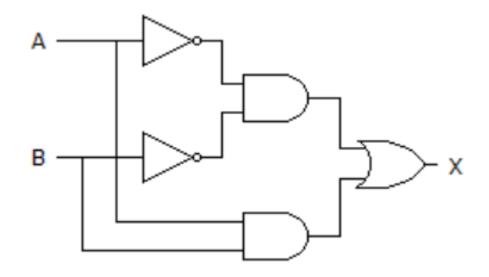
Find the Boolean equation of the following logic circuit

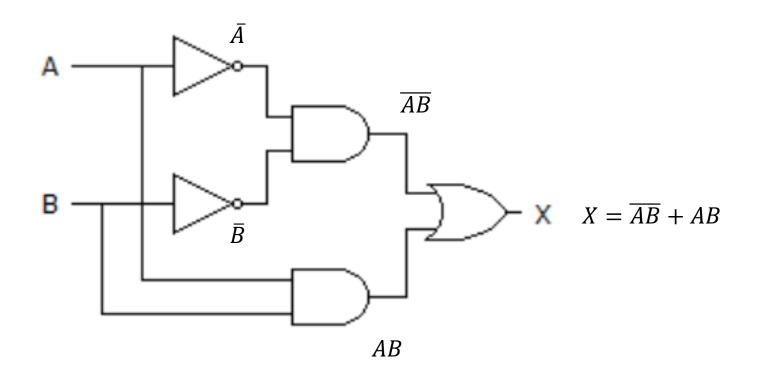




Example.

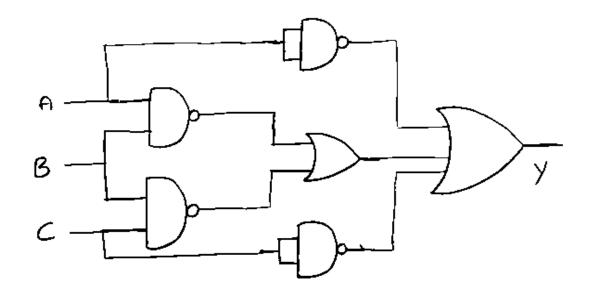
Find the logic expression for the logic circuit below

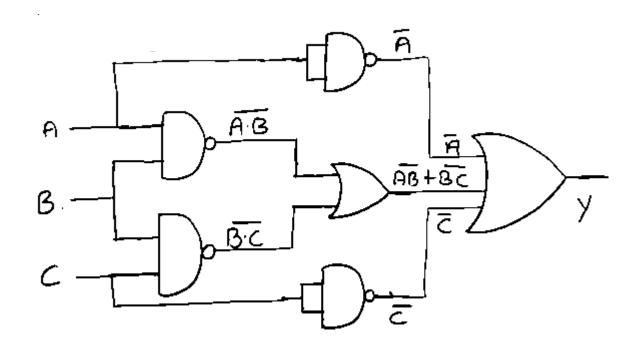




Example.

Find the output for the logic circuit below.





The output is

$$Y = \overline{A} + \overline{AB} + \overline{BC} + \overline{C}$$

$$= \overline{A} + \overline{A} + \overline{B} + \overline{B} + \overline{C} + \overline{C}$$

$$= \overline{A} + \overline{B} + \overline{C}$$

## References

M. Morris Mano, Digital Design, 5<sup>th</sup> ed, Prentice Hall, 2012, **Chapter 2** 



## **Next Topic: K-MAP**