

Diploma of Associate Engineer

Computer Information Technology
(2nd Year)



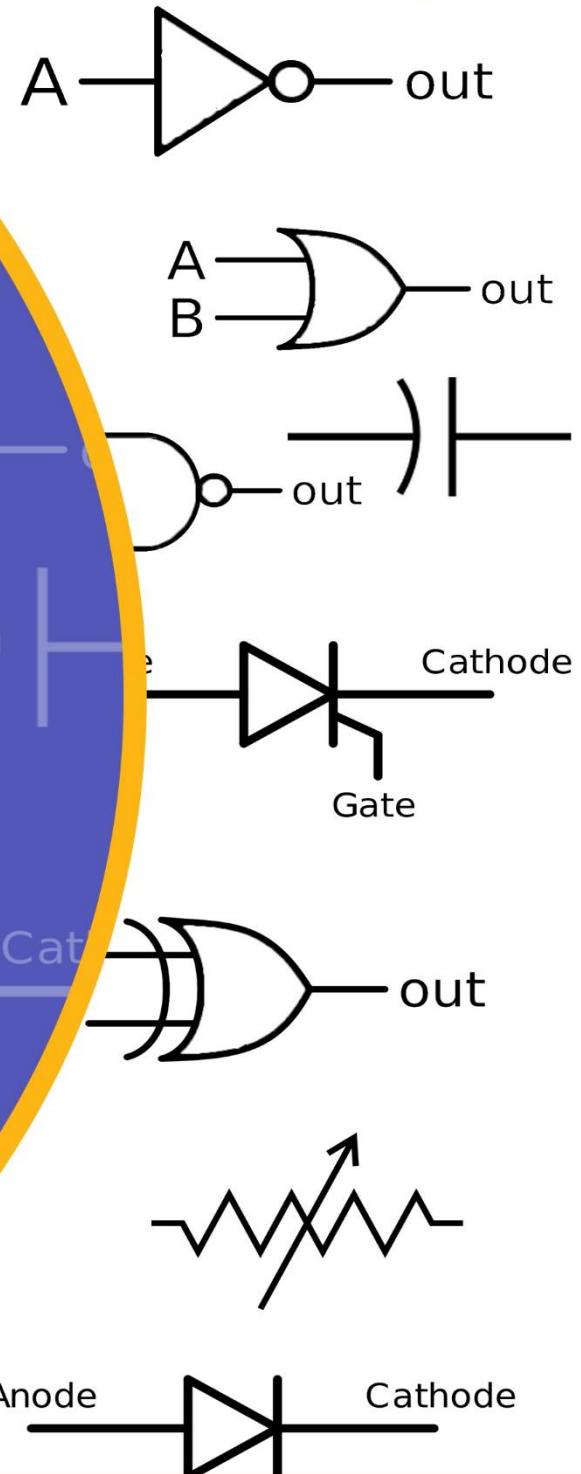
Approved by TEVTA

Text Book of

Electronics-II

CIT-244

Text Book of Electronics-II CIT-244



Academics Wing

Technical Education & Vocational Training Authority
Punjab

ELECTRONICS-II

CIT-244

FOR DAE 2ND YEAR

**TECHNICAL EDUCATION & VOCATIONAL
TRAINING AUTHORITY PUNJAB**

PREFACE

We are thankful to Almighty ALLAH who gave us an opportunity to write the book under the Title “Electronics-II” as a textbook for Diploma of Associate Engineer (DAE) 2nd Year CIT Technology. This book is intended to cover the syllabus of the subject “Electronics-II”, according to the new scheme of studies. The book overall addresses the challenges of learning when prerequisite knowledge varies from student to student.

The main objectives of the course outline have been covered and a very simple and easy approach has been focused for the elaboration of the various topics. Frequent use of illustrative figures has been made for clarity.

This book also includes objective type, short and long questions at the end of each chapter for self-test, which will serve as a quick learning tool for students.

We have no valuable words to express our thanks, but our hearts are full of favours received from every person whose valuable recommendations have made the book user friendly.

We made every effort to make the book valuable both for students and teachers; however, we shall gratefully welcome to receive any suggestion for the further improvement of the book.

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BOOLEAN ALGEBRA**CHAPTER-1****Objectives**

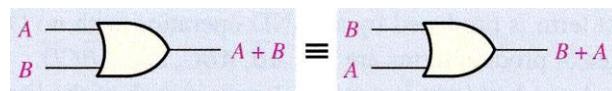
At the end of this chapter, a student will be able to

- Use Boolean Expressions and Truth Tables.
- Use Min-term Expressions, Sum of Products.
- Use Max-term Expressions, Product of Sums.
- Describe Un-simplified Boolean Expression & develop Schematic Circuits.
- Apply Logic Simplifications.
- Use Boolean Simplification.
- Use De-Morgan's Theorems.
- Use Karnaugh Mapping.

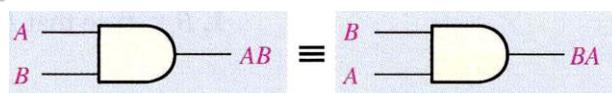
*Boolean algebra was invented by **George Boole** in 1854. Boolean Algebra is used to analyze and simplify the digital (logic) circuits. It uses only the binary numbers i.e. 0 and 1.*

BOOLEAN LAWS***COMMUTATIVE LAWS***

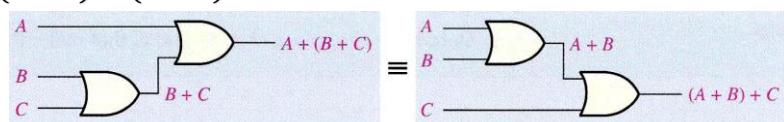
$$1- A + B = B + A$$



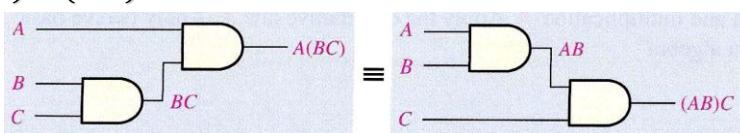
$$2- A \cdot B = B \cdot A$$

***ASSOCIATIVE LAWS***

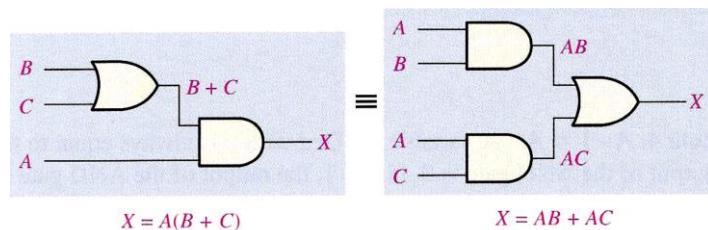
$$1- A + (B + C) = (A + B) + C$$



$$2- A \cdot (B \cdot C) = (A \cdot B) \cdot C$$

***DISTRIBUTIVE LAW***

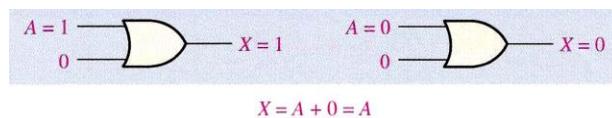
$$A \cdot (B + C) = A \cdot B + A \cdot C$$



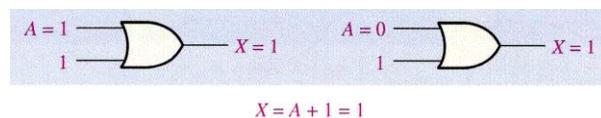
BOOLEAN RULES

OR RULES

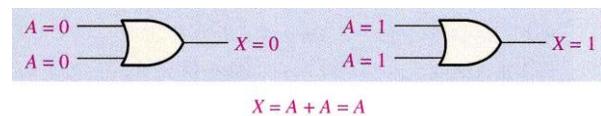
1- $A + 0 = A$



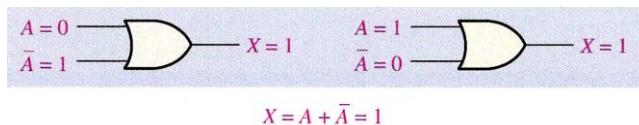
2- $A + 1 = 1$



3- $A + A = A$

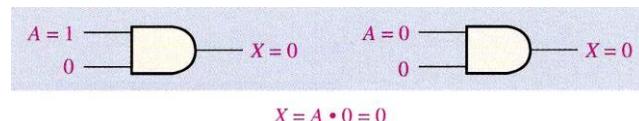


4- $A + \bar{A} = 1$

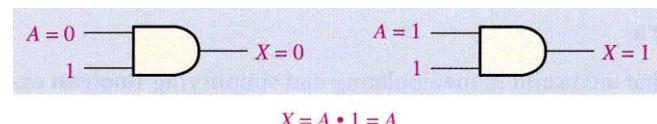


AND RULES

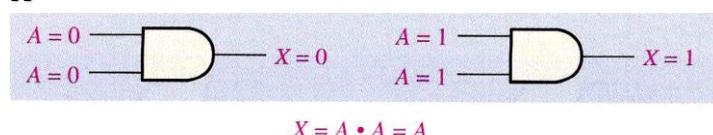
5- $A \cdot 0 = 0$



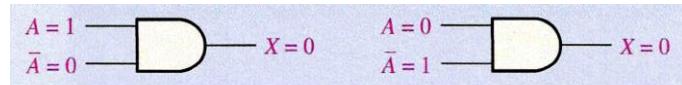
6- $A \cdot 1 = A$



7- $A \cdot A = A$



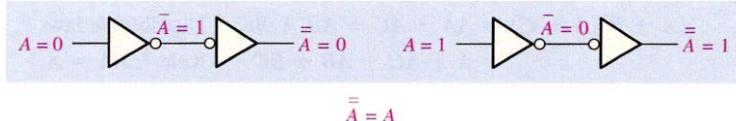
8- $A \cdot \bar{A} = 0$



$$X = A \cdot \bar{A} = 0$$

NOT RULE

9- $\bar{\bar{A}} = A$



$$\bar{\bar{A}} = A$$

SPECIAL RULES

10- $A + AB = A$

$$= A \cdot (1 + B) = A \cdot 1 = A$$

11- $A + \bar{A} \cdot B = A + B$

$$= (A + AB) + \bar{A}B \quad A = A + AB$$

$$= (AA + AB) + \bar{A}B \quad A = AA$$

$$= AA + AB + A\bar{A} + \bar{A}B \quad A\bar{A} = 0$$

$$= (A + \bar{A})(A + B)$$

$$= 1 \cdot (A + B) \quad A + \bar{A} = A$$

$$= A + B$$

12- $(A + B) \cdot (A + C) = A + B \cdot C$

$$= A \cdot A + A \cdot C + A \cdot B + B \cdot C$$

$$= A + A \cdot C + A \cdot B + B \cdot C \quad A \cdot A = A$$

$$= A(1 + C + B) + B \cdot C$$

$$= A \cdot 1 + B \cdot C \quad 1 + C + B = 1$$

$$= A + B \cdot C \quad A \cdot 1 = A$$

Logic Simplification by Boolean Algebra & Schematic Circuit

Example 1.1: Using Boolean algebra, simplify following expression.

$$AB + A(B + C) + B(B + C)$$

Solution:

$$AB + AB + AC + BB + BC \quad ; \text{Applying distributing law}$$

$$AB + AC + B + BC \quad ; AB + AB = AB, \quad BB = B$$

$$AB + AC + B(1 + C) = AB + AC + B \quad ; 1 + C = 1, \quad B \cdot 1 = B$$

$$AB + B + AC = B(A + 1) + AC = B + AC$$

Schematic Circuit:

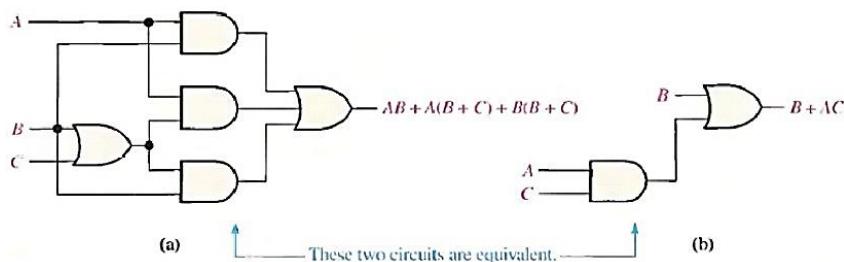


Fig. 1.1

SUM OF PRODUCTS

Product term is called a min-term. In min-term, we look for the functions where the output results in “1”. When two or more product terms are summed by Boolean addition, the resulting expression is a sum-of-products (SOP) also known as Sum of min-terms. Some examples are;

$$\begin{aligned} &AB + ABC \\ &ABC + CDE + \bar{B}CD \\ &\bar{A}B + \bar{A}B\bar{C} + AC \end{aligned}$$

Also, an SOP expression can contain a single-variable term, as in $A + \bar{A}BC + BC\bar{D}$

Implementing an SOP expression simply requires ORing the outputs of two or more AND gates. This is called AND-OR logic. Fig. 1.2 shows the implementation for the expression $AB + BCD + AC$.

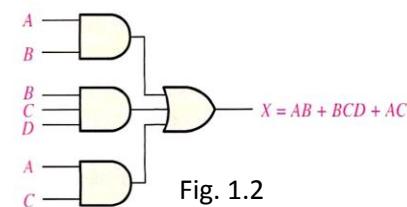


Fig. 1.2

Conversion of a general expression to SOP form

Any logic expression can be changed into SOP form by applying Boolean algebra techniques.

For example, the expression $A(B + CD)$ can be converted to SOP form by applying the distributive law:

$$A(B + CD) = AB + ACD$$

PRODUCT OF SUMS

Sum term is called max-term. In max-term, we look for the functions where the output results in “0”. When two or more sum terms are multiplied, the resulting expression is a product-of-sums (POS) also known as Product of max-terms. Some examples are

$$(\bar{A} + B)(A + \bar{B} + C)$$

$$(A + \bar{B} + C)(C + \bar{D} + \bar{E})(\bar{B} + C + D)$$

$$(A + B)(\bar{A} + B + \bar{C})(A + C)$$

A POS expression can contain a single-variable term, as in $\bar{A}(\bar{A} + \bar{B} + C)(B + C + \bar{D})$.

Implementing a POS expression simply requires ANDing the outputs of two or more OR gates. This is called OR-AND logic. Fig. 1.3 shows the implementation for the expression $(A+B)(B+C+D)(A+C)$.

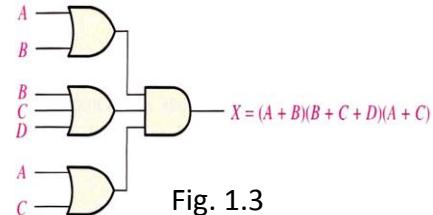


Fig. 1.3

DE-MORGAN'S LAWS

De-Morgan's theorems provide mathematical verification of the equivalency of the NAND and negative-OR gates and the equivalency of the NOR and negative-AND gates.

DE-MORGAN'S FIRST LAW

"The complement of a product of variables is equal to the sum of the complements of the variables." It can also be stated as,

"The complement of two or more ANDed variables is equivalent to the OR of the complements of the individual variables."

The formula for expressing this theorem for two variables is

$$\overline{XY} = \bar{X} + \bar{Y}$$

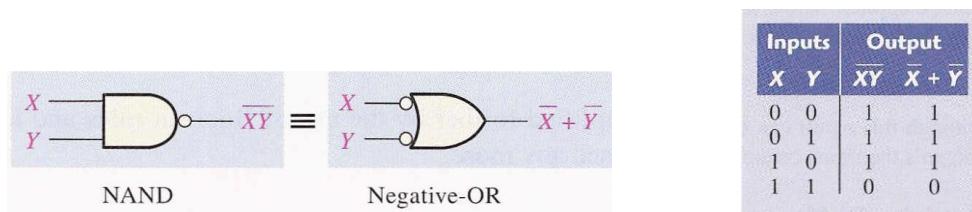


Fig. 1.4

DE-MORGAN'S SECOND LAW

"The complement of a sum of variables is equal to the product of the complements of the variables." It can also be stated as,

"The complement of two or more ORed variables is equivalent to the AND of the complements of the individual variables."

The formula for expressing this theorem for two variables is

$$\overline{X + Y} = \bar{X}\bar{Y}$$

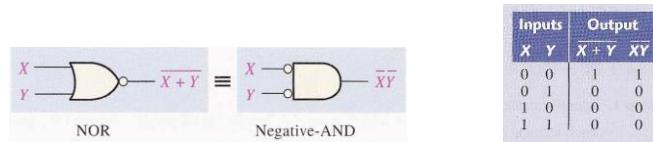


Fig. 1.5

Example 1.1: Apply De-Morgan's theorem to the expression $\overline{\bar{X} + \bar{Y} + \bar{Z}}$

Solution:

$$\overline{\bar{X} + \bar{Y} + \bar{Z}} = X + Y + Z$$

Example 1.2: Apply De-Morgan's theorem to the following expression.

$$\overline{(AB + C)(A + BC)}$$

Solution:

$$\overline{(AB + C)} + \overline{(A + BC)} = (\overline{AB})\bar{C} + \overline{A}(\overline{BC})$$

$$(\overline{A} + \overline{B})\bar{C} + \overline{A}(\overline{B} + \bar{C})$$

Example 1.3: Apply De-Morgan's theorem to the following expression.

$$\overline{\overline{A + BC} + D(\overline{E + F})}$$

Solution:

$$(\overline{A + BC}).(\overline{D(E + F)}) = (A + BC).\overline{(D(E + F))}$$

$$(A + BC).\left(\overline{D} + \left(\overline{\overline{E + F}}\right)\right) = (A + BC).\left(\overline{D} + E + F\right)$$

KARNAUGH MAP

A Karnaugh map provides a systematic method for simplifying Boolean expressions and will produce the simplest SOP or POS expression.

A Karnaugh map is similar to a truth table because it presents all of the possible values of input variables and the resulting output for each value. Karnaugh map is an array of cells in which each cell represents a binary value of the input variables. Karnaugh maps can be used for expressions with two, three, and four variables.

The cells in a Karnaugh map are arranged so that there is only a single-variable change between adjacent cells. Adjacency is defined by a single-variable change. In the 3-variable map the 010 cell is adjacent to the 000 cell, the 011 cell, and the 110 cell. The 010 cell is not adjacent to the 001 cell, the 111 cell, the 100 cell, or the 101 cell.

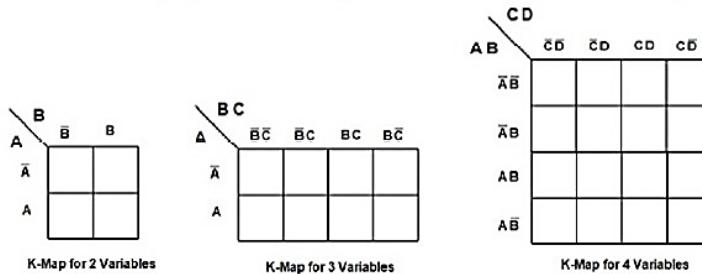


Fig. 1.6

The number of cells in a K-Map depends upon the number of variables and can be calculated using 2^N formula where N is the number of variables. Fig. 1.4 shows the format of K-map for two, three and four variables.

CONVERTING A TRUTH TABLE INTO K-MAP

In fig. 1.5 truth tables consisting of two, three and four variables and their respective K-maps are shown.

Truth Table	Boolean Expression	Karnaugh Map																																																																																																																																								
<table border="1" style="width: 100px; border-collapse: collapse;"> <thead> <tr> <th style="width: 30px;">A</th> <th style="width: 30px;">B</th> <th style="width: 30px;">Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <table border="1" style="width: 100px; border-collapse: collapse;"> <thead> <tr> <th style="width: 30px;">A</th> <th style="width: 30px;">B</th> <th style="width: 30px;">C</th> <th style="width: 30px;">Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <table border="1" style="width: 100px; border-collapse: collapse;"> <thead> <tr> <th style="width: 30px;">A</th> <th style="width: 30px;">B</th> <th style="width: 30px;">C</th> <th style="width: 30px;">D</th> <th style="width: 30px;">Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	A	B	Y	0	0	1	0	1	0	1	0	0	1	1	1	A	B	C	Y	0	0	0	1	0	0	1	0	0	1	0	0	0	1	1	1	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1	1	A	B	C	D	Y	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	1	1	0	1	1	0	0	0	1	1	1	0	1	0	0	0	0	1	0	0	1	0	1	0	1	0	0	1	0	1	1	0	1	1	0	0	1	1	1	0	1	1	1	1	1	0	0	1	1	1	1	0	$Y = \bar{A}\bar{B} + AB$ $Y = \bar{A}\bar{B}\bar{C} + \bar{A}BC + ABC$ $Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + AB\bar{C}\bar{D} + AB\bar{C}D$	<p>The Karnaugh maps show the mapped values from the truth tables for each variable combination. The first map has cells $\bar{B}\bar{A}$ and BA marked with 1. The second map has cells $\bar{A}\bar{B}\bar{C}$, $\bar{A}B\bar{C}$, and $AB\bar{C}$ marked with 1. The third map has cells $\bar{A}\bar{B}\bar{C}\bar{D}$, $\bar{A}\bar{B}\bar{C}D$, $AB\bar{C}\bar{D}$, and $AB\bar{C}D$ marked with 1.</p>
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Fig. 1.7

KARNAUGH MAP SOP MINIMIZATION

The Karnaugh map is used for simplifying Boolean expressions to their minimum form.

MAPPING A STANDARD SOP EXPRESSION

Step 1. Determine the binary value of each product term in the standard SOP expression. After some practice, you can usually do the evaluation of terms mentally.

Step 2. As each product term is evaluated, place a 1 on the Karnaugh map in the cell having the same value as the product term.

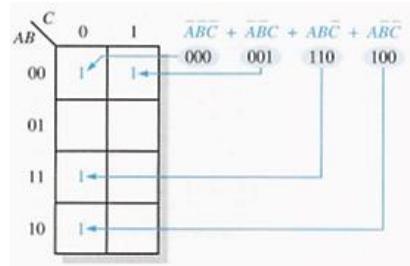


Fig. 1.8

KARNAUGH MAP SIMPLIFICATION OF SOP EXPRESSIONS

The process that results in an expression containing the fewest possible terms with the fewest possible variables is called minimization.

You can group 1s on the Karnaugh map according to the following rules by enclosing those adjacent cells containing 1s. The goal is to maximize the size of the groups and to minimize the number of groups.

1. A group must contain either 1, 2, 4, 8, or 16 cells, which are all powers of two. In the case of a 3-variable map, $2^3 = 8$ cells is the maximum group.
2. Each cell in a group must be adjacent to one or more cells in that same group, but all cells in the group do not have to be adjacent to each other.
3. Always include the largest possible number of 1s in a group in accordance with rule 1.
4. Each 1 on the map must be included in at least one group. The 1s already in a group can be included in another group as long as the overlapping groups include noncommon 1s.

DETERMINING THE MINIMUM SOP EXPRESSION FROM THE MAP

The following rules are applied to find the minimum product terms and the minimum SOP expression:

1. Group the cells that have 1s. Each group of cells containing 1s creates one product term composed of all variables that occur in only one form (either uncomplemented or complemented) within the group. Variables that occur both uncomplemented and complemented within the group are eliminated. These are called contradictory variables.
2. Determine the minimum product term for each group.
3. When all the minimum product terms are derived from the Karnaugh map, they are summed to form the minimum SOP expression.

Example 1.4: Using K-map simplify the following SOP expression.

$$A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$$

Step 1: First, draw three variable map and place “1” at the respective product terms given in SOP expression. Place “0” in rest of the cells as shown in fig.

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	1	1	1	0
A	1	1	0	0

Step 2: There are two groups containing “1” in above K-map. One is a quad and other is a pair.

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	1	1	1	0
A	1	1	0	0

Step 3: Simplify both groups. In quad \bar{B} is common whereas variables A & C are complemented to each other, so A & C are eliminated. In pair group \bar{A} and C are common whereas B variable is eliminated because this variable is complemented to each other.

Step 4: To form minimum SOP expression, sum the results of both groups which is $\bar{B} + \bar{A}C$

Example 1.5: Using K-map simplify the following SOP expression.

$$A\bar{B}CD + \bar{A}BCD + \bar{A}\bar{B}CD + \bar{A}BCD + ABC\bar{D} + ABC\bar{D}$$

Step 1: First, draw four variable map and place “1” at the respective product terms given in SOP expression. Place “0” in rest of the cells as shown in fig.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	0	1
$\bar{A}B$	0	0	1	1
$A\bar{B}$	0	0	0	1
AB	0	0	1	1

Step 2: There are three groups containing “1” in above K-map. One is a quad and other two are pairs.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	0	1
$\bar{A}B$	0	0	1	1
$A\bar{B}$	0	0	0	1
AB	0	0	1	1

Step 3: Simplify these groups. In quad $C\bar{D}$ is common whereas variables A & B are complemented to each other at left side, so A & B are eliminated. In first pair group \bar{A} , B, and C are common whereas D variable is eliminated because this variable is complemented to each other. In second pair group A, \bar{B} , and C are common whereas D variable is eliminated because this variable is complemented to each other.

Step 4: To form minimum SOP expression, sum the results of these three groups which is $C\bar{D} + \bar{A}BC + A\bar{B}C$

EXERCISE

SECTION-I (MCQ's)

1. Following is a POS expression.
 - (a) $A.B + C.D$
 - (b) $(A+B) . (C+D)$
 - (c) $(A+B). C.D$
 - (d) $A.B. (C+D)$
2. A 4-variable Karnaugh map has
 - (a) 4 cells
 - (b) 6 cells
 - (c) 8 cells
 - (d) 16 cells
3. $A + \bar{A}$ is equal to
 - (a) A
 - (b) \bar{A}
 - (c) 0
 - (d) 1
4. Product of Sum is also called
 - (a) Min Term
 - (b) Max Term
 - (c) Mid Term
 - (d) None of these
5. According to Boolean algebra $A + AB$ is equal to
 - (a) A
 - (b) \bar{A}
 - (c) B
 - (d) \bar{B}
6. In a K-map “1” indicates

- (a) Min Term (b) Max Term (c) Mid Term (d) None of these
7. $A(B+C) = AB + BC$ is law in Boolean algebra;
 (a) Commutative (b) Associative (c) Distributive (d) All of these
8. Following is commutative law of Boolean algebra
 (a) $A+B = A-B$ (b) $A+B = A.B$ (c) $A.B = A+B$ (d) $A+B = B+A$
9. The Boolean expression $A+B+C$ is a
 (a) Sum term (b) Min term (c) SOP (d) Literal
10. POS expression can be implemented by logic
 (a) AND-OR (b) OR-OR (c) OR-AND (d) AND-AND

ANSWER KEY

1.	b	2.	d	3.	d	4.	b	5.	a
6.	a	7.	c	8.	d	9.	a	10.	c

SECTION-II (Short Questions)

1. Define Boolean algebra.
2. Write four OR theorems.
3. Write four AND theorems.
4. Write Commutative Laws of Boolean algebra.
5. Write Associative Laws of Boolean algebra.
6. Write the equations of De -Morgan's Laws.
7. Prove that $A + AB = A$
8. Simplify the expression $B + A.B$
9. Define SOP expression with example.
10. Define POS expression with example.
11. What is the purpose of Karnaugh map?
12. Draw two variable Karnaugh map.
13. Draw three variable Karnaugh map.
14. How many cells are there in a 4 variables K-map?
15. What is the formula to calculate number of cells in a K-map?

SECTION-III (Long Questions)

1. Using Boolean algebra, simplify following expression and draw logic circuit of un-simplified and simplified circuit.

$$A\bar{B} + A(\bar{B} + \bar{C}) + B(\bar{B} + \bar{C})$$

2. Using K-map, simplify the following equation.

$$\bar{W}\bar{X}Y\bar{Z} + \bar{W}X\bar{Y}Z + \bar{W}\bar{X}YZ + WXY\bar{Z} + W\bar{X}\bar{Y}Z + \bar{W}XYZ + WX\bar{Y}\bar{Z}$$

3. Simplify using K-map.

$$F(W, X, Y, Z) = \sum(0, 1, 2, 5, 8, 10, 13)$$

4. Apply De-Morgan's theorems to the following expressions.

$$(a) \overline{ABC} + (\overline{D} + E) \quad (b) \overline{(A + B)C} \quad (c) \overline{A + B + C} + \overline{DE}$$

$$(d) \overline{\overline{XYZ}} + \overline{\overline{XY}\overline{Z}}$$

5. Prepare truth table for $\bar{X}\bar{Y}\bar{Z} + X\bar{Z} + \bar{X}Y\bar{Z}$

BINARY ARITHMETIC CIRCUITS

CHAPTER-2

Objectives

At the end of this chapter, a student will be able to

- Discuss Half Adder Circuit.
- Discuss Full Adder Circuit.
- Discuss N bit Binary Adder Circuit.
- Understand Binary Arithmetic functions with complements.
- Apply 2's and 1's Complement Notation in Addition and Subtraction.
- Discuss Binary Subtractor Circuit
- Discuss Binary Adder/ Subtractor Circuit.

Binary arithmetic circuits are carried out by combinational logic circuits which can perform basic arithmetic operations such as addition and subtraction. They include binary adder and binary subtractor. These circuits can be operated with binary values 0 and 1.

HALF ADDER

Half Adder is a logic circuit which adds two bits. The half-adder accepts two binary digits on its inputs and produces two binary digits on its outputs, a sum bit and a carry bit.

When we add two bits, we have to account two output bits called SUM and CARRY. The Carry output is a simple AND function, and the Sum is an Exclusive-OR. Thus, we can use two gates to add these two bits together.

Basic Rules of Binary Addition

$0 + 0 = 0$
$0 + 1 = 1$
$1 + 0 = 1$
$1 + 1 = 10$

Half adder Operation and Circuit

From the operation of the half-adder as stated in Table, expressions can be derived for the sum and the output carry as functions of the inputs. Notice that the output carry (C_0) is a 1 only when both A and B are 1s; therefore, C_0 can be expressed as the AND of the input variables.

$$C_{out} = AB$$

Now observe that the sum output (Σ) is a 1 only if the input variables, A and

B , are not equal. The sum can therefore be expressed as the exclusive-OR of the input variables.

$$\Sigma = A \oplus B$$

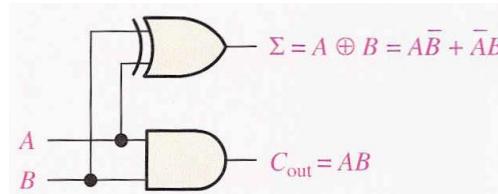


Fig. 2.1

From the above two equations, the logic implementation required for the half-adder function can be developed as shown in fig. 2.1.

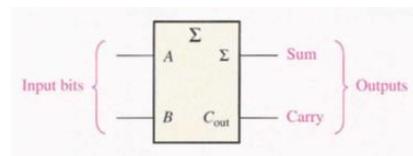
Truth Table and logic symbol of Half Adder

In fig. 2.2(a) and 2.2(b), truth table and logic symbol of half adder are shown.

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Fig. 2.2

(a)



(b)

FULL ADDER

Full Adder is a logic circuit which adds three bits. The full-adder accepts two input bits and an input carry and generates a sum output and an output carry.

We can use two half-adder circuits. The first will add A and B to produce a partial Sum, while the second will add C_{in} to that Sum to produce the final Σ output. If either half-adder produces a carry, there will be an output carry. Thus, C_{out} will be an OR function of the half-adder Carry outputs.

Full adder Operation and Circuit

The full-adder must add the two input bits and the input carry. For the input carry (C_{in}) to be added to the input bits, it must be ExORed with $A \oplus B$, yielding the equation for the sum output of the full adder.

$$\Sigma = (A \oplus B) \oplus C_{in}$$

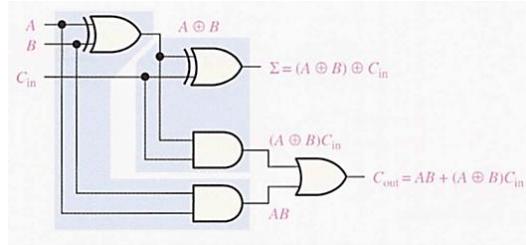


Fig. 2.3

The output carry is a 1 when both inputs to the first XOR gate are 1s or when both inputs to the second XOR gate are 1s. The output carry of the full-adder is therefore produced by the inputs A ANDed with B and $A \oplus B$ ANDed with C_{in} . These two terms are ORed, as expressed in following equation.

$$C_{out} = AB + (A \oplus B)C_{in}$$

This function is implemented and combined with the sum logic to form a complete full-adder circuit, as shown in Fig 2.3.

Block diagram of Full Adder

Notice in fig. 2.3 there are two half-adders, connected as shown in the block diagram fig. 2.4, with their output carries ORed.

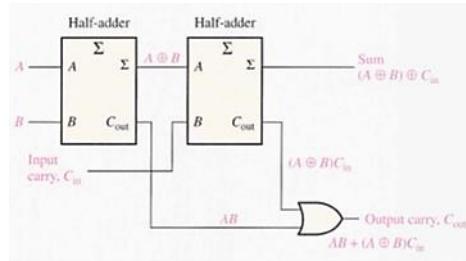


Fig. 2.4

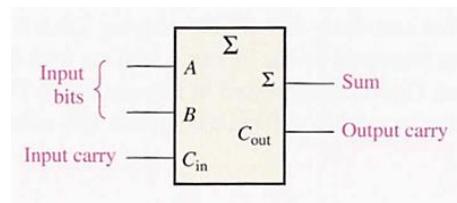
Truth Table and logic symbol of Full Adder

In fig. 2.5(a) and 2.5(b), truth table and logic symbol of half adder are shown.

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Fig. 2.5

(a)



(b)

N-BIT BINARY ADDER (PARALLEL ADDER)

Parallel adder is a logic circuit which can add two binary numbers. To add binary numbers with more than one bit, we must use additional full-adders. When one binary number is added to another, each column generates a sum bit and a 1 or 0 carry bit to the next column to the left, as illustrated here with 2-bit numbers.

$$\begin{array}{r}
 & 1 \\
 & | \\
 & 11 \\
 + & 01 \\
 \hline
 100
 \end{array}$$

2-bit parallel adder

To add two binary numbers, a full-adder is required for each bit in the numbers. So, for 2-bit numbers, two adders are needed as shown in fig.2.6.

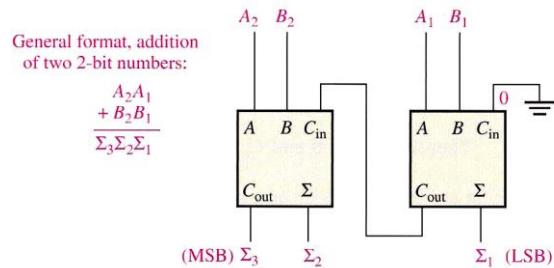


Fig. 2.6

3-bit parallel adder

For 3-bit numbers, three adders are needed. In the fig. 2.7, a 3-bit parallel adder is shown. In this adder two binary numbers 101 and 011 are being added.

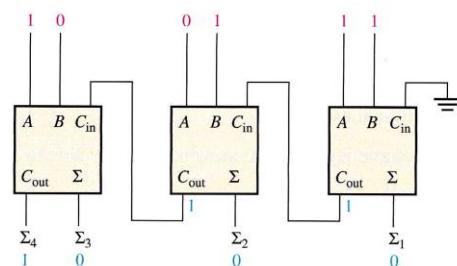


Fig. 2.7

4-bit parallel adder

A basic 4-bit parallel adder is implemented with four full-adder stages as shown in Fig. 2.8. The carry output of each adder is connected to the carry input of the next higher order adder as indicated. These are called internal carries.

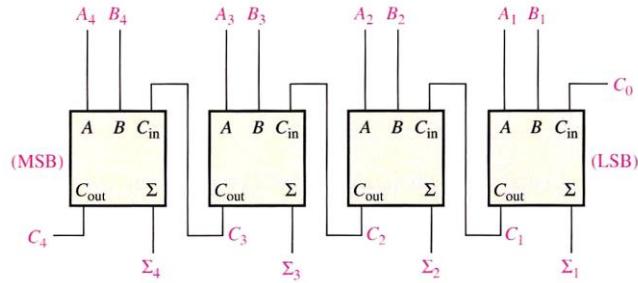


Fig. 2.8

1'S AND 2'S COMPLEMENT OF A BINARY NUMBER

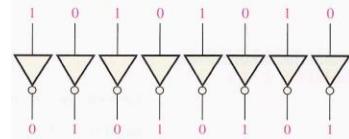
The 1's complement and the 2's complement of a binary number are important because they permit the representation of negative numbers. The method of 2's complement arithmetic is commonly used in computers to handle negative numbers.

1's Complement

The 1's complement of a binary number is found by changing all 1s to 0s and all 0s to 1s, as illustrated below:

$$\begin{array}{r}
 1\ 0\ 1\ 1\ 0\ 0\ 1\ 0 \quad \text{Binary number} \\
 \downarrow\downarrow\downarrow\downarrow\downarrow\downarrow\downarrow \\
 0\ 1\ 0\ 0\ 1\ 1\ 0\ 1 \quad \text{1's complement}
 \end{array}$$

The simplest way to obtain the 1's complement of a binary number with a digital circuit is to use parallel inverters.



2's Complement

The 2's complement of a binary number is found by adding 1 to the LSB of the 1's complement.

$$\text{2's complement} = (\text{1's complement}) + 1$$

Find the 2's complement of 10110010.

$$\begin{array}{r}
 10110010 \quad \text{Binary number} \\
 01001101 \quad \text{1's complement} \\
 + \quad 1 \quad \text{Add 1} \\
 \hline
 01001110 \quad \text{2's complement}
 \end{array}$$

Subtracting using 1's Complement

- i- To write down 1's complement of the subtrahend.
- ii- To add this with the minuend.
- iii- If the result of addition has a carry over, then it is dropped and 1 is added in the last bit.

iv- If there is no carry over, then 1's complement of the result of addition is obtained to get the final result and it is negative.

Example 2.1: Solve $(1011)_2 - (0111)_2$ using 1's complement method.

Solution:

$$\begin{array}{r}
 1 & 0 & 1 & 1 \\
 - 0 & 1 & 1 & 1 \\
 \hline
 & & & \\
 \end{array} \Rightarrow \begin{array}{r}
 1 & 0 & 1 & 1 \\
 + 1 & 0 & 0 & 0 \\
 \hline
 1 & 0 & 0 & 1 & 1 \\
 \hline
 & & & + 1 \\
 & & & \hline
 0 & 1 & 0 & 0
 \end{array}$$

Example 2.2: Solve $(0011)_2 - (1001)_2$ using 1's complement method.

Solution:

$$\begin{array}{r}
 0 & 0 & 1 & 1 & 3 \\
 - 1 & 0 & 0 & 1 & -9 \\
 \hline
 = -6
 \end{array} \Rightarrow \begin{array}{r}
 0 & 0 & 1 & 1 \\
 + 0 & 1 & 1 & 0 \\
 \hline
 1 & 0 & 0 & 1
 \end{array}$$

There is no carry. So, taking 1's complement of 1001 and it will be negative number.
0 1 1 0 = -6

Subtracting using 2's Complement

- i- At first, 2's complement of the subtrahend is found.
- ii- Then it is added to the minuend.
- iii- If the final carry over of the sum is 1, it is dropped and the result is positive.
- iv- If there is no carry over, the two's complement of the sum will be the result and it is negative.

Example 2.3: Solve $(1011)_2 - (0111)_2$ using 2's complement method.

Solution:

$$\begin{array}{r}
 1 & 0 & 1 & 1 \\
 - 0 & 1 & 1 & 1 \\
 \hline
 & & &
 \end{array} \Rightarrow \begin{array}{r}
 1 & 0 & 1 & 1 \\
 + 1 & 0 & 0 & 1 & \text{2's complement of subtrahend} \\
 \hline
 1 & 0 & 1 & 0 & 0 \\
 \hline
 & & & \xrightarrow{\text{Discard this carry}} \\
 & & & 0 & 1 & 0 & 0
 \end{array}$$

Example 2.4: Solve $(0011)_2 - (1001)_2$ using 1's complement method.

Solution:

$$\begin{array}{r}
 0 & 0 & 1 & 1 & 3 \\
 - 1 & 0 & 0 & 1 & -9 \\
 \hline
 = -6
 \end{array} \Rightarrow \begin{array}{r}
 0 & 0 & 1 & 1 \\
 + 0 & 1 & 1 & 1 & \text{2's complement of subtrahend} \\
 \hline
 1 & 0 & 1 & 0
 \end{array}$$

There is no carry. So, taking 2's complement of 1010 and it will be negative number.
0 1 1 0 = -6

HALF SUBTRACTOR

A half-subtractor is a combinational circuit that can be used to subtract one binary digit from another to produce a DIFFERENCE output and a BORROW output. Truth table of half subtractor is shown in fig. 2.9.

A	B	B_0	D
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

Fig. 2.9

Boolean Equations

The Boolean expressions for the two outputs are given by the equations.

$$D = \bar{A}B + A\bar{B}$$

$$B_0 = \bar{A}B$$

The expression for the DIFFERENCE (D) output is that of an EX-OR gate, the expression for the BORROW output (B_0) is that of an AND gate with input A complemented before it is fed to the gate. Fig. 2.10 shows the logic implementation of a half-subtractor and its symbol.

Circuit & Logic symbol

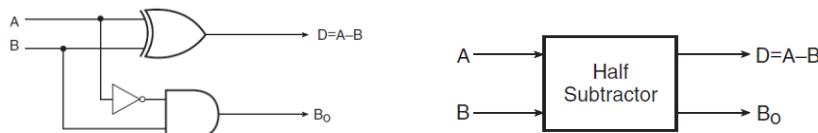


Fig. 2.10

FULL SUBTRACTOR

A full subtractor performs subtraction operation on two bits, a minuend and a subtrahend, and also takes into consideration whether a '1' has already been borrowed by the previous adjacent lower minuend bit or not. As a result, there are three bits to be handled at the input of a full subtractor, namely the two bits to be subtracted and a borrow bit designated as B_{in} .

A	B	B_{in}	B_0	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Fig. 2.11

There are two outputs, namely the DIFFERENCE output D and the BORROW output B_o . The BORROW output bit tells whether the minuend bit needs to borrow a '1' from the next possible higher minuend bit.

Truth table of half subtractor is shown in fig. 2.11.

Full Subtractor Boolean Equations

The Boolean equations for Difference output D and Borrow output B_o are given as follows:

$$B_o = \overline{A} \cdot B + \overline{A} \cdot B_{in} + B \cdot B_{in}$$

$$D = \overline{A} \cdot \overline{B} \cdot B_{in} + \overline{A} \cdot B \cdot \overline{B}_{in} + A \cdot \overline{B} \cdot \overline{B}_{in} + A \cdot B \cdot B_{in}$$

Full Subtractor Circuit

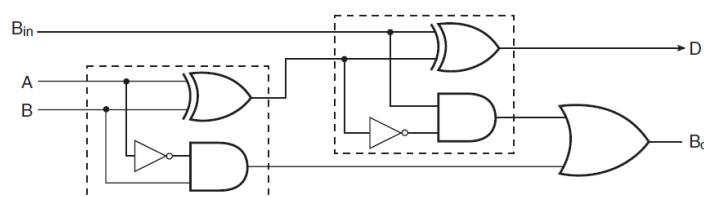


Fig. 2.12

Full Subtractor Block diagram

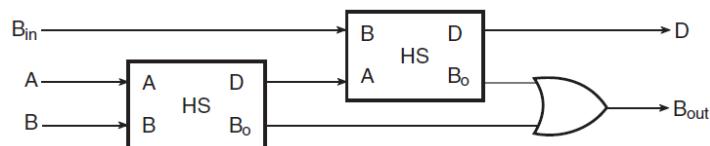


Fig. 2.13

BINARY ADDER / SUBTRACTOR

A binary adder/subtractor is a circuit that can be used to add as well as subtract two binary numbers using a control input.

Circuit Diagram

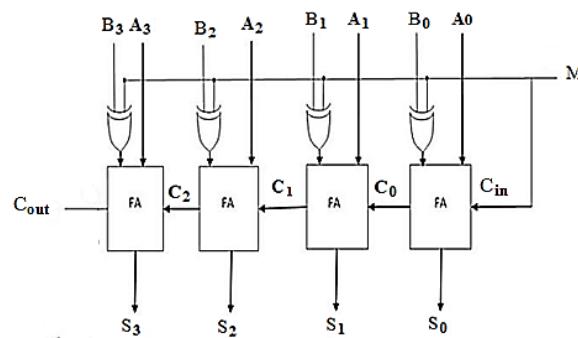


Fig. 2.14

An adder-subtractor is a circuit that is capable of adding or subtracting binary numbers. We can use Exclusive-OR gates to control whether we will add or subtract. With a control input of 0, the circuit acts as adder while with a control input of 1, the circuit acts as Subtractor.

Working

When the M input is in logic '0' state, the four bits of the binary number ($B_3 B_2 B_1 B_0$) are passed on as such to the B inputs of the corresponding full adders. The outputs of the full adders in this case give the result of addition of the two numbers.

When the M input is in logic '1' state, four bits of one of the numbers, ($B_3 B_2 B_1 B_0$) in the present case, get complemented. If the same '1' is also fed to the CARRY-IN of the LSB full adder, what we finally achieve is the addition of 2's complement and not 1's complement. Thus, in the adder arrangement of Fig. 2.14, we are basically adding 2's complement of ($B_3 B_2 B_1 B_0$) to ($A_3 A_2 A_1 A_0$). The outputs of the full adders in this case give the result of subtraction of the two numbers. The final carry (the CARRY-OUT of the MSB full adder) is ignored if it is not displayed.

EXERCISE

SECTION-I (MCQ's)

1. A full adder has

(a) 2-inputs, 2-outputs	(b) 2-inputs, 3-outputs
(c) 3-inputs, 2-outputs	(d) 3-inputs, 3-outputs
2. A logic circuit which adds only 2-bits is called

(a) Half Adder	(b) Full Adder	(c) Parallel Adder	(d) Both a & b
----------------	----------------	--------------------	----------------
3. If inputs to a half adder are $A = 1$ and $B = 1$, then outputs are

(a) $\Sigma = 1$, $Co = 0$	(b) $\Sigma = 1$, $Co = 1$	(c) $\Sigma = 0$, $Co = 1$	(d) $\Sigma = 0$, $Co = 0$
-----------------------------	-----------------------------	-----------------------------	-----------------------------
4. A full adder consists of

(a) Two XOR gates	(b) Two half adders and one OR gate
(c) Two AND gates	(d) Both a & c
5. A half adder consists of

(a) XOR and OR gate	(b) AND and NOT gate
(c) XOR and AND gate	(d) OR and AND gate
6. If inputs to a full adder are $A = 1$, $B = 1$, and $Cin = 0$, then outputs are

(a) $\Sigma = 0$, $Co = 1$	(b) $\Sigma = 1$, $Co = 1$	(c) $\Sigma = 1$, $Co = 0$	(d) $\Sigma = 0$, $Co = 0$
-----------------------------	-----------------------------	-----------------------------	-----------------------------
7. A half adder has

(a) 2-inputs, 2-outputs	(b) 2-inputs, 3-outputs
-------------------------	-------------------------

ANSWER KEY

1.	c	2.	a	3.	c	4.	b	5.	c
6.	a	7.	a	8.	b	9.	d	10.	c

SECTION-II (Short Questions)

1. Define half adder.
 2. Draw symbol of half adder.
 3. Draw logic diagram of half adder.
 4. Which logic gates are used in half adder circuit?
 5. When carry bit will be high in a two-bit adder?
 6. Develop the truth table for half adder.
 7. Write Boolean equations of half adder.
 8. Define full adder.
 9. Draw the logic diagram full adder.
 10. Write Boolean equations of full adder.
 11. Draw symbol of full adder.
 12. What is meant by 1's compliment?
 13. How can we find 2's complement of a binary number?
 14. Define half subtractor.
 15. Draw the diagram of half subtractor.
 16. Draw the symbol of half subtractor.
 17. Draw the truth table for half subtractor.
 18. Define full subtractor.
 19. Draw the symbol of full subtractor.
 20. What is meant by parallel adder?

SECTION-III (Long Questions)

1. Draw and explain the circuit of half adder with help of truth table.

2. Explain subtraction of two binary numbers using 2's complement method with examples.
3. Explain 4-bit adder subtractor using logic diagram.
4. Draw the logic diagram of full adder using half adders and explain its working.
5. Solve following subtractions using both 1's and 2's complement methods.
 - (a) $(10010)_2 - (01101)_2$
 - (b) $(01011)_2 - (10010)_2$

COMBINATIONAL LOGIC CIRCUITS

CHAPTER-3

Objectives

At the end of this chapter, a student will be able to

- Describe Word Problem.
- Construct truth Table and create a logic equation from a truth table.
- Simplify the logic Equation and develop combinational logic circuits.
- Differentiate Level of Integration (SSI, MSI, LSI)
- Describe BCD to Decimal Converter.
- Describe Decimal to BCD Converter.
- Describe Binary to Hexadecimal Converter.
- Describe BCD to seven segment Decoder.
- Describe Multiplexing Circuits.
- Describe Demultiplexing Circuits.

Combinational Logic Circuits are memoryless digital logic circuits whose output at any instant in time depends only on the combination of its inputs.

Combinational circuit is a circuit in which we combine the different gates in the circuit, for example encoder, decoder, multiplexer and demultiplexer. Some of the characteristics of combinational circuits are following.

- The output of combinational circuit at any instant of time, depends only on the inputs.
- The previous state of input does not have any effect on the present state of the circuit.
- A combinational circuit can have an n number of inputs and m number of outputs.

COMBINATIONAL LOGIC WORD PROBLEMS

To work on combinational logic word problems, a standard "procedure" is recommended for obtaining the key points and limitations of the problem and formulating its solution.

Design Procedure of a word problem

Following standard procedure is recommended for extracting the key points and constraints of the problem and formulating its solution.

1. Understand the problem
2. Formulate the Problem in a suitable representation.

3. Choose an Implementation.
4. Apply the Design Procedure.

Understand the problem

The very first thing you must do is to understand the problem. The place to start is with the input/output behavior of the object being designed. Identify the inputs, outputs, and control signals. Sometimes it is helpful to draw a diagram, relating inputs, outputs, and control, to obtain a better understanding of the problem.

Formulate the Problem in a suitable representation

For combinational logic word problems, the appropriate representations are almost always Boolean equations or truth tables. These representations show the relationships between inputs, control, and outputs.

Choose an Implementation

The next step is to map this into something more effective, like logic gates. Before you can implement the system, you must choose a technology for implementation.

The kinds of choices available are two-level combinational networks of discrete gates or PALs/PLAs, MUX, Decoders, multilevel networks, memories such as ROMs etc.

Apply the Design Procedure

You have formulated the solution in terms of Boolean equations or truth tables, you have chosen an implementation approach, and now you must follow the algorithm to map your digital representation into an actual implementation.

For two-level networks, you will apply the techniques of Karnaugh Map to derive a circuit with the fewest number of product terms.

The approach is the same whether the implementation target is discrete gates or programmable logic.

For a ROM-based design, only the truth table is needed; there is no need to minimize your logic description first.

Example 3.1: Suppose three water tanks are used to supply water in a residential colony. These tanks are filled through a water pump. Design a system that if two or more than two water tanks are empty, water pump should be ON otherwise it will remain OFF.

Step No: 1. In this problem, water tanks are inputs namely A, B, and C. Water pump is an output namely Y. A logic "0" shows empty tank and logic "1" shows full tank for the inputs. At the output side, a logic "0" shows OFF pump, whereas logic "1" shows ON pump.

Step No: 2. We make a truth table of above problem.

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Converting this truth table into Boolean expression, we get

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + AB\bar{C}$$

Step No: 3. We choose discrete gates technology for implementation. For this purpose, we have to minimize the above Boolean equation.

Step No: 4. For simplifying the Boolean equation, we use Karnaugh Map technique.

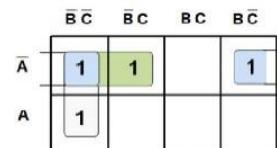


Fig. 3.1

Simplified Boolean Equation is $Y = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$

Step No: 5. Develop Combinational Logic Circuit.

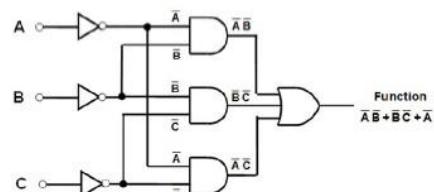


Fig. 3.2

LEVELS OF INTEGRATION

Small-Scale Integration (SSI)

(SSI) describes fixed-function ICs that have up to ten equivalent gate circuits on a single chip, and they include basic gates and flip-flops.

Medium-Scale Integration (MSI)

Medium-scale integration (MSI) describes integrated circuits that have from 10 to 100 equivalent gates on a chip. They include logic functions such as encoders, decoders, counters, registers, multiplexers, arithmetic circuits, small memories, and others.

Large-Scale Integration (LSI)

Large-scale integration (LSI) is a classification of ICs with complexities of from more than 100 to 10,000 equivalent gates per chip, including memories.

Very Large-Scale Integration (VLSI)

Very large-scale integration (VLSI) describes integrated circuits with complexities of from more than 10,000 to 100,000 equivalent gates per chip.

Ultra-Large-Scale Integration (ULSI)

Ultra-large-scale integration (ULSI) describes very large memories, larger micro-processors, and larger single-chip computers. Complexities of more than 100,000 equivalent gates per chip are classified as ULSI.

BINARY TO HEXA-DECIMAL CONVERTER (DECODER)

A decoder is a combinational circuit that decodes the information on n input lines to a maximum of 2^n unique output lines. A decoder generally decodes a binary value into a non-binary one by setting exactly one of its n outputs to logic “1”.

In the fig. 3.3, a binary to hexa-decimal decoder is shown. This decoder is also called 4 lines to 16 lines decoder because it has 4 input lines and 16 output lines.

It consists of an array of 16 AND gates. The 4 binary inputs labelled A, B, C and D are decoded into one of 16 outputs. Each output represents one of the min-terms of the 4 input variables, (each output = a min-term).

The binary inputs A, B, C and D determine which output line from Y_0 to Y_{15} is “HIGH” while the remaining outputs are held “LOW”. So only one output can be active (HIGH) at any one time. Therefore, whichever output line is “HIGH” identifies the binary code present at the input, in other words it “de-codes” the binary input.

For example, when ABCD = 0001, only the Y_1 output is HIGH. If ABCD changes to 0100, only the Y_4 output goes HIGH.

If we check all possibilities (0000 to 1111), we will find that the subscript of the high output always equal to the hexa-decimal equivalent of ABCD as shown in table.

Some binary decoders have an additional input pin labelled “Enable” that controls the outputs from the device. This extra input allows the decoders outputs to be turned “ON” or “OFF” as required.

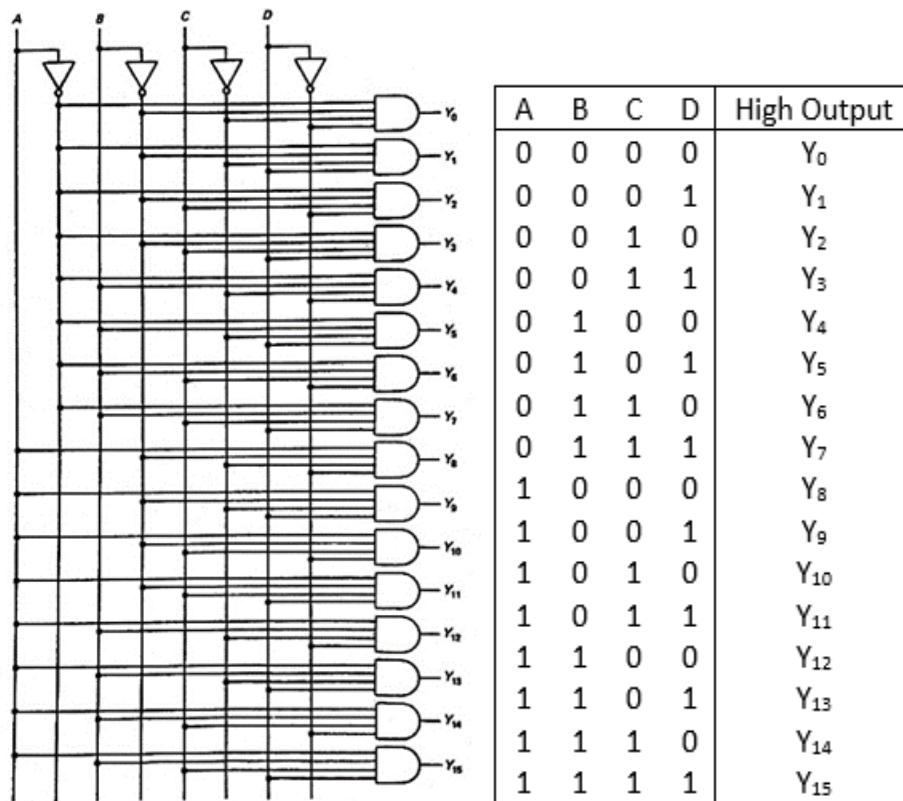


Fig. 3.3

Normally, a decoder is not built with separate inverters and AND gates. Instead we would use an IC such as the 74154. This IC is called a decoder-de-multiplexer because it can be used either as a decoder or a de-multiplexer.

BCD TO DECIMAL CONVERTER (DECODER)

The BCD-to-decimal decoder converts each BCD code to its decimal equivalent. BCD-to-decimal decoder has 4 inputs and 10 outputs. It accepts an input value consisting of a binary-coded decimal integer value and activates one specific, unique output for every input value in the range 0 to 9 (decimal). All outputs are held inactive when a non-decimal value is applied to the inputs. It is frequently referred as a 4-line-to-10-line decoder or a 1-of-10 decoder.

The method of implementation is the same as for the 1-of-16 decoder, except that only ten decoding gates are required because the BCD code represents only the ten decimal digits 0 through 9.

The binary inputs A, B, C and D determine which output line from Y_0 to Y_9 is "HIGH" while the remaining outputs are held "LOW". So only one output can be active (HIGH) at any one time. Therefore, whichever output line is "HIGH" identifies the binary code present at the input.

For example, when ABCD = 0001, only the Y_1 output is HIGH. If ABCD changes to 0100, only the Y_4 output goes HIGH.

All outputs are held inactive (LOW), when a non-decimal value (1010 to 1111) is applied to the inputs.

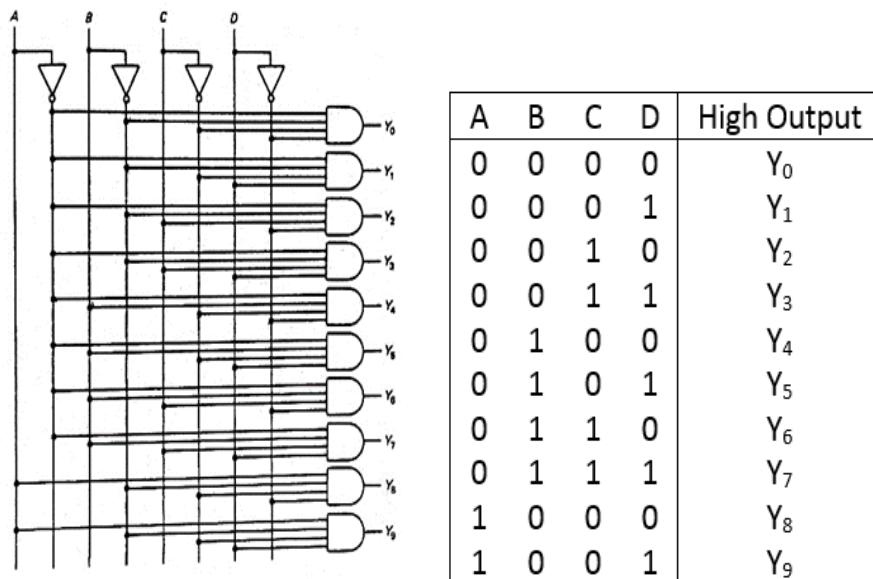


Fig. 3.4

The 74HC42 is an integrated circuit BCD-to-decimal decoder.

DECIMAL TO BCD CONVERTER (ENCODER)

An encoder is a combinational logic circuit that essentially performs a "reverse" decoder function. An encoder accepts an active level on one of its inputs representing a digit, such as a decimal or octal digit, and converts it to a coded output, such as BCD or binary.

The output lines of a digital encoder generate the binary equivalent of the input line whose value is equal to "1" and are available to encode either a decimal or hexadecimal input pattern to typically a binary or BCD (binary coded decimal) output code.

This type of encoder has ten inputs- one for each decimal digit-and four outputs corresponding to the BCD code, as shown in Fig. 3.5. This is a basic 10-line-to-4-line encoder.

The switches are push button switches like those of a pocket calculator. When button 3 is pressed, the Y_1 and Y_0 OR gates have high inputs and the output word becomes

$$Y_3 Y_2 Y_1 Y_0 = 0011$$

When switch 9 is pressed,

$$Y_3 Y_2 Y_1 Y_0 = 1001$$

The output word always equals the BCD equivalent of the switch being pressed.

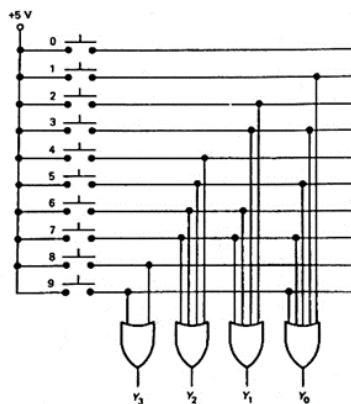


Fig. 3.5

The IC 74147 is available for a decimal to BCD encoder. The 74147 is a priority encoder because it gives priority to the highest-order input. If all inputs are low, the highest of these, D_9 , is encoded to get an output.

SEVEN SEGMENT DISPLAY

It is an electronic display device for displaying decimal numerals. It consists of 7 LEDs connected in parallel that can be lit in different combinations to display the numbers (0, 1, 2, 3, 4, 5, 7, 8, 9, A, B, C, D, E, F, etc.). Each segment (LED) is denoted by letters A to G.

The eighth segment called “Decimal Point” is denoted by DP and is used for the display of non-integer numbers.

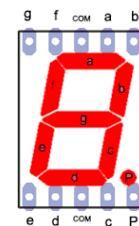
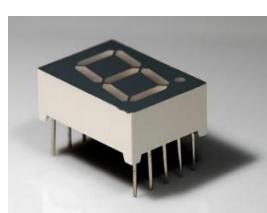


Fig. 3.6

There are two types of seven segment display.

1. Common anode display
2. Common cathode display

If anodes of all the LEDs are connected together and all the cathode are left alone, then we refer to the display as “Common Anode Type”.

If cathodes of all the LEDs are connected together and all the anodes are left alone, then we refer to the display as “Common Cathode Type”.

Internal connections of both displays are shown in fig. 3.7

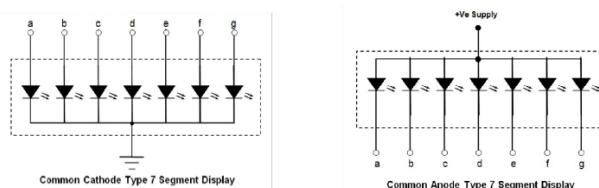


Fig. 3.7

BCD TO SEVEN SEGMENT DECODER

A seven-segment display has seven LED's but a BCD input consists of four bits. To drive a seven-segment display, a decoder is used which accepts 4-inputs and provides 7-outputs to produce a decimal readout. This decoder is called BCD to 7-segment decoder.

A BCD to seven segment decoder decodes the BCD code in such a way, that if we apply this decoded output to seven segment display then a decimal character is displayed equal to BCD input. In fig. 3.8, BCD code of “5” is applied to a BCD to seven segment decoder. At the output of decoder, a, c, d, f and g outputs becomes high whereas b and e outputs becomes low due to which the decimal number “5” displays as shown in fig. 3.8.

A truth table for common cathode type BCD to seven segment decoder is also shown. For Common Anode type seven segment LED display, we only have to interchange all ‘0’s and ‘1’s in the output side.

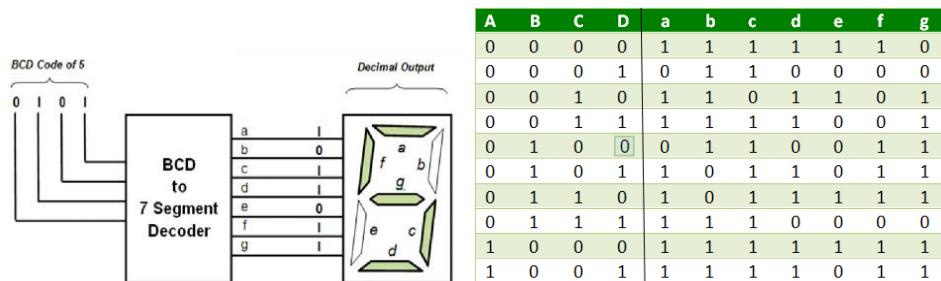


Fig. 3.8

7446 & 7448 IC

There are two types of decoder-drivers, corresponding to the common-anode and common-cathode indicators.

IC 7446 is used to drive a common-anode indicator. Logic circuits inside the 7446 convert the BCD input to the required output. For instance, if the BCD input is 0111, the internal logic of the 7446 will force LED's a, b, and c to conduct. As a result, digit 7 will appear on the indicator. You have to connect external current-limiting resistors between indicator and 7446.

IC 7448 is used to drive a common-cathode indicator. Logic circuits inside the 7448 convert the BCD input to the required output. For instance, if the BCD input is 0100, the internal logic of the 7448 will force LED's b, c, f, and g to conduct. As a result, digit 4 will appear on the indicator. Unlike the 7446, the 7448 has its own current limiting resistors on the chip.

MULTIPLEXER

A logic circuit which selects one input from many inputs by means of a control input. With help of rotary switch, we can select any input from n inputs as shown in fig. 3.9. This method is for analog as well as digital multiplexing.

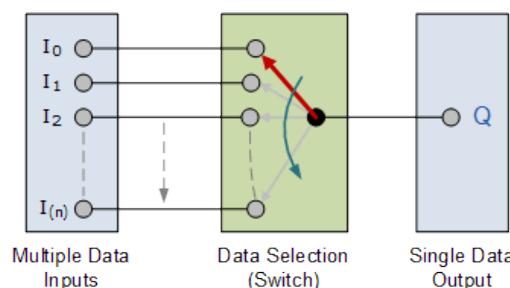


Fig. 3.9

In digital electronics, multiplexers are also known as data selectors because they can “select” each input line. In the fig. 3.10, inputs a and b are control inputs. A, B, C and D are data inputs. We can select any one input using a control word at a and b inputs.

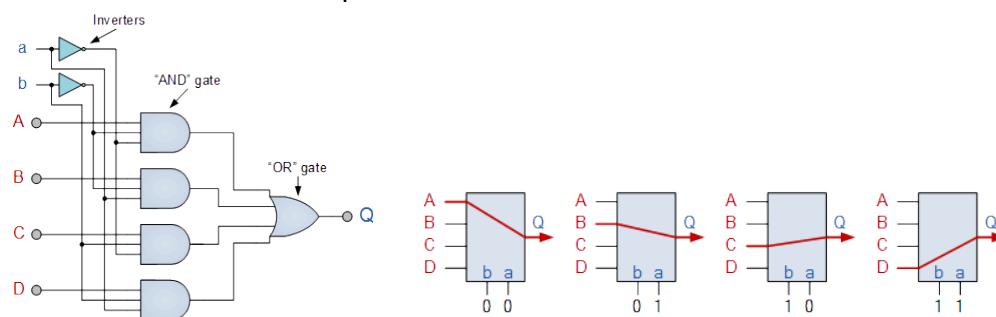


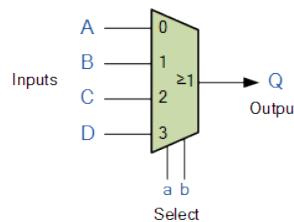
Fig. 3.10

We can show the selection of the data through the multiplexer as a function of the data select bits as shown.

Adding more control address lines, (n) will allow the multiplexer to control more inputs as it can switch 2^n inputs but each control line configuration will connect only ONE input to the output.

Multiplexer Symbol

The symbol used in logic diagrams to identify a multiplexer is as follows.



Multiplexer IC

74150 is a 16×1 multiplexer. It has 16 data inputs (D_0 to D_{15}), 4 Control inputs (A, B, C and D), One output (Y), One strobe and V_{CC} , Ground pins.

DEMULTIPLEXER

A logic circuit for transmitting a digital input one of N lines by means of a control word. The de-multiplexer takes one single input data line and then switches it to any one of a number of individual output lines one at a time as shown in fig. 3.11.

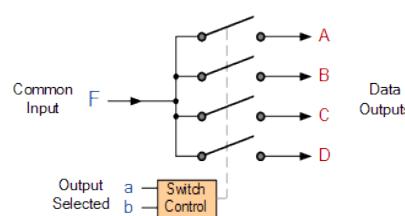


Fig. 3.11

In digital electronics, de-multiplexers are also known as data distributor. In the fig. 3.12, inputs a and b are control inputs. A, B, C and D are data outputs. Individual solid-state switches are selected by the binary input address code on the output select pins "a" and "b" as shown.

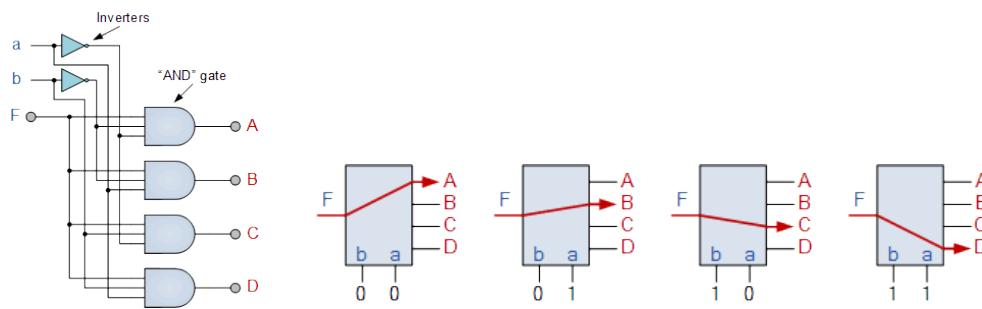
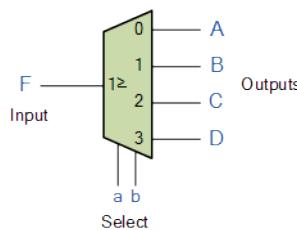


Fig. 3.12

Adding more address line inputs, it is possible to switch more outputs giving a 1-to- 2^n data line outputs.

De-Multiplexer Symbol

The symbol used in logic diagrams to identify a de-multiplexer is as follows.



De-Multiplexer IC

74150 is a 16×1 multiplexer. It has 16 data inputs (D_0 to D_{15}), 4 Control inputs (A, B, C and D), One output (X), One strobe and V_{CC} , Ground pins.

EXERCISE

SECTION-I (MCQ's)

1. A logic circuit which converts a decimal number to binary number is called
(a) Encoder (b) Decoder (c) Multiplexer (d) De-Multiplexer
2. Multiplexer is also called
(a) Decoder (b) Data Selector (c) Data Distributor (d) Encoder
3. When all LED's of seven segment are ON, the digit will be display
(a) 6 (b) 7 (c) 8 (d) 0
4. Which IC is 4×16 decoder?
(a) 74121 (b) 74154 (c) 74138 (d) 74151
5. An encoder converts a decimal number into
(a) Binary (b) Hexa-decimal (c) Decimal (d) None of these
6. A logic circuit which selects one input from many inputs by means of a control input.

ANSWER KEY

1. a 2. b 3. c 4. b 5. a
6. b 7. b 8. a 9. c 10. d
11. a

SECTION-II (Short Questions)

1. Define combinational logic circuit.
 2. What are integration levels of IC's?
 3. Differentiate SSI and MSI.
 4. Differentiate LSI and VLSI.
 5. Define seven segment display.
 6. Name types of seven segment display.
 7. Draw circuit connection of common anode display.
 8. Why display driver is used in seven segment display?
 9. Define encoder (Decimal to BCD converter).
 10. Define decoder (BCD to Decimal converter).
 11. What is the function of multiplexing circuit?
 12. What is the function of de-multiplexing circuit?

SECTION-III (Long Questions)

1. Explain decimal to BCD encoder with diagram.
 2. Draw the circuit of 8×1 multiplexer and explain its working.
 3. Explain the working of BCD to seven segment decoder.
 4. Explain BCD to decimal conversion with diagram.

SEQUENTIAL LOGIC CIRCUITS***CHAPTER-4*****Objectives**

At the end of this chapter, a student will be able to

- Describe Latches.
- Describe RS Flip Flop.
- Describe Clocked RS Flip Flop.
- Understand JK Flip Flop.
- Describe Operation of JK Flip Flop.
- Describe Positive and Negative Edge Trigger.
- Describe Positive-Level and Negative Level Trigger.
- Describe Master Slave Flip Flop.
- Describe D type Flip Flop.
- Describe T type Flip Flop.
- Understand 555 Timer IC.
- Explain 555 Timer as Monostable Multivibrator.
- Explain 555 Timer as Astable Multivibrator.

A sequential circuit is a logical circuit, where the output depends on the present value of the input signal as well as the sequence of past inputs. A sequential circuit is a combination of combinational circuit and a storage element. Bi-stable latches and flip-flops are the basic building blocks of sequential logic circuits.

R-S LATCH (NOR GATE)

The latch is a type of temporary storage device that has two stable states, called SET and RESET. Latches are bi-stable devices, in which the outputs are connected back to the opposite inputs.

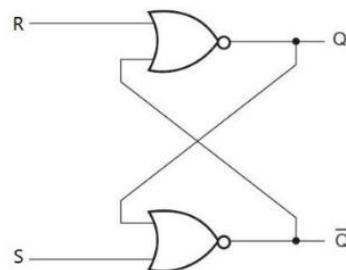


Fig. 4.1

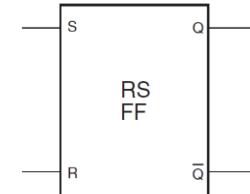
An active-HIGH input S-R (SET- RESET) latch is formed with two cross-coupled NOR gates, as shown in Fig. 4.1. Notice that the output of each gate is connected to an input of the opposite gate. This produces the regenerative feedback that is characteristic of all latches and flip-flops.

Working

1. SET = RESET = 0 is the normal resting condition of the flip-flop. It has no effect on the output state of the flip-flop. Both Q and \bar{Q} outputs remain in the logic state they were in prior to this input condition.
2. SET = 1 and RESET = 0 sets the flip-flop. Q and \bar{Q} respectively go to the '1' and '0' state.
3. SET = 0 and RESET = 1 resets or clears the flip-flop. Q and \bar{Q} respectively go to the '0' and '1' state.
4. SET = RESET = 1 is forbidden as such a condition tries to set (that is, $Q = 1$) and reset (that is, $Q = 0$) the flip-flop at the same time. To be more precise, SET and RESET inputs in the R-S flip-flop cannot be active at the same time.

Truth table and Symbol

Inputs		Outputs		Comments
R	S	Q	\bar{Q}	
0	0	Q	\bar{Q}	No Change
0	1	1	0	Set
1	0	0	1	Reset
1	1	Not Allowed		Forbidden



R-S LATCH (NAND GATE)

An active-LOW input S-R (SET- RESET) latch is formed with two cross-coupled NAND gates, as shown in Fig. 4.2. Notice that the output of each gate is connected to an input of the opposite gate. This produces the regenerative feedback that is characteristic of all latches and flip-flops.

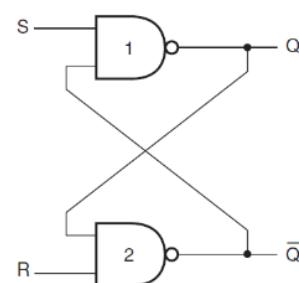


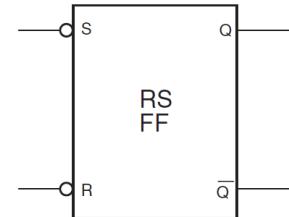
Fig. 4.2

Working

1. SET = RESET = 1 is the normal resting condition of the flip-flop. It has no effect on the output state of the flip-flop. Both Q and \bar{Q} outputs remain in the logic state they were in prior to this input condition.
2. SET = 0 and RESET = 1 sets the flip-flop. Q and \bar{Q} respectively go to the '1' and '0' state.
3. SET = 1 and RESET = 0 resets or clears the flip-flop. Q and \bar{Q} respectively go to the '0' and '1' state.
4. SET = RESET = 0 is forbidden as such a condition tries to set (that is, $Q = 1$) and reset (that is, $Q = 0$) the flip-flop at the same time. To be more precise, SET and RESET inputs in the R-S flip-flop cannot be active at the same time.

Truth table and Symbol

Inputs		Outputs		Comments
R	S	Q	\bar{Q}	
0	0	Not Allowed		Forbidden
0	1	0	1	Reset
1	0	1	0	Set
1	1	Q	\bar{Q}	No Change



CLOCKED R-S FLIP FLOP

A clocked (gated) latch requires a clock input. The S and R inputs control the state to which the latch will go when a HIGH level is applied to the CLK input. The latch will not change until CLK is HIGH; but as long as it remains HIGH, the output is controlled by the state of the S and R inputs.

Circuit Diagram

Fig. 4.3 shows the circuit of a clocked flip-flop that has active HIGH inputs. The two NAND gates at the input have been used to couple the R and S inputs to the flip-flop inputs under the control of the clock signal.

When the clock signal is HIGH, the two NAND gates are enabled and the S and R inputs are passed on to flip-flop inputs with their status complemented. The outputs can now change states as per the status of R and S at the flip-flop inputs. For instance, when S = 1 and R = 0 it will be passed on as 0 and 1 respectively when the clock is HIGH.

When the clock is LOW, the two NAND gates produce a '1' at their outputs, irrespective of the S and R status. This produces a logic '1' at both inputs of the flip-flop, with the result that there is no effect on the output states.

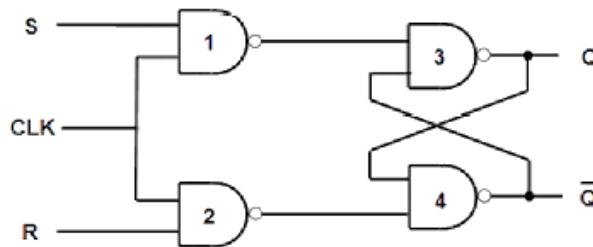
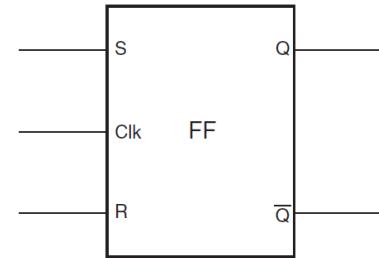


Fig. 4.3

Truth Table and Symbol

In puts			Out puts	
CLK	R	S	Q	\bar{Q}
0	0	0	No Change	
0	0	1	No Change	
0	1	0	No Change	
0	1	1	No Change	
1	0	0	No Change	
1	0	1	1	0
1	1	0	0	1
1	1	1	Not Allowed	



D FLIP FLOP

The major drawback of the SR flip-flop is its non-allowed logic states. It is overcome by the D type flip-flop. The D Flip Flop is by far the most important of the clocked flip-flops as it ensures that inputs S and R are never equal to one at the same time.

Circuit of D-Flip Flop

The D-type flip flop are constructed from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (data) input. Then this single data input, labelled D, is used in place of the “set” signal, and the inverter is used to generate the complementary “reset” input thereby making a level-sensitive D-type flip-flop from a level-sensitive RS-latch as shown in fig. 4.4.

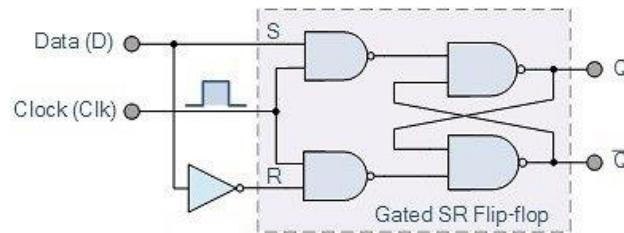


Fig. 4.4

Working of D-Flip Flop

As long as the clock input is low, changes at the D input make no difference to the outputs. The truth table shows this as a ‘don’t care’ state (X). Provided

that the CLK input is high, then whichever logic state is at D will appear at output Q and (unlike the SR flip-flops) \bar{Q} is always the inverse of Q).

If D = 1, then S must be 1 and R must be 0, therefore Q is SET to 1.

Alternatively,

If D = 0 then R must be 1 and S must be 0, causing Q to be reset to 0.

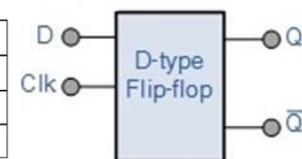
Equation

The “D flip flop” will store and output whatever logic level is applied to its data terminal so long as the clock input is HIGH.

$$Q = D \text{ if } \text{CLK} = \text{High}$$

Truth Table and Symbol

CLK	D	Q	\bar{Q}	Comments
0	X	Q	\bar{Q}	No Change
1	0	0	1	Reset
1	1	1	0	Set



METHODS OF TRIGGERING

Triggering

Triggering means making a circuit active. Making a circuit active means allowing the circuit to take input and give output. Like for example supposed we have a flip-flop. When the circuit is not triggered, even if you give some input data, it will not change the data stored inside the flip-flop nor will it change the output Q or Q'. The triggering is given in form of a clock pulse or gating signal. There are basically two types of triggering. Level and edge triggering.

Level Triggering

In level triggering the circuit will become active when the gating or clock pulse is on a particular level. We can have a negative level triggering in which the circuit is active when the clock signal is low or a positive level triggering in which the circuit is active when the clock signal is high. Both are shown in Fig. 4.5 (a) and (b).

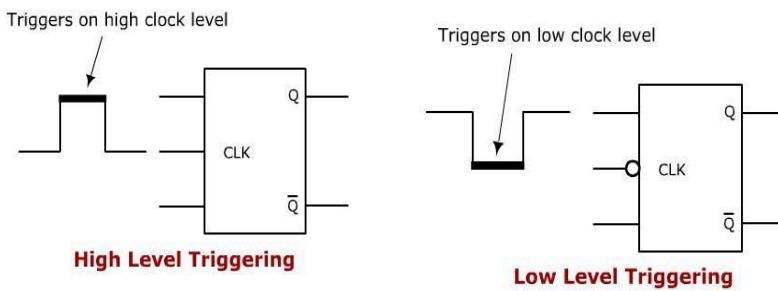


Fig. 4.5 (a)

Low Level Triggering

(b)

Edge Triggering

In edge triggering, the circuit becomes active at negative or positive edge of the clock signal. For example, if the circuit is positive edge triggered, it will take input at exactly the time in which the clock signal goes from low to high. Similarly, input is taken at exactly the time in which the clock signal goes from high to low in negative edge triggering. But keep in mind after the input, it can be processed in all the time till the next input is taken.

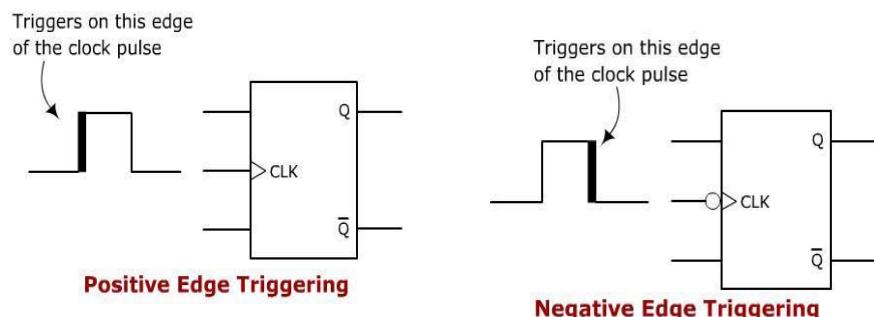


Fig. 4.6 (a)

(b)

Negative Edge Triggering

Latch and Flip-Flop

The main difference between latches and flip-flops is in the method used for changing their state. Whenever a multivibrator is enabled at transitional edge of a square-wave signal, we call it a flip-flop. If a multivibrator is level triggered, it is called a latch.

JK FLIP FLOP

JK flip Flop is the most widely used of all the flip-flop designs and is considered to be a universal flip-flop circuit. Both the S and the R inputs of the previous SR bi-stable have now been replaced by two inputs called the J and K inputs, respectively after its inventor Jack Kilby. Then this equates to: $J = S$ and $K = R$.

Circuit of JK Flip Flop

The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level "1". Due to this additional clocked input, a JK flip-flop has four possible input combinations, "logic 1", "logic 0", "no change" and "toggle".

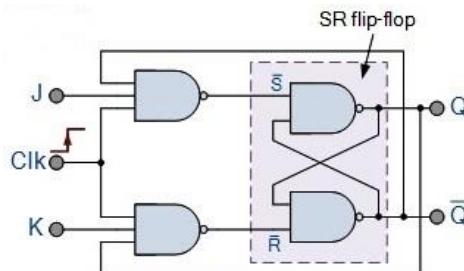


Fig. 4.7

The two 2-input AND gates of the gated SR bistable have now been replaced by two 3-input NAND gates with the third input of each gate connected to the outputs at Q and Q. This cross coupling of the SR flip-flop allows the previously invalid condition of S = "1" and R = "1" state to be used to produce a "toggle action" as the two inputs are now interlocked.

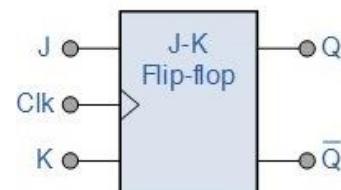
Working of JK Flip Flop

If the circuit is now "SET" the J input is inhibited by the "0" status of Q through the lower NAND gate. If the circuit is "RESET" the K input is inhibited by the "0" status of Q through the upper NAND gate.

Also, when both the J and the K inputs are at logic level "1" at the same time, and the clock input is pulsed "HIGH", the circuit will "toggle" from its SET state to a RESET state, or visa-versa. This results in the JK flip flop acting more like a T-type toggle flip-flop when both terminals are "HIGH".

Truth Table & Symbol

	Input		Output		Description
	J	K	Q	\bar{Q}	
same as for the SR Latch	0	0	0	0	Memory no change
	0	0	0	1	
	0	1	1	0	Reset Q \gg 0
	0	1	0	1	
	1	0	0	1	Set Q \gg 1
	1	0	1	0	
toggle action	1	1	0	1	Toggle
	1	1	1	0	



JK MASTER SLAVE FLIP FLOP

The basic JK flip flop can be improved further by adding a second JK flip-flop to its output that is activated on the complementary clock signal to produce a “Master-Slave JK flip flop”.

Circuit of JK MS Flip Flop

The Master-Slave Flip-Flop is basically two gated SR flip-flops connected together in a series configuration with the slave having an inverted clock pulse. The outputs from the “Slave” flip-flop are fed back to the inputs of the “Master” with the outputs of the “Master” flip flop being connected to the two inputs of the “Slave” flip flop.

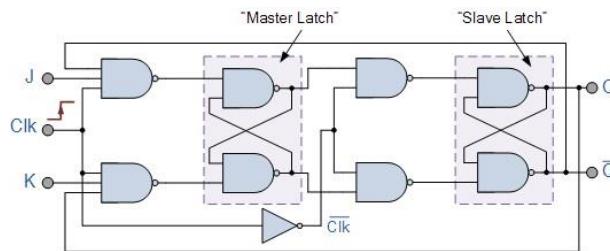


Fig. 4.8

Working of JK MS Flip Flop

The input signals J and K are connected to the gated “master” SR flip flop which “locks” the input condition while the clock (CLK) input is “HIGH” at logic level “1”. As the clock input of the “slave” flip flop is the inverse (complement) of the “master” clock input, the “slave” SR flip flop does not toggle. The outputs from the “master” flip flop are only “seen” by the gated “slave” flip flop when the clock input goes “LOW” to logic level “0”.

When the clock is “LOW”, the outputs from the “master” flip flop are latched and any additional changes to its inputs are ignored. The gated “slave” flip flop now responds to the state of its inputs passed over by the “master” section.

Then on the “Low-to-High” transition of the clock pulse, the inputs of the “master” flip flop are fed through to the gated inputs of the “slave” flip flop and on the “High-to-Low” transition the same inputs are reflected on the output of the “slave” making this type of flip flop edge or pulse-triggered. Then, the circuit accepts input data when the clock signal is “HIGH”, and passes the data to the output on the falling-edge of the clock signal. In other words, the Master-Slave JK Flip flop is a “Synchronous” device as it only passes data with the timing of the clock signal.

T FLIP FLOP

The T or "toggle" flip-flop changes its output on each clock edge, giving an output, which is half the frequency of the signal to the T input. It is useful for constructing binary counters and frequency dividers.

Circuit of T-Flip Flop

The simplest of the constructions of a T flip flop is with JK flip flop. The J input and K input of the JK flip flop are connected together and provided with the T input. The logic circuit of a T flip – flop constructed from a JK flip – flop is shown in Fig. 4.9.

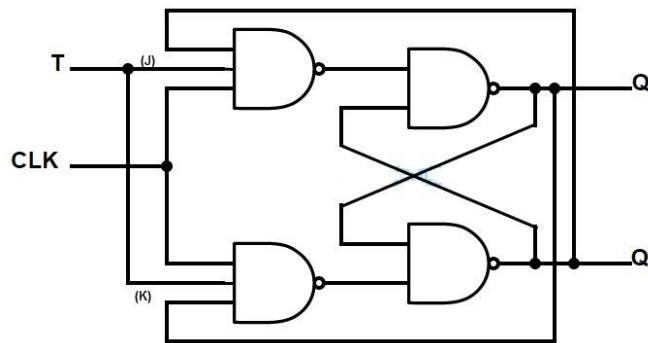


Fig. 4.9

Working of T-Flip Flop

T flip flop is an edge triggered device i.e. the low to high or high to low transitions on a clock signal of narrow triggers that is provided as input will cause the change in output state of flip flop.

If the output $Q = 0$, then the upper NAND is in enable state and lower NAND gate is in disable condition. This allows the trigger to pass the S inputs to make the flip – flop in SET state i.e. $Q = 1$.

If the output $Q = 1$, then the upper NAND is in disable state and lower NAND gate is in enable condition. This allows the trigger to pass the R inputs to make the flip flop in RESET state i.e. $Q = 0$.

In simple terms, the operation of the T flip flop is When the T input is low, then the next state of the T flip flop is same as the present state.

$T = 0$ and present state = 0 then the next state = 0

$T = 1$ and present state = 1 then the next state = 1

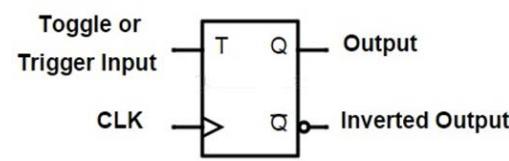
When the T input is high and during the positive transition of the clock signal, the next state of the T flip – flop is the inverse of present state.

$T = 1$ and present state = 0 then the next state = 1

$T = 1$ and present state = 1 then the next state = 0

Truth Table and Symbol

T	Previous		Next	
	Q _{Prev}	Q' _{Prev}	Q _{Next}	Q' _{Next}
0	0	1	0	1
0	1	0	1	0
1	0	1	1	0
1	1	0	0	1



555 TIMER IC

The 555 timer is a versatile and widely used IC device because it can be configured in two different modes as either a monostable multivibrator (one-shot) or as an astable multivibrator (free running oscillator).

Pin diagram of 555 timer IC

The single 555 Timer chip in its basic form is a Bipolar 8-pin mini Dual-in-line Package (DIP) device. A simplified “block diagram” representing the internal circuitry of the 555 timer is given in Fig. 4.10 with a brief explanation of each of its connecting pins.

Pin Description of 555 timer IC

Pin 1. – Ground, the ground pin connects the 555 timer to the negative (0V) supply rail.

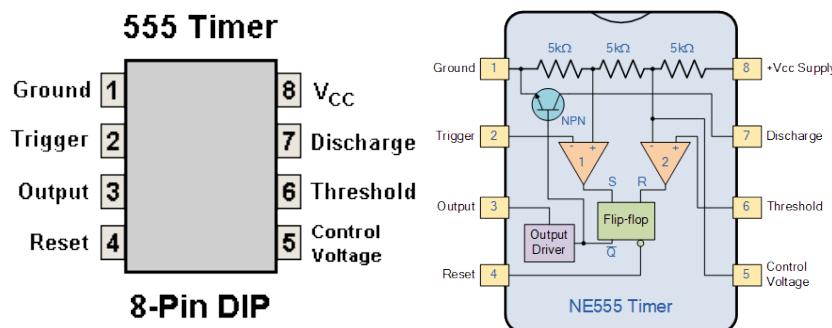


Fig. 4.10

Pin 2. – Trigger, The negative input to comparator No 1. A negative pulse on this pin “sets” the internal Flip-flop when the voltage drops below $\frac{1}{3}V_{cc}$ causing the output to switch from a “LOW” to a “HIGH” state.

Pin 3. – Output, the output pin can drive any TTL circuit, small speakers, LEDs or motors.

Pin 4. – Reset, this pin is used to “reset” the internal Flip-flop controlling the state of the output. It is generally connected to a logic “1” level when not used.

Pin 5. – Control Voltage, By applying a voltage to this pin, the width of the output signal can be varied independently of the RC timing network. When

not used it is connected to ground via a 10nF capacitor to eliminate any noise.

Pin 6. – Threshold, The positive input to comparator No 2. This pin is used to reset the Flip-flop when the voltage applied to it exceeds $\frac{1}{3}\text{Vcc}$ causing the output to switch from “HIGH” to “LOW” state. This pin connects directly to the RC timing circuit.

Pin 7. – Discharge, the discharge pin is connected directly to the collector of an internal NPN transistor which is used to “discharge” the timing capacitor to ground when the output at pin 3 switches “LOW”.

Pin 8. – Supply +Vcc, this is the power supply pin and for general purpose TTL 555 timers is between 4.5V and 15V.

Operation of 555 timer IC

The 555 Timers name comes from the fact that there are three $5\text{k}\Omega$ resistors connected together internally producing a voltage divider network between the supply voltage at pin 8 and ground at pin 1. The voltage across this series resistive network holds the negative inverting input of comparator B at $\frac{1}{3}\text{Vcc}$ and the positive non-inverting input to comparator A at $\frac{2}{3}\text{Vcc}$.

When the normally HIGH trigger input momentarily goes below $\frac{1}{3}\text{Vcc}$, the output of comparator B switches from LOW to HIGH and sets the S-R latch, causing the output (pin 3) to go HIGH and turning the discharge transistor Q_1 off.

The output will stay HIGH until the normally LOW threshold input goes above $\frac{2}{3}\text{Vcc}$ and causes the output of comparator A to switch from LOW to HIGH. This resets the latch, causing the output to go back LOW and turning the discharge transistor on.

555 TIMER IC AS MONOSTABLE MULTIVIBRATOR

The 555 timer can be configured as a monostable multivibrator (one-shot). Monostable multivibrator has only ONE stable state, and produce a single output pulse when it is triggered externally. Monostable multivibrator only return back to their first original and stable state after a period of time determined by the time constant of the RC coupled circuit.

Circuit of 555 timer monostable multivibrator

An external resistor and capacitor connected as shown in Fig. 4.11 are used to set up the 555 timer as a nonretriggerable one-shot. The pulse width of

the output is determined by the time constant of R_1 and C_1 according to the following formula:

$$t = 1.1 R_1 C_1$$

The control voltage input is not used and is connected to a decoupling capacitor C_2 to prevent noise.

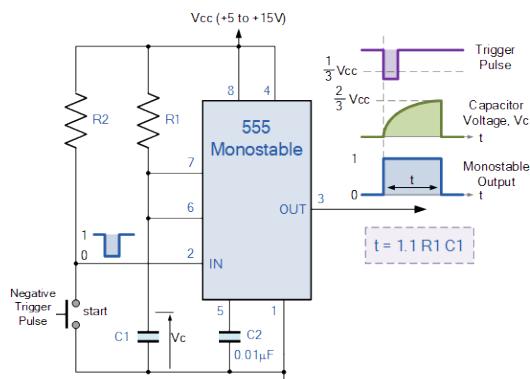


Fig. 4.11

Working of 555 timer monostable multivibrator

Initially, the output is LOW and the discharge transistor Q_1 is on, keeping C_1 discharged. When a negative going trigger pulse is applied at t_0 , the output goes HIGH and the discharge transistor turns off, allowing capacitor C_1 to begin charging through R_1 . When C_1 charges to $\frac{2}{3}V_{cc}$, the output goes back LOW at t_1 and Q_1 turns on immediately, discharging C_1 . The charging rate of C_1 determines how long the output is HIGH.

555 TIMER IC AS ASTABLE MULTIVIBRATOR

The 555 timer can be configured as a astable multivibrator (oscillator). An astable multivibrator has no stable states and therefore changes back and forth (oscillates) between two unstable states without any external triggering.

Circuit of 555 timer astable multivibrator

A 555 timer connected to operate as an astable multivibrator, which is a nonsinusoidal oscillator, is shown in Fig. 4.12. Notice that the threshold input (THRESH) is now connected to the trigger input (TRIG). The external components R_1 , R_2 , and C_1 form the timing network that sets the frequency of oscillation. The $0.01 \mu F$ capacitor, C_2 , connected to the control (CONT) input is strictly for decoupling and has no effect on the operation; in some cases it can be left off.

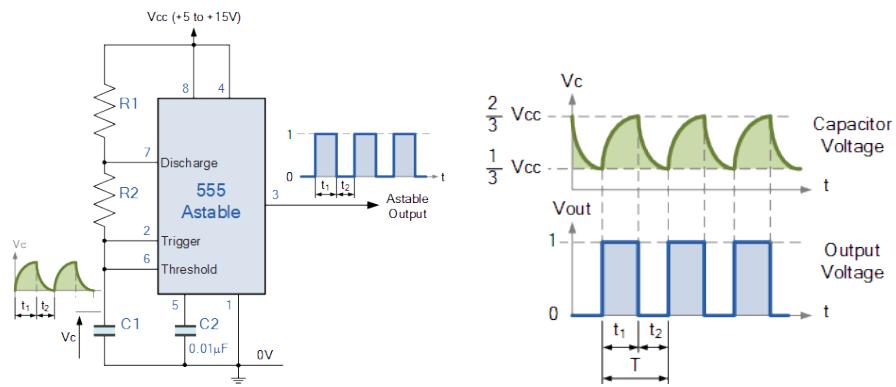


Fig. 4.12

Working of 555 timer astable multivibrator

Initially, when the power is turned on, the capacitor (C_1) is uncharged and thus the trigger voltage (pin 2) is at 0V. This causes the output of comparator B to be HIGH and the output of comparator A to be LOW, forcing the output of the latch, and thus the base of Q_1 , LOW and keeping the transistor off. Now, C_1 begins charging through R_1 and R_2 , as indicated in Fig. 4.13.

When the capacitor voltage reaches $\frac{2}{3}V_{CC}$, comparator A switches to its HIGH output state. This resets the latch, causing the base of Q_1 to go HIGH and turning on the transistor. This sequence creates a discharge path for the capacitor through R_2 and the transistor, as indicated. The capacitor now begins to discharge, causing comparator A to go LOW. At the point where the capacitor discharges down to $\frac{1}{3}V_{CC}$, comparator B switches HIGH; this sets the latch, making the base of Q_1 LOW and turning off the transistor. Another charging cycle begins, and the entire process repeats.

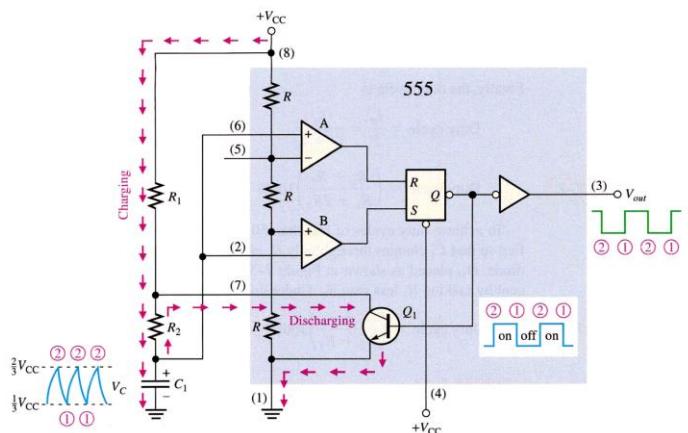


Fig. 4.13

The result is a rectangular wave output whose duty cycle depends on the values of R_1 and R_2 . The frequency of oscillation is given by the following formula.

$$f = \frac{1.44}{(R_t + 2R_2)C_1}$$

EXERCISE

SECTION-I (MCQ's)

1. Following is the reset condition of a flip flop.
 (a) $Q = 0 \& \bar{Q} = 1$ (b) $Q = 0 \& \bar{Q} = 0$ (c) $Q = 1 \& \bar{Q} = 0$ (d) $Q = 1 \& \bar{Q} = 1$
2. If $J = 1$ and $K = 0$, then condition of flip flop will be
 (a) Reset (b) Set (c) Toggle (d) Forbidden
3. A 555 timer IC has
 (a) 3 pins (b) 6 pins (c) 8 pins (d) 12 pins
4. A flip flop has number of stable states
 (a) One (b) Two (c) Three (d) Four
5. Which flip flop is called universal flip flop?
 (a) RS (b) D (c) JK (d) T
6. The pin number 6 of 555 timer IC is
 (a) Trigger (b) Threshold (c) Discharge (d) Control
7. D flip flop is also called
 (a) Data flip flop (b) Delay flip flop (c) D type latch (d) All of these
8. Following is the set condition of a flip flop.
 (a) $Q = 0 \& \bar{Q} = 1$ (b) $Q = 0 \& \bar{Q} = 0$ (c) $Q = 1 \& \bar{Q} = 0$ (d) $Q = 1 \& \bar{Q} = 1$
9. A 555 timer IC have comparators
 (a) Two (b) Three (c) Four (d) Five
10. In clocked RS flip flop when all three inputs are zero, then flip flop state is
 (a) Forbidden (b) Reset (c) Hold (d) Set

ANSWER KEY

- | | | | | | | | | | |
|----|---|----|---|----|---|----|---|-----|---|
| 1. | a | 2. | b | 3. | c | 4. | b | 5. | c |
| 6. | b | 7. | d | 8. | c | 9. | a | 10. | c |

SECTION-II (Short Questions)

1. Define sequential logic circuits.
2. What is the difference between flip flop and latch?
3. Name the types of flip flops.
4. Define RS flip flop.
5. Draw the truth table of active low RS latch.
6. Draw the truth table of active high RS latch.
7. What is meant by reset condition in a flip flop?
8. What is meant by set condition in a flip flop?

9. Write output equation of D-flip flop.
10. Draw truth table of D flip flop.
11. Define low level triggered flip flop.
12. Define high level triggered flip flop.
13. Define negative edge triggering.
14. Define positive edge triggering.
15. What is toggle mode of JK flip flop?
16. Define T-type flip flop?
17. What are synchronous inputs?
18. What are asynchronous inputs?
19. Define astable multivibrator.
20. Define monostable multivibrator.
21. How is the output pulse width set in IC type one shot?

SECTION-III (Long Questions)

1. Draw and explain 555 timer IC functional diagram.
2. Explain negative edge triggered JK flip flop using logic diagram and truth table.
3. Explain the working of 555 IC as mono-stable multivibrator using circuit diagram.
4. Write a detail note on clocked RS flip flop.
5. Explain master-slave JK flip flop using diagram.

SHIFT REGISTERS & COUNTERS

CHAPTER-5

Objectives

At the end of this chapter, a student will be able to

- Describe types of shift register.
- Understand integrated shift register.
- Understand discrete ripple counter.
- Understand discrete modulus- N ripple counter.
- Describe integrated ripple counter (7493)
- Describe discrete synchronous up Counter.
- Describe discrete down counter.
- Describe discrete modulus-synchronous counter.

Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data.

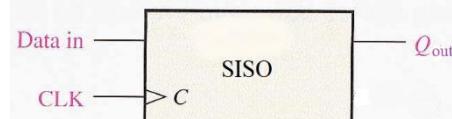
There are four types of shift registers.

- i- Serial In Serial Out
- ii- Serial In Parallel Out
- iii- Parallel In Serial Out
- iv- Parallel In Parallel Out

SERIAL IN SERIAL OUT (SISO) SHIFT REGISTER

The serial in/serial out shift register accepts data serially- that is, one bit at a time on a single line. It produces the stored information on its output also in serial form.

The SISO shift register is one of the simplest of the four configurations as it has only three connections, the serial input (SI) which determines what enters the left hand flip-flop, the serial output (SO) which is taken from the output of the right hand flip-flop and the sequencing clock signal (CLK).



SISO Circuit Diagram

Fig. 5.1 shows a 4-bit serial-in, serial out register. This register can store up to four bits of data.

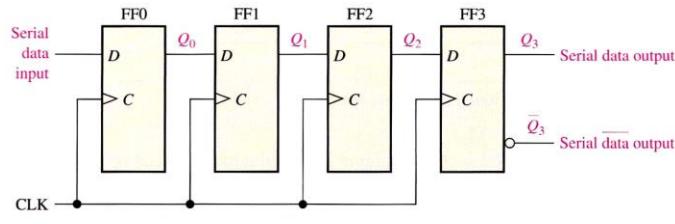


Fig. 5.1

Data In Serially

Fig. 5.2 illustrates entry of the four bits 1010 into the register. The register is initially clear.

- i. First the right-most bit “0” is put onto the data input line, making D = 0 for FF0. When the first clock pulse is applied, FF0 is reset, thus storing the 0.
- ii. Next the second bit, which is a 1, is applied to the data input, making D = 1 for FF0 and D = 0 for FF1 because the D input of FF1 is connected to the Q₀ output. When the second clock pulse occurs, the 1 on the data input is shifted into FF0, causing FF0 to set; and the 0 that was in FF0 is shifted into FF1.
- iii. The third bit, a 0, is now put onto the data-input line, and a clock pulse is applied. The 0 is entered into FF0, the 1 stored in FF0 is shifted into FF1, and the 0 stored in FF1 is shifted into FF2.
- iv. The last bit, a 1, is now applied to the data input, and a clock pulse is applied. This time the 1 is entered into FF0, the 0 stored in FF0 is shifted into FF1, the 1 stored in FF1 is shifted into FF2, and the 0 stored in FF2 is shifted into FF3. This completes the serial entry of the four bits into the shift register.

Data In Serially (1010)		FF0	FF1	FF2	FF3
1 st CLK Pulse	1 st Data Bit “0” In	0	0	0	0
2 nd CLK Pulse	2 nd Data Bit “1” In	1	0	0	0
3 rd CLK Pulse	3 rd Data Bit “0” In	0	1	0	0
4 th CLK Pulse	4 th Data Bit “1” In	1	0	1	0

Fig. 5.2

Data Out Serially

To get the data out of the register, the bits must be shifted out serially and taken off the Q₃ output. After CLK4 in the data entry operation just described, the right-most bit, 0, appears on the Q₃ output.

Data Out Serially (1010)		FF0	FF1	FF2	FF3
5 th CLK Pulse	1 st Data Bit "0" Out	0	1	0	1
6 th CLK Pulse	2 nd Data Bit "1" Out	0	0	1	0
7 th CLK Pulse	3 rd Data Bit "0" Out	0	0	0	1
8 th CLK Pulse	4 th Data Bit "1" Out	0	0	0	0

Fig. 5.3

When clock pulse CLK5 is applied, the second bit appears on the Q_3 output. Clock pulse CLK6 shifts the third bit to the output, and CLK7 shifts the fourth bit to the output. After CLK8 register is clear as shown in Fig. 5.3.

SERIAL IN PARALLEL OUT (SIPO) SHIFT REGISTER

The serial in/parallel out shift register accepts data serially- that is, one bit at a time on a single line. It produces the stored information on its output in parallel form.

A logical symbol of 4-bit serial in parallel out shift register is shown in Fig. 5.4. It has one serially data input, four lines to get parallel data at output and the sequencing clock signal (CLK).

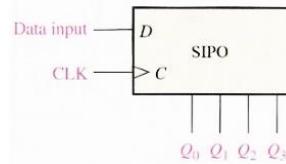


Fig. 5.4

SIPO Circuit Diagram

A serial-in parallel-out shift register is identical to a serial-in serial-out shift register except that in this case, all flip-flop outputs are also brought out on the IC terminals. Fig. 5.5. shows the logic diagram of a typical serial-in parallel-out shift register.

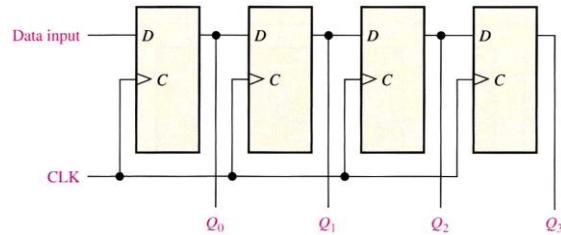


Fig. 5.5

Serial Data In

All registers are initially clear. Suppose we have to store 1011 in this register. On the first clock at t_1 , the bit "1" at SI is shifted from D to Q of the first shift register stage. After t_2 this first data bit is at Q_1 . After t_3 it is at Q_2 . After t_4 it is at Q_3 . Four clock pulses have shifted the first data bit all the way to the last

stage Q_3 . The second data bit a 1 is at Q_2 after the 4th clock. The third data bit a 0 is at Q_1 . The fourth data bit another 1 is at Q_0 . Thus, the serial data input pattern 1011 is contained in $(Q_0Q_1Q_2Q_3)$. It is now available on the four outputs.

Parallel Data Out

Output will available on the four outputs from just after clock t_4 to just before t_5 . This parallel data must be used or stored between these two times.

PARALLEL IN SERIAL OUT (PISO) SHIFT REGISTER

In parallel in/serial out shift register, the bits are entered simultaneously into their respective stages on parallel lines and the stored information is received on its output in serial form.

Fig. 5.6. shows a logical symbol of 4-bit parallel in serial out shift register. It has four data-input lines, one serially data output, a clock signal (CLK) and a $SHIFT/LOAD$ input, which allows four bits of data to load in parallel into the register.

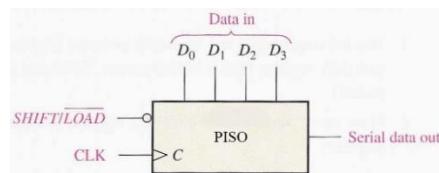


Fig. 5.6

PISO Circuit Diagram

Fig. 5.7. illustrates a 4-bit parallel in/serial out shift register. There are four data-input lines, D_0 , D_1 , D_2 , and D_3 .

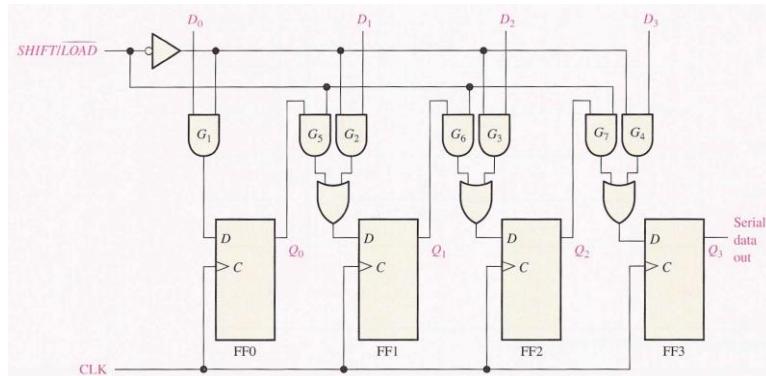


Fig. 5.7

Parallel Data In

When $SHIFT/LOAD$ is LOW, gates G_1 through G_4 are enabled , allowing each data bit to be applied to the D input of its respective flip-flop. When a

clock pulse is applied, the flip-flops with $D = 1$ will set and those with $D = 0$ will reset, thereby storing all four bits simultaneously.

Serial Data Out

When *SHIFT/LOAD* is HIGH, gates G_1 through G_4 are disabled and gates G_5 through G_7 are enabled, allowing the data bits to shift right from one stage to the next. The OR gates allow either the normal shifting operation or the parallel data-entry operation, depending on which AND gates are enabled by the level on the *SHIFT/LOAD* input. Notice that FF0 has a single AND to disable the parallel input, D_0 . It does not require an AND/OR arrangement because there is no serial data in.

PARALLEL IN PARALLEL OUT (PIPO) SHIFT REGISTER

For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits.

Fig. 5.7. shows a logical symbol of 4-bit parallel in parallel out register. It has four data-input lines, four data-output lines, and a clock signal (CLK).

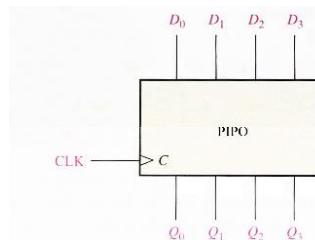


Fig. 5.7

PIPO Circuit Diagram

Fig. 5.8. illustrates a 4-bit parallel in/parallel out register. There are four data-input lines, D_0 , D_1 , D_2 , and D_3 , and four data-output lines Q_0 , Q_1 , Q_2 , and Q_3 .

Working

The four bit data is presented in a parallel format to the parallel input pins D_0 to D_3 and then transferred together directly to their respective output pins Q_0 to Q_3 by the same clock pulse. Then one clock pulse loads and unloads the register.

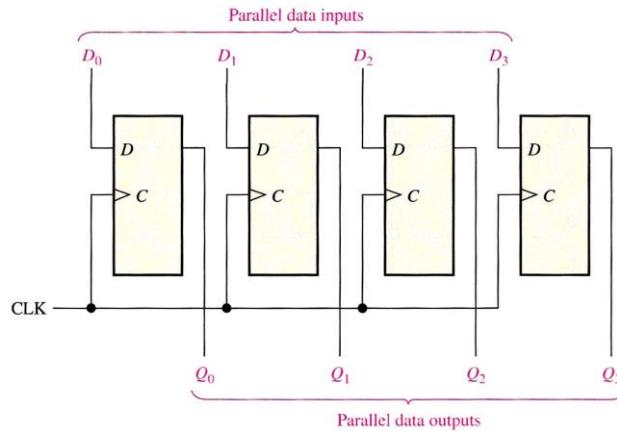


Fig. 5.8

BINARY COUNTERS

A binary counter is a combination of flip flops which counts the input clock pulses. The output of one flip-flop is sent to the input of the next flip-flop in the series. There are basically two types of a binary counter.

- i- Asynchronous Counter (Ripple Counter)
- ii- Synchronous Counter

Asynchronous counter is also called ripple or serial counter. In this counter first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the output of the preceding flip-flop.

Synchronous counter is also called a parallel counter. In synchronous counters, the clock input is connected to all of the flip-flops so that they are clocked simultaneously.

These counters can count in different ways based on their circuitry.

- UP COUNTER: Counts the values in ascending order.
- DOWN COUNTER: Counts the values in descending order.
- UP-DOWN COUNTER: Counts the values either in the ascending or descending direction.

DISCRETE ASYNCHRONOUS/RIPPLE COUNTER

A ripple counter is also called an asynchronous counter or a serial counter. It is a cascaded arrangement of flip-flops where the first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the output of the preceding flip-flop.

2-BIT ASYNCHRONOUS/RIPPLE COUNTER

The logic diagram of a 2-bit ripple up counter is shown in Fig. 5.9. The negative edge triggered JK flip-flops are being used in toggle mode. External clock is applied to the clock input of flip-flop FF0 and Q₀ output is applied to the clock input of the next flip-flop i.e. FF1.

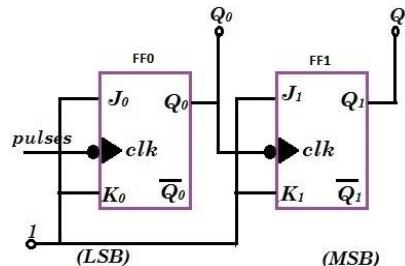


Fig. 5.9

Working

As we have applied a high voltage to all the JK inputs of flip-flops they are at the state 1, so they must toggle the state at the negative going end of the clock pulse.

From the timing diagram shown in Fig. 5.10, we can observe that Q₀ changes state only during the negative edge of the applied clock. Initially, the flip flop is at state 0. Flip-flop stays in the state until the applied clock goes from 1 to 0. As the JK values are 1, the flip flop should toggle. So, it changes state from 0 to 1. The process continues for all pulses of the clock.

Coming to the second flip flop, here the waveform generated by flip flop 1 is given as clock pulse. So, as we can see in the timing diagram when Q₀ goes transition from 1 to 0 the state of Q₁ changes. Note that the output values of Q₀ are considered as LSB and Q₁ are considered as MSB.

From the timing diagram, we can observe that the counter counts the values 00,01,10,11 then resets itself and starts again from 00,01,... until clock pulses are applied to first flip flop.

Truth Table & Timing Diagram

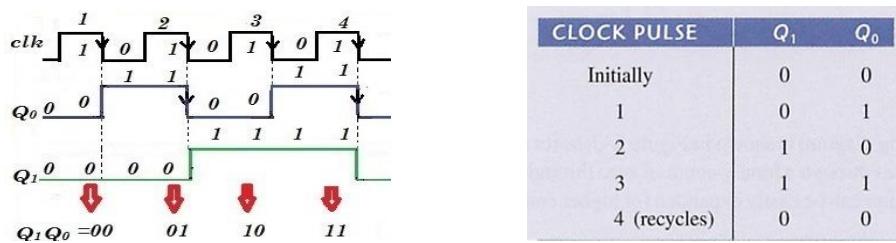


Fig. 5.10

3-BIT ASYNCHRONOUS/RIPPLE COUNTER

In the 3-bit ripple counter, three flip-flops are used in the circuit. This counter can count up to $2^3 = 8$ values. i.e. 000,001,010,011,100,101,110,111. The circuit diagram is shown in Fig. 5.11.

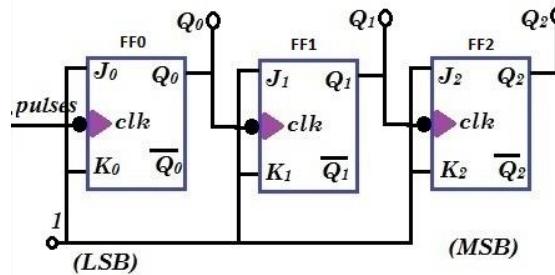


Fig. 5.11

Working

All the JK inputs of flip-flops are connected to HIGH. So, they must toggle the state at the negative going end of the clock pulse .i.e. at the transition 1 to 0 of the clock pulse.

Q_0 changes state only during the negative edge of the applied clock. When Q_0 goes transition from 1 to 0 the state of Q_1 changes. When Q_1 goes transition from 1 to 0 the state of Q_2 changes. The timing diagram of the binary ripple counter clearly explains this operation shown in Fig. 5.12. The output values of Q_0 is considered as LSB and Q_2 is considered as MSB.

Truth Table & Timing Diagram

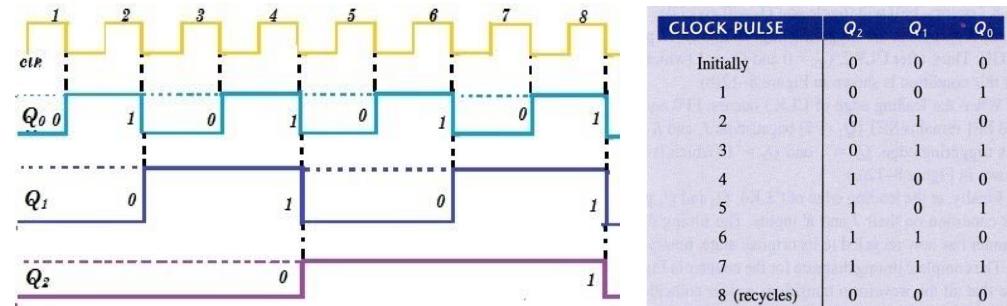


Fig. 5.12

Modulus of a counter

The modulus (MOD number) of a counter is the number of different logic states it goes through before it comes back to the initial state to repeat the count sequence. The maximum possible number of states (maximum modulus) of a counter is 2^n , where n is the number of flip-flops in the counter.

INTEGRATED ASYNCHRONOUS/RIPPLE COUNTER (7493)

Binary ripple counter is available in IC form. The 74LS93 is an example of a specific integrated circuit asynchronous counter.

Internal Logic Diagram

Fig. 5.13 shows the internal logic diagram of 74LS93 counter IC. This device consists of a single flip-flop and a 3-bit asynchronous counter. This arrangement is for flexibility. It can be used as a divide by-2 device if only the single flip-flop is used, or it can be used as a modulus-8 counter if only the 3-bit counter portion is used. This device also provides gated reset inputs, RO(1) and RO(2). When both of these inputs are HIGH, the counter is reset to the 0000 state.

All J and K inputs are internally connected HIGH.

Additionally, the 74LS93 can be used as a 4-bit modulus-16 counter (counts 0 through 15) by connecting the Q0 output to the CLK B input. It can also be configured as a decade counter (counts 0 through 9) with asynchronous recycling by using the gated reset inputs for partial decoding of count ten.

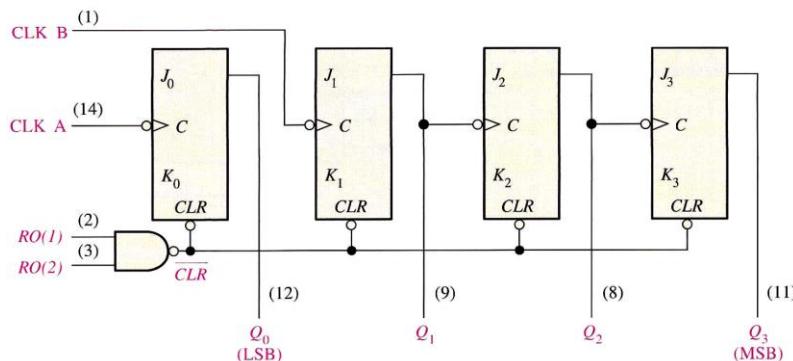


Fig. 5.13

SYNCHRONOUS COUNTER

Synchronous counter is also called a parallel counter. In synchronous counters, the clock input is connected to all of the flip-flops so that they are clocked simultaneously.

SYNCHRONOUS UP COUNTER

An UP counter is one that counts upwards or in the forward direction by one LSB every time it is clocked. A three-bit binary UP counter will count as 000, 001, 010, 011, 100, 101, 110 and 111.

2-bit synchronous up counter

Fig. 5.14 shows a 2-bit synchronous up counter. Notice that an arrangement must be used for the J_1 and K_1 inputs of FF1 in order to achieve a binary sequence.

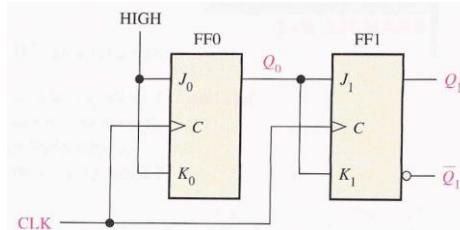


Fig. 5.14

Working

- i- First, assume that the counter is initially in the binary 0 state. When the positive edge of the first clock pulse is applied, FF0 will toggle and Q_0 will therefore go HIGH. Inputs J_1 and K_1 are both LOW because Q_0 , to which they are connected, has not yet gone HIGH. So, $J = 0$ and $K = 0$ when the leading edge of the first clock pulse is applied. This is a no-change condition, and therefore FF1 does not change state.
- ii- After CLK1, $Q_0 = 1$ and $Q_1 = 0$ (which is the binary 1 state). When the leading edge of CLK2 occurs, FF0 will toggle and Q_0 will go LOW. Since FF1 has a HIGH ($Q_0 = 1$) on its J_1 and K_1 inputs at the triggering edge of this clock pulse, the flip-flop toggles and Q_1 goes HIGH. Thus, after CLK2, $Q_0 = 0$ and $Q_1 = 1$ (which is a binary 2 state).
- iii- When the leading edge of CLK3 occurs, FF0 again toggles to the SET state ($Q_0 = 1$), and FF1 remains SET ($Q_1 = 1$) because its J_1 and K_1 inputs are both LOW ($Q_0 = 0$). After this triggering edge, $Q_0 = 1$ and $Q_1 = 1$ (which is a binary 3 state).
- iv- Finally, at the leading edge of CLK4, Q_0 and Q_1 go LOW because they both have a toggle condition on their J and K inputs. The counter has now recycled to its original state, binary 0. The complete timing diagram and truth table for the counter is shown in Fig. 5.15.

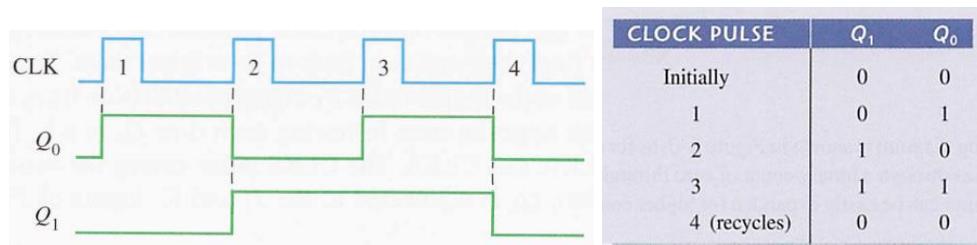


Fig. 5.15

3-bit synchronous up counter

A 3-bit synchronous up counter is shown in Fig. 5.16. with its truth table.

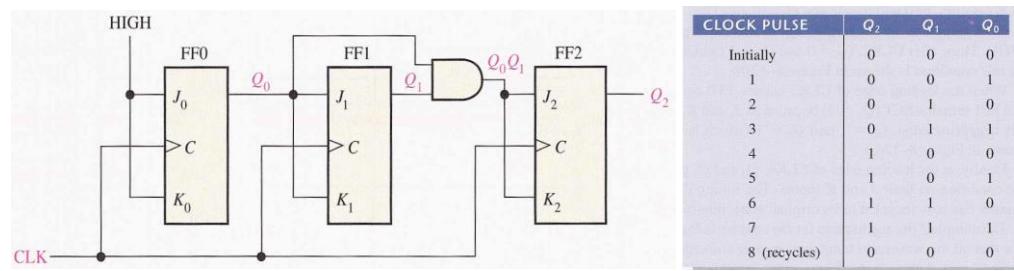
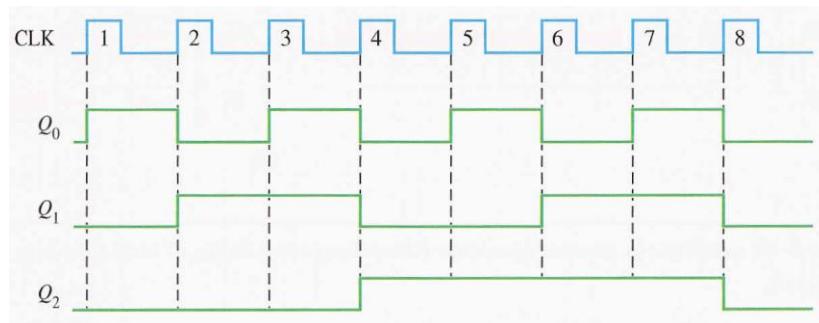


Fig. 5.16

Working

- i- FF0 is in the toggle mode by constant HIGHs on its J₀ and K₀ inputs. It changes its output at every positive edge of CLK.
- ii- Q₀ is connected to the J₁ and K₁ inputs of FF1. When Q₀ is a 1 and a clock pulse occurs, FF1 is in the toggle mode and therefore changes state. This change occurs at CLK2, CLK4, CLK6, and CLK8. When Q₀ is a 0, FF1 is in the no-change mode and remains in its present state.
- iii- The J₂ and K₂ inputs of FF2 are connected to the AND of Q₀ and Q₁. Whenever both Q₀ and Q₁ are HIGH, the output of the AND gate makes the J₂ and K₂ inputs of FF2 HIGH, and FF2 toggles on the CLK4 and CLK8. At all other times, the J₂ and K₂ inputs of FF2 are held LOW by the AND gate output, and FF2 does not change state.



DOWN COUNTERS

A down counter counts in the reverse direction or downwards by one LSB every time it is clocked. The three-bit binary down counter will count as 000, 111, 110, 1101, 100, 011, 010, 001 and 000. The down counter can be constructed as asynchronous or synchronous.

ASYNCHRONOUS DISCRETE DOWN COUNTER

If the flip-flops used to construct the counter are negative edge triggered and the clock inputs are fed from \bar{Q} outputs, the counter counts in the reverse or downward count sequence.

If the flip-flops used to construct the counter are positive edge triggered and the clock inputs are fed from Q outputs, the counter counts in the reverse or downward count sequence.

Circuit Diagram

A 3-bit binary asynchronous (ripple) down counter is shown in figure.

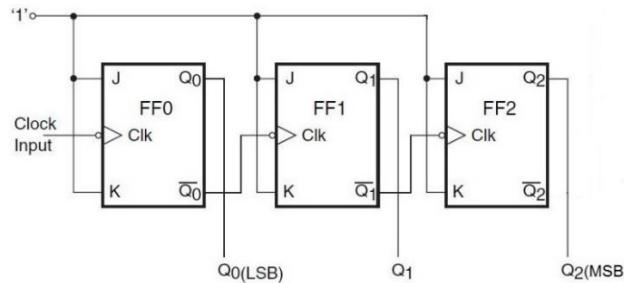


Fig. 5.17

Working

- i- The counter is initially in the 000 state. With the first clock pulse, Q_0 toggles from the '0' to the '1' state, which means \bar{Q}_0 toggles from '1' to '0'. Since \bar{Q}_0 here feeds the clock input of next flip-flop, flip-flop FF1 also toggles. Thus, Q_1 goes from '0' to '1'. Since flip-flops FF2 and FF3 are also clocked from complementary outputs of their immediately preceding flip-flops, they also toggle. Thus, the counter moves from the 000 state to the 111 state with the first clock pulse.

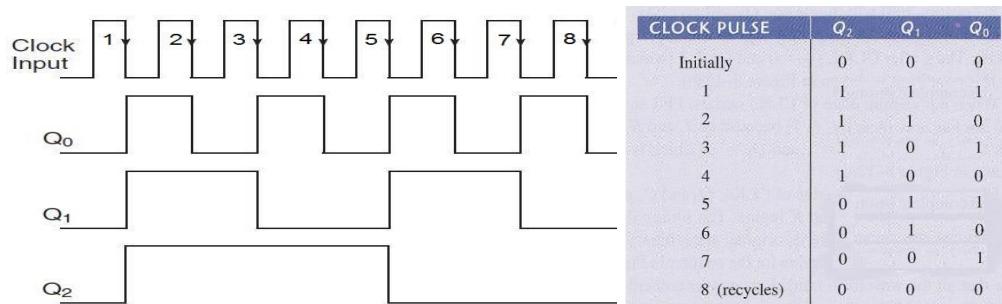


Fig. 5.18

- ii- With the second clock pulse, Q_0 toggles again, but the other flip-flops remain unaffected and the counter is in the 110 state.
- iii- With subsequent clock pulses, the counter keeps counting downwards by one LSB at a time until it reaches 000 again, after which the process repeats.
- iv- The count sequence is given as 000, 111, 110, 101, 100, 011, 010, 001 and 000. The timing waveforms and truth table are shown in Fig. 5.18.

SYNCHRONOUS DISCRETE DOWN COUNTER

we can easily construct a 3-bit Synchronous Down Counter by connecting the AND gate to the Q output of the flip-flops as shown in Fig. 5.19. Here the counter starts with all of its outputs HIGH (111) and it counts down on the application of each clock pulse to zero, (000) before repeating again.

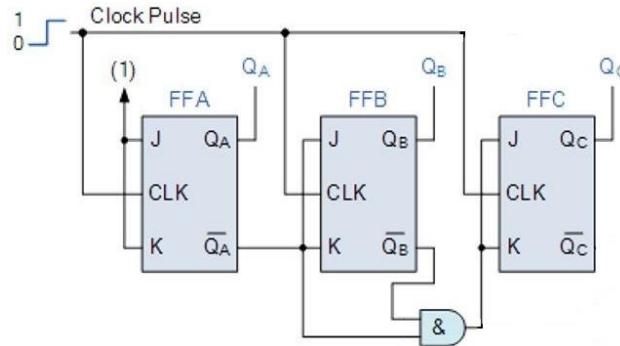


Fig. 5.19

EXERCISE**SECTION-I (MCQ's)**

1. Combination of flip flops which can store and shift data is called
(a) Counter (b) Register (c) Multiplexer (d) De-multiplexer
2. A 4-bit register consists of
(a) 2-Flip Flops (b) 4-Flip Flops (c) 12-Flip Flops (d) 16-Flip Flops
3. A shift register has characteristic
(a) Memory only (b) Shift only (c) Both a & b (d) None of these
4. A 3-bit counter has a maximum modulus of
(a) 3 (b) 6 (c) 8 (d) 9
5. Shift register is a type of memory
(a) Optical (b) Magnetic (c) Non-Volatile (d) Volatile
6. Shift register is constructed by combining
(a) diodes (b) Transistors (c) Flip flops (d) SCR's
7. To enter data into the register is called
(a) Loading data (b) Storing data (c) Writing data (d) All of these
8. Asynchronous counter is also called
(a) Ripple (b) Ring (c) Decade (d) Synchronous
9. Combination of flip flops which can count input pulses is called
(a) Counter (b) Register (c) Multiplexer (d) De-multiplexer
10. For shifting one byte into a register, number of clock pulses required
(a) 1 (b) 3 (c) 4 (d) 8
11. A counter consists of n flip flops, have maximum output states
(a) n (b) n^2 (c) 2^n (d) $2n^2$
12. A counter in which all flip flops triggers simultaneously is called

(a) Ripple	(b) Synchronous	(c) Asynchronous	(d) Serial
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ANSWER KEY

1.	b	2.	b	3.	c	4.	c	5.	d
6.	c	7.	d	8.	a	9.	a	10.	d
11.	c	12.	b						

SECTION-II (Short Questions)

1. Write four types of shift register.
2. What two principle functions are performed by a shift register?
3. Define serial in serial out register.
4. Draw logic symbol of SISO shift register.
5. Define serial in parallel out register.
6. Draw logic symbol of SIPO shift register.
7. Define parallel in serial out register.
8. What is function of LOAD/~~SHIFT~~ in PISO register?
9. Draw the logic symbol of parallel in serial out register.
10. Define parallel in parallel out register.
11. Which flip flop is commonly used in a register?
12. Draw logic symbol of PIPO shift register.
13. What is a counter?
14. Enlist types of counters.
15. Define ripple counter.
16. Define synchronous counter.
17. What is advantage of synchronous counter?
18. What is up counter?
19. What is down counter?
20. What is meant by modulus of a counter?
21. In which mode JK flip flop operates in counter circuit?

SECTION-III (Long Questions)

1. Explain the serial In Parallel out shift register with help of diagram.
2. Draw the circuit of 3-bit ripple counter and explain its working with timing diagram.
3. Explain the operation of 3-bit synchronous counter using diagram.
4. Explain integrated ripple counter (7493).
5. Define and explain serial-in-serial out shift register.

FAMILIES & SPECIFICATIONS**CHAPTER-6****Objectives**

At the end of this chapter, a student will be able to

- Discuss RTL (Resistor Transistor Logic)
- Discuss DTL (Diode Transistor Logic)
- Discuss ECL (Emitter Coupled Logic)
- Discuss TTL (Transistor Transistor Logic)
- Discuss IIL (Integrated Injection Logic)
- Discuss MOS (Metal Oxide Semiconductor)
- Discuss CMOS (Complementary MOS)
- Describe Interfacing Different Logic Families.
- Discuss Voltage & Current Levels.
- Discuss Fan-out, Fan-in.
- Understand Propagation Delay, Noise Margin and Power dissipation.

A logic family of monolithic digital integrated circuit devices is a group of electronic logic gates constructed using one of several different designs, usually with compatible logic levels and power supply characteristics within a family.

RTL LOGIC FAMILY

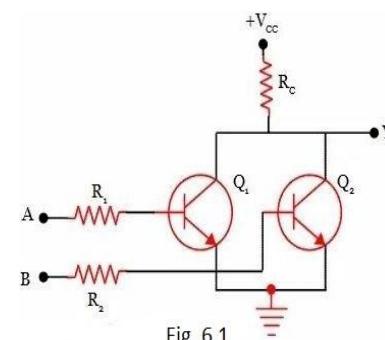
The resistor-transistor logic, also termed as RTL, was most popular kind of logic before the invention of IC fabrication technologies. As its name suggests, RTL circuits mainly consists of resistors and transistors that comprises RTL devices.

RTL NOR Gate Circuit

The basic RTL device is a NOR gate, shown in fig. 6.1. Each input is associated with one resistor and one transistor. The collectors of the transistors are tied together at the output.

Working

- When both the inputs A and B are at 0V, it is not enough to turn on the both transistors. Due to this, the voltage +V_{CC}



will appear at the output Y. Hence the output is logic 1 or logic HIGH at terminal Y.

- When any one of the inputs, either A or B is given HIGH voltage, then the transistor with HIGH input will be turned on. This will make a path for the supply voltage to go to the ground through the resistor R_C and transistor. Thus, there will be 0 v at the output terminal Y.
- When both the inputs are HIGH, it will drive both the transistor to turn on. It will make a path for the supply voltage to flow to the ground through resistor R_C and transistor. Therefore, there will be 0 v at the output terminal Y.

Characteristics of RTL

RTL family is characterized by poor noise margin, poor fan-out capability, low speed and high-power dissipation. Due to these undesirable characteristics, this family is now obsolete.

- It has a fan-out of 5.
- Propagation delay is 25 nS.
- Power dissipation is 12 mW.
- Noise margin for low signal input is 0.4 V.
- Voltage level for low level is 0.2 V.
- Voltage level for high level is 1 to 3.6 V.

DTL LOGIC FAMILY

The diode-transistor logic, also termed as DTL, replaced RTL family because of greater fan-out capability and more noise margin. As its name suggests, DTL circuits mainly consists of diodes and transistors that comprises DTL devices.

DTL NAND Gate Circuit

The basic DTL device is a NAND gate, shown in Fig. 6.2. Each input is associated with one diode. The diode and resistor form an AND gate, while transistor services as NOT gate.

Working

- If any input is LOW

The corresponding diode conducts current through V_{CC} and resistor to input node. The

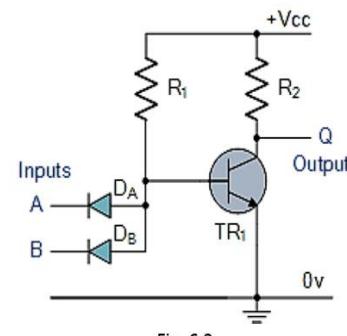


Fig. 6.2

voltage at base of transistor is equal to the diode drop. This is insufficient voltage for conduction of transistor. So the transistor is in cut-off region and the output is at logic HIGH.

- If all inputs are HIGH

In this case, no diode conducts. So, the voltage at base of transistor is equal to V_{CC} . The transistor is driven into saturation region. Hence the output is at logic LOW.

Characteristics of DTL

Due to number of diodes used in this circuit, the speed of the circuit is significantly low. Hence this family of logic gates is modified to transistor-transistor logic i.e. TTL family.

- It has a fan-out of 8.
- Propagation delay is average 30 nS.
- Power dissipation is 12 mW.
- Noise margin for low signal input is 0.7 V.

ECL LOGIC FAMILY

ECL is non-saturated digital logic family. This logic family implements the gates in differential amplifier configuration in which transistors are never driven in the saturation region thereby improving the speed of circuit to a great extent. The ECL family is fastest of all logic families.

ECL OR-NOR Gate Circuit

The basic gate of ECL family is NOR gate (OR and NOR together) as shown in Fig. 6.3. The output1 is OR output while output2 is NOR output.

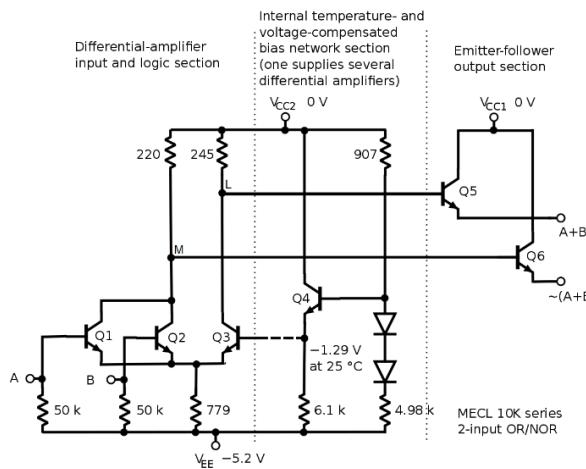


Fig. 6.3

The circuit consists of three parts.

- i- Differential input amplifier
- ii- Internal temperature and voltage compensated bias network.
- iii- Emitter follower output.

The emitter output requires a pull-down resistor for current flow.

Transistor Q_1 is applied with input and additional inputs are applied to transistors in parallel with Q_1 . Thus, input transistors and Q_3 are connected in differential amplifier configuration. Transistors Q_5 and Q_6 are emitter-followers used for DC level-shifting of output voltages. The positive supply terminal of the circuit is grounded while negative supply terminal is at negative 5.2V. This is done to minimize the effect of noise introduced by the power supply and also to protect the gate from short-circuit that might occur accidentally.

Both the outputs (HIGH/LOW) for OR and NOR are negative. Thus, to interface this logic family with other, a translator circuit is needed which converts negative voltages to compatible positive voltage levels.

Working

- If all inputs are at low level (-1.6V), both transistors are turn OFF and Q_3 conducts. Then at point L the potential is 0 volts. This is applied to the base of Q_5 , it is to be turn OFF. So, the output of OR gate is logic '0'.

At the same time , the potential at point M = V_{CC} is applied to the base of Q_6 , it is to be turn ON. So, the output of NOR is at logic '1'.

- If any input is at high level (-0.8V), the corresponding transistor is turned ON and Q_3 is turned OFF because it needs at least 0.6V to start conduction on. An input of -0.8V causes the transistor to conduct and apply -1.6V on the remaining emitters. Therefore, Q_3 is cut off. The voltage in resistor R_2 flows into the base of Q_5 ($L=V_{CC}$) then Q_5 is turned ON. The output is at logic '1'.

At the same time, at point M the voltage is 0V is applied to the base of the transistor Q_6 , it is to be turns off. So, the NOR output is logic '0'.

Characteristics of ECL

- Propagation delay is very LOW (<1ns)
- ECL is fastest logic family.
- ECL circuit usually operate with -Ve supplies. (+Ve terminal is connected to ground).
- In this logic family we consider the logic 0 as -1.6V and logic 1 as -0.8V.

TTL LOGIC FAMILY

TTL (Transistor Transistor Logic) family is most popular logic family. In TTL circuits, multi-emitter transistor is used at the input instead of diode. TTL IC are given the numerical designation as 5400 and 7400 series.

TTL NAND Gate Circuit

The basic gate of this family is TTL NAND gate shown in Fig. 6.4. The diodes D_1 and D_2 are replaced by emitter-base junctions of a multiple emitter transistor labeled Q_1 .

The extra output stage is known as totem-pole stage because three output components Q_3 and Q_4 and diode are stacked on one another. This arrangement will increase the speed and output current capability.

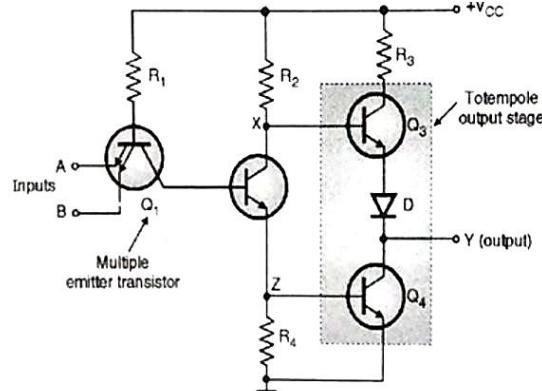


Fig. 6.4

The function of diode is to prevent both Q_3 and Q_4 being turned ON simultaneously.

Working

- When both or any input is low, transistor T_1 becomes forward bias and goes in saturation region, thus potential of Q_1 collector becomes low. Q_2 goes into cut off region. The potential of Q_2 emitter becomes low, which derives output transistor Q_3 . We receive a HIGH output at the collector of Q_3 . In this condition, Q_4 transistor remains in saturation region.
- When both inputs are high, reverse process takes place. Thus, output becomes LOW.

Characteristics of TTL

- TTL has greater speed than DTL.
- Less noise immunity.
- Power dissipation is 10 mW.
- It has fan-in of 6 and fan-out of 10.
- Propagation time delay is 5-15 nsec.

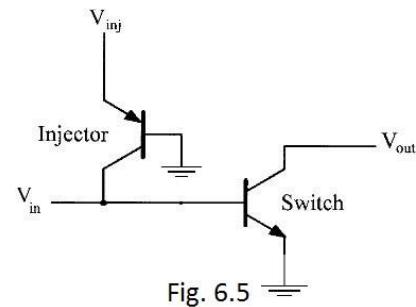
IIL (I²L) LOGIC FAMILY

Integrated injection logic (IIL or I^2L) is a class of digital circuits built with multiple collector bipolar junction transistors. The logic voltage levels are very close (High: 0.7V, Low: 0.2V), I^2L has high noise immunity because it operates by current instead of voltage.

I^2L NOT Gate Circuit

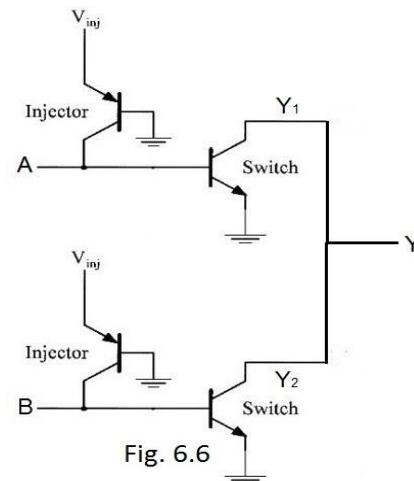
It uses no biasing resistor at all because resistor require lot of power and space on IC chip. This logic uses only bipolar junction transistors. Basic logic units use multi-collector NPN transistors which are powered from PNP transistors.

The heart of an I^2L circuit is the common emitter open collector inverter shown in Fig. 6.5.



Working

If the bias current is shunted to ground (low logic level), the transistor turns off and the collector floats (high logic level). If the bias current is not shunted to ground because the input is high-z (high logic level), the bias current flows through the transistor to the emitter, switching on the transistor, and allowing the collector to sink current (low logic level). When the outputs of two inverters are wired together, the result is a two-input NOR gate because the configuration (NOT A) AND (NOT B) is equivalent to NOT (A OR B).



Characteristics of I^2L

- This logic uses only bipolar junction transistors.
- It uses very small chip area.
- Easily fabricated and economical.
- Power dissipation is low (1mW).
- It has noise margin 0.35 V.
- It has fan-out of 8.
- Propagation time delay is 1 nSec.

CMOS LOGIC FAMILY

Complementary metal–oxide–semiconductor, abbreviated as CMOS is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits.

In CMOS circuit, both p-channel and n-channel enhancement MOSFET devices are fabricated on same chip. This causes density to be reduced and complex fabrication process. However, CMOS transistors are known for their efficient use of electrical power.

CMOS NAND gate

A CMOS NAND gate is shown in Fig. 6.7.

T_1 and T_2 are N-channel MOSFETs while T_3 and T_4 are P-channel MOSFETs.

When both inputs A & B are HIGH, then T_1 & T_2 are ON while T_3 & T_4 are OFF. Hence, output is connected to GND i.e. LOW.

If either input is LOW, then either T_3 or T_4 is ON, connecting output is $+V_{CC}$ i.e. HIGH.

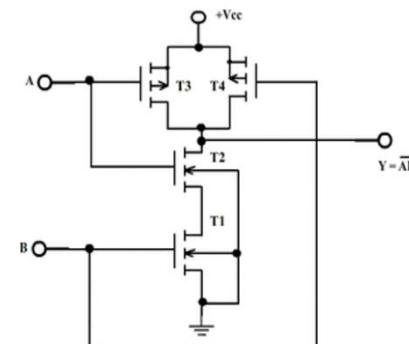


Fig. 6.7

CMOS NOR gate

Similar is working of CMOS NOR gate shown in Fig. 6.8.

Here, P-channel devices are in series and N-channel devices are in parallel.

Characteristics of CMOS

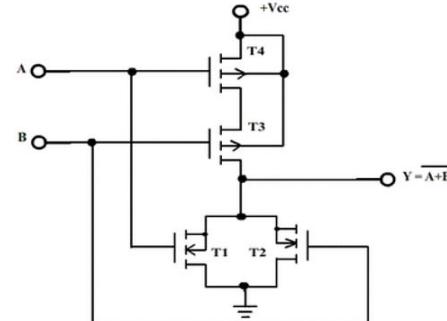


Fig. 6.8

- Dissipates low power. The power dissipation is typically 10 nW per gate.
- Short propagation delays: The propagation delays are usually around 25 nS to 50 nS.
- Rise and fall times are controlled: The rise and falls are usually ramps instead of step functions, and they are 20 - 40% longer than the propagation delays.
- Noise immunity approaches 50% or 45% of the full logic swing.
- Voltage levels range from 0 to VDD. A low level is anywhere between 0 and 1/3 VDD while a high level is between 2/3 VDD and VDD.

INTERFACING LOGIC FAMILIES

Interfacing can be defined as the design of the interconnections between circuits that shift the levels of voltage and current to make them compatible.

CMOS AND TTL INTERFACING

CMOS and TTL are the two most widely used logic families. Incompatibility of ICs belonging to different families mainly arises from different voltage levels and current requirements associated with LOW and HIGH logic states at the inputs and outputs.

CMOS driving TTL

For CMOS gate driving N TTL gates arrangement to operate properly, the following conditions are required to be satisfied,

$$V_{OH}(\text{CMOS}) \geq V_{IH}(\text{TTL})$$

$$V_{OL}(\text{CMOS}) \leq V_{IL}(\text{TTL})$$

$$-I_{OH}(\text{CMOS}) \geq NI_{IH}(\text{TTL})$$

$$I_{OL}(\text{CMOS}) \geq -NI_{IL}(\text{TTL})$$

The first possible type of CMOS-to-TTL interface is the one where both ICs are operated from a common supply. TTL family has a recommended supply voltage of 5 V, whereas the CMOS family devices can operate over a wide supply voltage range of 3–18 V. The CMOS output has a V_{OH} (min.) of 4.95V (for $V_{CC} = 5$ V) and a V_{OL} (max.) of 0.05 V, which is compatible with V_{IH} (min.) and V_{IL} (max.) requirements of approximately 2 and 0.8V respectively for TTL family devices.

For current level compatibility, a CMOS IC belonging to the 4000B family can feed one LS TTL or two low-power TTL unit loads. When a CMOS IC needs to drive a standard TTL or a Schottky TTL device, a CMOS buffer (4049B or 4050B) is used. 4049B and 4050B are hex buffers of inverting and noninverting types respectively, with each buffer capable of driving two standard TTL loads.

Fig. 6.9. shows a CMOS-to-TTL interface with both devices operating from 5V supply and the CMOS IC driving a low-power TTL or a low-power Schottky TTL device.

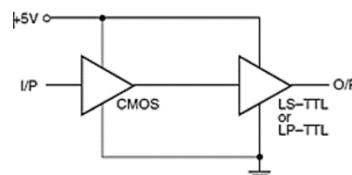


Fig. 6.9

Fig. 6.10. shows a CMOS-to-TTL interface where the TTL device in use is either a standard TTL or a Schottky TTL.

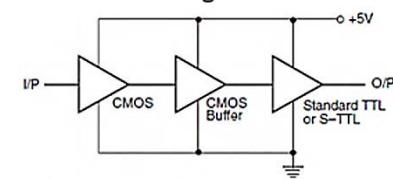


Fig. 6.10

The CMOS-to-TTL interface when the two are operating on different power supply voltages can be achieved in several ways. One such scheme is shown below. In this case, there is both a voltage level as well as a current level compatibility problem.

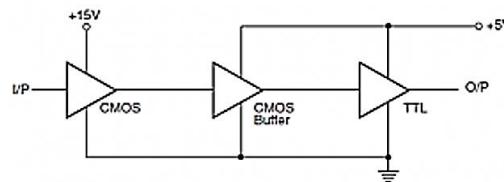


Fig. 6.11

TTL Driving CMOS

For TTL gate driving N CMOS gates arrangement to operate properly, the following conditions are required to be satisfied:

$$\begin{aligned} V_{OH}(\text{TTL}) &\geq V_{IH}(\text{CMOS}) \\ V_{OL}(\text{TTL}) &\leq V_{IL}(\text{CMOS}) \\ -I_{OH}(\text{TTL}) &\geq NI_{IH}(\text{CMOS}) \\ I_{OL}(\text{TTL}) &\geq -NI_{IL}(\text{CMOS}) \end{aligned}$$

In the TTL-to-CMOS interface, current compatibility is always there. The voltage level compatibility in the two states is a problem. V_{OH} (min.) of TTL devices is too low as regards the V_{IH} (min.) requirement of CMOS devices. When the two devices are operating on the same power supply voltage, that is, 5 V, a pull-up resistor of $10\text{ k}\Omega$ achieves compatibility as shown in Fig. 6.12. The pull-up resistor causes the TTL output to rise to about 5V when HIGH.

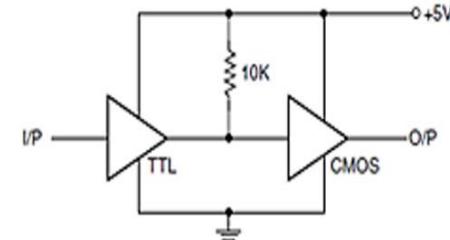


Fig. 6.12

When the two are operating on different power supplies, one of the simplest interface techniques is to use a transistor (as a switch) in-between the two, as shown in Fig. 6.13(a). Another technique is to use an open collector type TTL buffer as shown in Fig. 6.13(b).

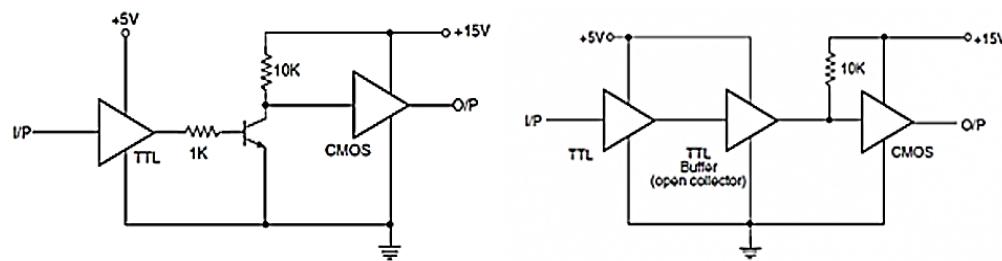


Fig. 6.13

(a)

(b)

LOGIC GATES PERFORMANCE FACTORS

Each logic family has different characteristics which are the key parameters in deciding the logic family for any circuit design. These parameters are supply voltage range, speed of operation, power dissipation, noise margin, fan in, fan out etc.

Voltage Levels

The following currents and voltages are specified which are very useful in the design of digital systems.

High-level input voltage, V_{IH} : This is the minimum input voltage which is recognized by the gate as logic 1.

Low-level input voltage, V_{IL} : This is the maximum input voltage which is recognized by the gate as logic 0.

High-level output voltage, V_{OH} : This is the minimum voltage available at the output corresponding to logic 1.

Low-level output voltage, V_{OL} : This is the maximum voltage available at the output corresponding to logic 0.

Current Levels

High-level input current, I_{IH} : This is the minimum current which must be supplied by a driving source corresponding to 1 level voltage.

Low-level input current, I_{IL} : This is the minimum current which must be supplied by a driving source corresponding to 0 level voltage.

High-level output current, I_{OH} : This is the maximum current which the gate can sink in 1 level.

Low-level output current, I_{OL} : This is the maximum current which the gate can sink in 0 level.

Propagation delay time

A pulse through a gate takes a certain amount of time to propagate from input to output. This interval of time known as the propagation delay of the gate. It is expressed in nS.

There are two delay times, $t_{p_{HL}}$: when the output goes from the HIGH state to the LOW state and $t_{p_{LH}}$, corresponding to the output making a transition from the LOW state to the HIGH state.

Fan out

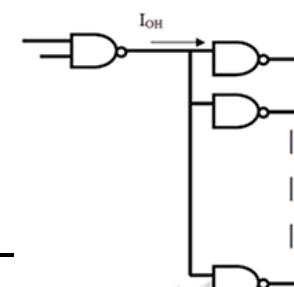


Fig. 6.14

It specifies the number of standard loads that the output of the gate can drive without affecting its normal operation. A standard load is usually defined as the amount of current needed by an input of another gate in the same family as shown in Fig. 6.14.

Fan in

Fan in is the number of inputs connected to the gate without any degradation in the voltage level. It is decided by the input current sinking capability of a logic gate as shown in Figure. It is expressed in terms of standard inputs or units loads (ULs).

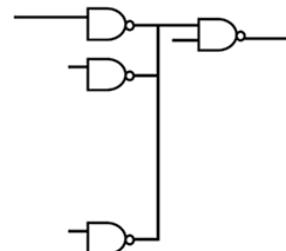


Fig. 6.15

Noise Margin

It is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. It is expressed in volts.

The noise margin is the difference between the guaranteed output voltage level and the required input voltage level of a logic gate.

- low level noise margin = $V_{IL(max)} - V_{OL(min)}$ = 0.4 V(74XX)
- high level noise margin = $V_{OH(min)} - V_{IH(max)}$ = 0.4 V(74XX)

Power Dissipation

Power dissipation is measure of power consumed by the gate when fully driven by all its inputs. It is expressed in milli watts.

Speed Power Product

A common means for measuring and comparing the overall performance of an IC family is the speed-power product which obtained by multiplying the gate propagation delay by the gate power dissipation. The smaller the product, the better the overall performance. It is expressed in Pico Joule.

Operating temperature

The IC gates and other circuits are temperatures sensitive being semiconductor devices. However, they designed to operate satisfactorily over a specified range of temperatures. The range specified for commercial applications is 0 to 70°C, for industrial it is 0 to 85°C and for military applications, it is -55°C to 125°C.

EXERCISE

SECTION-I (MCQ's)

ANSWER KEY

1.	a	2.	d	3.	c	4.	c	5.	b
6.	c	7.	b	8.	c	9.	b	10.	c

SECTION-II (Short Questions)

1. Enlist logic families.
 2. Define noise margin.
 3. Define propagation delay time.
 4. Define V_{IH} and V_{IL} .
 5. Define V_{OH} and V_{OL} .
 6. What is meant by totem pole output?
 7. Define Fan in.
 8. Define Fan out.
 9. What is input voltage level for TTL family?
 10. What is output voltage level for CMOS family?
 11. What are the disadvantages of RTL family?
 12. Define speed power product.

13. State the advantages of ECL.
14. Define interfacing of different logic families.
15. What are merits of I²L logic?

SECTION-III (Long Questions)

1. Draw and explain TTL NAND gate with totem pole output.
2. Draw circuit of CMOS NOR gate and explain its working.
3. Compare characteristics of TTL and CMOS logic families.
4. Explain briefly data sheet parameter of digital IC.

INTERFACING WITH ANALOG WORLD

CHAPTER-7

Objectives

At the end of this chapter, a student will be able to

- Discuss needs and applications of DACs
- Describe Binary weighted DAC
- Describe Ladder type DAC
- Discuss needs and applications of ADCs
- Describe the construction and working of Simultaneous ADC
- Describe the construction and working of Counter type ADC
- Describe the construction and working of Dual slop ADC
- Describe the construction and working of Successive Approximation ADC

NEED OF ADC AND DAC

In the real world, most of the signals sensed and processed by humans are analog signals such as sound, temperature, light, and velocity etc. Microprocessors can only perform processing on digitized signals. Analog-to-Digital provides a link between the analog world of transducers and the digital world of signal processing and data handling.

Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) are two converting interfaces which are necessary to allow digital electronic equipments to process the analog signals.

Example:

Take the audio signal processing in Fig. 7.1. as an example. ADC converts the analog signal collected by audio input equipment, such as a microphone, into a digital signal that can be processed by computer. DAC converts the processed digital signal back into the analog signal that is used by audio output equipment such as a speaker.



Fig. 7.1

APPLICATIONS OF ADC AND DAC

D/A Converter Applications

- i- Digital Audio: (CD)
- ii- Digital Video: (DVD, Digital Still Camera)
- iii- Communication Equipment: (Smartphones, FAX)
- iv- PCs: (Audio, Video cards)
- v- Measurement instruments: (Programmable power supplies, etc.)

A/D Converter Applications

- i- Digital Audio: (Sound recording, Pulse-code modulation)
- ii- Digital signal processing: (TV tuner cards, microcontrollers, digital storage oscilloscopes)
- iii- Scientific instruments: (radar systems, temperature sensors)

DIGITAL TO ANALOG CONVERTER

A digital-to-analog converter, or DAC, is an electronic device that converts a digital code to an analog signal such as a voltage or current. The digital signal is represented with a binary code, which is a combination of bits 0 and 1.

Block diagram of a general DAC is shown in Fig. 7.2.

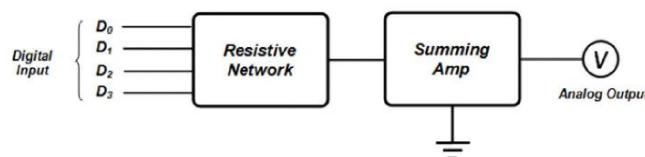


Fig. 7.2

There are two parts of a DAC. First is a resistor network which can be a binary weighted resistor network or a ladder network. Second part is a summing amplifier. The output voltage is proportional to the applied binary input. The output voltage can be calculated using following formula.

$$V_o = K \text{ (decimal equivalent of binary input)}$$

Where K is a constant whose value depends upon the values of resistors used in the circuit.

There are two types of digital to analog converters.

- i- Binary Weighted Resistor DAC
- ii- R-2R Ladder Type DAC

BINARY WEIGHTED RESISTOR DAC

The binary-weighted-resistor DAC employs the characteristics of the inverting summer Op Amp circuit. In this type of DAC, the output voltage is

the inverted sum of all the input voltages. This DAC consists of a resistor network and an operational amplifier with a feedback resistor. Values of input resistors are multiples of binary weights i-e 1, 2, 4, 8 and so on.

Construction

The circuit for a 4-bit DAC using binary weighted resistor network is shown in Fig. 7.3. This is constructed by using a summing amplifier and a set of resistors R, 2R, 4R and 8R as its inputs. The resistors are scaled to represent weights for the different input bits.

The resistor with the lowest value R corresponds to the highest weighted binary input D_3 (MSB) [$2^3 = 8$], and 2R, 4R, 8R correspond to the binary weights of D_2 ($2^2 = 4$), D_1 ($2^1 = 2$), and D_0 (LSB) [$2^0 = 1$] respectively.

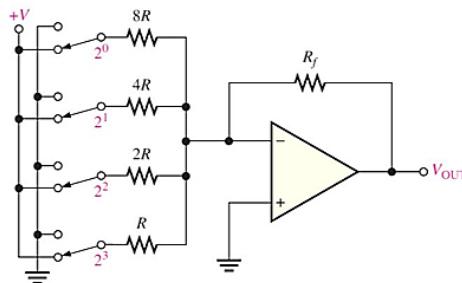


Fig. 7.3

Working

Suppose I_3 , I_2 , I_1 and I_0 are the currents flowing through the resistors R, 2R, 4R and 8R respectively. I_f is the current through feedback resistor R_f .

$$I_f = I_3 + I_2 + I_1 + I_0$$

If all switches are connected to +V point, then

$$I_3 = \frac{V}{R}, \quad I_2 = \frac{V}{2R}, \quad I_1 = \frac{V}{4R}, \quad I_0 = \frac{V}{8R}$$

$$I_f = \frac{V}{R} + \frac{V}{2R} + \frac{V}{4R} + \frac{V}{8R}$$

$$I_f = \frac{V}{R}(1 + 0.5 + 0.25 + 0.125) = 1.875 \frac{V}{R}$$

The above equation is the maximum current, when all switches are connected to "+V" point. This condition is equivalent to binary input "1111".

The above equation is written in general form as follows.

$$I_f = \frac{V}{R}(1D_3 + 0.5D_2 + 0.25D_1 + 0.125D_0)$$

Where D_3 , D_2 , D_1 , D_0 are binary inputs, which may be 0 or 1 depending on the switch positions.

The output voltage can be calculated as follows.

$$V_O = -I_f R_f$$

Advantages

- Simple analysis.
- Fast Conversion.
- Economical.

Dis-advantages

- When number of binary input increases, it is not easy to maintain the resistance ratio.
- Very wide ranges of different values of resistors are required.
- Different current flows through resistors, so their wattage ratings are also different.
- Accuracy and stability of conversion depends primarily on the absolute accuracy of the resistors.

R-2R LADDER TYPE DAC

The R-2R ladder DAC is modern type of resistor network. It has only two values of resistors the R and 2R. These values repeat throughout in the circuit. The OPAMP is used at output for scaling the output voltage.

Construction

The Fig. 7.4. shows the 4-bit R-2R ladder DAC circuit using op-amp. Here only two values of resistors are required i.e. R and 2R. The typical value of feedback resistor is $R_f = 2R$. The resistance R is normally selected any value between 2.5 kΩ to 10 kΩ.

Working

The operation of R-2R ladder DAC is easily explained considering the weights of the different bits one at a time. This can be followed by superposition to construct analog output corresponding any digital input word.

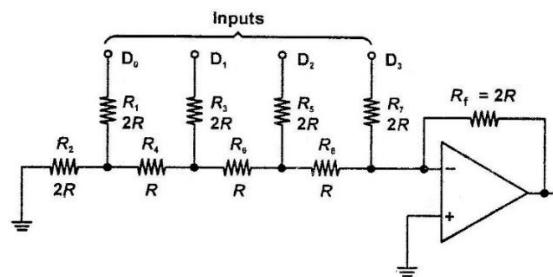


Fig. 7.4

Let $D_3D_2D_1D_0 = 1000$ at the input. A simplified equivalent circuit can be drawn as shown in Fig. 7.5. In this condition, $I = \frac{V}{2R}$

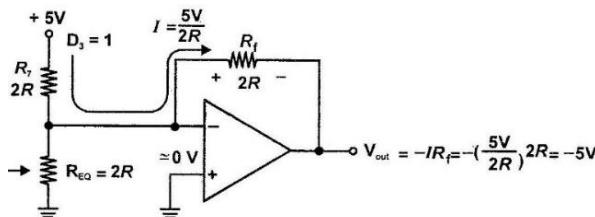


Fig. 7.5

Now suppose digital input of the same circuit is changed to $D_3D_2D_1D_0 = 0100$.

Then $I = \frac{V}{4R}$.

When $D_3D_2D_1D_0 = 0010$, I will be $\frac{V}{8R}$

For $D_3D_2D_1D_0 = 0001$, I will be $\frac{V}{16R}$

When all bits are high, then all these currents will be added. So, the equation will be as follows.

$$I = \frac{V}{2R} + \frac{V}{4R} + \frac{V}{8R} + \frac{V}{16R}$$

The output voltage can be calculated as follows.

$$V_O = -IR_f$$

$$V_O = -\frac{R_f V}{R} (0.5D_3 + 0.25D_2 + 0.125D_1 + 0.0625D_0)$$

Advantages

- Only two values of resistors are used; R and 2R.
- Does not require high precision resistors.

ANALOG TO DIGITAL CONVERTER

An analog-to-digital converter, or ADC, converts analog signals into digital signals without altering their essential content. Fig. 7.6. shows the block diagram of an ADC.

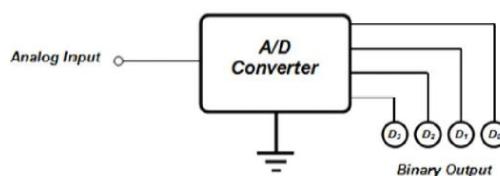


Fig. 7.6

The analog input is applied to a built-in comparator. This input is compared with a particular reference voltage. If analog voltage is greater than reference voltage, then a counter in circuit starts counting the clock pulses. When the reference voltage equals the analog voltage, counter stops the

process of counting. Hence, the output code of counter represents the digital output.

There are following types of analog to digital converters.

- i- Simultaneous or Flash DAC
- ii- Counter Type ADC
- iii- Dual Slope ADC
- iv- Successive Approximation ADC

SIMULTANEOUS ADC

The flash ADC provides a fast conversion time because of the parallel process. The flash ADC uses comparators that compare reference voltages with the analogue input voltage.

The flash ADC uses comparators that compare reference voltages with the analogue input voltage. When the analogue voltage exceeds the reference voltage for a given comparator, a High is generated. In general ($2^n - 1$) comparators are required. So, for 8-bit conversion 255 comparators are required.

Construction

The reference voltage for each comparator is set by the resistive voltage divider network. The output of each comparator is connected to an input of the priority encoder. The encoder is sampled by a pulse on the Enable input and a 3-bit binary code representing the analogue input appears on the encoder output. The binary code is determined by the highest order input having a High level.

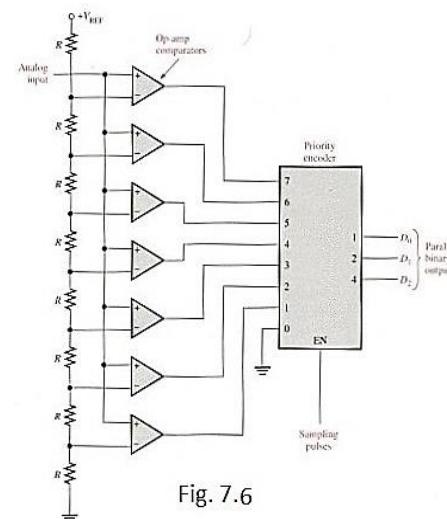


Fig. 7.6

Working

- The flash ADC comprises an array of comparators.
- Each comparator is connected to a resistive voltage divider and to the analogue input voltage.
- The resistive voltage divider consists of equal valued resistors connected in series with the reference voltage V_{REF} .

- Thus, each comparator compares the analogue input voltage with a slightly different voltage from the divider.
- Those comparators which are connected to divider resistors where the divider voltage is lower than the analogue input voltage will give a high output.
- The other comparators will produce a low output.
- Larger analogue input voltages will result in more comparator high outputs.
- The pattern of comparator high/low outputs is applied to encoder circuits which convert the data into a binary output number which is proportional to the ratio of the analogue input voltage to the reference voltage.

COUNTER TYPE ADC

The Counter type ADC is the basic type of ADC which is also called stair case approximation ADC. This circuit consists of N bit counter, DAC and Op-amp comparator.

Circuit

The counter type ADC is constructed using a binary counter, DAC and a comparator. The output voltage of a DAC is equivalent to corresponding digital input to DAC.

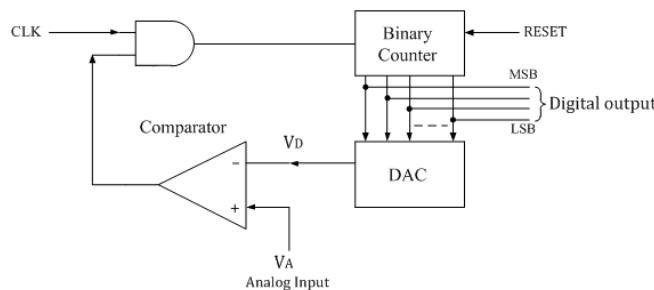


Fig. 7.7

Working

- The analog input voltage is given to non-inverting terminal of comparator.
- The counter type ADC is reset to zero count by reset pulse applied to reset terminal.
- The clock pulses go through the AND gate which is enabled by the voltage comparator high output. The number of pulses counted increase with time.

- The binary word representing this count is used as the input of a D/A converter whose output is staircase type as shown in Fig. 7.7.
- The analog output V_D of DAC is compared to the analog input V_A by the comparator. If $V_A > V_D$, the output of comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter.
- When $V_A < V_D$, the output of the comparator becomes low and the AND gate is disabled. This stops the counting at the time $V_A \leq V_D$ and the digital output of the counter represents the analog input output voltage V_A .
- For new value of analog input V_A , a second reset pulse is applied to clear the counter. Upon the end of the reset, the counting begins again.

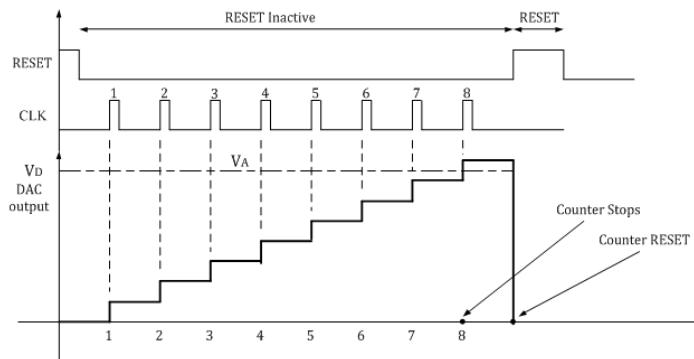


Fig. 7.8

Advantages

- Simple construction.
- Easy to design and less expensive.
- Speed can be adjusted by adjusting the clock frequency.
- Faster than dual slope type ADC.

Disadvantage

Low speed is the most serious drawback of this method. The conversion time can be as $(2^n - 1) T$ depending upon the magnitude of input voltage V_A .

DUAL SLOPE ADC

In the dual-slope technique, an integrator is used to integrate an accurate voltage reference for a fixed period of time. The same integrator is then used to integrate with the reverse slope, the input voltage, and the time required to return to the starting voltage is measured.

Circuit

In the dual-slope converter, the unknown input voltage is applied to the input of the integrator and allowed to ramp for a fixed time period. Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero. The logic diagram for the same is shown in Fig. 7.9.

Working

- The analog switch first connects V_A to the integrator. The binary counter is initially reset to 0000; the output of integrator reset to 0V and the input to the integrator is switched to the unknown analog input voltage V_A .
- The analog input voltage V_A is integrated by the inverting integrator and generates a negative ramp output. The output of comparator is positive and the clock is passed through the AND gate. This results in counting up of the binary counter.

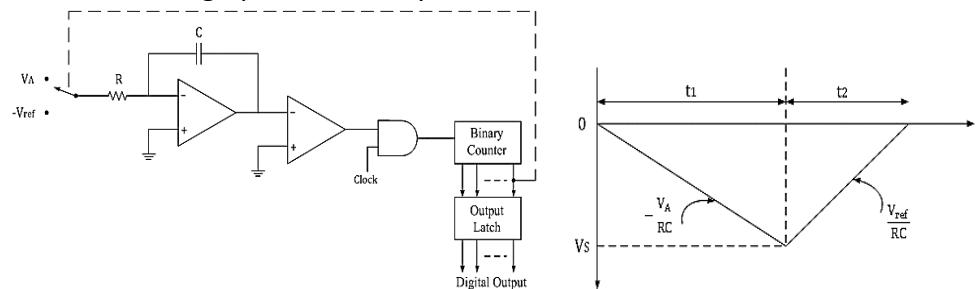


Fig. 7.9

- The negative ramp continues for a fixed time period t_1 , which is determined by a count detector for the time period t_1 . At the end of the fixed time period t_1 , the ramp output of integrator is given by

$$V_s = -\frac{V_A}{RC} \times t_1$$

- When the counter reaches the fixed count at time period t_1 , the binary counter resets to 0000 and switches the integrator input to a negative reference voltage $-V_{ref}$, providing a discharge path for the capacitor.
- Now the ramp generator starts with the initial value $-V_s$ and increases in positive direction until it reaches 0V and the counter gets advanced.
- When V_s reaches 0V, comparator output becomes at logic 0 and the AND gate is deactivated. The count stops and the value is stored in the register. Now, the conversion cycle is said to be completed and the positive ramp voltage is given by

$$V_S = \frac{V_{ref}}{RC} \times t_2$$

Advantages

Very precise. The sources of errors are only the comparison with zero and the clock period.

Disadvantage

Slow speed. The ADC needs time to ramp up and down the output voltage and doubles with each bit added to the representation, for a fixed clock period.

SUCCESSIVE APPROXIMATION ADC

A successive approximation ADC is a type of ADC that converts an analog input into a digital output via a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.

Construction

The ADC is interfaced to a controller - usually a microprocessor. It consists of a very special counter circuit known as a successive-approximation register, a DAC and a comparator. Analog input is applied to non-inverting input of comparator.

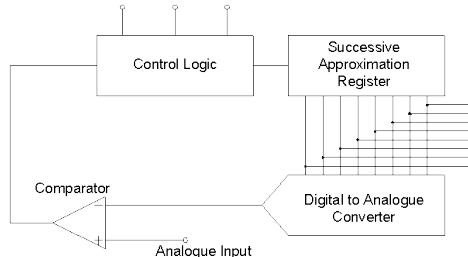


Fig. 7.10

Working

- The controller decides when a conversion is to be performed and initiates the conversion by asserting the Start Convert signal line into the control logic.
- The Control Logic monitors the input to determine whether the present contents of the register represent a value which is below or above the analogue input voltage.
- Each bit is set in turn starting with the MSB and working down to the LSB.

- The effect of setting each bit is noted by the control logic and if setting a particular bit results in a DAC output in excess of the analogue input voltage, the bit is cleared before moving on to the next bit, otherwise the bit is left set.
- At the end of the process, the LSB is adjusted and the conversion is complete.
- The control logic signals this to the controller/microprocessor by asserting the End of Conversion line and the digital output is taken from the register output.

EXERCISE

SECTION-I (MCQ's)

1. A digital to analog converter consists of;
 - (a) Resistors
 - (b) Op-Amp
 - (c) Diodes
 - (d) Both a & b
2. R-2R ladder type digital to analog converter has resistors of;
 - (a) Two values
 - (b) Four values
 - (c) Same values
 - (d) None of these
3. Digital to analog converter is also called
 - (a) Encoder
 - (b) Decoder
 - (c) Inverter
 - (d) Multiplexer
4. Resolution of a 4-bit DAC is
 - (a) 6.67%
 - (b) 3.39%
 - (c) 0.1%
 - (d) 6%
5. The highest speed ADC is
 - (a) Counter type
 - (b) Ramp generator
 - (c) Simultaneous
 - (d) All of these
6. A 3-bit simultaneous ADC has number of comparators
 - (a) 3
 - (b) 4
 - (c) 5
 - (d) 7
7. The slowest speed ADC is
 - (a) Counter type
 - (b) Ramp generator
 - (c) Dual Slope
 - (d) All of these
8. In weighted resistors DAC operational amplifier is used as
 - (a) Inverting amplifier
 - (b) Summing amplifier
 - (c) Non-inverting amplifier
 - (d) Both a & b
9. Simultaneous ADC is also called;
 - (a) Flash
 - (b) Dual Slope
 - (c) Ramp type
 - (d) Counter type
10. Counter type ADC is also called;
 - (a) Flash
 - (b) Dual Slope
 - (c) Staircase
 - (d) Ramp

ANSWER KEY

- | | | | | |
|------|------|------|------|-------|
| 1. d | 2. a | 3. b | 4. a | 5. c |
| 6. d | 7. c | 8. d | 9. a | 10. c |

SECTION-II (Short Questions)

1. Define analog to digital converter.

2. Define digital to analog converter.
3. Describe need of DAC.
4. Describe need of ADC.
5. Define transducer with example.
6. Name any two types of analog to digital converter.
7. Name two types of digital to analog converter.
8. Write the applications of DAC & ADC.
9. What is disadvantage of binary weighted resistor DAC?
10. Name two parts of a DAC circuit.
11. What is advantage of R-2R ladder DAC?
12. Define resolution of a digital to analog converter.
13. What is advantage of flash converter?
14. How many comparators are used in a 4-bit flash ADC?
15. What is disadvantage of dual slope ADC?

SECTION-III (Long Questions)

1. Explain binary weighted DAC with circuit diagram and truth table.
2. Describe briefly successive approximation A to D convertor working.
3. Explain the working of ladder type D to A converter using circuit.
4. Describe need and use of DAC and ADC in a digital circuit with example.
5. Explain working of Dual slope analog to digital convertor with diagram.

MEMORY**CHAPTER-8****Objectives**

At the end of this chapter, a student will be able to

- Discuss Memory Technologies.
- Discuss General Memory Operation.
- Describe Memory Considerations.
- List Types of Memories.
- Describe ROM.
- Describe RAM & its types.
- Describe PLDs.
- Describe Magnetic and Optical Memories
- Discuss applications in Digital systems.

A memory is just like a human brain. It is used to store data and instructions. Memory is major part of computers that categories into several types. Computer memory is any physical device capable of storing information temporarily or permanently.

TYPES OF MEMORY

Memory is primarily of three types

- Cache Memory (Inner Memory)
- Primary Memory (Main Memory)
- Secondary Memory (External Memory)

Cache Memory

Cache memory is a very high speed semiconductor memory which can speed up CPU. It is used to hold those parts of data and program which are most frequently used by CPU.

Primary Memory (Main Memory)

Primary memory holds only those data and instructions on which computer is currently working. RAM, ROM and Hard disk are examples of primary memory. Following are characteristics of main memory.

- These are semiconductor and magnetic memories
- Faster than secondary memories.
- A computer cannot run without primary memory.

Secondary Memory

This type of memory is also known as external memory. CPU directly does not access these memories. Contents of secondary memories are first transferred to main memory, and then CPU can access it. For example: disk, CD-ROM, DVD etc. Following are characteristics of secondary memory.

- These are magnetic and optical memories
- Computer may run without secondary memory.
- Slower than primary memories.

MEMORY TECHNOLOGIES

There are two major memory technologies.

- (a) Bipolar technology (b) MOS technology

Bipolar technology RAM and ROM mostly belongs to TTL and ECL logic families. These types of RAM and ROM used rarely because of low storage capacity, high cost and high power dissipation.

MOS technology memories are frequently used. It has low size. Thousands of data bits can be stored on a single chip. Power dissipation is very low and cost per bit is also low. N-channel MOSFETs are mostly used.

MEMORY OPERATION

Data must be put into the memory and data must be copied from the memory when needed. These tasks are completed by write and read operations respectively. The addressing operation, which is part of both the write and the read operations, selects the specified memory address.

Bit, Nibble, Byte and Word

The smallest unit of binary data, is the bit. An 8-bit unit is called a byte. The byte can be split into two 4-bit units that are called nibbles. A complete unit of information is called a word and generally consists of one or more bytes.

Write Operation

The write operation puts data into a specified address in the memory. Data units go into the memory during a write operation on a set of lines called the data bus. The data bus is bidirectional.

To store a byte of data in the memory, a code held in the address register is placed on a set of lines called the address bus as shown in Fig. 8.1.

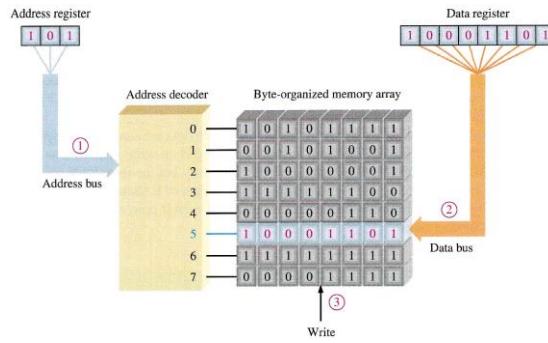


Fig. 8.1

Once the address code is on the bus, the address decoder decodes the address and selects the specified location in the memory. The memory then gets a write command, and the data byte held in the data register is placed on the data bus and stored in the selected memory address. When a new data byte is written into a memory address, the current data byte stored at that address is overwritten.

Read Operation

Data units come out of the memory during a read operation on the data bus. In read operation, a code held in the address register is placed on the address bus. The address decoder decodes the address and selects the specified location in the memory. The memory then gets a read command, and a "copy" of the data byte that is stored in the selected memory address is placed on the data bus and loaded into the data register. When a data byte is read from a memory address, it also remains stored at that address. This operation is shown in Fig. 8.2.

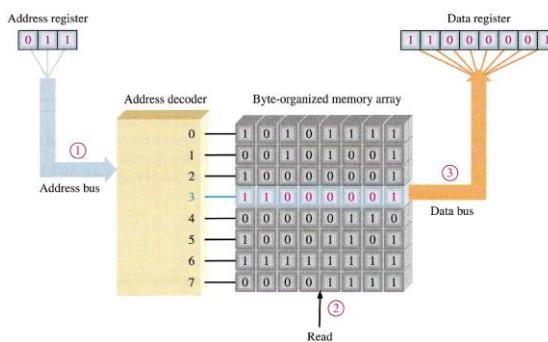
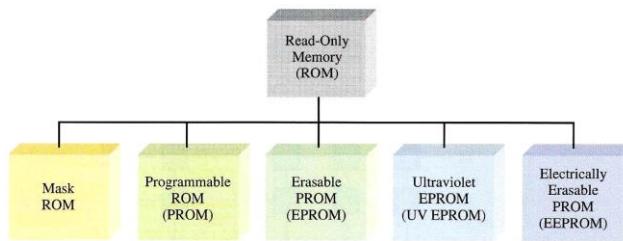


Fig. 8.2

READ ONLY MEMORY (ROM)

A ROM contains permanently or semi-permanently stored data, which can be read from the memory but either cannot be changed at all or cannot be changed without specialized equipment. ROMs retain stored data when the power is off and are therefore nonvolatile memories.

Semiconductor ROMs are categorized as follows.



Mask ROM

The mask ROM is the type in which the data are permanently stored in the memory during the manufacturing process. Once the memory is programmed, it cannot be changed. Fig. 8.3. shows MOS ROM cells. The presence of a connection from a row line to the gate of a transistor represents a 1 and no gate connection to a row line represents a 0.

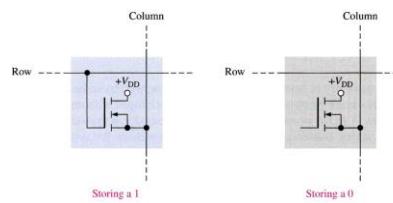


Fig. 8.3

PROM

The PROM, or programmable ROM, is the type in which the data are electrically stored by the user with the aid of specialized equipment. In the programming process, a sufficient current is injected through the fusible link to burn it open to create a stored 0. The link is left intact for a stored 1. Both the mask ROM and the PROM can be of either MOS or bipolar technology.

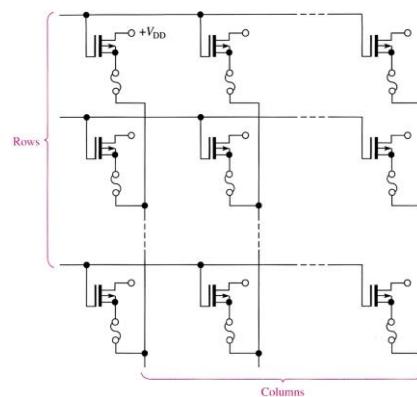


Fig. 8.4

EPROM

An EPROM is an erasable PROM. It can be reprogrammed. The data bits in this type of array are represented by the presence or absence of a stored gate charge. Erasure of a data bit is a process that removes the gate charge. Two basic types of erasable PROMs are the ultraviolet erasable PROM (UV EPROM) and the electrically erasable PROM (EEPROM).

UV PROM

UV EPROM device is recognized by the transparent quartz lid on the package, as shown in Fig. 8.5. Erasure is done by exposure of the chip to high-intensity ultraviolet radiation through the quartz window on top of the package. The positive charge stored on the gate is neutralized after several minutes to an hour of exposure time.

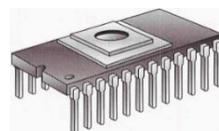


Fig. 8.5

EEPROM

An electrically erasable PROM can be both erased and programmed with electrical pulses. The EEPROM can be rapidly programmed and erased in-circuit for reprogramming.

Applications of ROM

A ROM stores data that are used repeatedly in system applications, such as tables, conversions, or programmed instructions for system initialization and operation.

RANDOM ACCESS MEMORY (RAM)

RAMs are read/write memories in which data can be written into or read from any selected address in any sequence. There are two types of RAM.

- i- Static Random Access Memory
- ii- Dynamic Random Access Memory

STATIC RANDOM ACCESS MEMORY (SRAM)

Static RAMs generally use latches as storage elements. As long as dc power is applied to a static memory cell, it can retain a 1 or 0 state indefinitely. If power is removed, the stored data bit is lost.

SRAM Cell

Fig. 8.6. shows a basic SRAM latch memory cell. The cell is selected by putting HIGH on row and column lines. A data bit (1 or 0) is written into the cell by

placing it on the Data in line. A data bit is read by taking it off the Data out line.

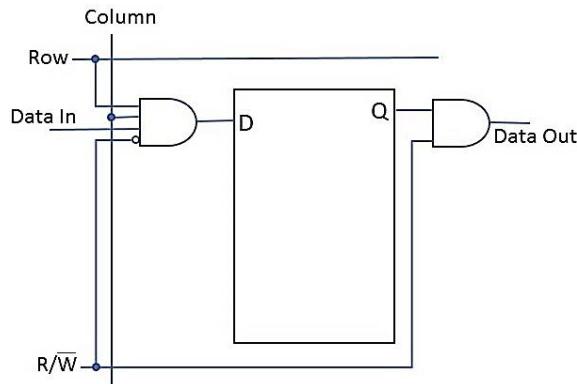


Fig. 8.6

Write operation in SRAM Cell

A HIGH on the row and column lines is applied to select the cell. To write a data unit, a bit (1 or 0) is applied to data input line. A LOW on the R/\bar{W} line (WRITE mode) enables the input AND gate and disables the output AND gate, which causes each data bit to be stored in a selected cell.

Read operation in SRAM Cell

A HIGH on the row and column lines is applied to select the cell. To read a data unit, the Read line is taken to its active state by applying HIGH on R/\bar{W} . This disables the input AND gate and enables the output AND gate. This causes the data bit stored in the selected cell to appear on the output.

DYNAMIC RANDOM ACCESS MEMORY (DRAM)

Dynamic memory cells store a data bit in a small capacitor. The advantage of this type of cell is allowing very large memory arrays to be constructed on a chip at a lower cost per bit. The disadvantage is that the capacitor lose the stored data bit unless its charge is refreshed periodically. To refresh requires additional memory circuitry and complicates the operation of the DRAM.

DRAM Cell

Figure shows a typical DRAM cell consisting of a single MOS transistor (MOSFET) and a capacitor. In this type of cell, the transistor acts as a switch. Input and output buffers are used for write and read operations. These buffers are controlled by R/\bar{W} signal. A refreshing buffer is also used for refreshing the data. These buffers are not shown in the cell for simplicity.

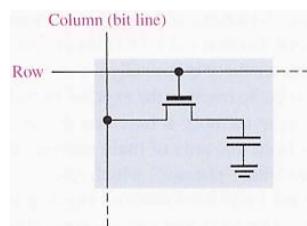


Fig. 8.7

Write operation in DRAM Cell

A LOW on the R/W line (WRITE mode) enables the tristate input buffer and disables the output buffer. A HIGH on the row line is applied to close the transistor. When a voltage is applied on the bit line, this will transfer to capacitor and store in it. When the row line is taken back LOW, the transistor turns off and disconnects the capacitor from the bit line.

Read operation in DRAM Cell

To read from the cell, the R/W (Read/Write) line is HIGH, enabling the output buffer and disabling the input buffer. When the row line is taken HIGH, the transistor turns on and connects the capacitor to the bit line and thus to the output buffer (sense amplifier), so the data bit appears on the data-output line.

Refreshing Process

For refreshing the memory cell, the R/W line is HIGH, the row line is HIGH, and the refresh line is HIGH. The transistor turns on, connecting the capacitor to the bit line. The output buffer is enabled, and the stored data bit is applied to the input of the refresh buffer, which is enabled by the HIGH on the refresh input. This produces a voltage on the bit line corresponding to the stored bit, thus refreshing the capacitor.

PROGRAMMABLE LOGIC DEVICES (PLDs)

Programmable Logic Devices (PLDs) are the integrated circuits that can be programmed in a laboratory to perform complex functions. They contain an array of AND gates & another array of OR gates. A PLD has an undefined function at the time of manufacture. A system designer implements a logic design with a device programmer that blows fuses on the PLD to control gate operation.

The process of entering the information into these devices is known as programming. Here, the term programming refers to hardware programming but not software programming.

Types of PLDs

PLD types can be classified into the following groups

- PROMs (Programmable Read Only Memory) - offer high speed and low cost for relatively small designs
- PLAs (Programmable Logic Array) - offer flexible features for more complex designs
- PALs (Programmable Array Logic) - offer good flexibility and are faster and less expensive than PLAs

PROM

PROM is a programmable logic device that has fixed AND array & Programmable OR array. The block diagram of PROM is shown in the Fig. 8.8.

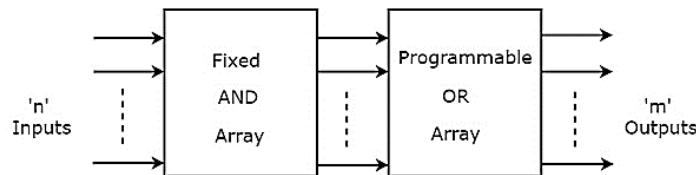


Fig. 8.8

Here, the inputs of AND gates are not of programmable type. So, we have to generate 2^n product terms by using 2^n AND gates having n inputs each.

Here, the inputs of OR gates are programmable. Since all the outputs of AND gates are applied as inputs to each OR gate. Therefore, the outputs of PROM will be in the form of sum of min terms.

PAL

Programmable array logic (PAL) architecture has a programmable AND array at the input and a fixed OR array at the output. The advantage of PAL is that we can generate only the required product terms of Boolean function by using programmable AND gates. The block diagram of PAL is shown in the Fig. 8.9.

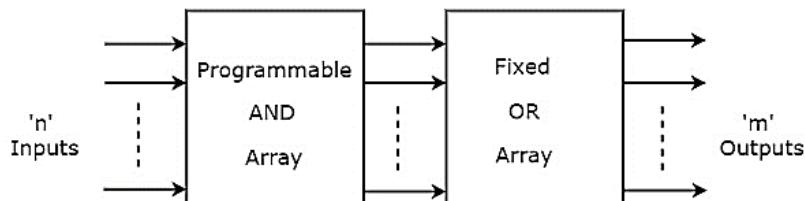


Fig. 8.9

Here, the inputs of AND gates are programmable. That means each AND gate has both normal and complemented inputs of variables.

Here, the inputs of OR gates are not of programmable type. Hence, apply those required product terms to each OR gate as inputs. Therefore, the outputs of PAL will be in the form of sum of products form.

PLA

A programmable logic array (PLA) device has a programmable AND array at the input and a programmable OR array at the output. Hence, it is the most flexible PLD. The block diagram of PLA is shown in the following figure.

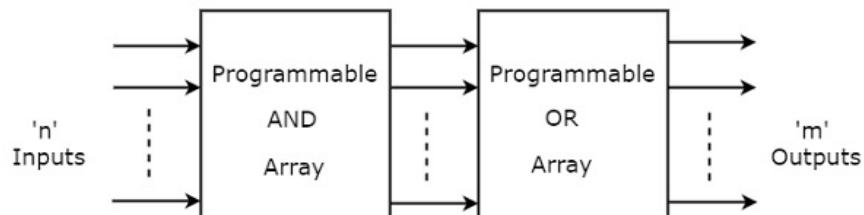


Fig. 8.10

Here, the inputs of AND gates are programmable. That means each AND gate has both normal and complemented inputs of variables.

Here, the inputs of OR gates are also programmable. Since all the outputs of AND gates are applied as inputs to each OR gate. Therefore, the outputs of PAL will be in the form of sum of products form.

MAGNETIC MEMORIES

A system of storing information through the alignment of small grains in a magnetic material is called magnetic memory. Once the grains have been aligned by an external magnetic field, the information remains stored for long periods of time.

MAGNETIC HARD DISKS

Computers use hard disks as the internal mass storage media. Hard disks consist of two or more platters made of aluminum alloy or a mixture of glass and ceramic covered with a magnetic coating. These platters are stacked to each other on a common shaft that turns the assembly at several thousand rpm. A hard disk drive is airtight sealed to keep the disks dust-free.

There is a read/write head for both sides of each disk since data are recorded on both sides of the disk surface.

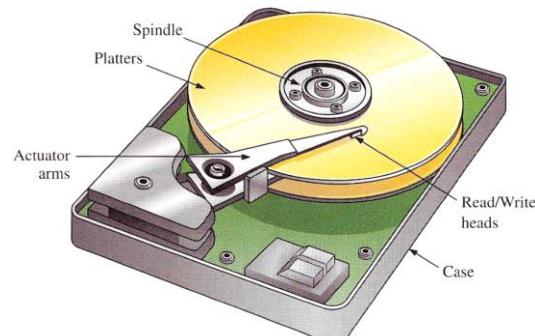


Fig. 8.11

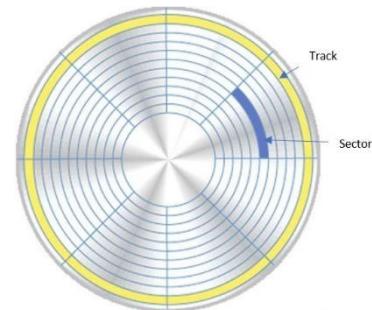
Basic Read /Write Head Principles

The read and write heads are usually combined in a single unit. The magnetic field produced by the write head according to the direction of a current pulse in the winding magnetizes a small spot on the disk surface in the direction of the magnetic field. A magnetized spot of one polarity represents a binary 1, and one of the opposite polarity represents a binary 0.

When the magnetic surface passes a read head, the magnetized spots produce magnetic fields in the read head, which induce voltage pulses in the winding. The polarity of these pulses indicates whether the stored bit is a 1 or a 0.

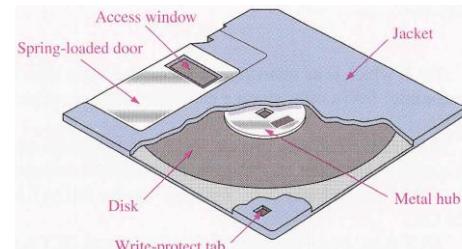
Hard Disk Format

Data is stored on the surface of a platter in sectors and tracks. The arrangement of tracks and sectors on a disk is known as the format. Tracks are concentric circles, and sectors are pie-shaped wedges on a track. A typical track is shown in yellow; a typical sector is shown in blue. A sector contains a fixed number of bytes -- for example, 256 or 512. Each track and sector have a physical address that is used by the operating system.



THE FLOPPY DISK

The floppy disk is an older technology and derives its name because it is made of a flexible polyester material with a magnetic coating on both sides. The early floppy disks were 5.25 inches in diameter and were packaged in a semi-flexible jacket. Current floppy disks or diskettes are 3.5 inches in diameter and are encased in a rigid plastic jacket. A spring-loaded shutter covers the access window and remains closed until the disk is inserted into a disk drive. A metal hub has one hole to center the disk and another for spinning it within the protective jacket.



Floppy disks are formatted into tracks and sectors similar to hard disks except for the number of tracks and sectors. The high-density 1.44 MB floppies have 80 tracks per side with 18 sectors.

OPTICAL MEMORIES

Optical memory is an electronic storage medium that uses a laser beam to store and retrieve the data.

CD-ROM

The basic Compact Disk-Read-Only Memory is a 120 mm diameter disk. The CD-ROM disk is formatted in a single spiral track and has a capacity of 680 MB. Data are prerecorded at the factory in the form of indentations called pits and the flat area surrounding the pits called lands.

A CD player reads data from the spiral track with a low-power infrared laser. Laser light reflected from a pit is 180° out-of-phase with the light reflected from the lands. As the disk rotates, a photodiode detects the reflected light. The result is a series of 1s and 0s corresponding to the configuration of pits and lands along the track.

CD-R

The CD-Recordable allows multiple write sessions to different areas of the disk. The CD-R disk has a spiral track like the CD-ROM. The CD-R uses a laser to burn microscopic spots into an organic dye surface. When heated beyond a critical temperature with a laser during read, the burned spots change color and reflect less light than the nonburned areas. Therefore, 1s and 0s are represented on a CD-R by burned and nonburned areas. Like the CD-ROM, the data cannot be erased once it is written.

CD-RW

The CD-Rewritable disk can be used to read and write data. The CD-RW commonly uses a crystalline compound with a special property. When it is heated to a certain temperature, it becomes crystalline when it cools; but if it is heated to a certain higher temperature, it melts and becomes amorphous when it cools. To write data, the focused laser beam heats the material to the melting temperature resulting in an amorphous state. The resulting amorphous areas reflect less light than the crystalline areas, allowing the read operation to detect 1s and 0s. The data can be erased or overwritten by heating the amorphous areas to a temperature above the crystallization temperature but lower than the melting temperature that causes the amorphous material to revert to a crystalline state.

DVD-ROM

Originally DVD was an abbreviation for Digital Video Disk but eventually came to represent Digital Versatile Disk. Like the CD-ROM, DVD-ROM data are prestored on the disk. However, the pit size is smaller than for the CD-ROM,

allowing more data to be stored on a track. The major difference between CD-ROM and DVD-ROM is that the CD is single-sided, while the DVD has data on both sides.

EXERCISE

SECTION-I (MCQ's)

1. To construct the PROM, technology is used;
 (a) MOS (b) Bipolar (c) Diode (d) Both a & b
2. Dynamic RAM has disadvantage;
 (a) Low density (b) Low cost (c) Refreshing data (d) None of these
3. CD-ROM is a type of memory;
 (a) Magnetic (b) Optical (c) Mechanical (d) Semiconductor
4. The process to combine memory cells with each other is called;
 (a) Addressing (b) Read (c) Write (d) Array
5. In Static RAM, the data is stored in;
 (a) Capacitor (b) Fuse (c) Flip Flop (d) Diode
6. 32 bits data word consists of;
 (a) 2 bytes (b) 4 bytes (c) 4 nibbles (d) 8 bytes
7. A memory which is programmed once by the user is called;
 (a) ROM (b) PROM (c) RAM (d) DRAM
8. A 1 Kilo Byte memory has memory locations;
 (a) 1000 (b) 1024 (c) 1048 (d) 1056
9. To retrieve data from memory is called;
 (a) Writing (b) Reading (c) Storing (d) Addressing
10. Hard Disk is a type of memory;
 (a) Magnetic (b) Optical (c) Mechanical (d) Semiconductor

ANSWER KEY

- | | | | | |
|------|------|------|------|-------|
| 1. d | 2. c | 3. b | 4. d | 5. c |
| 6. b | 7. b | 8. b | 9. b | 10. a |

SECTION-II (Short Questions)

1. Enlist types of memory.
2. What is cache memory?
3. Name magnetic storage devices.
4. Define volatile memory with example.
5. Define non-volatile memory with example.
6. Define ROM.

7. What is static RAM?
8. What is dynamic RAM?
9. How data is erased in EEPROM?
10. How data is erased in UV PROM?
11. What is meant by write operation in memory?
12. What is meant by read operation in memory?
13. Name optical storage devices.
14. What is meant by CD-RW?
15. What is meant by hard disk format?
16. Define programmable array logic?
17. Define programmable logic array?

SECTION-III (Long Questions)

1. Discuss construction, types and characteristics- of ROM.
2. Explain write and read operation in a static RAM cell with diagram.
3. Explain programmable ROM in detail with diagram.
4. Describe the construction and working of a hard disk.
5. Discuss types and characteristics of optical memories.

**BIPOLAR JUNCTION & FIELD
EFFECT TRANSISTORS****CHAPTER-9****Objectives**

At the end of this chapter, a student will be able to

- Draw and label physical structure and symbols for NPN and PNP transistors.
- Describe the operation of a transistor.
- Understand transistor parameters and ratings.
- Sketch the input and output static characteristics curves for common CB, CE and CC amplifiers.
- Discuss the operation of transistor as a voltage amplifier, switch and clipper.
- Sketch the construction of n-channel JFET & its symbol.
- Explain the principle of the n-channel JFET using illustrations.
- Sketch the construction of p-channel JFET & its symbol.
- Explain the principle of the p-channel JFET using illustrations.
- Sketch & label a family of drain characteristics of a n-channel JFET.
- Define the major data-sheet parameter of a JFET.
- Explain the principle of n-channel enhancement MOSFET.
- Sketch & label the family of drain characteristics of n-channel enhancement MOSFET.
- Explain the principle of n-channel depletion-enhancement MOSFET.
- Sketch symbols for p & n-channel JFET, n-channel enhancement MOSFET, p- and n- channel depletion- enhancement MOSFET.
- List three advantages of n-channel over p-channel MOSFET.
- List the applications of MOSFET.
- Sketch the cross section of complementary MOSFET (CMOS).
- List the applications of CMOS.
- Draw DC load line and locate bias point on the family of drain characteristic curves of JFET.
- Draw a self-bias arrangement p-channel & n-channel JFET.
- Set the Q-point for a self-biased JFET.
- Explain the Q-point stability of a JFET.

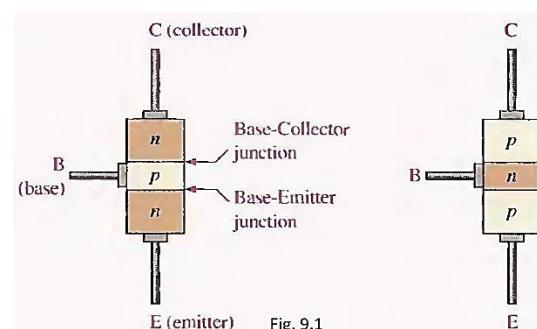
BIPOLAR JUNCTION TRANSISTOR

Bipolar Junction Transistor (BJT) is a semiconductor device constructed with three doped semiconductor regions separated by two p-n Junctions. Current is produced by both types of charge carriers, hence the name Bipolar.

BJT Construction

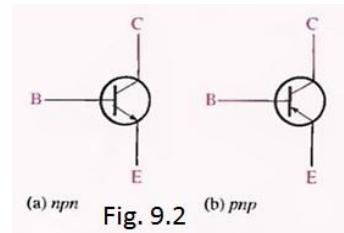
The BJT is constructed with three doped semiconductor regions separated by two PN junctions as shown in Fig. 9.1. The three regions are called emitter, base, and collector.

There are two types of transistor. One is NPN and other is PNP. The junction between base and emitter region is called the base-emitter junction and the junction between base and collector region is called the base-collector junction.



BJT Symbol

Fig. 9.2. shows the schematic symbols for the NPN and PNP bipolar junction transistors.



BJT Operation

Fig. 9.3. shows that base-emitter (BE) junction is forward-biased and the base-collector (BC) junction is reverse-biased.

The free electrons of heavily doped n-type emitter region easily diffuse through the forward-biased BE junction into the p-type base region. The base region is lightly doped and very thin. Thus, only a small percentage of all the electrons flowing through the BE junction can combine with the available holes in the base. These few recombined electrons flow out of the base lead as valence electrons, forming the small base electron current.

Rest of the electrons diffuse into the BC depletion region and are pulled through the reverse-biased BC junction.

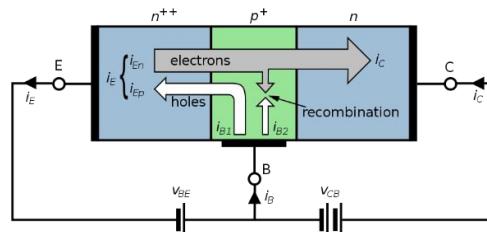


Fig. 9.3

The electrons now move through collector lead, into the positive terminal of the collector voltage source. This forms the collector electron current. The collector current is much larger than the base current.

Hence, emitter current divides into base and collector currents. So,

$$I_E = I_B + I_C$$

OPERATION MODES OF A BJT

There are four operation modes of a bipolar junction transistor.

- i- Saturation Mode
- ii- Active Mode
- iii- Cut off Mode
- iv- Reverse active mode

In the saturation mode, the collector-base and base-emitter junctions, both are forward-biased. Transistor acts as close switch in this mode.

In the active region the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased. Transistor acts as an amplifier in this mode.

In the cut off region the collector-base and base-emitter junctions, both are reverse-biased. Transistor acts as open switch in this mode.

In reverse active mode, the collector-base and base-emitter junctions, both are reverse-biased. This mode is used in some analog switching circuits.

TRANSISTOR PARAMETERS AND RATINGS

TRANSISTOR PARAMETERS

There are two important parameters, β_{DC} and α_{DC} are used to analyze a transistor circuit.

β_{DC}

The ratio of the dc collector current (I_C) to the dc base current (I_B) is the dc beta (β_{DC}), which is the dc current gain of a transistor. Typical values of β_{DC} range from less than 20 to 200 or higher.

$$\beta_{DC} = \frac{I_C}{I_B}$$

α_{DC}

The ratio of the dc collector current (I_C) to the dc emitter current (I_E) is the dc alpha (α_{DC}). Typically, values of α_{DC} range from 0.95 to 0.99.

$$\alpha_{DC} = \frac{I_C}{I_E}$$

TRANSISTOR RATINGS

A transistor has limitations on its operation which are stated as maximum ratings. Typically, maximum ratings are given for collector-to-base voltage,

collector-to-emitter voltage, emitter-to-base voltage, collector current, and power dissipation.

The product of V_{CE} and I_C must not exceed the maximum power dissipation.

TRANSISTOR AS VOLTAGE AMPLIFIER

Amplification is the process of linearly increasing the amplitude of an electrical signal. When a transistor is biased in the active (or linear) region, it works as an amplifier. In the Fig. 9.4., a BJT voltage amplifier is shown.

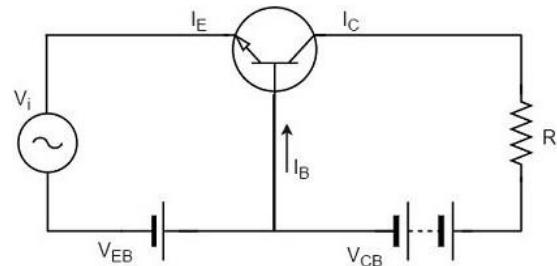


Fig. 9.4

WORKING

When a weak signal is applied to the input, a small change in signal voltage causes a change in emitter current (say a change of 0.1V in signal voltage causes a change of 1mA in the emitter current) because the input circuit has very low resistance. This change is almost the same in collector current because of the transmitter action.

In the collector circuit, a load resistor R_L of high value is connected. When collector current flows through such a high resistance, it produces a large voltage drop across it. Thus, a weak signal (0.1V) applied to the input circuit appears in the amplified form (10V) in the collector circuit.

INPUT OUTPUT STATIC CHARACTERISTICS OF CB AMPLIFIER

In common base configuration, emitter is the input terminal, collector is the output terminal and base is connected as a common terminal. NPN transistor in common base configuration is shown in Fig. 9.5.

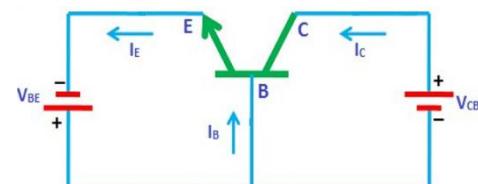


Fig. 9.5

INPUT CHARACTERISTICS

The input characteristics of CB configuration describe the relationship between input current (I_E) and the input voltage (V_{BE}) with constant output voltage (V_{CB}).

At different output voltage levels, the graph between I_E and V_{EB} parameters, shows the input characteristics of common base configuration.

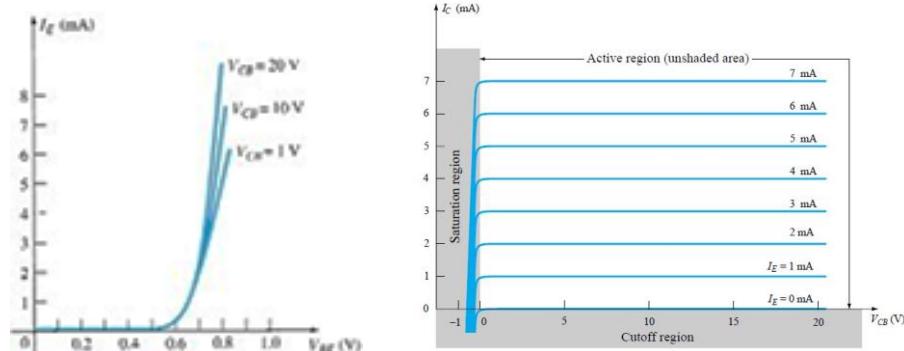


Fig. 9.6 (a) CB input characteristics

(b) CB output characteristics

OUTPUT CHARACTERISTICS

The output characteristics of CB configuration describe the relationship between output current (I_C) and the output voltage (V_{CB}) with constant input current (I_E).

Plot the graph between V_{CB} and I_C at different constant I_E values. The Fig. 9.6 shows input and output characteristics of common base configuration.

The output characteristics has three basic regions; the active, cut off, and saturation.

INPUT OUTPUT STATIC CHARACTERSTICS OF CE AMPLIFIER

In common emitter configuration, base is the input terminal, collector is the output terminal and emitter is connected as a common terminal. NPN transistor in common base configuration is shown in Fig. 9.7.

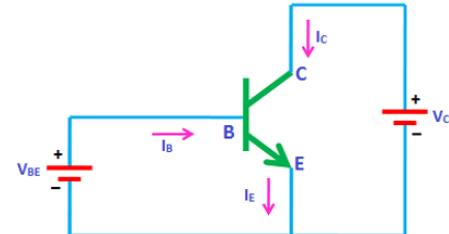


Fig. 9.7

INPUT CHARACTERISTICS

The input characteristics of CE configuration describe the relationship between input current (I_B) and the input voltage (V_{BE}) with constant output voltage (V_{CE}).

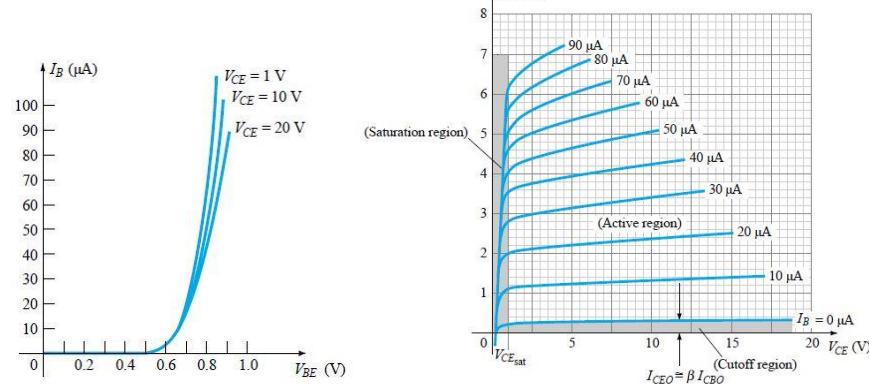


Fig. 9.8 (a) CE input characteristics (b) CE output characteristics

At different output voltage levels, the graph between I_B and V_{BE} parameters, shows the input characteristics of common emitter configuration.

OUTPUT CHARACTERISTICS

The output characteristics of CE configuration describe the relationship between output current (I_C) and the output voltage (V_{CE}) with constant input current (I_B).

Plot the graph between V_{CE} and I_C at different constant I_B values. The Fig. 9.8 shows the input and output characteristics of common emitter configuration.

The output characteristics has three basic regions; the active, cut off, and saturation.

INPUT OUTPUT STATIC CHARACTERSTICS OF CC AMPLIFIER

In common collector configuration, base is the input terminal, emitter is the output terminal and collector is connected as a common terminal. NPN transistor in common collector configuration is shown in Fig. 9.9.

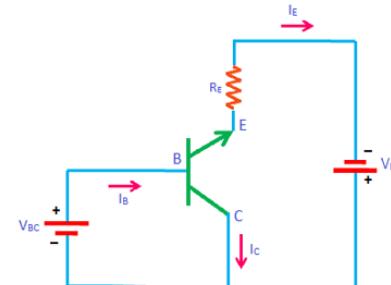


Fig. 9.9

The input characteristics of CC configuration describe the relationship between input current (I_B) and the input voltage (V_{BC}) with constant output voltage (V_{EC}).

At different output voltage levels, the graph between I_B and V_{BC} shows the input characteristics of common collector configuration.

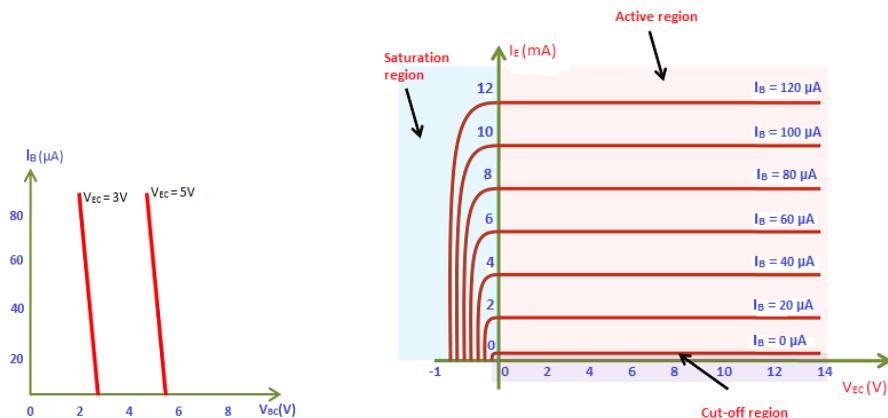


Fig. 9.8 (a) CC input characteristics

(b) CC output characteristics

OUTPUT CHARACTERISTICS

The output characteristics of CC configuration describe the relationship between output current (I_E) and the output voltage (V_{EC}) with constant input current (I_B).

Plot the graph between V_{EC} and I_E at different constant I_B values. The Fig. 9.8. shows the input and output characteristics of common collector configuration.

The output characteristics has three basic regions; the active, cut off, and saturation.

TRANSISTOR AS A SWITCH

When used as an electronic switch, a transistor is normally operated alternately in cutoff and saturation.

TRANSISTOR AS OPEN SWITCH

Fig. 9.9 (a) illustrates the basic operation of the transistor as an open switch. The transistor is in the cutoff region because the base-emitter junction is not forward biased. Neglecting leakage current, all of the currents are zero, and V_{CE} is equal to V_{CC} .

As we know that;

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_{CC}$$

In this condition, there is, ideally, an open between collector and emitter, as indicated by the switch equivalent.

TRANSISTOR AS CLOSE SWITCH

Fig. 9.9 (b) shows the basic operation of the transistor as a close switch. The transistor is in the saturation mode because both junctions are forward-biased. The base current is made large enough to cause the collector current to reach its saturation value. In this condition, there is, ideally, a short between collector and emitter, as indicated by the switch equivalent.

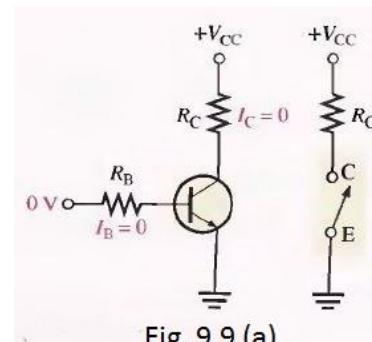


Fig. 9.9 (a)

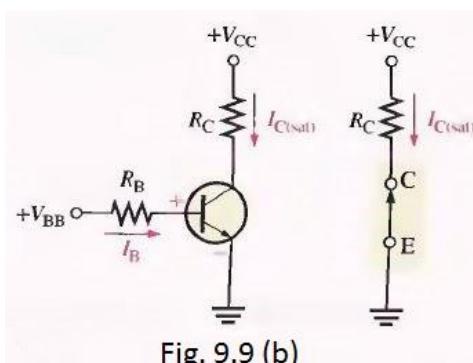
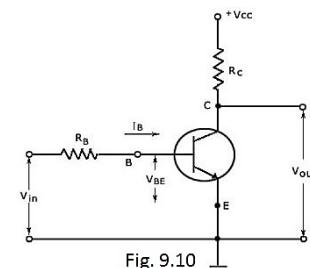


Fig. 9.9 (b)

TRANSISTOR CLIPPER

When any input signal passes through the transistor, from cut-off region to the active region or from the active region to the saturation region, a portion of the input signal will be clipped off. In the Fig. 9.10, a circuit of transistor clipper is shown.



TRANSISTOR CLIPPER WORKING

- When the input voltage is from 0V to 0.7V, the transistor will be working in the cut-off region. At this moment, output voltage is at V_{CC} level.
- When the voltage reaches 0.7 V, the transistor starts conducting and will switch to the active region. The output voltage starts to decrease.
- When the voltage is between 3V to 5V and back to 3V, the transistor switches to the saturation region. In this period, output voltage is at $V_{CE(sat)}$ level approximately equal to 0V.
- Again, when input voltage is between 3V to 0.7V, transistor works in active region and output voltage starts to increase.
- When the input voltage is below 0.7V including negative cycle, transistors goes into cut off region.

The input and output waveforms are shown in the Fig. 9.11.

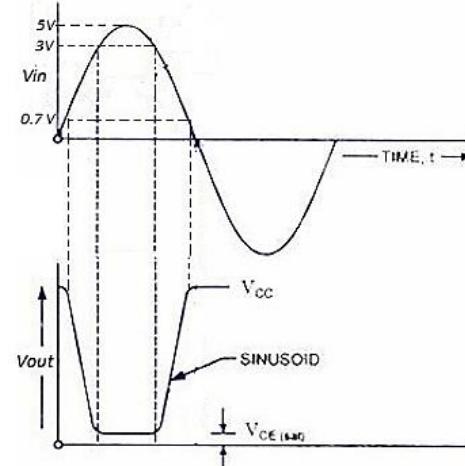


Fig. 9.11

FIELD EFFECT TRANSISTOR

Field Effect Transistors are unipolar devices because they operate only with one type of charge carrier. The voltage between two of the terminals (gate and source) controls the current through the device. A major feature of FETs is their very high input resistance.

N CHANNEL JFET

CONSTRUCTION AND SYMBOL

Fig. 9.12(a) shows the basic structure of an n-channel JFET. The drain is at the upper end, and the source is at the lower end. Two p-type regions are

diffused in the N-type material to form a channel, and both p-type regions are connected to the gate lead. For simplicity, the gate lead is shown connected to only one of the p regions.

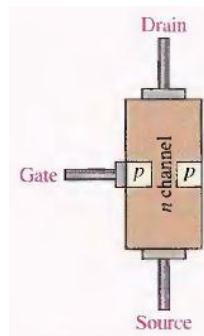


Fig. 9.12 (a) Construction

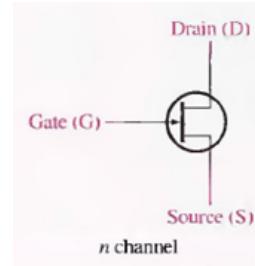


Fig. 9.12 (b) Symbol

The schematic symbol for n-channel JFETs is shown in Fig. 9.12(b). The arrow on the gate points "in" for n-channel JFET.

OPERATION OF N CHANNEL JFET

In n-channel JFET, the majority charge carriers are electrons. In fig. 9.13, a biased n-channel JFET is shown.

Case I: Consider V_{DS} to be positive while V_{GS} is 0. At this state, the current flows from the source to the drain as the electrons within the channel move towards the drain from the source. The value of this current is restricted only by the channel resistance. However, when V_{DS} reaches at V_p , the current I_D saturates at a particular level I_{DSS} .

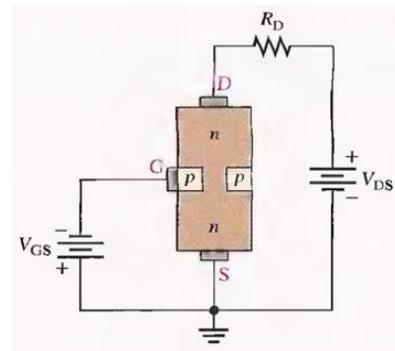


Fig. 9.13

Case II: When a reverse voltage V_{GS} is applied between gate and source terminals, the width of depletion layer is increased. Consequently, the current from source to drain is decreased. Drain current decreases at a faster rate as the V_{GS} becomes more and more negative. The current ceases to flow as the value of V_{GS} becomes equal to V_p , turning the device into OFF state.

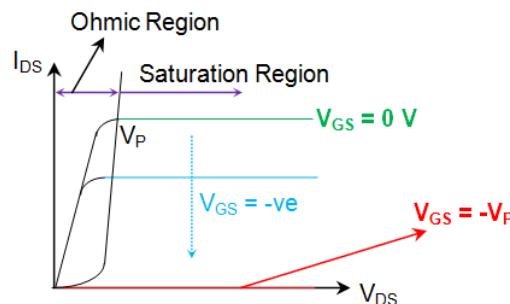


Fig. 9.14

DRAIN CHARACTERISTICS CURVES OF N-CHANNEL JFET

Let's connect a bias voltage, V_{GG} , from gate to source as shown in fig. 9.15(a). As V_{GS} is set to increasingly more negative values by adjusting V_{GG} , a family of drain characteristic curves is produced as shown in fig. 9.15(b). I_D decreases as the magnitude of V_{GS} is increased to larger negative values because of the narrowing of the channel. Therefore, the amount of drain current is controlled by V_{GS} .

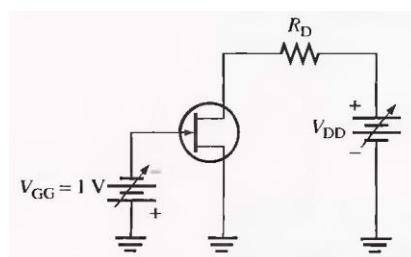
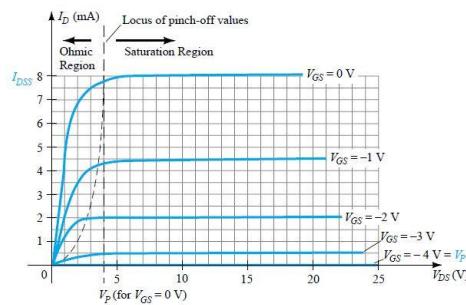


Fig. 9.15 (a) Biased Circuit



(b) Family of drain characteristics curves

JFET PARAMETERS

i- Pinch Off Voltage

For $V_{GS} = 0V$, the value of V_{DS} at which I_D becomes essentially constant is the pinch-off voltage, V_p .

ii- Cut Off Voltage

The value of V_{GS} that makes I_D approximately zero is called cut-off voltage, $V_{GS(off)}$. $V_{GS(off)}$ and V_p are always equal in magnitude but opposite in sign.

iii- Drain to Source Current with Gate Shorted.

I_{DSS} is the maximum drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for $V_{GS} = 0V$.

P-CHANNEL JFET

CONSTRUCTION AND SYMBOL

Fig. 9.16(a) shows the basic structure of an p-channel JFET. The drain is at the upper end, and the source is at the lower end. Two n-type regions are diffused in the P-type material to form a channel, and both n-type regions are connected to the gate lead. For simplicity, the gate lead is shown connected to only one of the n regions. The schematic symbol for p-channel JFETs is shown in Fig(b). The arrow on the gate points "out" for p-channel JFET.

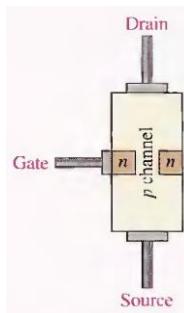
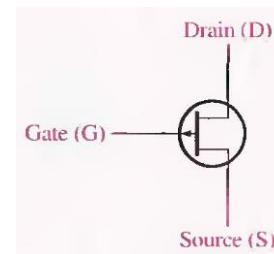


Fig. 9.16



(a) Construction

(b) Symbol

OPERATION OF P CHANNEL JFET

In p-channel JFET, the majority charge carriers will be the holes. In fig. 9.17, a biased p-channel JFET is shown.

Case I: Now consider V_{DS} to be negative while V_{GS} is 0. At this state, the current flows from the source to the drain as the holes within the channel move towards the drain from the source. The value of this current is restricted only by the channel-resistance. However, when V_{DS} reaches at V_P , the current I_D saturates at a particular level I_{DSS} .

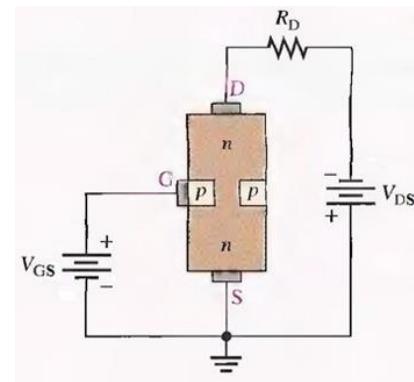


Fig. 9.17

Case II: When a reverse voltage V_{GS} is applied between gate and source terminals, the width of depletion layer is increased. Consequently, the current from source to drain is decreased. Drain current decreases at a faster rate as the V_{GS} becomes more and more positive. The current ceases to flow as the value of V_{GS} becomes equal to V_P , turning the device into OFF state.

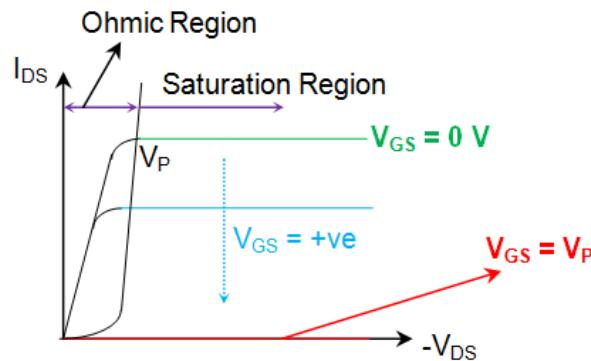


Fig. 9.18

DRAIN CHARACTERISTICS CURVES OF P-CHANNEL JFET

The drain characteristics curves of p-channel are the same as the n-channel device but with a reversal of current directions and polarities for the voltages

V_{GS} and V_{DS} . I_D decreases as the magnitude of V_{GS} is increased to larger positive values because of the narrowing of the channel as shown in fig. 9.19(b). Therefore, the amount of drain current is controlled by V_{GS} .

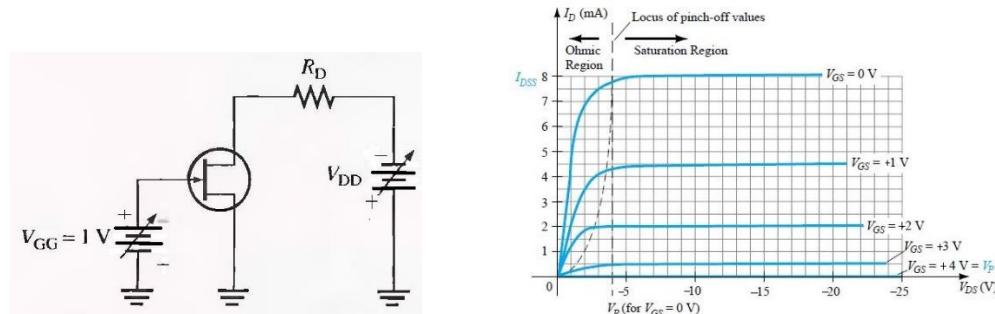


Fig. 9.19 (a) Biased Circuit (b) Family of drain characteristics curves

N-CHANNEL ENHANCEMENT MOSFET (E-MOSFET)

CONSTRUCTION AND SYMBOLS

The E-MOSFET can be operated only in enhancement mode. Fig. 9.20(a) shows the basic structure of an n-channel E-MOSFET. A thin layer of metal oxide, usually silicon dioxide (SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. The E-MOSFET has no channel between source and drain. The substrate is connected to the source internally so that a MOSFET has three terminals such as Source (S), Gate (G) and Drain(D).

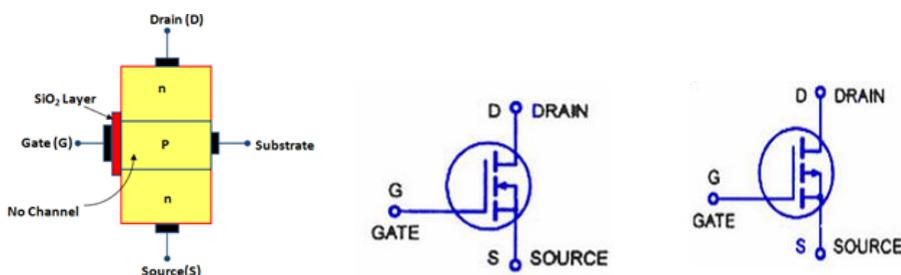


Fig. 9.20 (a) Construction

(b) Symbols

E-MOSFET OPERATION

Fig. 9.21 shows the circuit of n-channel E-MOSFET. The circuit action is as under:

- (i) **When $V_{GS} = 0\text{ V}$,** as shown in fig. (a), there is no channel connecting source and drain. The p-substrate has only a few thermally produced free electrons so that drain current is almost zero. For this reason, E-MOSFET is normally OFF when $V_{GS} = 0\text{ V}$.

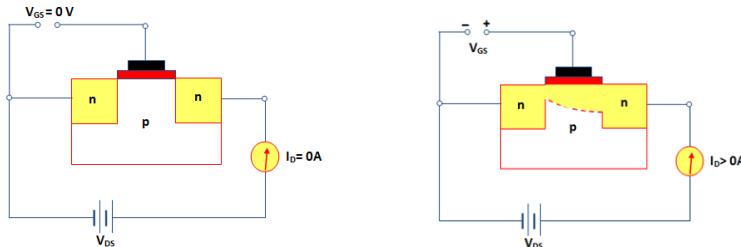


Fig. 9.21 (a)

(b)

(ii) When V_{GS} is positive, i.e. gate is made positive as shown in fig. (b), it attracts free electrons into the p region. The free electrons combine with the holes next to the SiO_2 layer.

If V_{GS} is positive enough, all the holes touching the SiO_2 layer are filled and free electrons begin to flow from the source to drain. The effect is same as creating a thin layer of n-type material i.e. inducing a thin n-layer adjacent to the SiO_2 layer. Thus, the E-MOSFET is turned ON and drain current I_D starts flowing from the source to the drain. The minimum value of V_{GS} that turns the E-MOSFET ON is called threshold voltage [$V_{GS(th)}$].

(iii) When V_{GS} is less than $V_{GS(th)}$, there is no induced channel and the drain current I_D is zero. When V_{GS} is equal to $V_{GS(th)}$, the E-MOSFET is turned ON and the induced channel conducts drain current from the source to the drain. Beyond $V_{GS(th)}$, if the value of V_{GS} is increased, the newly formed channel becomes wider, causing I_D to increase. If the value of V_{GS} decreases not less than $V_{GS(th)}$, the channel becomes narrower and I_D will decrease.

DRAIN CHARACTERISTICS CURVES OF E-MOSFET

The V-I characteristics of the E-MOSFET are given in fig. 9.22. This characteristic mainly gives the relationship between drain- source voltage (V_{DS}) and drain current (I_D). The small voltage at the gate controls the current flow through the channel.

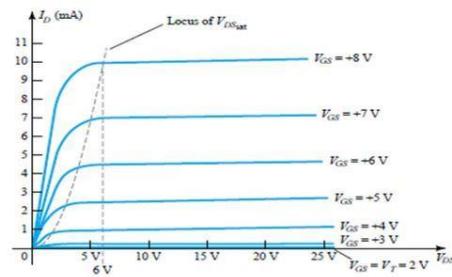


Fig. 9.22

N-CHANNEL DEPLETION ENHANCEMENT MOSFET (DE-MOSFET)

CONSTRUCTION AND SYMBOLS

The DE-MOSFET can be operated in both depletion mode and the enhancement mode. Fig. 9.23(a) shows the basic structure of an n-channel DE-MOSFET. A thin layer of metal oxide, usually silicon dioxide (SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel.

The substrate is connected to the source internally so that a MOSFET has three terminals such as Source (S), Gate (G) and Drain(D).

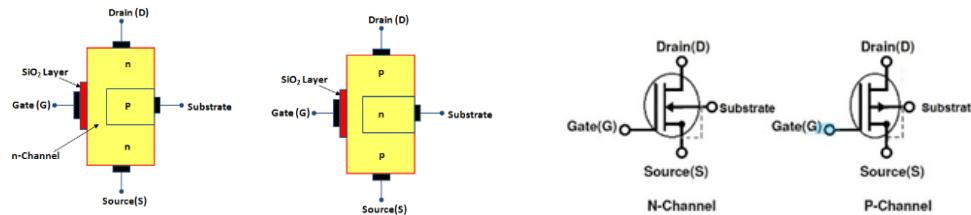


Fig. 9.23 (a) Construction

(b) Symbols

DEPLETION MODE OPERATION

Fig. 9.24(a) shows depletion mode operation of n-channel DE-MOSFET.

Since gate is negative, it means electrons are on the gate. These electrons repel the free electrons in the n-channel, leaving a layer of positive ions in a part of the channel. Therefore, lesser number of free electrons are available for current conduction through the n-channel.

The greater the negative voltage on the gate, the lesser is the current from source to drain. Thus, by changing the negative voltage on the gate, we can vary the current from source to drain.

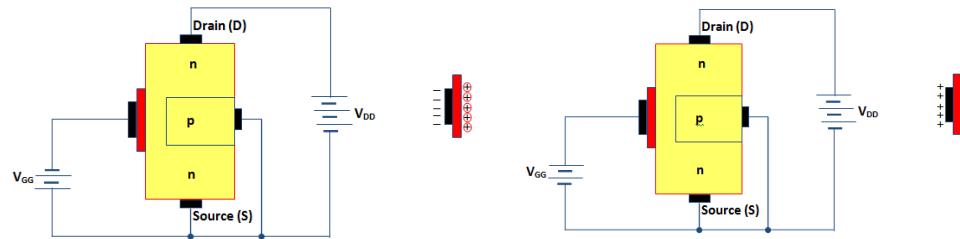
As the action with negative gate depends upon depleting the channel of free electrons, the negative-gate operation is called depletion mode.

ENHANCEMENT MODE OPERATION

Fig. 9.24(b) shows enhancement mode operation of n-channel DE-MOSFET. Since the gate is positive, it induces negative charges in the n-channel. The total number of free electrons in the channel is increased.

The greater the positive voltage on the gate, greater the conduction from source to drain. Thus, by changing the positive voltage on the gate, we can change the conductivity of the channel.

Because the action with a positive gate depends upon enhancing the conductivity of the channel, the positive gate operation is called enhancement mode.



(a) Depletion Mode

(b) Enhancement Mode

DRAIN CHARACTERISTICS CURVES OF DE-MOSFET

The V-I characteristics of the depletion mode MOSFET transistor are shown in fig. 9.25. This characteristic mainly gives the relationship between drain-source voltage (V_{DS}) and drain current (I_D). The small voltage at the gate controls the current flow through the channel.

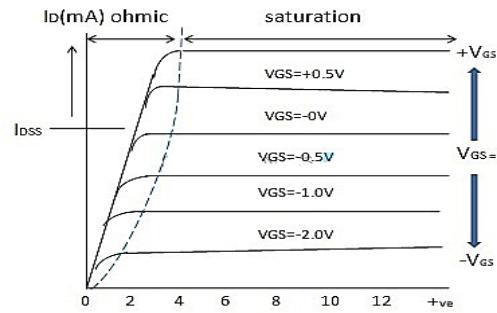


Fig. 9.25

COMPARISON B/W NMOS & PMOS

- i. The hole mobility is nearly 2.5 times lower than the electron mobility. Thus a PMOS occupies a larger area than the NMOS having the same I_D rating.
- ii. The n-channel devices will be smaller in size. In other words the packing density of N-channel devices is more.
- iii. NMOS are fast switching devices than PMOS.
- iv. The N channel MOSFETs are TTL compatible. As the applied gate voltage and drain supply are positive for an n-channel enhancement MOSFET.
- v. The drain resistance of PMOS is 3 times higher than that for an identical NMOS.

APPLICATIONS OF MOSFET

Following are the applications of MOSFET

- These are used as switch.
- MOSFET's are used in DC-DC power supplies.
- These are also used as an amplifier.
- It is used in linear voltage regulator.
- MOSFET is used in chopper circuit.

CMOS (COMPLEMENTARY METAL OXIDE SEMICONDUCTOR)

In CMOS technology, both p-channel and an n-channel MOSFET on the same substrate are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.

THE CROSS SECTION OF CMOS

In the fig. 9.26, the cross section of complementary MOSFET is shown.

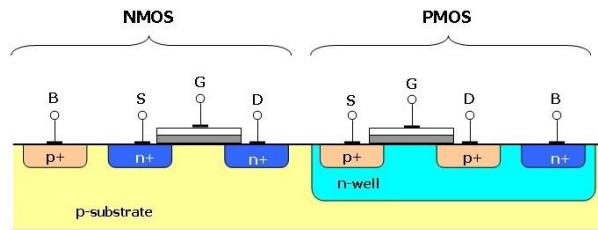


Fig. 9.26

WORKING OF CMOS

In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (V_{SS} or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named V_{DD}).

Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa.

APPLICATIONS OF CMOS

CMOS technology is used for constructing integrated circuit (IC) chips, including microprocessors, microcontrollers, memory chips (including BIOS), and other digital logic circuits. CMOS technology is also used for analog circuits such as image sensors, data converters, RF circuits, and highly integrated transceivers for many types of communication.

ADVANTAGES OF CMOS

CMOS offers relatively high speed, low power dissipation, high noise margins in both states, and will operate over a wide range of source and input voltages (provided the source voltage is fixed).

JFET BIASING

The purpose of biasing is to select the proper dc gate-to-source voltage to establish a desired value of drain current and, thus, a proper Q-point. There are two types of bias circuits. self-bias and voltage-divider bias.

Self-Biasing of a JFET

A JFET must be operated such that the gate-source junction is always reverse-biased. This condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for a p-channel JFET. This can be achieved using the self-bias arrangements shown in Fig. 9.27. There is no voltage drop across gate resistor, and therefore the gate remains at 0V.

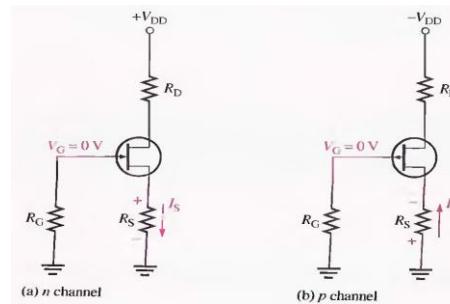


Fig. 9.27

Self-Bias Calculation

For the n-channel JFET in Fig. 9.27, I_S produces a voltage drop across R_S .

Since $I_S = I_D$ and $V_G = 0$, then $V_S = I_D R_S$. The gate-to-source voltage is

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

For the p-channel; $V_{GS} = V_G - V_S = 0 + I_D R_S = +I_D R_S$

The drain voltage is determined as follows:

$$V_D = V_{DD} - I_D R_D$$

The drain to source voltage is

$$V_{DS} = V_D - V_S = V_{DD} - I_D (R_D + R_S)$$

Setting the Q-Point of a Self- Biased JFET

The basic approach to establishing a JFET bias point is to determine I_D for a desired value of V_{GS} or vice versa. Then calculate the required value of R_S using the following relationship.

$$R_S = \left| \frac{V_{GS}}{I_D} \right|$$

For a desired value of V_{GS} , I_D can be determined in either of two ways: from the transfer characteristic curve for the particular JFET or, more practically, from following equation using I_{DSS} and $V_{GS(\text{off})}$ from the JFET data sheet.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2$$

Q-POINT STABILITY

Suppose, a 2N5459 JFET is replaced in a given bias circuit with another 2N5459, the transfer characteristic curve can vary greatly, as illustrated in fig. In this case, the maximum I_{DSS} is 16 mA and the minimum I_{DSS} is 4 mA. Likewise, the maximum V_{GS} (off) is -8V and the minimum V_{GS} (off) is -2V.

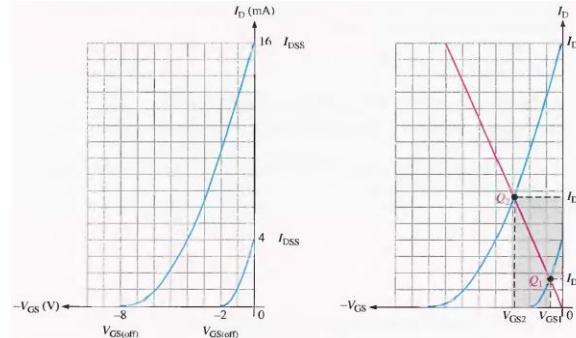


Fig. 9.28

If a self-bias dc load line is drawn as illustrated in Fig. 9.25, the same circuit using a 2N5459 can have a Q-point anywhere along the line from Q_1 , the minimum bias point, to Q_2 , the maximum bias point. Accordingly, the drain current can be any value between I_{D1} and I_{D2} , as shown by the shaded area. This means that the dc voltage at the drain can have a range of values depending on I_D . Also, the gate-to-source voltage can be any value between V_{GS1} and V_{GS2} as indicated.

EXERCISE

SECTION-I (MCQ's)

1. Lightly doped terminal of BJT is;
 - (a) Gate
 - (b) Emitter
 - (c) Collector
 - (d) Base
2. BJT works as a switch in mode;
 - (a) Cut Off
 - (b) Saturation
 - (c) Active
 - (d) Both a & b
3. JFET is a device which is controlled by;
 - (a) Voltage
 - (b) Current
 - (c) Frequency
 - (d) Power
4. A JFET gate to source diode is;
 - (a) Forward
 - (b) Reverse
 - (c) Both a & b
 - (d) None of these
5. The output is inverse of the input in amplifier;
 - (a) Common base
 - (b) Common collector
 - (c) Common emitter
 - (d) All of these
6. The region of transistor is moderately doped;

- (a) Gate (b) Emitter (c) Collector (d) Base
7. Impedance of common base circuit is;
 (a) Very high (b) High (c) Very low (d) Low
8. N Channel EMOSFET $V_{GS(On)}$ are;
 (a) $> V_{GS(Th)}$ (b) $< V_{GS(Th)}$ (c) $= V_{GS(off)}$ (d) $> V_{DS(On)}$
9. According to biasing of junction transistor have mode of operations;
 (a) Two (b) Three (c) Four (d) Five
10. Normally a common base amplifier is used for amplification of;
 (a) Power (b) Current (c) Voltage (d) All of these
11. The minimum value of V_{GS} that turns the E-MOSFET ON is called
 (a) $V_{GS(off)}$ (b) $V_{GS(On)}$ (c) $V_{GS(Sat)}$ (d) $V_{GS(Th)}$
12. The value of V_{GS} that makes I_D approximately zero is called
 (a) $V_{GS(off)}$ (b) $V_{GS(On)}$ (c) $V_{GS(Sat)}$ (d) $V_{GS(Th)}$
13. BJT works as an amplifier in mode;
 (a) Cut Off (b) Saturation (c) Active (d) Reverse

ANSWER KEY

- | | | | | | | | | | |
|-----|---|-----|---|-----|---|----|---|-----|---|
| 1. | d | 2. | d | 3. | a | 4. | b | 5. | c |
| 6. | c | 7. | b | 8. | a | 9. | c | 10. | c |
| 11. | d | 12. | a | 13. | c | | | | |

SECTION-II (Short Questions)

1. Why BJT is called bipolar?
2. Draw the symbol of PNP and NPN transistor.
3. Write the characteristics of common base amplifier.
4. Enlist types of field effect transistor.
5. Define α_{DC} .
6. Define β_{DC} .
7. Define break down voltage of a transistor.
8. Name three terminals of a JFET.
9. Define pinch off voltage.
10. Draw the construction of N-channel JFET.
11. Define transistor clipper.
12. Write the names of BJT modes of operation.
13. Define I_{DSS} drain source saturation current.
14. Write the applications of CMOS.
15. Draw DC biasing of JFET.
16. What stands for MOSFET.
17. Enlist the names of transistor amplifier according to configuration.

18. What is saturation mode of transistor?
19. What is cut off mode of transistor?
20. Why FET is called unipolar?

SECTION-III (Long Questions)

1. Draw BJT construction and explain BJT operation modes.
2. Explain briefly transistor as an amplifier.
3. Discuss the operation of transistor as a switch with diagram.
4. Explain construction, working and biasing of N-channel JFET.
5. Write a note on JFET data sheet parameters.
6. Explain the construction of DE-MOSFET. Also draw its drain curves.

SPECIAL DEVICES**CHAPTER-10****Objectives**

At the end of this chapter, a student will be able to

- Understand the characteristics and applications of Zener diode.
- Understand the characteristics and applications of Optical diodes.
- Understand the characteristics and application of tunnel diode.
- Understand thyristor family with their applications.
- Understand Uni-junction Transistor characteristics and application.
- Understand properties of Photo-sensitive BJT & LASCR.
- Understand optocouplers and their types.

ZENER DIODE

A Zener diode is a silicon semiconductor device that permits current to flow in either a forward or reverse direction. The diode consists of a special, heavily doped p-n junction, designed to conduct in the reverse direction when a certain specified voltage is reached.

ZENER DIODE CONSTRUCTION

The P type and N type silicon used is doped more heavily than a standard PN diode. This results in a relatively thin junction layer, and consequently a reverse breakdown voltage that can be much lower than in a conventional diode. The actual breakdown voltage is controlled during manufacture by adjusting the amount of doping used. Breakdown voltages can be selected between about 3V and 300V. The construction and symbol of zener diode is shown in fig. 10.1.

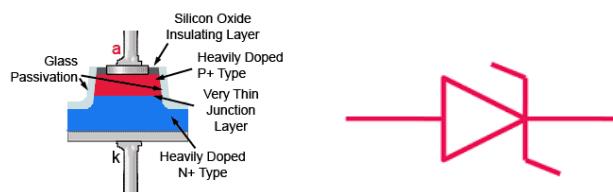


Fig. 10.1 (a) Zener diode construction (b) Zener diode symbol

ZENER DIODE OPERATION

The Zener diode operates just like the normal diode when in the forward-bias mode, and has a turn-on voltage of between 0.3 and 0.7 V. However, when connected in the reverse mode, which is usual in most of its applications, a

small leakage current may flow. As the reverse voltage increases to the predetermined breakdown voltage (V_z), a current starts flowing through the diode. The current increases to a maximum, which is determined by the series resistor, after which it stabilizes and remains constant over a wide range of applied voltage.

The voltage point at which the voltage across the zener diode becomes stable is called the “zener voltage”, (V_z) and for zener diodes this voltage can range from less than one volt to a few hundred volts. This zener breakdown voltage on the I-V curve is almost a vertical straight line.

V-I CHARACTERISTICS CURVE

V-I characteristics curve of Zener diode is shown in fig. 10.2. We can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode.

This voltage remains almost constant even with large changes in current providing the zener diodes current remains between the breakdown current $I_{Z(\min)}$ and its maximum current rating $I_{Z(\max)}$.

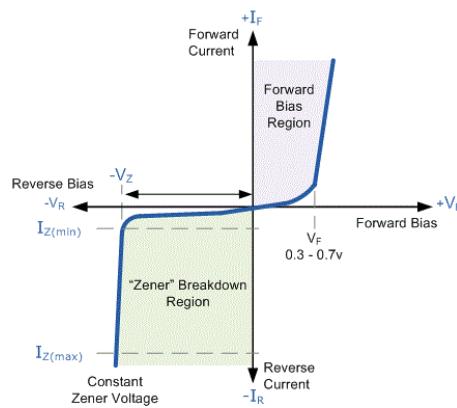


Fig. 10.2

ZENER DIODE APPLICATIONS

Zener diodes are used for following applications.

- ❖ Voltage regulation
- ❖ Surge suppressor
- ❖ Over voltage protection
- ❖ Clipping circuits
- ❖ Switching circuits

ZENER DIODE AS VOLTAGE REGULATOR

The purpose of a voltage regulator is to maintain a constant voltage across a load regardless of variations in the applied input voltage and variations in the load current.

A typical Zener diode shunt regulator is shown in Fig. 10.3. The resistor is selected so that when the input voltage is at $V_{IN(min)}$ and the load current is at $I_{L(max)}$ that the current through the Zener diode is at least $I_Z(\min)$. Then for all other combinations of input voltage and load current the Zener diode conducts the excess current thus maintaining a constant voltage across the load. The Zener conducts the least current when the load current is the highest and it conducts the most current when the load current is the lowest.

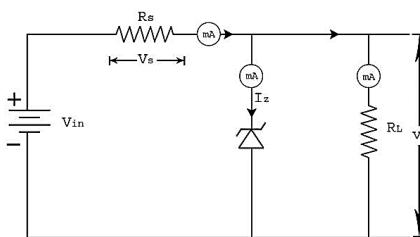


Fig. 10.3

If there is no load resistance, shunt regulators can be used to dissipate total power through the series resistance and the Zener diode.

A zener diode of break down voltage V_Z is reverse connected to an input voltage source V_i across a load resistance R_L and a series resistor R_S . The voltage across the zener will remain steady at its break down voltage V_Z for all the values of zener current I_Z as long as the current remains in the break down region. Hence a regulated DC output voltage $V_O = V_Z$ is obtained across R_L , whenever the input voltage remains within a minimum and maximum voltage.

OPTICAL DEVICES

Optical devices are such devices that focuses on light emitting or light detecting. Light-emitting devices use voltage and current to produce light. Light-detecting devices, such as phototransistors, are designed to convert received light energy into electric current or voltage. Following are opto-electronic devices

- ❖ Light Emitting Diode
- ❖ Photo Diode
- ❖ LASER Diode
- ❖ Photo Transistor
- ❖ Solar Cell
- ❖ Light Dependent Resistor
- ❖ Light Activated SCR

- ❖ Fiber Optics
- ❖ Opto Coupler

LIGHT EMITTING DIODE

Light-emitting diode is a P-N semiconductor diode in which the recombination of electrons and holes yields a photon. When the anode becomes more positive than its cathode (typically by a voltage ranging from 0.6 to 2.2V), the electrons recombine with the holes within the device and release energy in the form of photons. This effect is called as electroluminescence. It is the conversion of electrical energy into light. The colour of the light is decided by the energy band gap of the material.

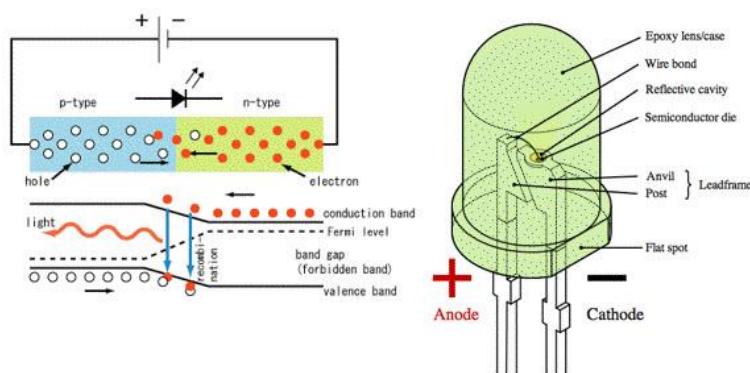


Fig. 10.4 Operation of a LED

COLOUR OF LED

The colour of a light emitting diode is determined by the wavelength of the light emitted, which is determined by the actual semiconductor compound used in forming the PN junction during manufacture. The material used in LED's are given in table.

Typical LED Characteristics			
Semiconductor Material	Wavelength	Colour	$V_F @ 20mA$
GaAs	850-940nm	Infra-Red	1.2v
GaAsP	630-660nm	Red	1.8v
GaAsP	605-620nm	Amber	2.0v
GaAsP:N	585-595nm	Yellow	2.2v
AlGaP	550-570nm	Green	3.5v
SIC	430-505nm	Blue	3.6v
GaN	450nm	White	4.0v

APPLICATIONS OF LED'S

- LED is used as a bulb in the homes and industries
- LED's are used in the motorcycles and cars

- These are used in the mobile phones to display the message
- At the traffic light signals LED's are used
- LED's are used in camera flashes

LIQUID CRYSTAL DISPLAY

LCD is a form of visual display used in electronic devices, in which a layer of a liquid crystal is sandwiched between two transparent electrodes as shown in fig. 10.5. The LCD works on the modulating property of light. The light modulation is the technique of sending and receiving the signal through the light. The liquid crystal consumes a small amount of energy because they are the reflector and the transmitter of light.

CONSTRUCTION OF LCD

The liquid crystals are the organic compound which is in liquid form. The layer of liquid crystals is deposited on the inner surface of glass electrodes for the scattering of light. The liquid crystal cell is of two types; they are Transmittive Type and the Reflective Type.

Transmittive Type – In transmittive cell both the glass sheets are transparent so that the light is scattered in the forward direction when the cell becomes active.

Reflective Type – The reflective type cell consists the reflecting surface of the glass sheet on one end. The light incident on the front surface of the cell is scattered by the activated cell.

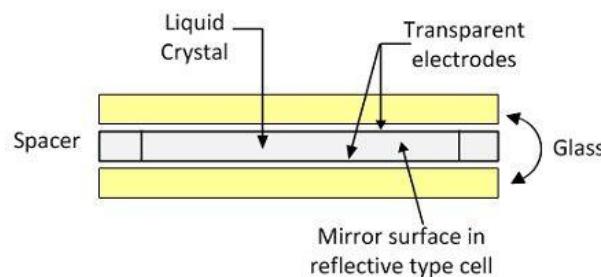


Fig. 10.5

WORKING PRINCIPLE OF LCD

The working principle of the LCD is of two types. They are the dynamic scattering type and the field effects type.

DYNAMIC SCATTERING

When the potential carrier flows through the light, the molecular alignment of the liquid crystal disrupts, and they produce disturbances. The liquid becomes transparent when they are not active. But when they are active their molecules turbulence causes scattered of light in all directions, and

their cell appears bright. This type of scattering is known as the dynamic scattering. The construction of the dynamic scattering of the liquid crystal cell is shown in the fig. 10.6.

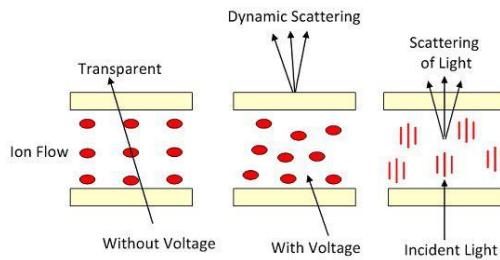


Fig. 10.6

Field Effect Type

The field effect type LCD uses a transparent liquid that causes the polarization. The light after passing through the material passing through the optical filters and appears bright. When the cell has energised no twisting of light occurs, and the cell appears dull.

COMPARISION BETWEEN LED AND LCD

- The resolution of the LED is much better than that of LCD.
- The display area of the LED is less as compared to the LCD.
- The cost of the LED is more as compared to LCD.
- The switching time of the LED is less as compared to LCD.
- The power consumption of LCD is low than that of LED.

APPLICATIONS

LCDs are commonly used for portable electronic games, in laptop computer screen, TVs, and in cell phones.

PHOTO DIODE

A photodiode is a PN-junction diode that consumes light energy to produce electric current. It is also called as photo-detector, a light detector, and photo-sensor. These diodes are particularly designed to work in reverse bias condition.

CONSTRUCTION OF PHOTO DIODE

A photodiode is constructed using a very thin n-type semiconductor together with a thicker p-type semiconductor. The photodiode has a small transparent window that allows light to strike the PN junction.

OPERATION OF PHOTO DIODE

When the photodiode is not exposed to radiation, a very small reverse current flows through the device that is termed as dark current. This current is totally the result of the flow of minority carriers.

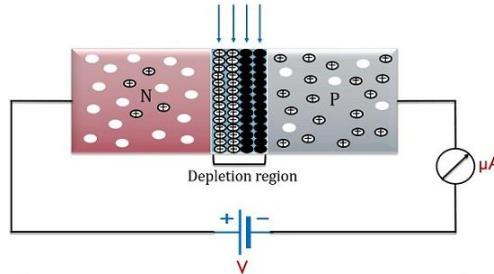


Fig. 10.7

As the light of sufficient energy falls on the surface of the junction, then the temperature of the junction gets increased. This causes the electron and hole to get separated from each other. The electrons from n side gets attracted towards the positive potential of the battery. Similarly, holes present in the p side get attracted to the negative potential of the battery. This movement then generates high reverse current through the device.

With the rise in the light intensity, more charge carriers are generated and flow through the device. So, we can say the intensity of light energy is directly proportional to the current through the device.

CHARACTERISTIC CURVE OF A PHOTODIODE

The fig. 10.8. shows the VI characteristic curve of a photodiode. The first curve represents the dark current that generates due to minority carriers in the absence of light.

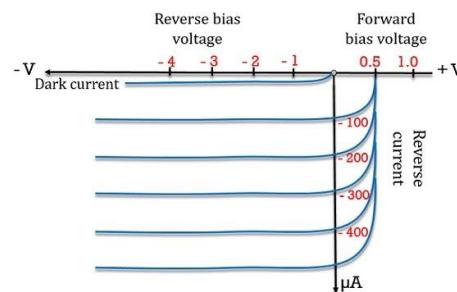


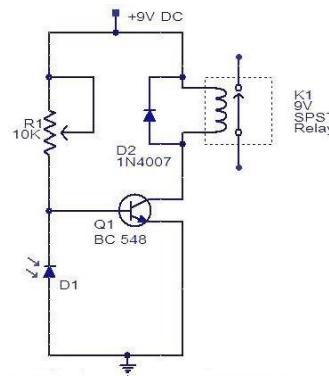
Fig. 10.8

APPLICATIONS OF PHOTO DIODE

Photodiodes are used in many types of circuits and different applications such as cameras, medical instruments, safety equipments, smoke detectors, compact disc players, TV and remote controls in VCRs, street lights, industries, communication devices and industrial equipments.

PHOTO ELECTRIC RELAY

A photo relay or light activated relay is a circuit which opens and closes the relay contacts according to the light. When light falls on diode, the current due to the minority carriers increase and the diode offers a low resistance. As a result, the voltage across the diode will not be sufficient to make the transistor Q_1 forward biased and the relay will OFF. When there is darkness the photo diode resistance increases and the voltage across it will become enough to forward bias the transistor Q_1 making the relay ON. The diode D_2 is used as a freewheeling diode to protect the transistor from transients produced to the switching of relay.



TUNNEL DIODE

The tunnel diode is a highly conductive, heavily doped PN-junction diode in which the current induces because of the tunneling. The tunneling is the phenomenon of conduction in the semiconductor material in which the charge carrier punches the barrier instead of climbing through it.

TUNNEL DIODE SYMBOL AND CONSTRUCTION

The tunnel diode exhibits a special characteristic known as negative resistance. This feature makes it useful in oscillator and microwave amplifier applications. The tunnel diode symbol is shown in figure.



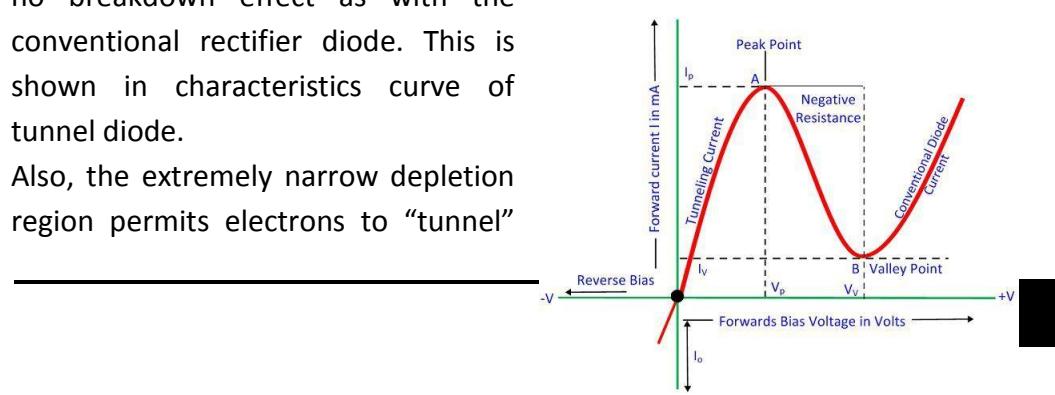
Fig. 10.9

Tunnel diodes are constructed with germanium or gallium arsenide by doping the p and n regions much more heavily than in a conventional rectifier diode. This heavy doping results in an extremely narrow depletion region.

TUNNEL DIODE CHARACTERISTIC CURVE

The heavy doping allows conduction for all reverse voltages so that there is no breakdown effect as with the conventional rectifier diode. This is shown in characteristics curve of tunnel diode.

Also, the extremely narrow depletion region permits electrons to "tunnel"



through the PN junction at very low forward-bias voltages, and the diode acts as a conductor. This is shown in fig. between origin and point A. At point A, the forward voltage begins to develop a barrier, and the current begins to decrease as the forward voltage continues to increase. This is the negative-resistance region. At point B, the diode begins to act as a conventional forward biased diode.

TUNNEL DIODE OSCILLATOR

The tunnel diode helps in generating a very high frequency signal of nearly 10GHz. A practical tunnel diode circuit may consist of a switch, a resistor R and a supply source V, connected to a tank circuit through a tunnel diode D.

The value of resistor selected should be in such a way that it biases the tunnel diode in the midway of the negative resistance region. The fig. 10.10 shows the practical tunnel diode oscillator circuit.

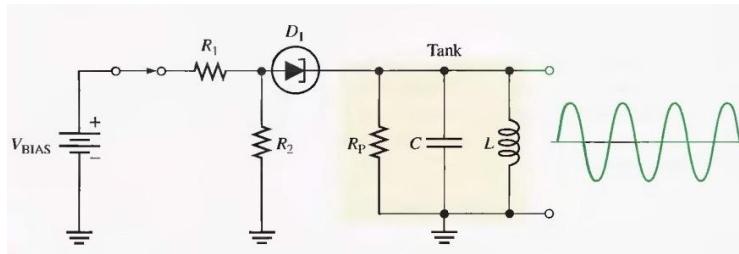


Fig. 10.10

In this circuit, the resistor R_1 sets proper biasing for the diode and the resistor R_2 sets proper current level for the tank circuit. The parallel combination of resistor R_p inductor L and capacitor C form a tank circuit, which resonates at the selected frequency.

When the switch S is closed, the circuit current rises immediately towards the constant value, whose value is determined by the value of resistor R and the diode resistance. However, as the voltage drop across the tunnel diode V_D exceeds the peak-point voltage V_P , the tunnel diode is driven into negative resistance region.

In this region, the current starts decreasing, till the voltage V_D becomes equal to the valley point voltage V_v . At this point, a further increase in the voltage V_D drives the diode into positive resistance region. As a result of this, the circuit current tends to increase. This increase in circuit will increase the voltage drop across the resistor R which will reduce the voltage V_D .

LASER DIODE

Laser (light amplification by stimulated emission of radiation) is a source of highly monochromatic, coherent and directional light. It operates under stimulated emission condition. The function of a laser diode is to convert electrical energy into light energy. The beam of a typical laser has 4×0.6 mm extending at a distance of 15 meters.

CONSTRUCTION OF A LASER DIODE

Laser diode uses gallium arsenide doped with elements such as selenium, aluminum, or silicon to produce P type and N type semiconductor materials. An additional layer of intrinsic gallium arsenide, sandwiched between the P and N layers. It is in this layer that the laser light is produced.

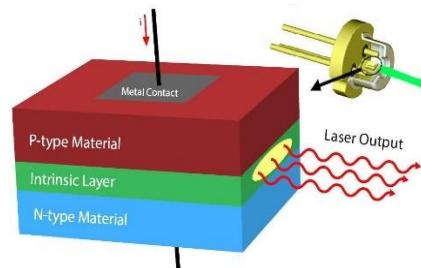


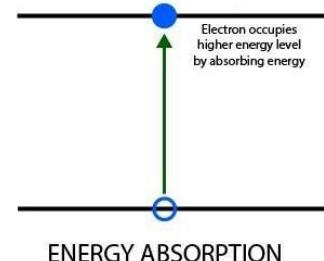
Fig. 10.11 Construction of LASER Diode

WORKING OF A LASER DIODE

The working of a laser diode takes place in three main steps:

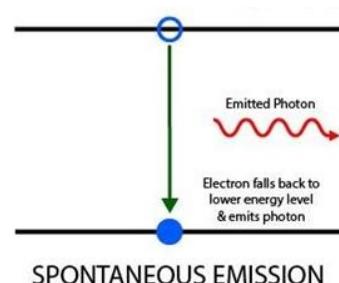
Energy Absorption

When a certain voltage is applied at the p-n junction, the electrons absorb energy and they transition to a higher energy level. Holes are formed at the original position of the excited electron. The electrons stay in this excited state without recombining with holes for a very small duration of time. This time is about a nanosecond for most laser diodes.



Spontaneous Emission

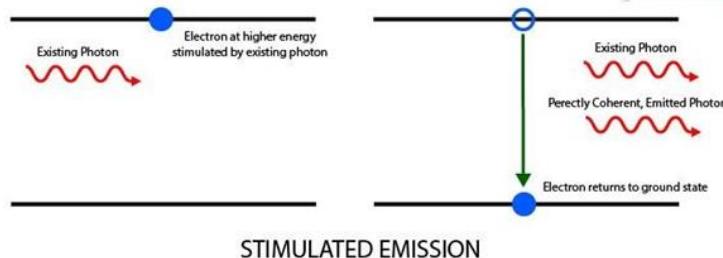
After the upper-state lifetime of excited electrons, they recombine with holes. As the electrons fall from higher energy level to a lower energy level, the difference in energy is converted into photons or electromagnetic radiation.



Stimulated Emission

A partially reflecting mirror is used on either side of the diode so that the photons released from spontaneous emission are trapped in the p-n junction until their concentration reaches a threshold value. These trapped photons

stimulate the excited electrons to recombine with holes even before their recombination time. This results in the release of more photons that are in exact phase with the initial photons and so the output gets amplified resulting in a bright monochromatic coherent light.



APPLICATIONS OF LASER DIODE

Consumer Electronics: CD/DVD players, Laser printers, Fiber Optic Communication, Barcode Readers etc.

Medical Machines: Laser diodes are used in machines used to remove unwanted tissues, eliminating cancer cells, non-invasive and cataract surgeries etc.

Scientific Instrumentation: Lasers are used in devices used for remote contactless measurements, spectrometry, range finders etc.

Industrial Applications: Laser Diodes are used as a source of high intensity laser beam for precise cutting of materials. They are also used in 3D printing to soften the substrate.

THYRISTOR

The P-N-P-N devices with zero, one or two gates constitute the basic thyristor. The thyristor family members include diac, triac, SCR (silicon-controlled rectifier), Shockley diode, SCS (silicon-controlled switch), SBS (silicon bilateral switch), SUS (silicon unilateral switch), LASCR (light activated SCR), LAS (light activated switch) and LASCS (light activated SCS).

SILICON CONTROLLED RECTIFIER

SCR SYMBOL

The SCR is a four-layer (P-N-P-N) semiconductor device that contains three PN junctions in series, and is represented by the symbol as shown in fig. 10.12. The SCR is a unidirectional device, that is it will only conduct current in one direction only.

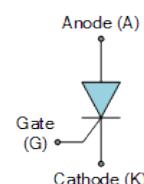
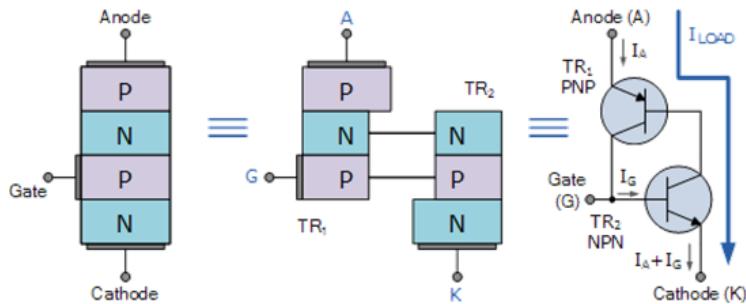


Fig. 10.12

SCR EQUIVALENT CIRCUIT

The SCR is a three-terminal device labelled: “Anode”, “Cathode” and “Gate” and consisting of three PN junctions.



The two-transistor equivalent circuit shows that the collector current of the NPN transistor TR₂ feeds directly into the base of the PNP transistor TR₁, while the collector current of TR₁ feeds into the base of TR₂.

Modes of Operation in SCR

OFF state (forward blocking mode) – Here the anode is assigned a positive voltage, the gate is assigned a zero voltage (disconnected) and the cathode is assigned a negative voltage. As a result, Junctions J₁ and J₃ are in forward bias while J₂ is in reverse bias. J₂ reaches its breakdown avalanche value and starts to conduct. Below this value, the resistance of J₁ is significantly high and is thus said to be in the off state.

ON state (conducting mode) – An SCR is brought to this state either by increasing the potential difference between the anode and cathode above the avalanche voltage or by applying a positive signal at the gate. Immediately the SCR starts to conduct, gate voltage is no longer needed to maintain the ON state and is, therefore, switched off by decreasing the current flow through it to the lowest value called holding current.

Reverse blocking – In this mode of operation, cathode is made positive with respect to anode. Then the junctions J₁ and J₃ are reverse biased and J₂ is forward biased. This reverse voltage drives the SCR into reverse blocking region results to flow a small leakage current through it. There will be a considerable damage to the SCR when the reverse voltage applied more than V_{BR}.

Once the thyristor has self-latched into its “ON” state and passing a current, it can only be turned “OFF” again by either removing the supply voltage and therefore the Anode (I_A) current completely, or by reducing its Anode to Cathode current by some external means (the opening of a switch for example) to below a value commonly called the “minimum holding current”, I_H.

VI characteristics curve of the SCR

All these three modes are shown in the VI characteristics curve of the SCR. Note that in the VI characteristic fig. 10.13, if the gate current value is high, the minimum will be the time to come in conduction mode as $I_{G2} > I_{G1} > I_{G0} = 0$.

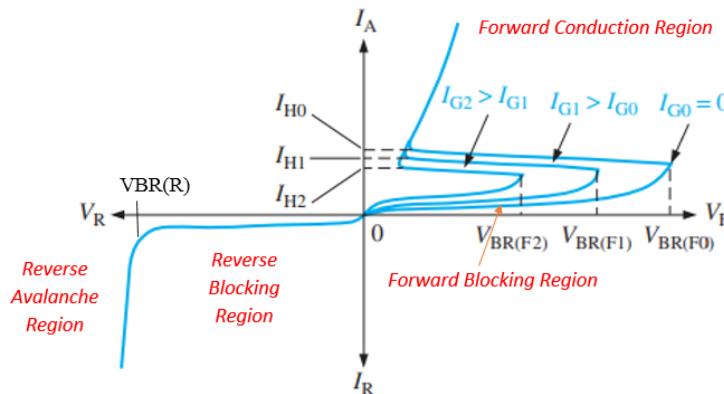


Fig. 10.13

SCR APPLICATIONS

Due to the wide variety of advantages, makes the SCR to be used in a variety of applications. These applications include switching, rectification, regulation, protection, etc. The SCRs are used for home appliance control include lighting, temperature control, fan speed regulation, heating, and alarm activation. For industrial applications, SCRs are used to control the motor speed, battery charging and power conversions.

PHASE-CONTROL OF AN SCR

In ac circuits the SCR can be turned-on by the gate at any angle. This angle θ is called the firing angle and power control is obtained by varying the firing angle. This is known as phase control. A basic AC phase-control circuit can be constructed as shown in fig. 10.14.

During the positive half-cycle, capacitor charges up via resistor R_1 following the AC supply voltage. The Gate is activated only when the voltage at point A has risen enough to cause the trigger diode D_1 , to conduct and the capacitor discharges into the Gate of the thyristor turning it "ON".

The time duration in the positive half of the cycle at which conduction starts is controlled by RC time constant set by the variable resistor, R_1 .

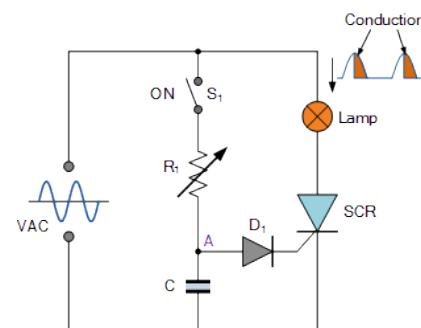


Fig. 10.14

Increasing the value of R_1 has the effect of delaying the triggering voltage and current supplied to the thyristors Gate which in turn causes a lag in the device's conduction time. As a result, the fraction of the half-cycle over which the device conducts can be controlled between 0 and 180 degree.

DC SCR SWITCHING CIRCUIT

The circuit shown in fig. 10.15, uses the thyristor as a switch to control a lamp.

The thyristor is forward biased and is triggered into conduction by closing the normally-open "ON" push button, S_1 which connects the gate terminal to the DC supply via the gate resistor, R_G thus allowing

current to flow into the Gate. If the value of R_G is set too high with respect to the supply voltage, the thyristor may not trigger.

Once the circuit has been turned "ON", it stays "ON" even when the push button is released. providing the load current is more than the thyristors latching current. The Gate-cathode resistor R_{GK} is generally included to reduce the Gate's sensitivity.

A normally-open switch is connected in parallel with the thyristor. Activation of switch S_2 momentarily applies a short circuit between the thyristors Anode and Cathode stopping the device from conducting by reducing the holding current to below its minimum value.

SCR OVER VOLTAGE CROWBAR OR PROTECTION CIRCUIT

The SCR over voltage crowbar or protection circuit is connected between the output of the power supply and ground. The Zener diode voltage is chosen to be slightly above that of the output rail. Typically a 5 volt rail may run with a 6.2 volt Zener diode. When the Zener diode voltage is reached, current will flow through the Zener and trigger the silicon controlled rectifier or thyristor. This will then provide a short circuit to ground, thereby protecting the circuitry that is being supplied form any damage and also blowing the fuse that will then remove the voltage from the series regulator.

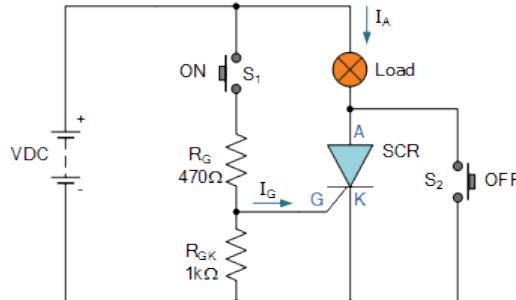


Fig. 10.15

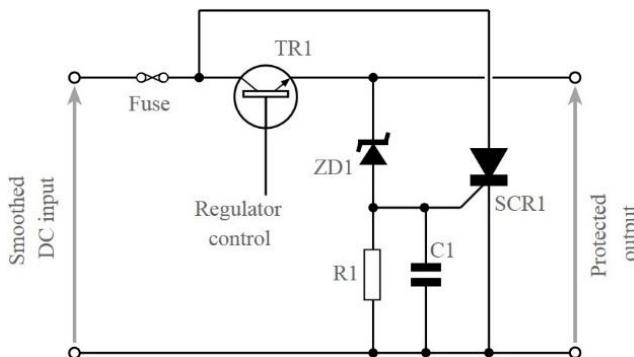


Fig.10.16 (Protection Circuit)

DIAC

A DIAC is a diode that conducts electrical current only after its breakdown voltage (V_{BO}) has been reached. DIAC stands for “Diode for Alternating Current”. A DIAC has two electrodes, and it is a member of the thyristor family. DIACs are used in the triggering of thyristors.

DIAC SYMBOL

The DIAC is a combination of two diodes in parallel, one in forward bias and the other one is in reverse bias condition with respect to both sides. DIAC is a specially constructed diode, which allows current to pass in both directions when certain conditions are met. The fig. 10.17. shows a symbol of a DIAC, which resembles the connection of two diodes in parallel.

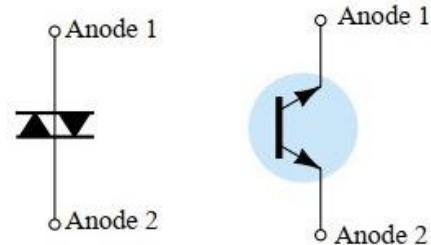


Fig. 10.17

DIAC CONSTRUCTION

The DIAC construction has two main terminals, Anode 1, and Anode 2. The DIAC construction uses two P-type materials and three N-type materials without the gate terminal as shown in fig. 10.18. Three N-type regions are shown with the name of n_1 , n_2 , and n_3 . P-type regions are shown as p_1 and p_2 .

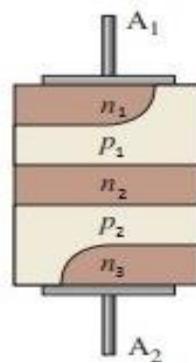


Fig. 10.18

OPERATION OF A DIAC

As soon as the supply voltage whether positive or negative is applied across the terminals of a diac, only a small leakage current flows through the device. So the device operates in either forward or reverse blocking modes. When the applied voltage is increased to a value such that it is equal to the breakdown voltage, an avalanche breakdown occurs at the reverse biased

junction. Then, it starts conducting and exhibits negative resistance characteristics. The current flow increases quickly when it comes into the conduction mode. Therefore, for a safe operating level of this conduction current in either direction, a resistance is connected in series with the diac. When A_1 is positive with respect to A_2 , the semiconductor layers of particular interest are $p_1n_2p_2$ and n_3 . For A_2 positive with respect to A_1 , the applicable layers are $p_2n_2p_1$ and n_1 .

The conduction continues until the current decreases to a certain value called as holding current.

V-I CHARACTERISTICS OF DIAC

The fig. 10.19 shows the V-I characteristics of DIAC which indicates the current flow through the diac with respect to the voltage across it. As long as the voltage across it is within its breakdown limits that is from $-V_{BO}$ to $+V_{BO}$, the resistance offered by the diac is very high.

Once the positive or negative applied voltage is more than the respective breakdown voltages that means at point A, the diac begins to conduct and the voltage drop across the device becomes few volts. The portion AB represents the conduction of diac. This conduction continues until the device current falls below its holding current level.

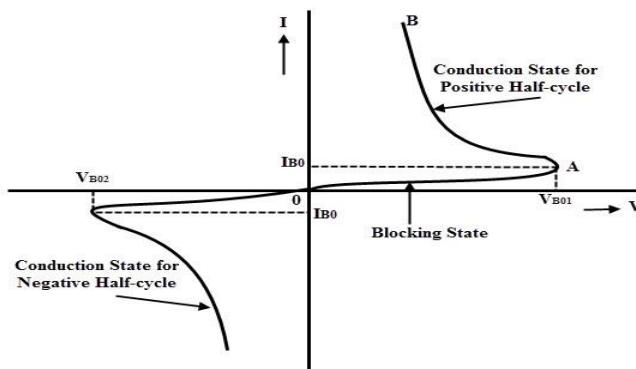


Fig. 10.19

TRIAC

Triac is a three terminal AC switch which can conduct in both the directions that is whether the applied gate signal is positive or negative, it will conduct. TRIAC stands for “Triode for Alternating Current” This device can be used for AC systems as a switch.

SYMBOL & CONSTRUCTION OF TRIAC

The construction, P-N doping and schematic symbol used to represent a triac is shown in fig. 10.20. It consists of three terminals namely, main terminal 1(MT₁), main terminal 2(MT₂), and gate terminal G. Two SCRs are connected in inverse parallel with gate terminal as common. Gate terminals is connected to both the N and P regions due to which gate signal may be applied which is irrespective of the polarity of the signal. TRIAC works for both the polarities which means that device is bilateral.

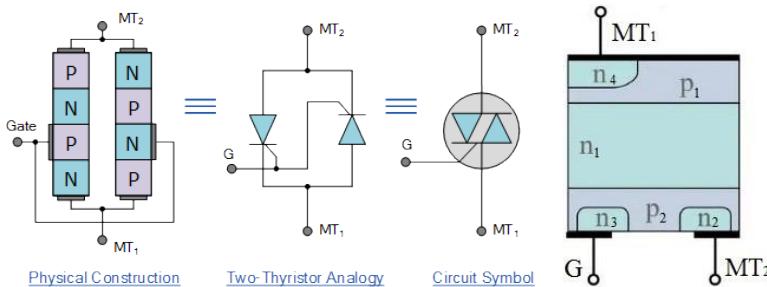


Fig. 10.20

OPERATION OF TRIAC

There are four different modes of operations.

1. When MT₂ and Gate being Positive with respect to MT₁, current flows through the path P₁-N₁-P₂-N₂. Here, P₁-N₁ and P₂-N₂ are forward biased but N₁-P₂ is reverse biased. The triac is said to be operated in positively biased region. Positive gate with respect to MT₁ forward biases P₂-N₂ and breakdown occurs.
2. When MT₂ is Positive but Gate is Negative with Respect to MT₁. The current flows through the path P₁-N₁-P₂-N₂. But P₂-N₃ is forward biased and current carriers injected into P₂ on the triac.
3. When MT₂ and Gate are Negative with Respect to MT₁. Current flows through the path P₂-N₁-P₁-N₄. Two junctions P₂-N₁ and P₁-N₄ are forward biased but the junction N₁-P₁ is reverse biased. The triac is said to be in the negatively biased region.
4. When MT₂ is Negative but Gate is Positive with Respect to MT₁. P₂-N₂ is forward biased at that condition. Current carriers are injected so the triac turns on.

V-I CHARACTERISTICS OF TRIAC

The characteristic curve of a triac is shown in fig. 10.21. Notice that the breakover potential decreases as the gate current increases. The triac ceases to conduct when the anode current drops below the holding current. Fig. shows the triac being triggered into both directions of conduction.

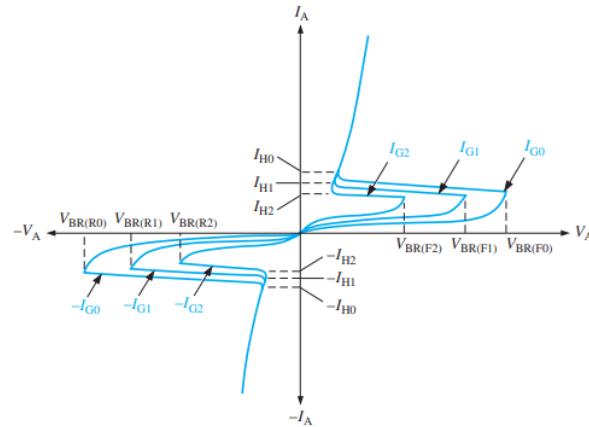


Fig. 10.21

PHASE SHIFT CONTROL OF TRIAC & DIAC

The DIAC is designed specifically to trigger TRIAC or an SCR to make the switching more even for both halves of the cycle as shown in fig. 10.22.

As the AC supply voltage increases at the beginning of the cycle, capacitor, C is charged through the series combination of the fixed resistor, R_1 and the potentiometer, VR_1 . When the charging voltage reaches the breakdown voltage of the DIAC (about 30 V), the DIAC breaks down and the capacitor discharges through the DIAC.

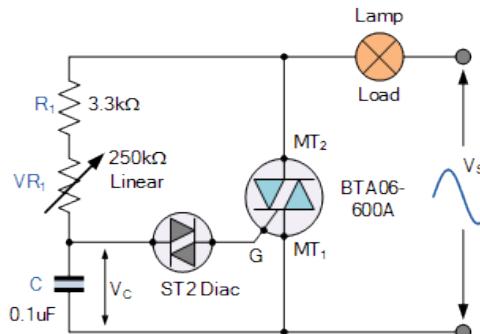


Fig. 10.22

The discharge produces a sudden pulse of current, which fires the triac into conduction. The phase angle at which the triac is triggered can be varied using VR_1 , which controls the charging rate of the capacitor. Resistor, R_1 limits the gate current to a safe value when VR_1 is at its minimum. Once the triac has been fired into conduction, it is maintained in its "ON" state.

At the end of the half cycle the supply voltage falls to zero, reducing the current through the triac below its holding current, I_H turning it "OFF" and the DIAC stops conduction. The supply voltage then enters its next half-cycle, the capacitor voltage again begins to rise (this time in the opposite direction)

and the cycle of firing the triac repeats over again. TRIAC conduction waveform is shown in fig. 10.23.

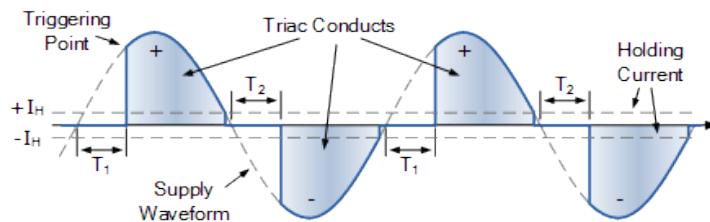


Fig. 10.23

UNI JUNCTION TRANSISTOR

The Unijunction Transistor or UJT, is a solid state three terminal device that can be used in gate pulse, timing circuits and trigger generator applications.

UJT CONSTRUCTION & EQUIVALENT CIRCUIT

Unijunction transistor is constructed from separate P-type and N-type semiconductor materials forming a single PN-junction within the main conducting N-type channel of the device. The channel has two outer connections marked as Base 2 (B_2) and Base 1 (B_1). The third connection, marked as the Emitter (E) is located along the channel. The emitter terminal is represented by an arrow pointing from the P-type emitter to the N-type base. Fig. 10.24 shows the symbol, construction, and equivalent circuit of the UJT.

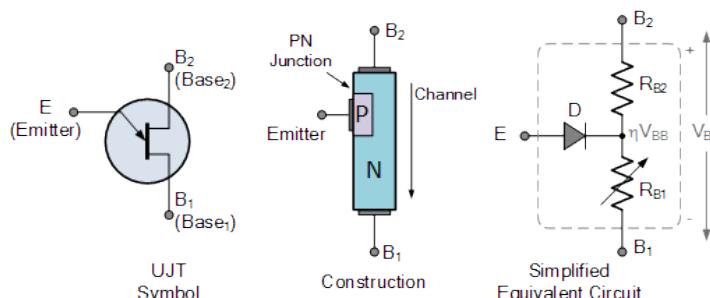


Fig. 10.24

We can see from the equivalent circuit above, that the N-type channel basically consists of two resistors R_{B2} and R_{B1} in series with an equivalent diode. R_{B1} is given between the emitter, E and terminal B_1 , while R_{B2} is given between the emitter, E and terminal B_2 . The total resistance of the silicon bar can be represented by R_{BB} .

UJT OPERATION

Suppose a voltage V_{BB} is applied across the UJT between B_2 and B_1 so that B_2 is biased positive relative to B_1 . With zero Emitter input applied, the voltage developed across R_{B1} can be calculated as:

$$V_{RB1} = \frac{R_{B1}}{R_{B1} + R_{B2}} \times V_{BB}$$

For a unijunction transistor, the resistive ratio of R_{B1} to R_{BB} is called the intrinsic stand-off ratio and is given the Greek symbol: η (eta). Typical standard values of η range from 0.5 to 0.8 for most common UJT's.

If a small positive input voltage which is less than ηV_{BB} is now applied to the emitter input terminal, the diode p-n junction is reverse biased, thus offering a very high impedance and the device does not conduct. The UJT is switched "OFF" and zero current flows.

However, when the emitter input voltage is increased and becomes greater than V_P ($\eta V_{BB} + 0.7V$), the p-n junction becomes forward biased and the unijunction transistor begins to conduct. The result is that emitter current, now flows from the emitter into the base region.

The effect of the additional emitter current flowing into the base reduces the resistive portion of the channel between the emitter junction and the B_1 terminal. The effect of this results in a negative resistance at the emitter terminal.

V-I CHARACTERISTICS OF UJT

The V-I characteristics of UJT is shown in fig. 10.25.

- i- Initially, in the cut-off region, as V_E increases from zero, slight leakage current due to the minority carriers flows from terminal B_2 to the emitter.
- ii- Above a certain value of V_E , forward I_E begins to flow, increasing until the peak voltage V_P and I_P are reached at point P.
- iii- After the peak point P, an attempt to increase V_E is followed by a sudden increase in emitter current I_E with a corresponding decrease in V_E . This is a negative resistance portion of the curve.
- iv- The negative portion of the curve lasts until the valley point V is reached with valley voltage V_V and valley current I_V . After the valley point, the device is driven to saturation.

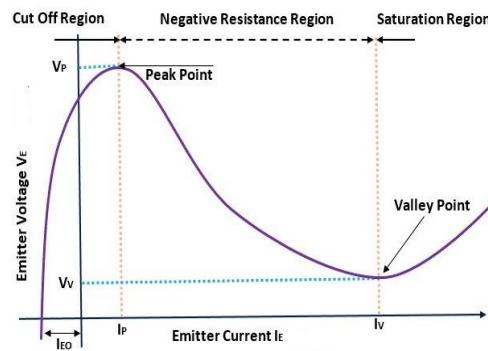


Fig. 10.25

UJT RELAXATION OSCILLATOR

The applications of a unijunction transistor include a triggering device for SCR's and TRIAC's, saw-toothed generators, phase control, and timing circuits. The simplest of all UJT circuits is the relaxation oscillator producing non-sinusoidal waveforms. A UJT relaxation oscillator circuit is shown in fig. 10.26.

OSCILLATOR OPERATION

Initially, UJT is “OFF” and the capacitor C_1 is fully discharged. When a voltage (V_s) is applied, capacitor begins to charge up exponentially through resistor R_3 . As the capacitor voltage becomes greater than the peak voltage, the p-n junction behaves as a normal diode and becomes forward biased triggering the UJT into conduction. The unijunction transistor is “ON”. As the ohmic value of resistor R_1 is very low, the capacitor discharges rapidly through the UJT and a fast-rising voltage pulse appears across R_1 .

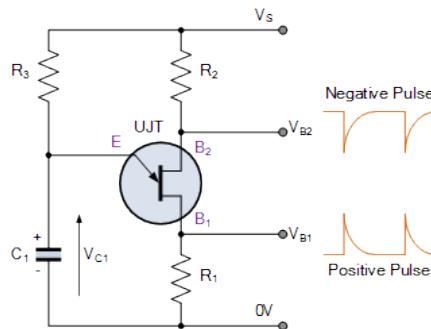


Fig. 10.26

When the voltage across the capacitor decreases below the holding point of the p-n junction (V_{OFF}), the UJT turns “OFF” and no current flows into the Emitter junction so once again the capacitor charges up through resistor R_3 and this charging and discharging process between V_{ON} and V_{OFF} is constantly repeated while there is a supply voltage, V_s applied.

UJT OSCILLATOR WAVEFORMS

The frequency of operation of the oscillator is directly affected by the value of the charging resistance R_3 , in series with the capacitor C_1 and the value of η . The output pulse shape generated from the Base1 (B_1) terminal is that of a sawtooth wave.

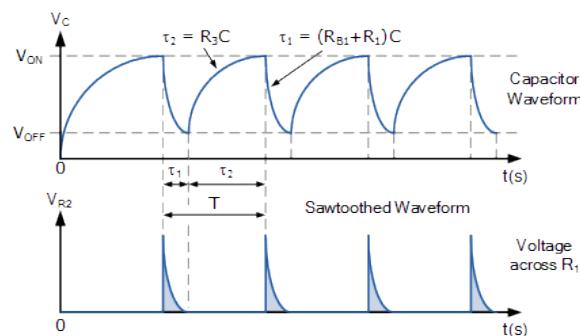


Fig. 10.27

PHOTO TRANSISTOR

The phototransistor is a three-layer semiconductor device which has a light-sensitive base region. The base senses the light and converts it into the current which flows between the collector and the emitter region.

A phototransistor is similar to a regular BJT except that the base current is produced and controlled by light instead of a voltage source. The collector-base PN junction is exposed to incident light through a lens opening in the transistor package. When there is no incident light, there is only a small thermally generated leakage current. This dark current is typically in the nA range. When light strikes the collector-base PN junction, a base current, I_λ , is produced that is directly proportional to the light intensity.

A phototransistor can be either a two-lead or a three-lead device. In the three-lead configuration, the base lead is brought out so that the device can be used as a conventional BJT with or without the additional light-sensitivity feature. In the two-lead configuration, the base is not electrically available, and the device can be used only with light as the input.

Collector current controlling factors

The output of the phototransistor depends on various factors like

- Wavelength of the incident light.

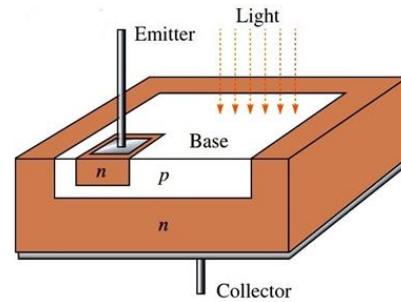


Fig. 10.28

- Area of the light-exposed collector-base junction.
- DC current gain of the transistor.

PHOTO DARLINGTON

In photodarlington, the two transistors connected back to back through the base shown in the fig. 10.29. In this arrangement, the phototransistor induces much higher power, i.e., their sensitivity rises.

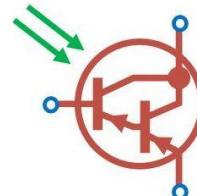
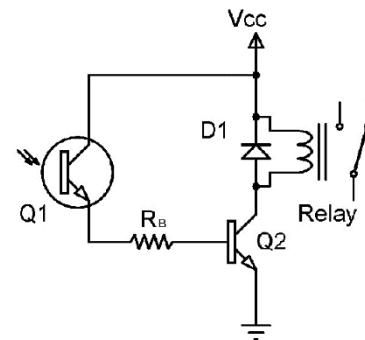


Fig. 10.29

LIGHT OPERATED RELAY

When there is enough light falling on the phototransistor Q_1 , it turns ON and provides a base current to transistor Q_2 . As a result, Q_2 is turned ON and the relay is energized.



LIGHT ACTIVATED SCR (LASCR)

A light activated silicon-controlled rectifier (LASCR) is a silicon-controlled rectifier that conducts when the gate is exposed to light. The gate still operates as a normal gate in a SCR, but is in many cases left disconnected. LASCR has a lens that focuses light on its gate.

LASCR CONSTRUCTION

The LASCR is a semiconductor electronic switch which has a lens that focuses light on its gate. If sufficient light does not fall on the LASCR then it remains in off state. The basic construction of light activated silicon-controlled rectifier (LASCR) is shown in the fig. 10.30.

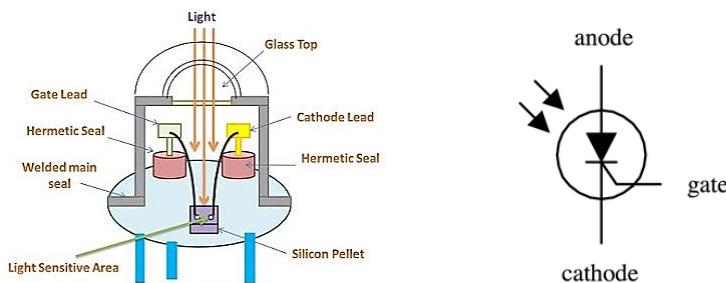


Fig. 10.30

WORKING OF LASCR

The incident photons will generate electron hole pairs, when light is focused on LASCR. The number of optically generated electron hole pairs is proportional to the intensity of light. These electrons will constitute a gate current for LASCR and due to the internal current multiplication, the LASCR is

latched into ON state. The LASCR is most sensitive to light when its gate terminal is left open. Its sensitivity can be reduced and controlled to some extent by inserting a resistor between its gate and cathode terminals.

Sometimes a combination of both light source and gate signal is used to trigger an SCR. For this, the gate is biased with voltage or current slightly less than that required to turn it on.

The LASCR will remain ON until the polarities of the anode and cathode are reversed or the power is cut.

OPTO COUPLER

An Optocoupler, is an electronic component that interconnects two separate electrical circuits by means of a light sensitive optical interface.

CONSTRUCTION OF OPTOCOUPLER

The basic design of an optocoupler, also known as an Opto-isolator, consists of an LED that produces infra-red light and a semiconductor photo-sensitive device which can be a single photo-diode, photo-transistor, photo-resistor, photo-SCR, or a photo-TRIAC that is used to detect the emitted infra-red beam. Both the LED and photo-sensitive device are enclosed in a light-tight body or package with metal legs for the electrical connections as shown in fig. 10.31.

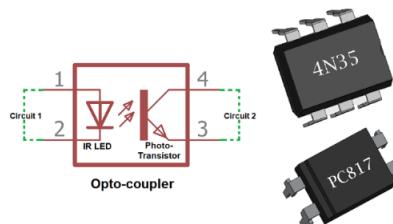


Fig. 10.31

WORKING

Current from the source signal passes through the input LED which emits an infra-red light whose intensity is proportional to the electrical signal. This emitted light falls upon the base or gate of the photo-sensitive device, causing it to switch-ON and conduct in a similar way to a normal bipolar transistor.

OPTOCOUPLER TYPES

Optocouplers are available in four general types, each one having an infra-red LED source but with different photo-sensitive devices. The four

optocouplers are called the: *Photo-transistor*, *Photo-Darlington*, *Photo-SCR* and *Photo-triac* as shown in fig. 10.32.

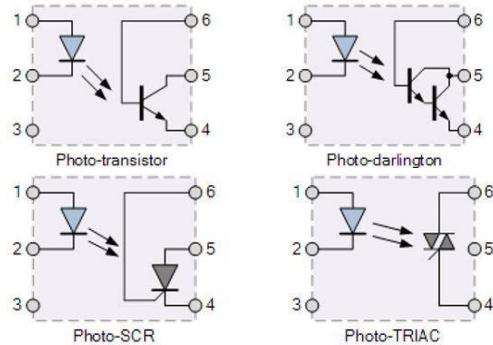


Fig. 10.32

APPLICATIONS OF OPTOCOUPLER

Optocouplers can either be used on their own as a switching device, or used with other electronic devices to provide isolation between low and high voltage circuits. You'll typically find these devices being used for:

- Microprocessor input/output switching
 - DC and AC power control
 - Communications equipment protection
 - Power supply regulation

EXERCISE

SECTION-I (MCQ's)

- (a) UJT (b) Tunnel diode (c) Diac (d) Resistor
9. Following is a light sensitive device;
 (a) LASCR (b) Zener diode (c) Tunnel diode (d) TRIAC
10. In an optocoupler, input device is a;
 (a) Photo diode (b) LASCR (c) LED (d) Photo transistor
11. The output waveform of a relaxation oscillator is;
 (a) Sine (b) Cosine (c) Non-Sinusoidal (d) None of these
12. The value of intrinsic stand-off ratio in a UJT is
 (a) 1 to 5 (b) Less than 1 (c) 2 to 4 (d) Greater than 10
13. Two thyristors which conduct in both directions;
 (a) SCR & DIAC (b) SCR & TRIAC (c) DIAC & TRIAC (d) Shockley & SCS
14. In LCD, the organic compound is used which is in the form;
 (a) Solid (b) Liquid (c) Solid (d) All of these

ANSWER KEY

1.	c	2.	a	3.	d	4.	a	5.	c
6.	d	7.	c	8.	d	9.	a	10.	c
11.	c	12.	b	13.	c	14.	b		

SECTION-II (Short Questions)

1. Draw the current and voltage characteristics curve of Zener diode.
2. Define optical devices.
3. Define LASER diode
4. Define dark current.
5. Differentiate the LED and LCD.
6. Define photo diode and draw its symbol.
7. Write the application of Zener diode.
8. Define thyristor.
9. Draw the symbol of DIAC and TRIAC.
10. Describe the construction of Zener diode.
11. Describe the electro luminescence process in a LED.
12. Draw the characteristics curve of tunnel diode.
13. Write the method of turning off the SCR.
14. Describe the biasing of UJT.
15. Draw the characteristics curve of DIAC.
16. Sketch equivalent circuit for UJT.
17. Sketch the circuit of photo Darlington pair.
18. List the applications of opto-coupler.
19. List types of output devices used in opto-coupler.

SECTION-III (Long Questions)

1. Explain Zener diode as voltage regulator with circuit.
2. Explain the working of an SCR.
3. What is photo transistor? Explain its construction and working.
4. Sketch and label the V-I characteristics for an SCR.