MTS4 MTS4B

±0.1°C/±0.5°C accuracy, 16bitADC, ultra-low power consumption, I² C interface/single bus interface digital temperature sensing chip

1. summarize

MTS4 series is a digital-analog mixed-signal temperature sensing chip with the highest temperature measurement accuracy of ±0.1°C, and users do not need to carry out calibration. The temperature chip sensing principle is based on the characteristic relationship between the temperature of CMOS semiconductor PN node and the bandgap voltage, after small signal amplification, analog-to-digital conversion, digital calibration and compensation, the digital bus output, with high precision, good consistency, fast temperature measurement, low power consumption, programmable configuration and flexible, long life and other advantages.

The chip has a built-in 16-bit ADC with a resolution of 0.004°C and an ultra-wide operating range of -103°C to +153°C. The chip is 100% tested and calibrated at the factory and the calibration coefficients are fitted according to the temperature error characteristics. The chip is 100% calibrated before shipment, and the calibration coefficients are fitted according to the temperature error characteristics, and the compensation calculation is performed automatically inside the chip. The chip supports digital I² C communication interface, temperature measurement data memory access, function configuration, etc. can be realized through digital protocol commands. I² C interface is suitable for high speed board application scenarios, the maximum interface speed can be up to 2MHz.

The chip has a built-in non-volatile E² PROM memory cell, which is used to store the chip ID number, high and low temperature alarm thresholds, temperature calibration correction values, and user-defined information, such as sensor node number, location information, and so on.

2. specificities

- Maximum temperature measurement accuracy: ±0.1°C/±0.5°C
- Temperature range: -103°C~+153°C
- Low power consumption: Typical standby current 0.01μA, peak temperature current 0.36mA, average temperature current 2μA
  (AVG=8, 1 measurement/s)
- Wide operating voltage range: 1.8V~5.5V
- Sensing resolution: 16-bit output 0.004°C
- Temperature transition time configurable: 15.3ms/8.5ms/5.2ms/2.2ms
- Configurable single/periodic measurements

- Maximum 112bit Additional E^2 PROM space for user information
- Standard I^2 C interface, also compatible with digital single bus interface
- Self-diagnostic function of heating chip

3. appliance

- smart wearable
- electronic thermometer
- Animal body temperature testing
- medical electronics
- Cold chain logistics, warehousing
- smart home
- Heat meter gas meter water meter
- Replaces PT100/PT1000
- Board Level Temperature Monitoring
- Industrial and agricultural ambient temperatures
- smart home appliance
- consumer electronics
- Temperature measurement instrumentation

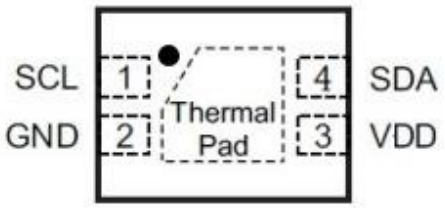
Product Information

model number	highest precision	Maximum precision interval	address location	seal inside
MTS4	±0.1°C	+28°C to +43°C	0x41	DFN4L
MTS4Z	±0.1°C	0°C to +50°C	0x41	DFN4L
MTS4P	±0.1°C	-25°C to +25°C	0x41	DFN4L
MTS4B	±0.5°C	0°C to +60°C	0x41	DFN4L

Note: For other temperature interval accuracy characteristics, see " 7 Temperature measurement performance indicators."

catalogs

4. Package Pin Description



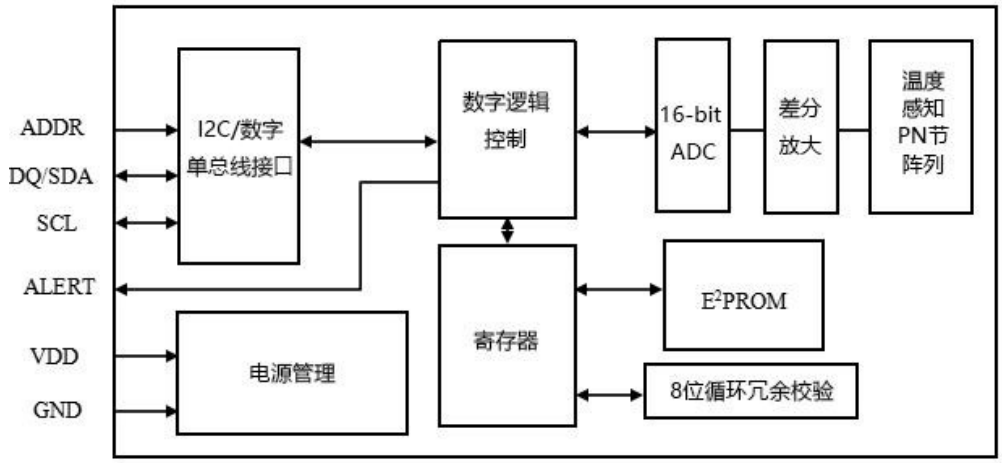
(Front perspective view)

Pin Number	Pin Name	I/O	clarification
1	SCL	Input/Output	I² C Clock Line
2	GND	-	structural particle: used before a verb or adjective, linking it preceding the verb or adjective
3	VDD	-	power supply
4	SDA	Input/Output	I² C/single bus data line DQ
Thermally Conductive Pad	NC	-	Suspended or grounded (1)

NOTE 1: Circuits are designed so that the thermally conductive pads can be suspended or grounded.

1) If the ambient temperature is measured on the PCB, it is recommended that the thermal pads be connected to ground on the PCB;
2) It is recommended not to ground the device if it is attached to a PCB or if the thermal pads are attached to a metal sheet for contact detection.

5. system block diagram

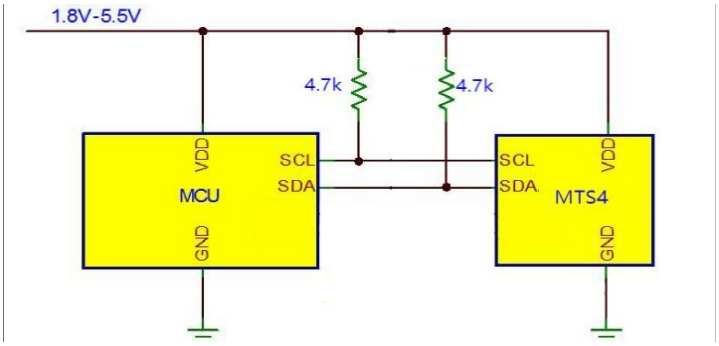


The block diagram of the temperature sensor is shown above. The staging register contains a two-byte temperature register that stores the digital output from the sensor. In addition, the staging and extended staging registers provide alarm trigger threshold registers. The configuration register allows the user to set the temperature transition repeatability and continuous measurement frequency. The status register allows querying of the alarm status. Data can be stored in a non-volatile unit, so that data will not be lost when the chip

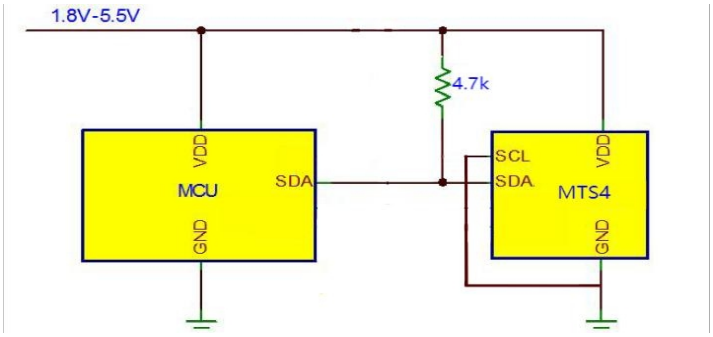
is powered down.

6. Typical Application Circuit

6.1 I² C Protocol Typical Circuit Diagram



6.2 Typical Circuit Diagram for Single Bus Protocol



In single-bus mode, the SCL pin is not dangling and can be connected to GND or VDD.

7. Temperature Measurement Performance Indicators

parameters	notation	prerequisite	minimal	typical case	greatest
Temperature range	-	-	-103°C	-	+153°C
temperature error	tERR	MTS4	-	-	±0.1°C@+28°C to +43°C ±0.5°C@-10°C to +60°C
		MTS4Z	-	-	±0.1°C@0°C to +50°C ±0.2°C@-10°C to +60°C ±0.5°C@-25°C to +75°C
		MTS4P	-	-	±0.1°C@-25°C to +25°C ±0.5°C@-55°C to +55°C
		MTS4B	-	-	±0.5°C@0°C to +60°C
		MTS4 Series	-	±2°C@-103°C to +153°C	-
repeatable	-	AVG=1	-	0.02°C	(1)

		AVG=8		0.01°C	-
		AVG=16	-	0.008°C	-
		AVG=32	-	0.007°C	-
resolution (of a photo)	-	-	-	0.004°C	-
long term drift	-	-	-	-	0.03°C/year

Note 1: The higher the average number, the longer the conversion time, but the higher the output accuracy, see Table 9.3-2.

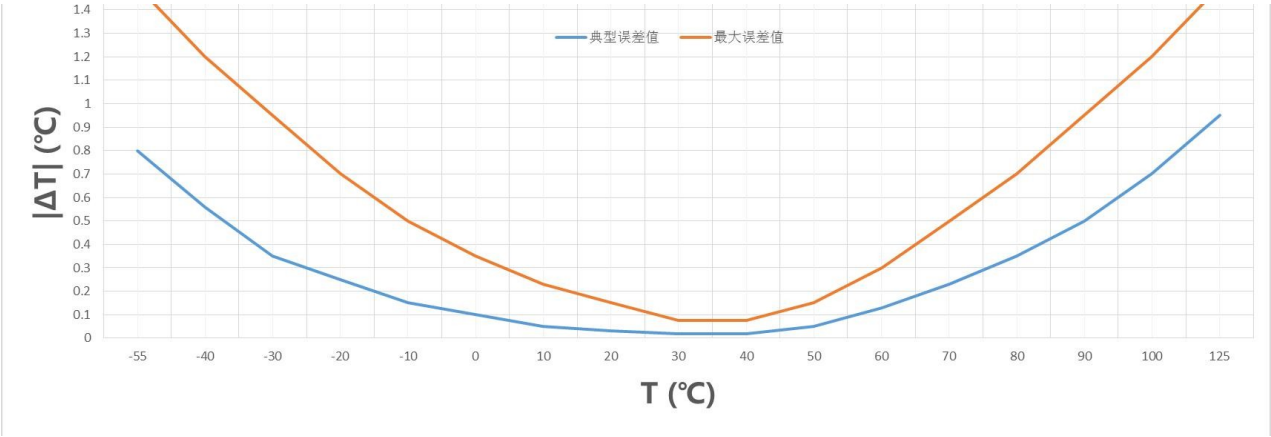


Figure 7-1MTS4 Accuracy Error Curve

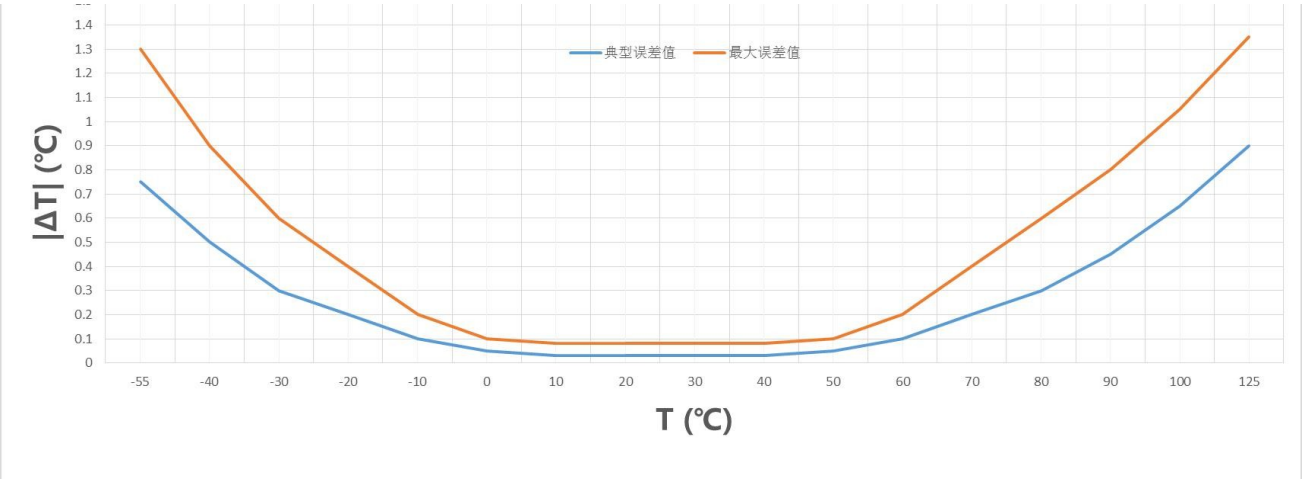


Figure 7-2MTS4Z Accuracy Error Curve

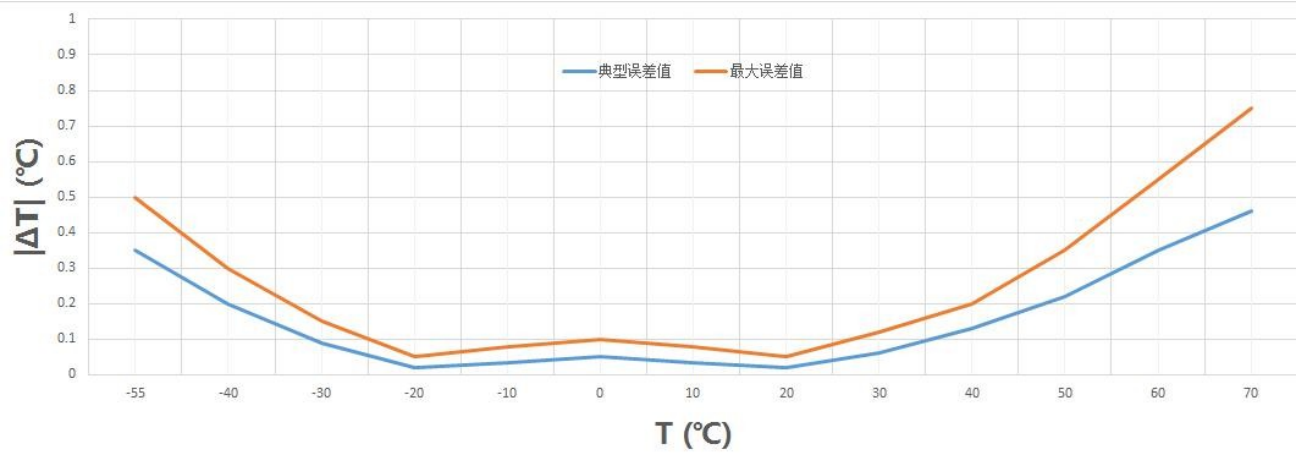


Figure 7-3MTS4P Accuracy Error Curve

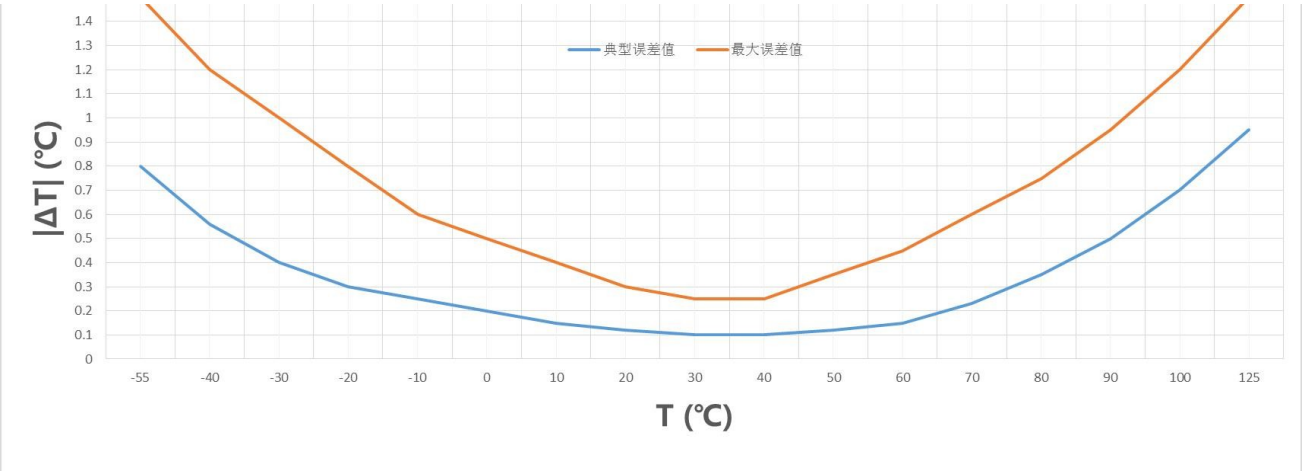


Figure 7-4 MTS4B Accuracy Error Curve

8. Electrical Specifications

8.1 Absolute maximum rating

The following are limit parameters and this specification does not apply to functional operation of the device in environments at or above these limit conditions. Please note that prolonged exposure to this limiting environment will affect the reliability of the device.

parameters	rating	unit (of measure)
Supply Voltage VDD	-0.3 to 6	V
Maximum voltage on pins	-0.3 to 6	V
Input current on pin	±100	mA
Operating temperature range	-103 to 153	℃
Storage temperature range	-103 to 153	℃
welding temperature	Reference to IPC/JEDEC J-STD-020 specification	
ESD HBM (Human Body Discharge Mode)	±8	kV

8.2 Electrical Characteristics

Typical values in the table are for T=25°C and VDD=3.3V.

parameters	notation	prerequisite	minimal	typical case	greatest	unit (of measure)	note
power supply							
Supply Voltage	VDD	-	1.8	3.3	5.5	V	Chip Pin Voltage
Supply Current	IDD	idle state (single measurement mode)	-	0.01	-	uA	In single measurement mode Standby Current
		idle state (Periodic measurement mode)	-	50	-	uA	Periodic Measurement Mode Standby Current
		measured peak value	-	360	-	uA	Current during measurement
		average value	-	2	-	uA	Single measurement mode, (AVG=8. 1 measurement/s)
Digital inputs/outputs							
Input Logic Low	VIL	SCL, SDA	-	-	0.3*VDD	V	
Input Logic High	VIH	SCL, SDA	0.7*VDD	-	-	V	
Output Low Level input voltage	VOL	IOL = -3 mA	-	-	0.4	V	
Input Leakage Current	IIN	-	-0.1	-	0.1	uA	
pull-up resistor	Rup		1	4.7	10	kΩ	

8.3 AC Electrical Characteristics-Non-Volatile Memory

-55°C to +125°C; V_{DD} = 1.8V to 5.5V

parameters	notation	prerequisite	lowest	typical case	greatest	unit (of measure)
Non-volatile memory write cycles	tWR	-	-	-	40	ms
E^2 PROM Number of writes	NEEWR	-55°C to +55°C	50000	-	-	substandard
E^2 PROM Data	tEEDR	-55°C to +55°C	-	10	-	surnam

Retention						eNian

9. Functional Description

The sensor enters an idle state after power-up. To initiate temperature measurement, the host must issue a temperature measurement command to the slave by rewriting the temperature measurement command register. After the conversion time, the resulting 16-bit temperature data is stored in the first 2 bytes of the Temperature Register (Temp_lsb/Temp_lsb). The conversion time is related to the average number of settings, the higher the average number, the longer the conversion time. See chapter 9.3 for more information on averaging times and the corresponding temperature conversion times.

9.1 Temperature output and conversion formulas

The temperature digital output is a 16bit signed binary complement, the lowest bit LSB resolution is 1/256 °C, S is the sign bit. The data is stored in the registers Temp_lsb and Temp_msb in the following format:

Table 9.1 Temperature Registers (Temp_lsb/Temp_msb), Addresses 0x00 & 0x01

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
low byte	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**
high byte (computing)	S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

and Celsius degrees are converted as:

$$T[℃] = \frac{S_T}{256} + 25$$

For example, 25 °C corresponds to the register value 0x 00 00.

153 °C Corresponding register value 0x 7F FF

-103 °C Corresponding register value 0x 80 00

9.2 instruction register

The instruction register contains two bytes, the temperature measurement instruction register and the E^2 PROM instruction register. The Temperature Measurement Instruction Register (Temp_Cmd) consists of measurement mode and heating function configuration bits as described below:

Table 9.2-1 Temperature Measurement Instruction Register (Temp_Cmd) Address 0x04

classifier for honorific people	Description	Default value
7:6	Measurement mode selection (Measurement) 00: Continuous measurement mode 01: Stop measuring 10: Continuous measurement mode, readback value 00 11: Single measurement mode	'01'
5:4	reserve	'00'

3:0	Heater function 1010: Heating function on	'OOOO'

	Other: Heating function off, readback value 0000	

The chip stops measuring by default after powering up and waits for the host to send the measurement command. A single measurement only completes one temperature conversion, and the chip will enter the sleep state after the completion of the measurement, unless the bit0 of Temp_Cfg is set to 0. Continuous measurement mode will carry out the cycle of temperature measurement according to the bit7~bit5 (MPS) of Temp_Cfg, and the chip won't enter the sleep state in the interval between the two conversions, even if the bit0 of Temp_Cfg is set to 1. The chip will not go to sleep between two transitions, even if bit0 of Temp_Cfg is set to 1. In continuous measurement mode, when the host computer writes 01 to bit7~bit6, the chip will exit the continuous measurement mode.

The E² PROM instruction register (E² PROM_Cmd) includes the E² PROM read/write operations and the soft reset configuration bits, which are described as follows: Table 9.2-2 E² PROM instruction

classifier for honorific people	Description	Default value
7:0	E² PROM operation 0xB6: Load the value of E² PROM to the staging memory 0x08: Write the value of the temporary memory to E² PROM 0x6A: System soft reset, while loading the value of E² PROM to the staging registers, all staging registers are restored to their default values Other: no operation, readback value 0x00	'OOOOOOOO'

9.3 configuration register

The configuration register (Temp_Cfg) includes configuration bits for cycle measurement frequency, temperature measurement average times, low-power mode, etc. The details are described as

classifier for honorific people	Description	Default value
7:5	Measurements per second configuration (MPS) 000: 8 per second 001: 4 times per second 010: 2 times per second 011: 1 time per second 100: 1 time in 2 seconds 101: 1 time in 4 seconds 110: 1 time in 8 seconds 111: 16 seconds 1 time	'011'
4:3	Temperature measurement average number of configurations (AVG) 00: AVG=1 01: AVG=8 10: AVG=16 11: AVG=32	'01'
2:1	reserve	'OO'
0	Low power mode switch (Sleep_en) 0: do not enter low-power mode after executing the instruction 1: Enter low-power mode after executing instructions	'1'

Table 9.3-2 Correspondence between average number of times and conversion time

AVG[1:0]		Number of data averages	Conversion time t_{CONV}
0	0	1	2.2ms
0	1	8	5.2ms
1	0	16	8.5ms
1	1	32	15.3ms

9.4 status register

The Status register (Status) is in read-only mode and contains information such as temperature transition status, alarm status, E² PROM status, heating status, etc. It is described as follows:

Table 9.4 Status address 0x03

classifier for honorific people	Description	Default value
7	Temperature high line alarm tracking 0: Temperature alarm not triggered 1: Temperature alarm triggered	'0'
6	Temperature low line alarm tracking 0: Temperature alarm not triggered 1: Temperature alarm triggered	'0'
5	Temperature conversion status 0: Temperature conversion completed 1：Temperature conversion in process	'0'
4	E² PROM Status 0: not in read/write state 1: in read/write state	'0'
3	Heating status 0: not in heating state 1：Heating state	'0'
2	Temperature alarm error message 0: TH greater than TL1: TH less than or equal to TL	'0'
1:0	reserve	'00'

9.5 CRC Checksum Function

The chip includes a CRC data check function to improve communication reliability, and the CRC value is stored in a specific address bit, which corresponds to the following register combination:

(1) The CRC checksum of 2 bytes of data from address bits 0x00 to 0x01 is done as Crc_temp and stored in address bit 0x02;

(2) The CRC checksum of 8 bytes of data from address bits 0x03 to 0x0A is done as a Crc_scratch and stored in address bit 0x0B;

(3) The CRC checksum of 10 bytes of data from address bits 0x0C to 0x15 is done as Crc_scratch_ext and stored in address bit 0x16.

The computational polynomial for the specific CRC is:

$$CRC = X^8 + X^5 + X^4 + 1$$

This algorithm circuit consists of a shift register and an iso-gate circuit with an initial value of 0x00 and the following structure:

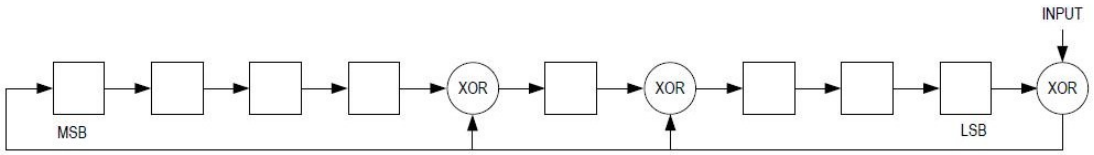


Figure 9.5 CRC Generator

I² C can read (1) one CRC checksum byte and a single bus can read (1、2、3) three CRC checksum bytes.

9.6 Alarm function

The Alert mode is used to monitor the ambient temperature and is realized by configuring the Alert Mode register (Alert_Mode), as well as the Alarm High/Low Threshold register (Th/Tl). In addition, the Status register (Status) bit has dedicated bits to indicate the alarm status, as described in chapter 9.4.

Alert_Mode register (Alert_Mode) includes configuration bits such as alarm switch, mode selection, etc. The contents of the specific configuration registers are described as follows: Table 9.6 Alert_Mode Register (Alert_Mode) Address 0x06

classifier for honorific people	Description	Default value
7	Alarm function switch (Alert_en) 0: off 1: Open	'0'
6	Alarm Mode (IM) Selection 0: above TH alarm + below TL alarm release 1: Alarm above TH + Alarm below TL	'0'
5:0	reserve	'000000'

The alarm threshold registers include the high threshold register (Th) and the low threshold register (Tl), both corresponding to the resolution of the temperature registers (Temp_lsb/Temp_msb), as described in Chapter 9.1. The 16-bit signed number of the alarm threshold will be compared with the 16-bit standard output temperature value to determine whether the alarm condition has been met, so the resolution of the temperature alarm threshold is the same as $\Delta T \approx 0.004°C$. The resolution of the alarm threshold is the same as that of the temperature register (Temp_lsb/Temp_msb).

When the alarm function is turned on, the Alert Mode is activated whenever the sensor performs a measurement operation. If the alarm function needs to be turned off, the host can set bit7 of the Alarm Configuration Register (Alert_Mode) to 1. Additionally, the alarm function can be turned off by setting the Alarm Low Line Setpoint to a value greater than or equal to the Alarm High Line Setpoint (Tl≥Th). The following alarm modes can be realized by changing the Alarm Mode bit (IM) of the Alarm Mode Register:

（1） Higher than the high limit alarm, lower than the low limit to release the alarm mode

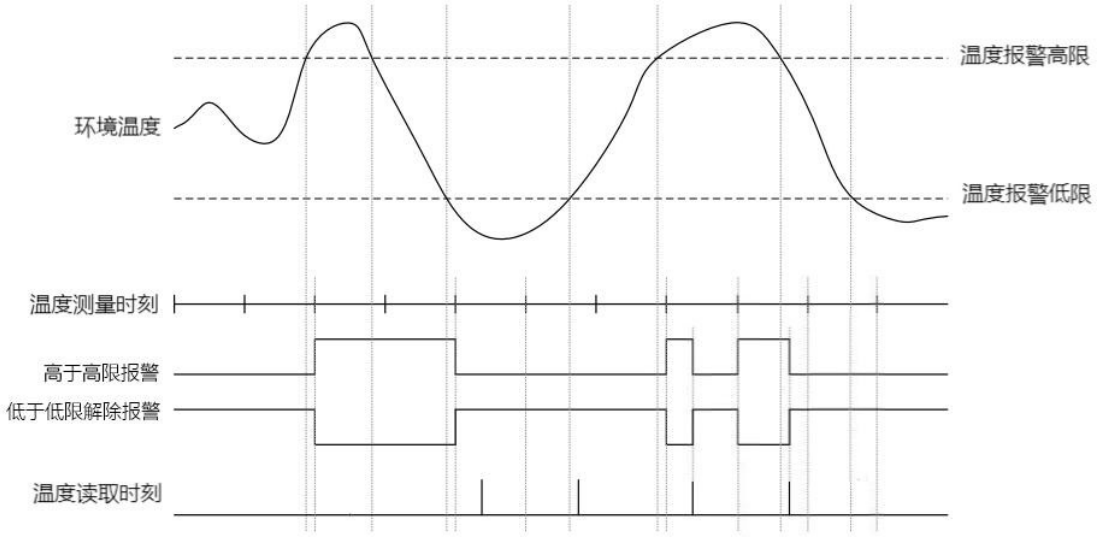


Fig. 9.6-1 Timing Diagram of Alarm Mode for Higher Than High Limit Alarm and Lower Than Low Limit Disarm Mode

This mode corresponds to IM=0, bit7 in the status register (Status) is the same as the flag bit of the above figure for exceeding the high limit alarm, bit6 is 0.

（2） Higher than high limit alarm, lower than low limit alarm mode

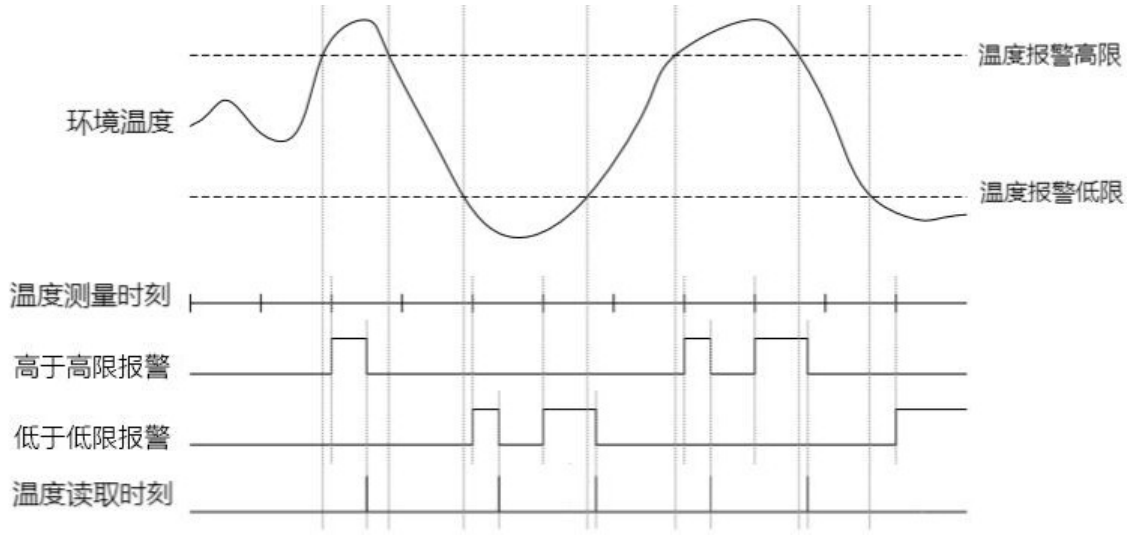


Fig. 9.6-2 Timing Diagram for Higher than High Limit Alarm, Lower than Low Limit Alarm Mode

This mode corresponds to IM=1, bit7 in the status register (Status) is the same as the flag bit for exceeding the high limit alarm as shown above, and bit6 is the same as the flag bit for falling below the low limit alarm as shown above.

9.7 Heating self-diagnosis function

The chip is equipped with an internal heating resistor to heat the chip, and the host can read the temperature value before and after heating to determine whether the chip's temperature measurement function is normal or not. The heating power is 7.8mW, and the temperature increase is above 0.1°C. The temperature measurement function is performed by the Temp_cmd instruction register. The function is activated and deactivated by bit3~bit0 in the Temp_cmd instruction register, please refer to section 9.2 for configuration details.

9.8 Temperature measurement status flag bit

The flag bit signal indicating the temperature measurement status is stored in the Status register. When the temperature measurement is in progress, bit5 of the status register = 1; when the temperature measurement is completed, bit5 of the status register = 0.

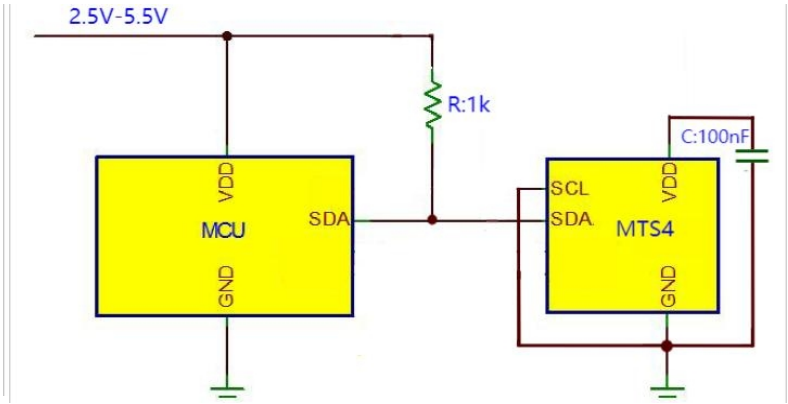
9.9 soft reset (electronics)

The host can realize the soft reset function of the chip by writing 0x6A to the E^2 PROM instruction register (E^2 PROM_Cmd). During soft reset, the register values corresponding to E^2 PROM will be reloaded, and other register values not corresponding to E^2 PROM will be reset to the power-on default values. Please refer to Chapter 10 for the correspondence between specific registers and E^2 PROM.

9.10 parasitic mode

The chip can be powered by the external power supply on the VDD pin under the single bus protocol, or it can be powered by the "parasitic" mode, which enables the chip to work without external power supply. The following figure shows the circuit diagram of the chip in parasitic mode, the VDD supply range of the MCU side is 2.5V-5.5V, and the SDA pin is used as a DQ, which is used to "steal" the power supply through the DQ pin when the DQ is high. when the DQ is high, part of the charge is stored in the storage capacitor (C) in order to supply power to

the chip when the bus is low. In parasitic mode, the storage capacitor can supply enough current to the chip as long as the specified capacitance and voltage requirements are met (see DC Characteristics and AC Characteristics).



Note: Figure 9.10 Parasitic Mode

Typical Circuit Diagram Remarks: The recommended pull-up resistor resistance value is 1kΩ, and the energy storage capacitance is not less than 100nF.

This application is limited to the single bus protocol and requires the register value at logical address 0x63 to be modified to 0x0A under the condition that the chip VDD is powered from an external power supply.

Table 9.10 Operating Mode Configuration Register (PPM_Cfg) Address 0x63

classifier for honorific people	Description	Default value
7:4	reserve	'OOOO'
3:0	Parasitic Mode Function Switch 1010: On Other: closed	'OOOO'

9.11 Chip ID

The chip ID is 16-bit and is stored in the chip ID register (Device_id) following format:

Table 9.11 Chip ID Register (Device_id_lsb/ Device_id_msb) Addresses 0x18 & 0x19

classifier for honorific people	Description	numerical value
7:0	Chip ID Low 8-bit	0x01
15:8	Chip ID 8 bits high	0x16

10. storage system

10.1 register list

The sensor's memory is organized as shown in Table 10.1. The memory contains an SRAM register as well as expanded storage non-volatile storage E² PROM for the high and low temperature alarm trigger lines (Th and Tl) the Temperature Configuration Register (Temp Cfg) the Alert Mode Register (Alert Mode) and a 10-byte user

programmable area (User_define) Note that if the sensor's alarm function is not used, the alarm high Line (Th) and Alarm Low Line (Tl) registers can be used as general purpose memory areas. All memory function definitions are described in detail in Section 9.

Table 10.1 Mapping of Register List to E² PROM

Register Name	bit width	register logical ground sites	Single bus read	Single Bus Write	E² PROM logical address (computing)	Single Bus Write E2PROM	Single bus loading E2PROM	Power-on reset default value
Temp_lsb	8	00h	Read temperature (0xBC)	NA	NA	NA	NA	00h
Temp_msb	8	01h		NA	NA	NA	NA	00h
Crc_temp	8	02h		NA	NA	NA	NA	NA
Status	8	03h	Read scratchpad (0xBE)	NA	NA	NA	NA	00h
Temp_Cmd	8	04h		Write config (0x4E)	NA	NA	NA	40h
Temp_Cfg	8	05h			00h	Copy page (0x48)	Recall EE (0xB8) / Recall page (0xB6)	69h
Alert_Mode	8	06h			01h			00h
Th_lsb	8	07h			02h			FFh
Th_msb	8	08h			03h			7Fh
Tl_lsb	8	09h			04h			00h
Tl_msb	8	0Ah			05h			80h
Crc_scratch	8	0Bh		NA	NA			NA
User_define_0	8	0Ch	Read scratchpad extension (0xDD)	Write scratchpad extension (0x77)	06h			00h
User_define_1	8	0Dh			07h			00h
User_define_2	8	0Eh			08h			00h
User_define_3	8	0Fh			09h			00h
User_define_4	8	10h			0Ah			00h
User_define_5	8	11h			0Bh			00h
User_define_6	8	12h			0Ch			00h
User_define_7	8	13h			0Dh			00h
User_define_8	8	14h			0Eh			00h
User_define_9	8	15h			0Fh			00h
Crc_scratch_ext	8	16h		NA	NA	NA	NA	NA
E2PROM_Cmd	8	17h	NA	NA	NA	NA	NA	00h
Device_id_lsb / Romcode1	8	18h	Read romcode (0x33)	NA	NA	NA	NA	01h
Device_id_msb / Romcode2	8	19h		NA	NA	NA	NA	16h
Romcode3	8	1Ah		NA	10h	NA	Recall EE (0xB8)	NA
Romcode4	8	1Bh			11h			NA
Romcode5	8	1Ch			12h			NA
Romcode6	8	1Dh			13h			NA
Romcode7	8	1Eh			14h			NA
crc_romcode	8	1Fh		NA	NA			NA

Note: There is also 11 bytes of E² PROM space inside the chip for analog performance, special function configuration, and information storage, which can be obtained by contacting the manufacturer.

10.2 E² PROM

The host needs to realize the function trigger of E² PROM by writing a specific value to the E² PROM instruction register (E² PROM_Cmd). To permanently write data from a register to the E² PROM, the host must write 0x08 to the E² PROM instruction register to accomplish this.The data in the E² PROM registers are held at power down and automatically loaded into the appropriate register location at power up. Data can also be reloaded by the host by writing 0xB6 to the E² PROM instruction register. Please note that the write operation to the E² PROM operates in 16 bytes as a whole, and you need to make sure that the contents of all 16 registers are correct before making a unified copy.

The operating status of the E² PROM is reflected in bit4 of the Status register: when the E² PROM read/write is in progress, bit4 of the Status register = 1; when the E² PROM read/write is finished, bit4 of the Status register = 0.

10.3 I² C with single bus instructions

The chip supports two communication modes: I² C and single bus. Table 10-3 shows the operation methods of the two communication modes corresponding to different functions.

Table 10-3I² C and Single Bus Function List

name (of a thing)	functionality	I² C Function Trigger	single-bus instruction
search rom	Search for romcode	-	0xF0
read rom	Read romcode	Read corresponding byte	0x33
match rom	Match rmcode	-	0x55
skip rom	Ignore romcode	-	0xCC
alarm search	Search for Alarm Chips	-	0xEC
convert temperature	measured temperature	Write Temp_Cmd (address: 0x04)	0x44
read temperature	Read two bytes of the temperature value	Read corresponding byte	0xBC
heat_on	Chip internal heating resistor on	Write Temp_Cmd (address: 0x04)	0x91
heat_off	Chip internal heating resistor off	Write Temp_Cmd (address: 0x04)	0x92
soft reset	Reset the entire chip, load the E² PROM data into the registers, the Restore other registers to their initial values at power-up	Write E² PROM_Cmd (Address: 0x17)	0x6A
break	Stop cycle measurement mode	Write Temp_Cmd (address: 0x04)	0x93
read scratchpad	Reading a scratch area	Read corresponding byte	0xBE
write config	Setting the config area	Write the corresponding byte	0x4E
read scratchpad extension	Read scratch extended area	Read corresponding byte	0xDD

write scratchpad extension	Setting the scratch extended area	Write the corresponding byte	0x77
copy page	Save register data to	Write E^2 PROM_Cmd (Address: 0x17)	0x48
recall page	Load E^2 PROM Data to Registers	Write E^2 PROM_Cmd (Address: 0x17)	0xB6
recall EE	Load all 32 bytes of E^2 PROM data into registers	Write E^2 PROM_Cmd (Address: 0x17)	0xB8

11. I² C Bus Protocol

The sensor implements the I² C bus communication interface protocol via the SDA and SCL dual pins, and can support fast modes up to 1 MHz.Each transmission sequence starts with a START condition (S) and ends with a STOP condition (P), as described in the I² C bus specification.

11.1. I² C Address

The slave I² C address bit is 0x41.

11.2. read-write function

I² C bus communication, the host first sends the slave address and the write flag bit (Slave Address + W) followed by the register logical address (Register Address) For read timing, the host then sends the Slave Address and Read Flag bit again (Slave Address + R) and then the slave sends data from Register to the host; for write timing, the host then sends data directly to the slave (Data to Register) Note that the width of the slave address is 7 bits, the write flag bit W=0, and the read flag bit R=1. The specific read/write timing diagram is as follows:

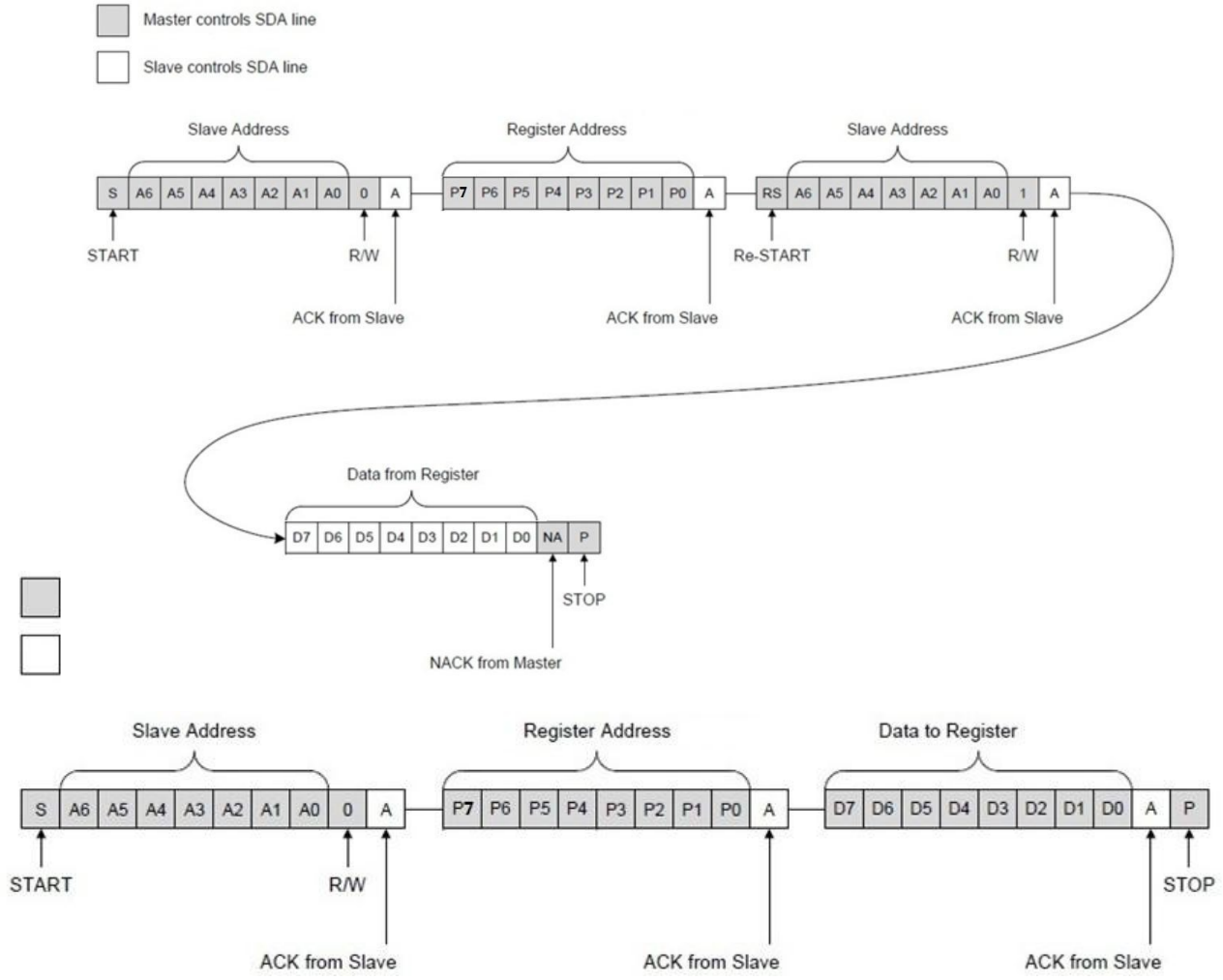


Figure 11.2-1 I² C Read Timing

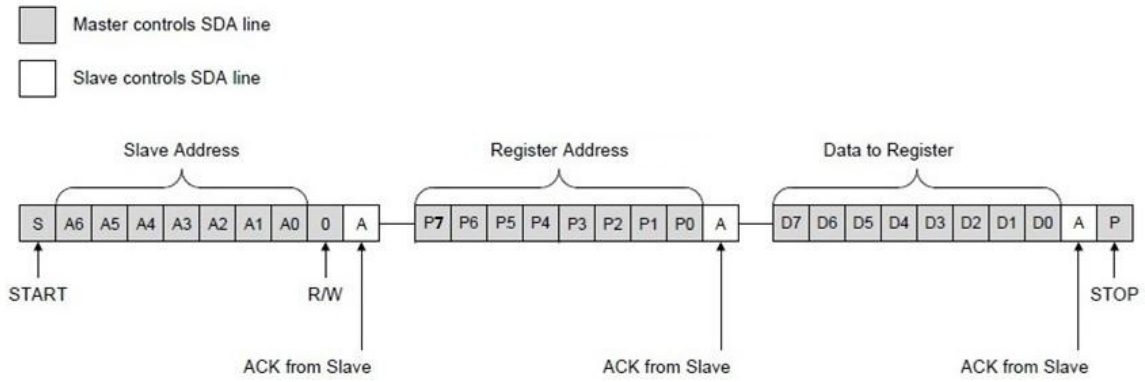


Figure 11.2-2 I² C Write Timing

For reading the low Temp_lsb and high Temp_msb of the temperature register, in order to verify the correctness of the transmitted data, the host can continue to read the Crc_temp register without sending Stop immediately after reading the data in the Temp_msb register, and then send Stop again.

11.3. I² C Timing Characteristics

Table 11.3 I² C Bus Timing Characteristics

parameters	notation	Standard Model		fast mode		unit (of measure)
		minimum value	maximum values	minimum value	maximum values	
SCL Frequency	fSCL	0	400	0	1000	kHz
SCL Low Level Time	tLOW	1300	-	400	-	ns
SCL high level time	tHIGH	600	-	450	-	ns
Duration of SCL high after SDA is pulled low at start(restart).	tHD;STA	400	-	100	-	ns
Interval from when SCL is pulled down to when SDA data is changed	tHD;DAT	0	0.9	0	-	μs
Interval from the start of SDA data stabilization to SCL pull up	tSU;DAT	100	-	50	-	ns
Hold high time of SCL before SDA pulls down at restart.	tSU;STA	400	-	150	-	ns
Interval from SCL to SDA pull-up at stop	tSU;STO	400	-	100	-	ns
Interval between start and stop	tBUF	1300	-	500	-	ns
SCL/SDA Time required for rising edge	tRC	20+0.1 C_b (1)	1000	20+0.1 C_b (1)	50	ns
Time required for SCL/SDA falling edge	tFC	20+0.1 C_b (1)	300	20+0.1 C_b (1)	100	ns

NOTE 1: Cb = I² Total capacitance of the C bus in pF.

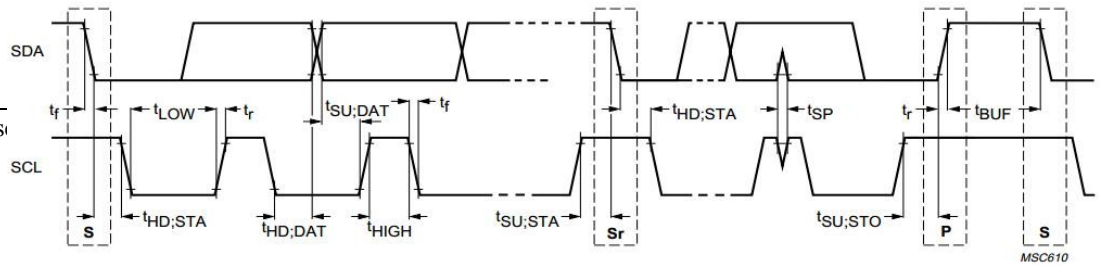


Figure 11.3 I² C Timing Parameters

12. single-bus system

MTS4, MTS4B default IO is I²C interface, through the mode register Mode_Cfg (0X68) write 10101010, I/O can be changed to a single-bus interface, at this time the SDA is a single-bus DQ. after switching modes need to be sent to the Copy EEPROM command for power-down preservation, the command can be contacted with the manufacturer to obtain.

Single bus systems use a single signal line with a master controlling one or more slave devices. Sensors are always slave devices. When there is only one slave device on the bus, the system is referred to as a "single-point" system; when there are multiple slave devices on the bus, it is referred to as a "multipoint" system. All data and instruction transfers a single bus start at the lowest bit. The following description of a single-bus system is divided into three topics: hardware configuration, transmission sequences, and single-bus signaling (signal types and timing)

12.1 Hardware configuration

By definition, a single bus has only one data line. Each device (master or slave) is connected to the data line through an open-drain or tri-state port. This allows the device to "free" the data line when no data is being transferred, and thus the bus is available to other devices.

The internal equivalent circuit of the sensor's single bus port (DQ pin) is an open drain as shown in Figure 12.1. The single bus requires an external pull-up resistor of approximately 4.7 kΩ so that the idle state of the single bus is high. If for any reason a transmission needs to be paused, the bus must remain idle until the transmission returns. During resume, the resume time between data bits can be infinitely long as long as the single bus remains in the inactive (high) state. If the bus is pulled low for more than 480 μs, all devices hanging on the bus will be reset.

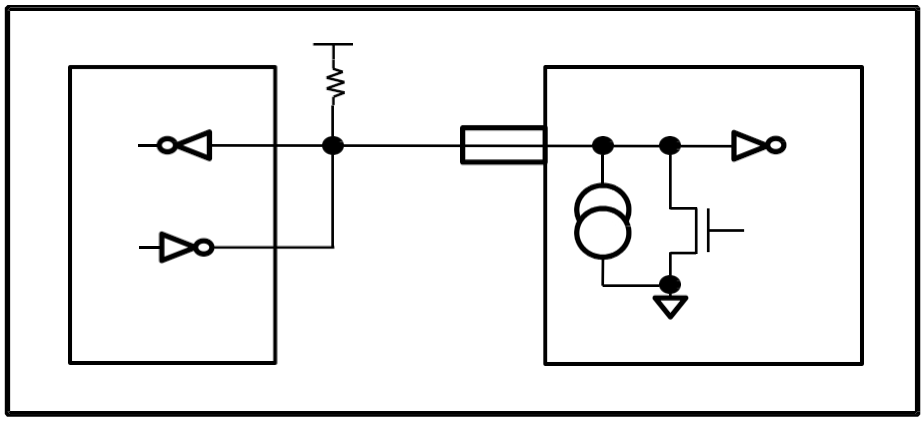


Figure 12.1 Single Bus Hardware Configuration

12.2 transmission sequence

The transmission sequence for accessing the sensor is as follows: Step 1 Initialization

Step 2 ROM instruction (follows any required data exchange)

Step 3 Sensor function command (following any necessary data exchange)

It is important to ensure this sequence every time the sensor is accessed, as any steps missing or in the wrong

order will result in the sensor not responding. The only exceptions are the Search ROM [F0h] and Alarm Search [ECh] commands. When these ROM instructions are issued, the host must return to step 1 in the sequence.

12.3 initialization

All execution (processing) over a single-wire bus begins with an initialization sequence. The initialization sequence consists of a reset pulse issued by the bus controller followed by a presence pulse issued by the slave. The presence pulse lets the bus host know that the slave device is on the bus and ready to operate. The timing of the reset and presence pulses is detailed in the Single Bus Signal Timing section.

12.4 ROM operation commands

When the bus host detects the presence of a pulse, it can issue ROM instructions. These instructions operate on a 64-bit ROM code unique to each slave device and allow the host to address specific slaves individually if there are multiple slaves hooked up to a single bus. These instructions also allow the host to determine how many of what type of devices are on the bus and whether any of the devices meet the alarm conditions. There are five ROM instructions, each 8 bits long. The master must issue an appropriate ROM instruction before issuing a functional instruction for the sensor.

SEARCH ROM [F0h]

When a system is initialized and powered up, the host must identify the ROM codes of all slave devices on the bus so that the host can determine the number and type of slave devices. The host recognizes the ROM codes through a process of elimination, which requires the host to execute a Search ROM loop (e.g., the Search ROM instruction follows the data exchange) repeatedly until all slaves are recognized. If there is only one slave device on the bus, a simple Read ROM (below) instruction can be used instead of the Search ROM instruction. After each Search ROM cycle, the bus host can return to step 1 (initial state) of the transfer sequence or follow a functional instruction.

Read ROM [33h]

This instruction allows the bus host to read the 64-bit ROM code of the sensor. This instruction can only be used if there is a single sensor on the bus. If there is more than one slave on the bus, a data conflict will occur when all slaves attempt to respond at the same time.

Match ROM [55h]

Matching ROM instructions, followed by a 64-bit ROM code sequence, allow the bus host to address a specific sensor on a multipoint or single-point bus. Only

Only sensors with an exact match of the 64-bit ROM code sequence will respond to a function command from the master. All other slaves will wait for a reset pulse.

Skip ROM [CCh]

This instruction allows the host to address all devices on the bus simultaneously without sending any ROM codes. For example, the host can cause all sensors on the bus to perform a temperature conversion at the same time by issuing a Skip ROM instruction followed by a Convert T [44h] instruction.

Note that the Read Scratchpad [BEh] instruction can only follow the Skip ROM instruction if a single slave device is hooked up to the bus. In this case, time can be saved by allowing the master to read the slave without sending the 64-bit device ROM code. If there is more than one slave device on the bus, a Skip ROM instruction following a Read Scratchpad instruction will result in a data conflict because multiple devices will attempt to transmit data at the same time.

Alarm Search [ECh]

The flowchart for this instruction is the same as for Search ROM; however, only sensors that have the alarm flag bit set will respond to this instruction. This

The command allows the host device to know if any of the sensors reached a temperature alarm condition at the most recent temperature transition. After each Alarm Search cycle (e.g., the Alarm Search instruction follows a data exchange), the bus host can return to Step 1 (Initialization) of the transfer sequence or follow a functional instruction. The Operation-Alarm Signaling section explains the operation of the Alarm Flag bit.

12.5 functional instruction

When a bus host addresses a sensor it wishes to communicate with using a ROM instruction, the host can issue one of the sensor's functional instructions. These instructions allow the host to write or read data from the sensor's register, initiate temperature conversions, and understand the power supply mode. The sensor's functional instructions, described below, are summarized in Table 12.5.

CONVERT TEMPERATURE [44h]

This instruction initiates a temperature conversion. After the conversion, the collected temperature data is stored in the first two bytes of the temperature register, and then the sensor will enter a low power state. The host can issue a read time slot after the Convert Temperature instruction and the sensor will respond with a 0 or 1 to indicate that the temperature conversion is in progress or has completed.

read temperature [bkh]

This instruction allows the host to read the contents of the temperature value register. The data transfer begins with the lowest bit of byte 0x00 and continues by traversing the register until byte 0x02 (Temperature Cyclic Redundancy Verification Code) is read. after all 3 bytes have been read, the sensor enters low power mode by default.

WRITE CONFIG [4Eh]

This instruction allows the host to write up to 7 bytes of data to the sensor register. The data transfer begins at the lowest bit of byte 0x04 and continues traversing the register until the highest bit of byte 0xA. All 7 bytes must be written before the host sends a reset signal or the data may be corrupted(This means that the host can abort the write at any time with a reset)

read scratchpad [beh]

This instruction allows the host to read the contents of the Scratch register. The data transfer begins at the lowest bit of byte 0x03 and continues by traversing the register until byte 0xB (Scratch Cyclic Redundancy Verification Code) is read. 9 bytes are read and the sensor enters a low power mode by default. If only a portion of the data in the register is needed, the host can terminate the read at any time by issuing a reset signal.

WRITE SCRATCH_EXTENSION [77h]

This instruction allows the host to write up to 10 bytes of data to the sensor register. The data transfer begins at the lowest bit of byte 0xC and continues traversing the register until the highest bit of byte 0x15. All 10 bytes must be written before the host signals a reset or the data may be corrupted. (This means that the host can abort the write at any time with a reset)

READ SCRATCH_EXTENSION [DDh]

This instruction allows the host to read the contents of the Scratch Extension register. The data transfer begins with the lowest bit of byte 0xC and continues by traversing the register until byte 0x16 (the Scratch Extension Cyclic Redundancy Verification Code) is read. 11 bytes are read, and the sensor enters a low-power mode by default. If only a portion of the data in the register is needed, the host can terminate the read at any time by issuing a reset signal.

COPY PAGE [48h]

This instruction copies 16 bytes of data from the register to the E² PROM (see Table 10.1 for correspondence)

RECALL PAGE [B6h]

This instruction loads 16 bytes of data from the E² PROM into the register (see Table 10.1 for correspondence) The host device can follow the RECALL PAGE instruction by issuing successive read time slots, and then the sensor indicates the status of the load, transmitting a 0 to indicate that the load is in progress, or a 1 to indicate that the load is complete.

RECALL EE [B8h]

This instruction loads all 32 bytes of data from the E² PROM into the register (see Table 10.1 for correspondence) The host device can follow the RECALL EE instruction with successive read slots, and the sensor will then indicate the status of the load, transmitting a 0 to indicate that the load is in progress, or a 1 to indicate that the load is complete. This load is performed automatically at power-up, so the sensor will have valid data in its registers immediately after power-up.

Table 12.5 Temperature Sensor Function Instruction Set

directives	descriptive	protocols	Activity on the single bus after the command is issued	note
Temperature conversion command				
Convert Temperature	Initiate temperature conversion	44h	The sensor transmits the transition status to the host: a read time slot result of 0 is busy; is 1, the conversion is complete	
read and write commands				
Read Temperature	Read temperature two bytes + cyclic redundancy check	BCh	Sensor transmits 2 bytes of temperature value + CRC to host	
Read Scratchpad	Read all Scratch register contents + cyclic redundancy calibration	BEh	Sensor transmission 8 bytes + CRC host	(1)
Write Scratchpad	Write data to Scratch register	4Eh	Host Transmission 7 Byte Sensor	(2)
Read scratchpad extension	Read all Scratch extended registers + cyclic redundancy check	DDh	The sensor transmits up to 11 bytes to the host	(1)
Write scratchpad extension	Write Data to Scratch Extended Register Contents	77h	Host transmits 10 bytes of data from the expansion register to the sensor.	(2)
Break	Stop continuous measurement mode	93h	not have	
Copy Page	Copy 16 bytes of data from register to E² PROM	48h	Write E² PROM Time 40ms	
Recall Page	Load 16 bytes of data from E² PROM to registers	B6h	The sensor transmits the call status to the master crucial point	
Recall EE	Load all 32 bytes of data from the E² PROM and send to depositor (computing)	B8h	The sensor transmits the call status to the master crucial point	

chip instruction				
Soft Reset	Reset chip, load E^2 PROM data to register device, restores other registers to their initial values at power-up	6Ah	not have	
Heat_On	Chip internal heating resistor on	91h	not have	
Heat_Off	Chip internal heating resistor off	92h	not have	

NOTE 1: The host can interrupt the data transfer at any time by issuing a reset signal. Note 2: All bytes must be written before the reset signal is issued.

12.6 Single Bus Signal Timing

The sensor uses a strict single bus communication protocol to ensure data integrity. The protocol defines several signaling types: Reset Pulse, Presence Pulse, Write 0, Write 1, Read 0, Read 1. With the exception of the Presence Pulse, all signaling is initiated by the bus host.

Initialization program - reset and presence pulse

All communication with a sensor begins with an initialization sequence that consists of a reset pulse from the host following a presence pulse from a sensor. Figure 12.6-1 explains this sequence. When a sensor sends a presence pulse in response to a reset pulse, it indicates to the host that it is hooked up to the bus and is ready to operate. During the initialization sequence, the host sends a reset pulse by pulling the single bus down for at least 480µs. The bus host then releases the bus into receive mode. When the bus is released, a pull-up resistor pulls the bus high. When the sensor detects this rising edge, it waits 15µs to 60µs and then issues a presence pulse by pulling the single bus down 60µs to 240µs.

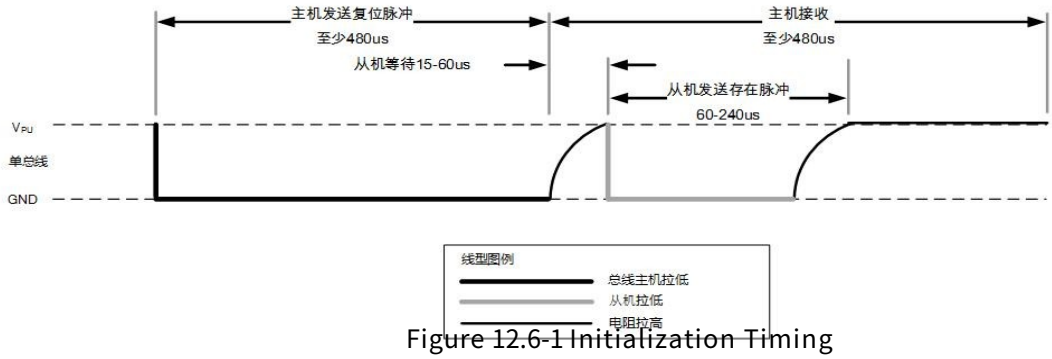


Figure 12.6-1 Initialization Timing

Note: If the power supply voltage of the chip is 1.75V ~ 1.85V, please be careful to extend the reset low level (Reset) to 2000us in order to ensure stable communication.

Read/Write Time Slot

The bus host writes data to the sensor in write time slots and reads data from the sensor in read time slots. Each time slot transfers one data bit on a single bus.

Write Time Slot

There are two write time slots: the "Write 1" time slot and the "Write 0" time slot. The bus host writes a logic 1 to the sensor via the Write 1 time slot and logic 0 to the sensor via the Write 0 time slot. All write time slots must last a minimum of 60µs with a minimum 1µs recovery time between write time slots. Both write time slots are initiated by the host pulling the single bus low (see Figure 12.6-2)

To generate a write 1 time slot, the bus host must release the single bus within 15µs after pulling the single bus low. After the bus is released, the pull-up resistor pulls the bus high. To generate a Write 0 time slot, after pulling the single bus low, the bus host must keep the bus low continuously (at least 60µs) for the entire time slot.

The sensor samples a single bus in a time window of at least 15µs to 60µs after the host initiates a write time slot. If the bus is high during this sampling time window, a 1 is written to the sensor. If the bus is low, a 0 is written to the sensor.

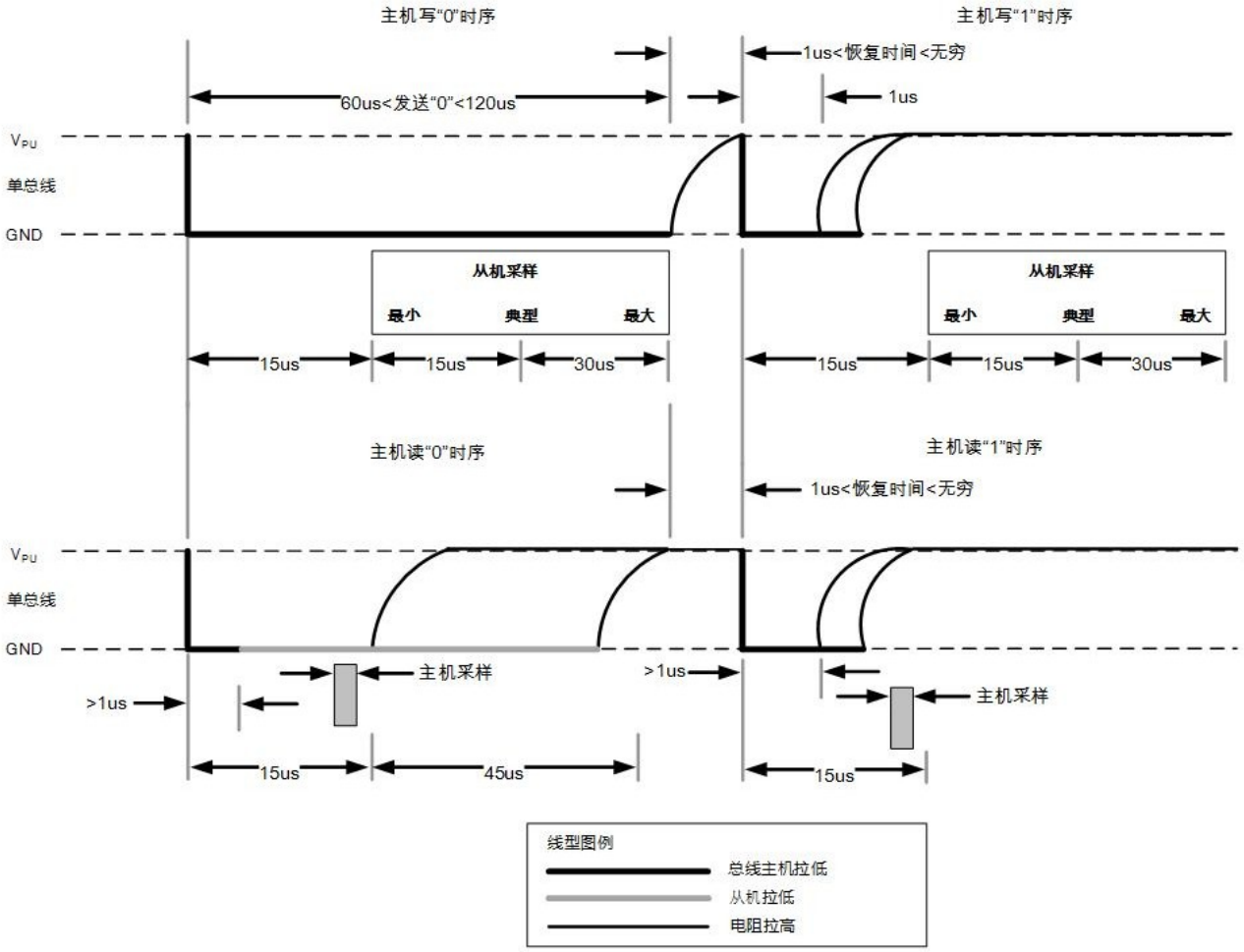


Figure 12.6-2 Read/Write Time Slot Timing

read a time slot

The sensor can only transmit data to the host during the time the host issues a Read Scratchpad. All, the host must generate a read time slot immediately after issuing a Read Scratchpad [BEh] instruction so that the sensor can provide the requested data. Alternatively, the host can generate a read time slot after issuing a Convert T [44h] or Recall E2 [B8h] instruction for operational status. This part of the mechanism is explained in detail in the Sensor Function Instructions section. All read slots must last at least 60µs with a recovery time of at least 1µs between writes. read slots are generated by the host pulling down a single bus for at least 1µs and then releasing the bus (see Figure 12.6-2) After the host initiates a read time slot, the sensor will begin transmitting a 1 or 0 on the bus. the sensor sends a 1 by holding the bus high and a 0 by pulling the bus low. when transmitting a 0, the sensor releases the bus at the end of the time slot, and the bus is pulled back to the high idle state by the pull-up resistor. the sensor's output data will be returned to the high idle state at the end of the time slot. The sensor's output data is valid for 15µs after the falling edge of the startup time slot. Therefore, the host must release the bus and sample the bus state within 15µs of the startup time slot. Figure 12.6-3 illustrates that the sum of t_{INIT} , t_{RC} , and t_{SAMPLE} must be less than 15µs in a read time slot. Figure 12.6-4 shows that the system's time margin can be maximized by keeping t_{INT} and t_{RC} as short as possible and by placing the host sample time at the end of the 15µs period of the read time slot.

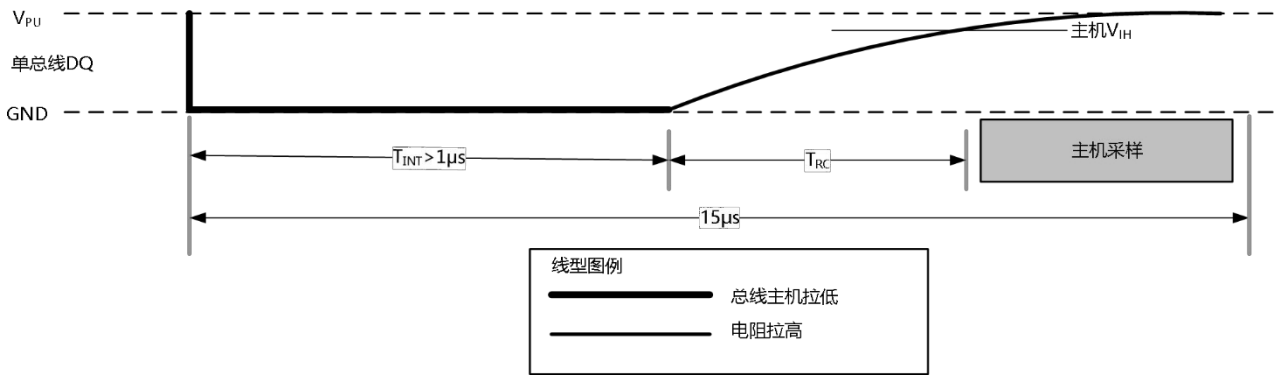


Figure 12.6-3 Detailed Host Read 1 Timing Sequence

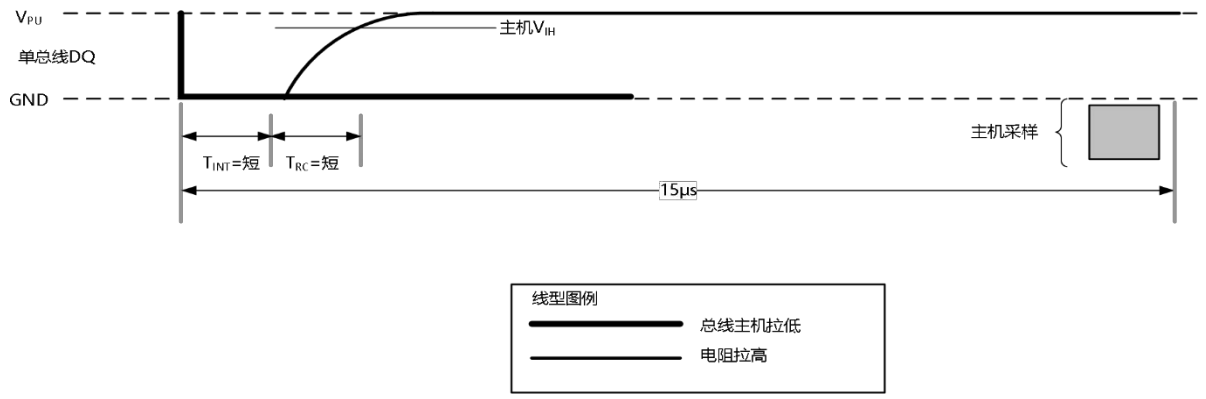


Figure 12.6-4 Recommended Timing for Host Read 1

12.7 Temperature Sensor Operation Example 1

In this example there are multiple sensors on the bus. The bus host reads its buffer after initiating a temperature conversion for a particular sensor and then recalculates the cyclic redundancy checksum to validate the data.

Host Mode	Data (lowest first)	directives
dispatch	reset (a dislocated joint, an electronic device etc)	Host sends reset pulse
reception (of transmitted signal)	remain	The sensor responds by the presence of impulses
dispatch	55h	Host sends Match ROM command
dispatch	64-bit ROM encoding	Host sends sensor ROM code
dispatch	44h	Host sends Convert T command
	DQ line stays high	Mainframe keeps DQ high during temperature transition times
dispatch	reset (a dislocated joint, an electronic device etc)	Host sends reset pulse
reception (of transmitted signal)	remain	The sensor responds by the presence of impulses
dispatch	55h	Host sends Match ROM command
dispatch	64-bit ROM encoding	Host sends sensor ROM code
dispatch	BCh	Host sends Read Temperature command

reception (of transmitted signal)	3 data bytes	The host reads the entire register including the cyclic redundancy check. The host then recalculates the register The cyclic redundancy check of the first 2 bytes of the data is compared to the cyclic redundancy check of the read (word).

		Section 3) for comparison. If it matches, the host continues; otherwise, the entire read operation is repeated

12.8 Temperature Sensor Operation Example 2

In this example there is only one sensor on the bus. The host writes data including Tha_Set_lsb, Tla_Set_lsb, Tha_Set_msb, and Tla_Set_msb to the sensor register. The host then copies the contents of the staging and extended staging registers to the E^2 PROM.

Host Mode	Data (lowest first)	directives
dispatch	reset (a dislocated joint, an electronic device etc)	Host sends reset pulse
reception (of transmitted signal)	remain	The sensor responds by the presence of impulses
dispatch	CCh	Host sends Skip ROM command
dispatch	4Eh	Host sends Write Scratchpad command
dispatch	7 data bytes	The host sends 7 data bytes to the staging area (including Tha_Set_lsb, Tla_Set_lsb, Tha_Set_msb and Tla_Set_msb-)
dispatch	reset (a dislocated joint, an electronic device etc)	Host sends reset pulse
dispatch	remain	The sensor responds by the presence of impulses
dispatch	CCh	Host sends Skip ROM command
dispatch	48h	Host sends Copy Page0 command
dispatch	DQ line stays high	The host keeps the DQ high for at least 40ms during a copy operation.

12.9 Single Bus Timing Characterization

parameters	notation	prerequisite	minimal	typical case	greatest	unit (of measure)
slot length	tSLOT	See Remarks	60		120	µs
recovery time	tREC	See Remarks	1	5		µs
Write 0 Low Time	tLOW0	See Remarks	60	60	120	µs
Write 1 Low Time	tLOW1	See Remarks	1	5	15	µs
Read Data Valid Time	tRDV	See Remarks		5	15	µs
Reset Low Time	tRSTL	See Remarks	480	960		µs
Presence detection high level time	tPDHIGH	See Remarks	15	30	60	µs
Presence detection low level time	tPDLOW	See Remarks	60	115	240	µs

Note: See Figure 12.9 below for more information on time slots.

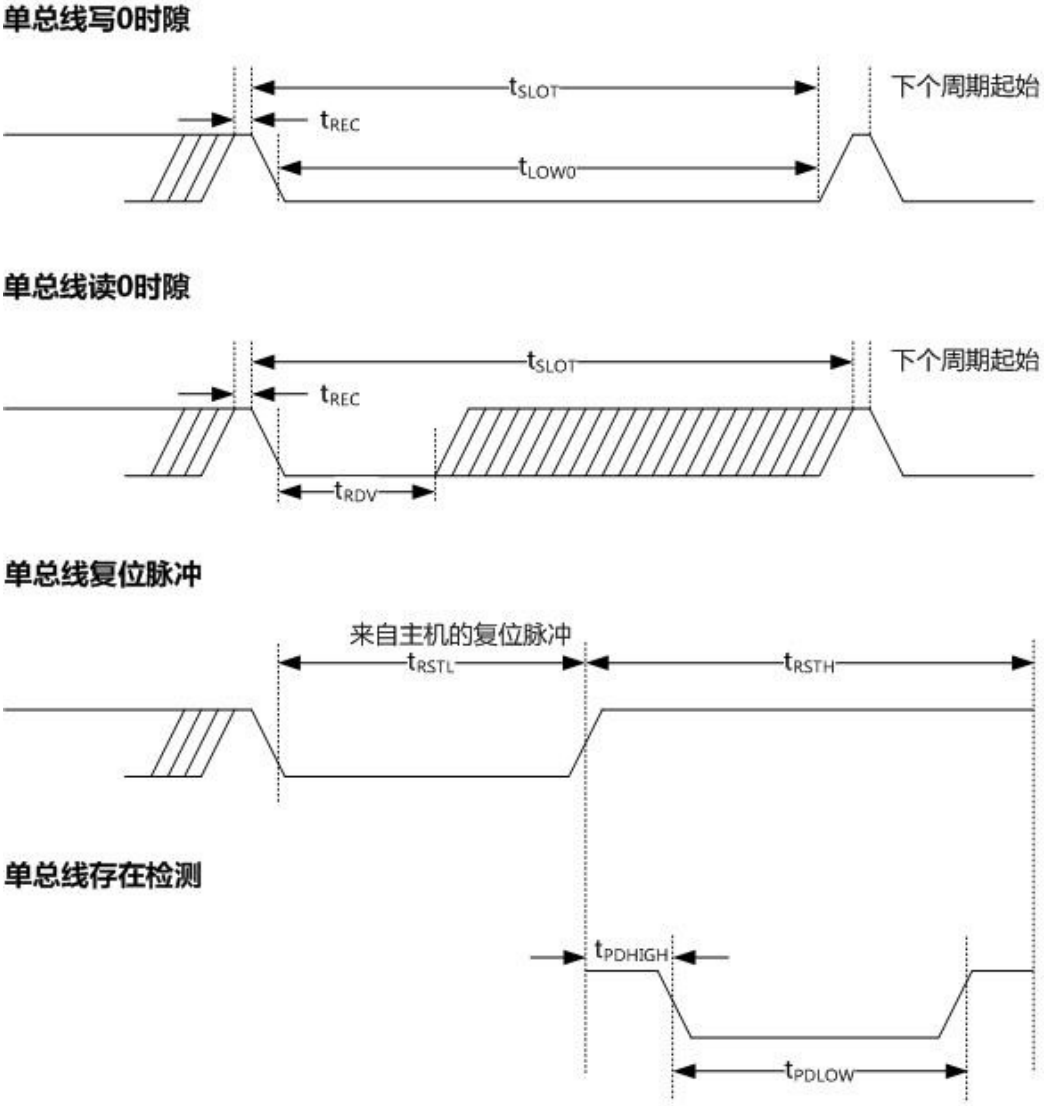
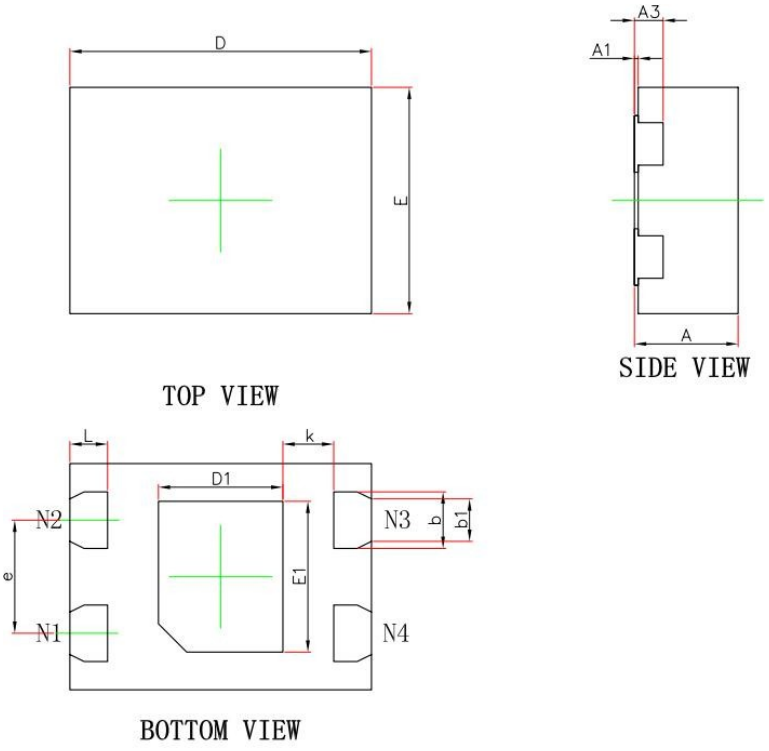


Figure 12.9 Time-slot diagram

13. package diagram



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.152REF.		0.006REF.	
D	1.500	1.700	0.059	0.067
E	1.100	1.300	0.043	0.051
D1	0.560	0.760	0.022	0.030
E1	0.700	0.900	0.028	0.035
b	0.250	0.350	0.010	0.014
b1	0.175	0.275	0.007	0.011
e	0.600TYP.		0.024TYP.	
L	0.150	0.250	0.006	0.010
k	0.200MIN.		0.008TYP.	

Figure 12 Package Dimensions DFN4L (1.6X1.2X0.55mm)