DIR-V GRAND CHALLENGE

VEGA Processor Tutorial

Centre for Development of Advanced Computing(C-DAC)

Oct 22, 2025

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Introduction to C-DAC & VEGA Processors

Centre for Development of Advanced Computing (C-DAC)

About C-DAC

Premier R&D organization of the Ministry of Electronics and Information Technology (MeitY) for carrying out R&D in IT, Electronics and associated areas


High Performance Computing


Quantum Computing

AI and Multilingual Computing


Software Technologies


Health Informatics


Education and Training


Strategic Electronics


Cyber Security and Forensics

Digital India RISC-V (DIR-V) Program

- Launched by Ministry of Electronics and Information Technology (MeitY)
- Aligned with “Atmanirbhar Bharat” vision – promoting indigenous semiconductor capability
- Objective is to Develop advanced microprocessors within India for both domestic and global markets
- Focus Areas:
  - Achieving high-quality silicon production
  - Gaining industry recognition through successful designs
  - Building a sustainable RISC-V ecosystem in India
- Key Outcome:
  - C-DAC developed a series of indigenous microprocessors under the brand “VEGA Processors” as part of the DIR-V initiative

RISC-V Architecture

- RISC-V is an open-source implementation of RISC based Instruction Set Architecture (ISA)
- Open-source and royalty-free: Specifications are freely available without any licensing fees to academia and industry
- Standardized base ISA
  - RISC-V provides a standardized base ISA, which includes a minimal set of instructions
- Extensibility: RISC-V supports
  - Standardized extensions - Provides additional instructions to the base ISA, allowing for specialized processing that can improve performance in specific applications
  - User-defined custom extensions - Allows for the addition of new instructions (new opcode fields) without changing the core ISA

DIR-V VEGA Processor

- Series of High-performance CPUs
- Fully compliant with the RISC-V ISA
- 32/64 bit, single/Multi core, In-Order/ Out-of-Order CPU variants
    - India's First Indigenous 64-bit Multi-core Out-of-Order Superscalar Processor
- Customizable to suit different application domains
- Integrated Multi level MMU, L1 and L2 caches
- AXI4 bus interface
- Linux / Zephyr / FreeRTOS capable

VEGA Processors

Overview

VEGA ET1031	VEGA AT1051	VEGA AS1061	VEGA AS1161	VEGA AS2161	VEGA AS4161
• 32-bit • Single Core • RV32IM • 3-Stage Pipeline • In-Order	• 32-bit • Single Core • RV32IMA • 5-Stage Pipeline • In-Order	• 64-bit • Single Core • RV64IMAFDC • 6-Stage Pipeline • In-Order	• 64-bit • Single Core • RV64IMAFD • 16 Stage Pipeline • Out-of-Order Superscalar	• 64-bit • Dual Core • RV64IMAFD • 16 Stage Pipeline • Out-of-Order Superscalar	• 64-bit • Quad Core • RV64IMAFD • 16 Stage Pipeline • Out-of-Order Superscalar

VEGA SoC ASIC

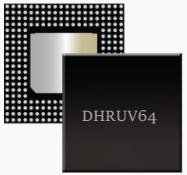
Overview

THEJAS32 Single Core SoC

Silterra 130 nm

THEJAS64 Single Core SoC

SCL 180 nm



DHRUV64 Dual Core SoC

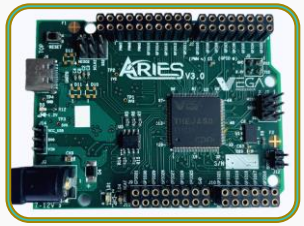
TSMC 28 nm

DHANUSH64 Quad Core SoC

TSMC

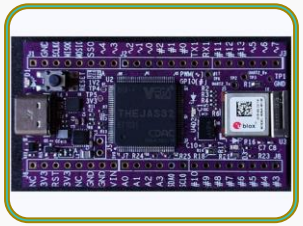
ARIES Boards

Overview

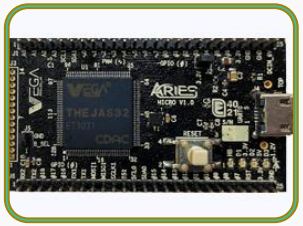


ARIES V3

ARIES Eco



ARIES Nova

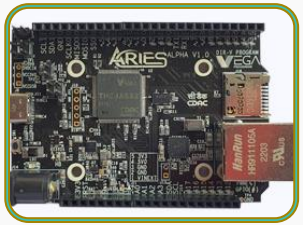


ARIES Micro

ARIES IoT

ARIES V2

ARIES Dot



ARIES Alpha

BUY

amazon

ROBU.IN
Your Ideas, Our Parts

VEGA PROCESSOR

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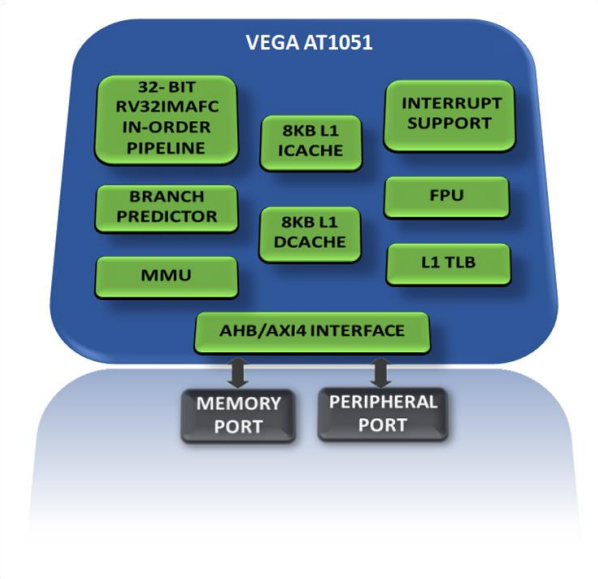
VEGA Processor Tutorial

VEGA TRISUL32 SoC Architecture

Centre for Development of Advanced Computing (C-DAC)

VEGA AT1051

- VEGA AT1051 features a 32-bit CPU IP core based on RISC-V Instruction Set Architecture
- It's capable of delivering high performance with support for single precision floating point instructions, and MMU for Linux based applications
- AT1051 has a 5-stage pipeline with branch prediction for efficient branch execution, and Instruction and Data caches
- Features include
  - PLIC and vectored interrupts for serving various types of system events
  - An AXI or AHB standard interface enables ease of system integration

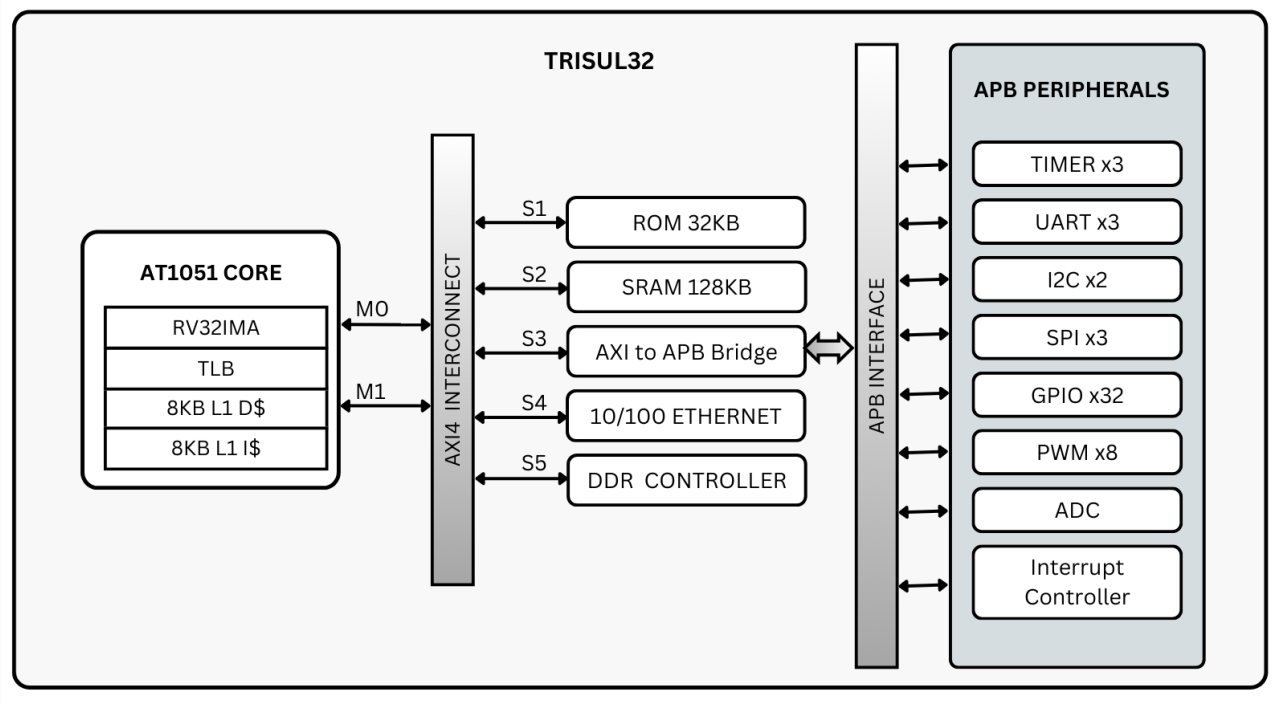


TRISUL32 SoC

- TRISUL32 is an SoC based on VEGA AT1051 Microprocessor which is a small and efficient 5-stage in-order 32-bit RISC-V processor core
- This SoC can be used to build robust systems in low power IoT domain
- The peripherals that are available in TRISUL32 SoC are
  - Interrupt Controller
  - Timers
  - RAM
  - DDR Controller
  - SPI, UART, I2C
  - GPIOs (GPIO0-GPIO32), PWM
  - ADC
  - Ethernet

TRISUL32 SoC

Block Diagram



VEGA Processor/ SoC for DIR-V Grand Challenge

VEGA AT1051	
Key Features	Details
RISC-V ISA	RV32IMA
No of cores	1
Pipeline	In-Order
Pipeline Stages	5-Stage
Processor modes	Machine/Supervisor/User
MMU	Yes
Debug	Yes
Branch Predictor	Yes
L1 ICaches	Icache 8KB, Dcache 8KB

TRISUL32 SoC	
Key Features	Details
Processor	**VEGA AT1051**
DRAM	256MB
SRAM	128KB
Ethernet	10/100
GPIO	32
Interrupt Controller	Yes
Timers	3
SPI	3
UART	3
PWM	8
I2C	2
ADC	4-channels

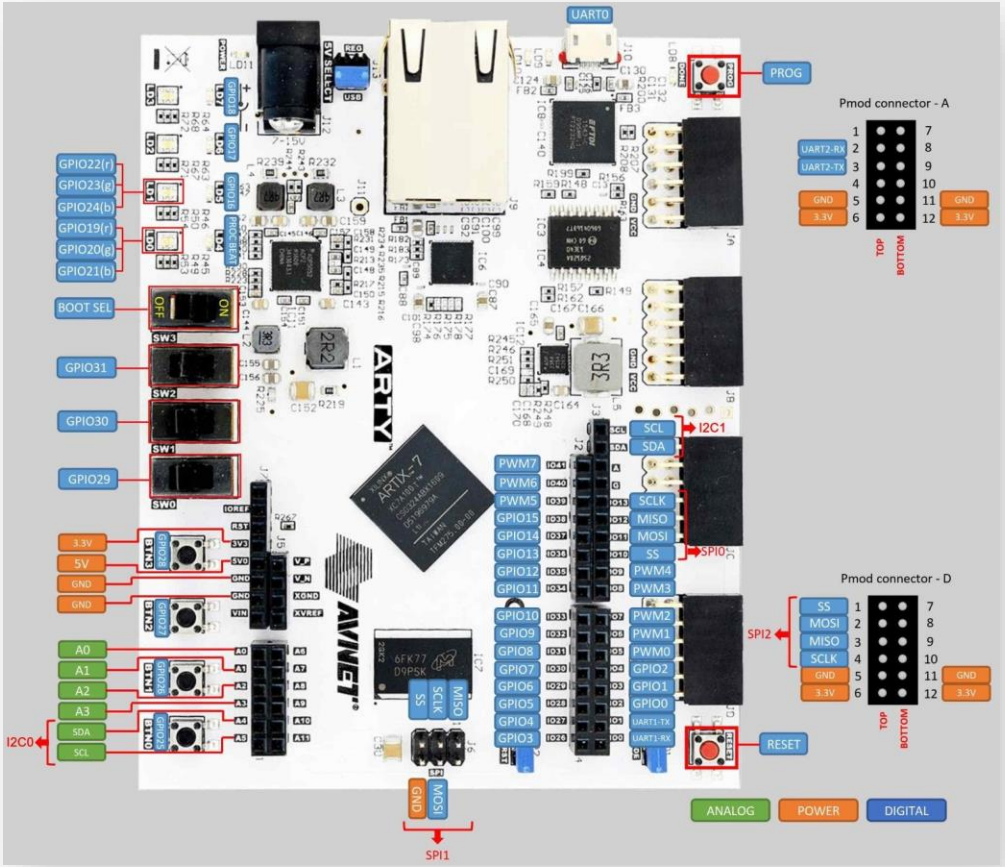
TRISUL32 SoC

Address Mapping

Peripheral	Start Address	End Address	Interrupt Number
RISC-V Debug	0x0000_0100	0x0000_0FFF	
Boot ROM	0x0001_0000	0x0001_7FFF	
Internal RAM	0x0002_0000	0x0003_FFFF	
UART0	0x1000_0100	0x1000_01FF	1
UART1	0x1000_0200	0x1000_02FF	2
UART2	0x1000_0300	0x1000_03FF	3
SPI0	0x1000_0600	0x1000_06FF	6
SPI1	0x1000_0700	0x1000_07FF	7
I2C0	0x1000_0800	0x1000_08FF	8
I2C1	0x1000_0900	0x1000_09FF	9
TIMER0	0x1000_0A00	0x1000_0A10	10
TIMER1	0x1000_0A14	0x1000_0A24	11
TIMER2	0x1000_0A28	0x1000_0A38	12
TIMERSINTSTATUS	0x1000_0AA0		
TIMERSEOI	0x1000_0AA4		
TIMERSRAWINT STATUS	0x1000_0AA8		
ADC	0x1000_1000	0x1000_1FFF	
GPIO0	0x1008_0000	0x100C_0000	20 - 36
GPIO1	0x1018_0000	0x101C_0000	
SPI2	0x1020_0100	0x1020_01FF	52
PWM	0x1040_0000	0x1040_00FF	54 - 61
PLIC	0x2001_0000	0x2001_FFFF	
ETHERNET	0x2003_0000	0x2003_FFFF	4
DRAM	0x8000_0000	0x8FFF_FFFF	

TRISUL32 SoC

Pin Mapping



Tools Installation – Ubuntu

Vivado Lab Edition :

- First the user has to create a Free Xilinx Account.
- Once the account is created, login and download Vivado Lab Edition 2018.3 (full version not required), extract the package and install as follows. Also please install dependent libraries using the below command.
  "**sudo apt install libtinfo5 libncurses5**"
  cd Xilinx_Vivado_Lab_Lin_2018.3_1207_2324
  ./xsetup
- For details about installation refer Vivado Lab Edition installation video.
  Install the Xilinx cable drivers. Goto Vivado_Lab installation directory and
  cd Vivado_Lab/2018.3/data/xicom/cable_drivers/lin64/install_script/install_drivers
  sudo ./install_drivers
  Warning
  Cable(s) on the system must be unplugged and then plugged back, in order for the driver scripts to update the cables.
- Add Vivado Lab Edition main directory path (Eg :-/home/user/Vivado_Lab) to VEGA_VIVADO_PATH variable.
  export VEGA_VIVADO_PATH=/home/user/Vivado_Lab

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VEGA TRISUL32 SoC FPGA Programming

Centre for Development of Advanced Computing (C-DAC)

Setting Up The Board

Few Selected Sensors…


IR Proximity Sensor


Bluetooth Module


Servo Motor


Passive Piezo Buzzer


RYG LED Strip


LDR Sensor


4-Digit Display


Touch Sensor


DC Relay


OLED Display


RTC


Pressure Sensor

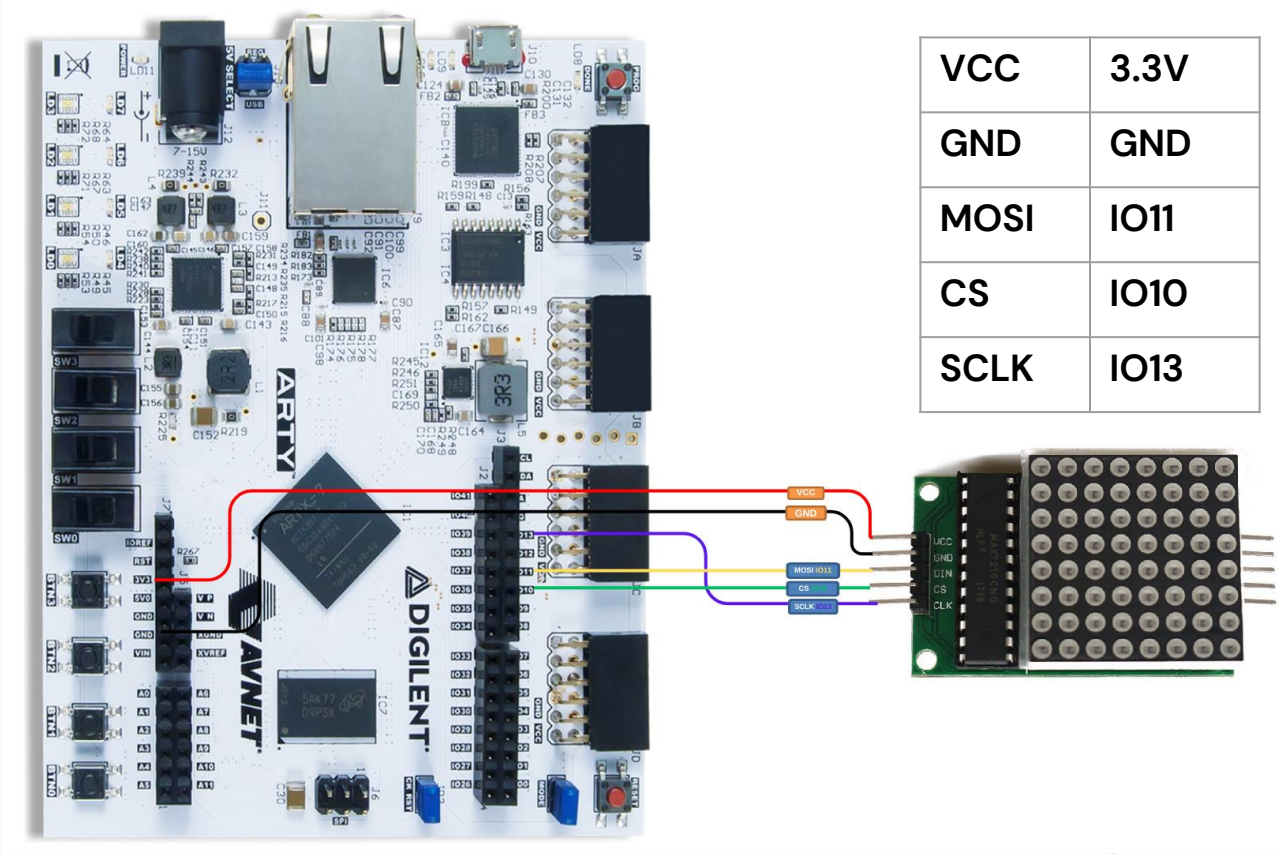

WIFI Module


RFID Module


LED Matrix

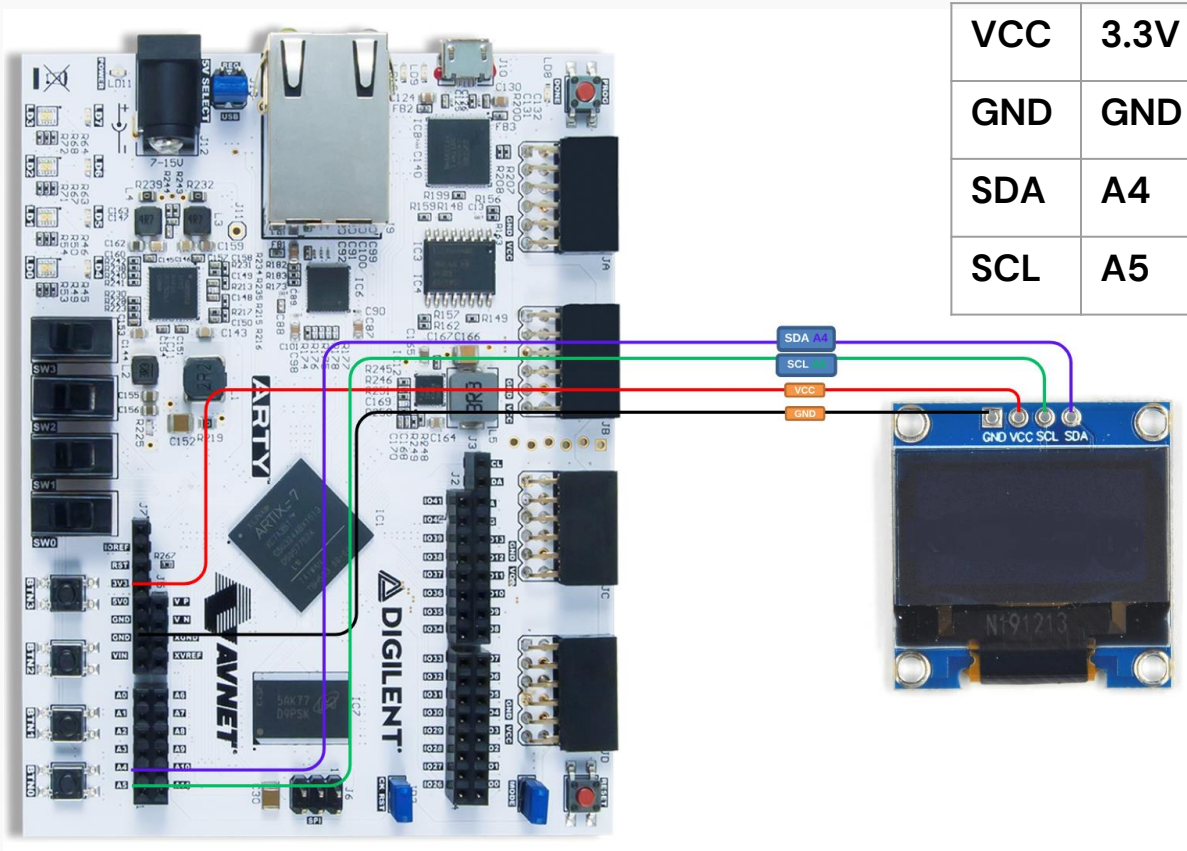
Interfacing a LED Dot Matrix using SPI

VCC	3.3V
GND	GND
MOSI	IO11
CS	IO10
SCLK	IO13



Interfacing an OLED Display using I2C

VCC	3.3V
GND	GND
SDA	A4
SCL	A5



OS Ported

Linux

NuttX RTOS

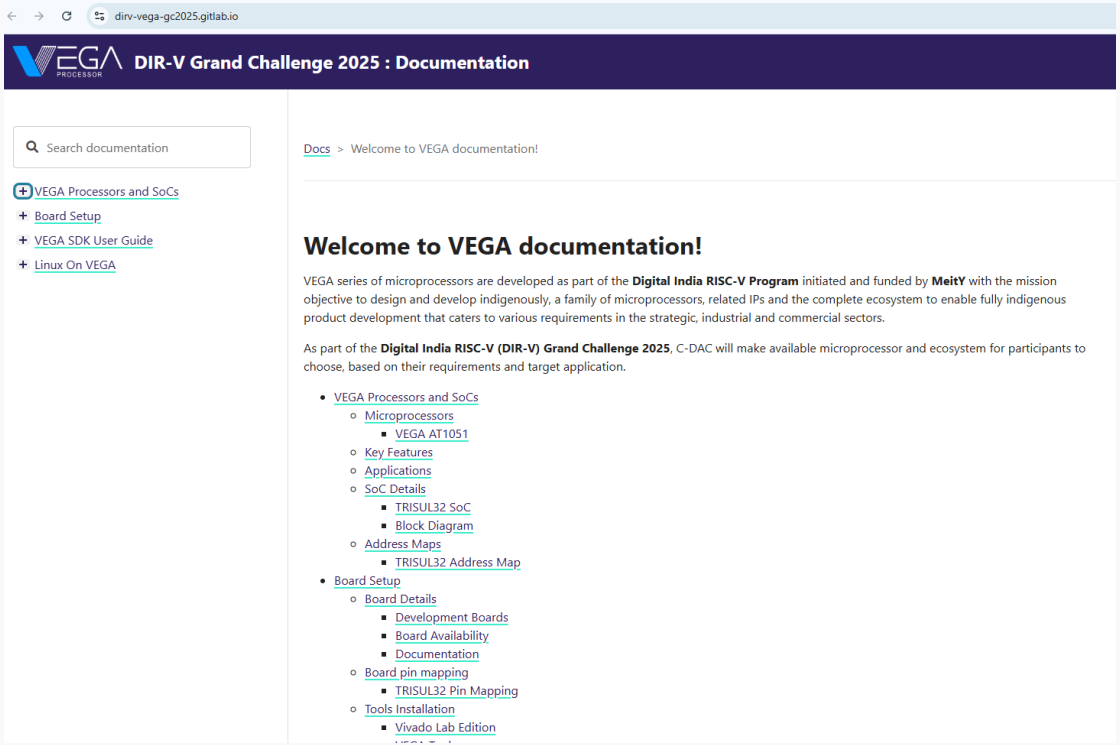
Zephyr

FREE RTOS

Applications

- Embedded & Hardware Control Applications
- Automation & Control Applications
- Monitoring & Reporting Systems
- Security & Access Control
- Network & Communication Applications

Product Development – Documentation



https://dirv-vega-gc2025.gitlab.io/

Support

GitLab https://dirv-vega-gc2025.gitlab.io/

Groups.io https://groups.io/g/vegaprocessors/

YouTube https://www.youtube.com/@VEGAProcessors

groups.io/g/vegaprocessors

https://www.youtube.com/@VEGAProcessors

https://www.linkedin.com/in/vegaprocessor/

https://x.com/vegaprocessor?lang=en

https://vegaprocessors.in/

Thank You

demo : https://www.youtube.com/watch?v=PFtjhh-8pHA

vega : https://www.youtube.com/watch?v=3OxJHEsq0W4