DIR-V GRAND CHALLENGE
Indigenous VEGA Processor based SoC Design

DDR Configuration guide for AT1051 SoC on ARTY 100T FPGA

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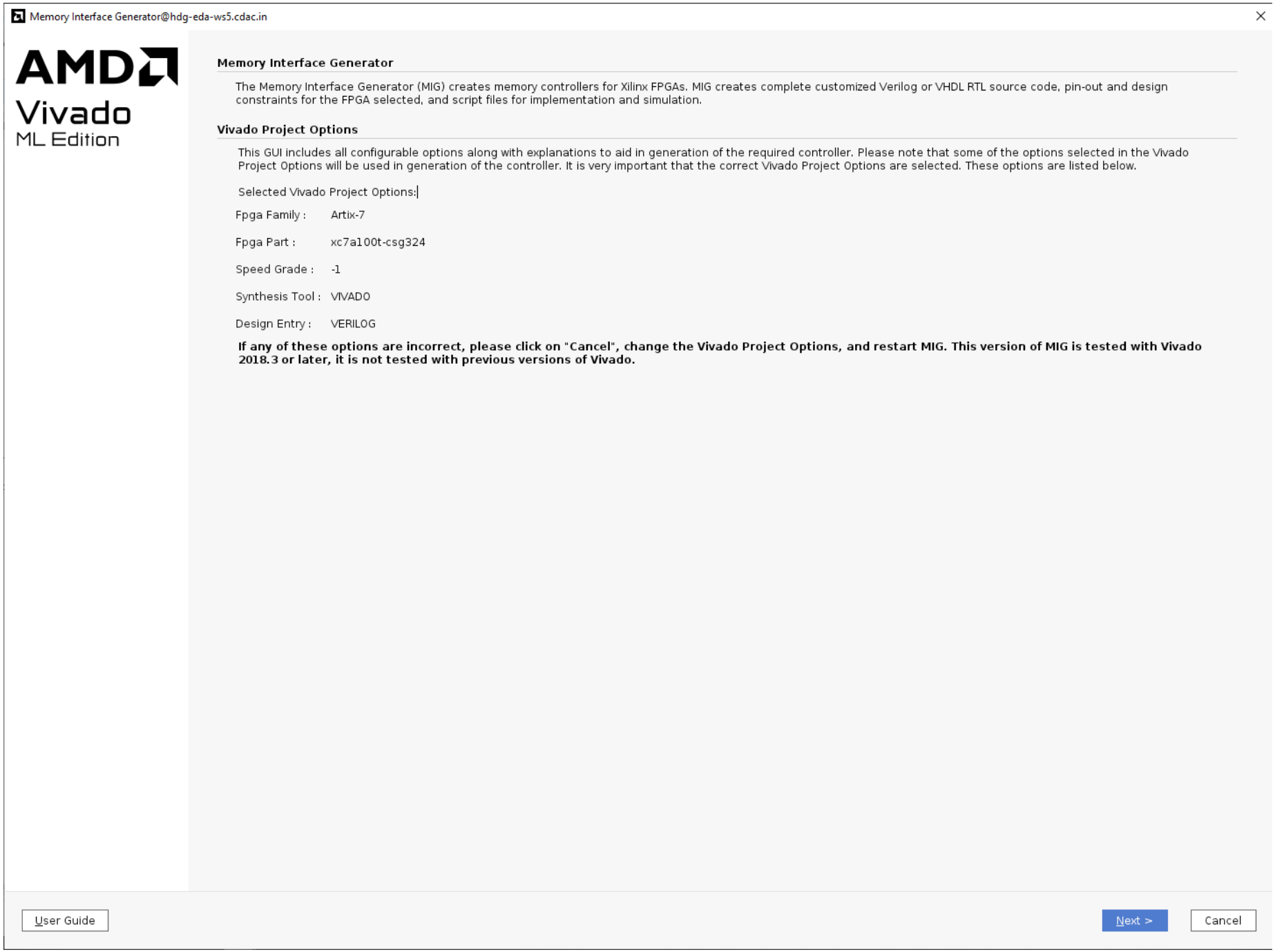
Memory Interface Generator@hdg-eda-ws5.cdac.in
AMD
Vivado
ML Edition
Memory Interface Generator
The Memory Interface Generator (MIG) creates memory controllers for Xilinx FPGAs. MIG creates complete customized Verilog or VHDL RTL source code, pin-out and design constraints for the FPGA selected, and script files for implementation and simulation.
Vivado Project Options
This GUI includes all configurable options along with explanations to aid in generation of the required controller. Please note that some of the options selected in the Vivado Project Options will be used in generation of the controller. It is very important that the correct Vivado Project Options are selected. These options are listed below.
Selected Vivado Project Options:
Fpga Family : Artix-7
Fpga Part : xc7a100t-csg324
Speed Grade : -1
Synthesis Tool : VIVADO
Design Entry : VERILOG
If any of these options are incorrect, please click on "Cancel", change the Vivado Project Options, and restart MIG. This version of MIG is tested with Vivado 2018.3 or later, it is not tested with previous versions of Vivado.
User Guide
Next >
Cancel

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MIG Output Options

Create Design
Select this option to generate a memory controller. Generating a memory controller will create RTL, XDC, implementation and simulation files.

Verify Pin Changes and Update Design
Selecting this feature verifies the modified XDC for a design already generated through MIG. This option will allow you to change the pin out and validate it instantly. It updates the input XDC file to be compatible with the current version of MIG. While updating the XDC it preserves the pin outs of the input XDC. This option will also generate the new design with the Component Name you selected in this page.

Component Name

Please specify the component name for the memory interface. The design directories will be generated under a directory with this name. Three directories will be created "example_design","user_design" and "docs". The user_design will contain the generated memory interface. The example_design adds a simple example application connected to the generated memory interface.

Component Name T1051_SOC_mig_7series_0_1

Multi-Controller

Up to maximum of 8 controllers with a combination of DDR3 SDRAM, QDRII+ SRAM or RLDRAM II can be generated. The number of controllers that can be accommodated may be limited by the data width and the number of banks available in device. Refer user guide for more information

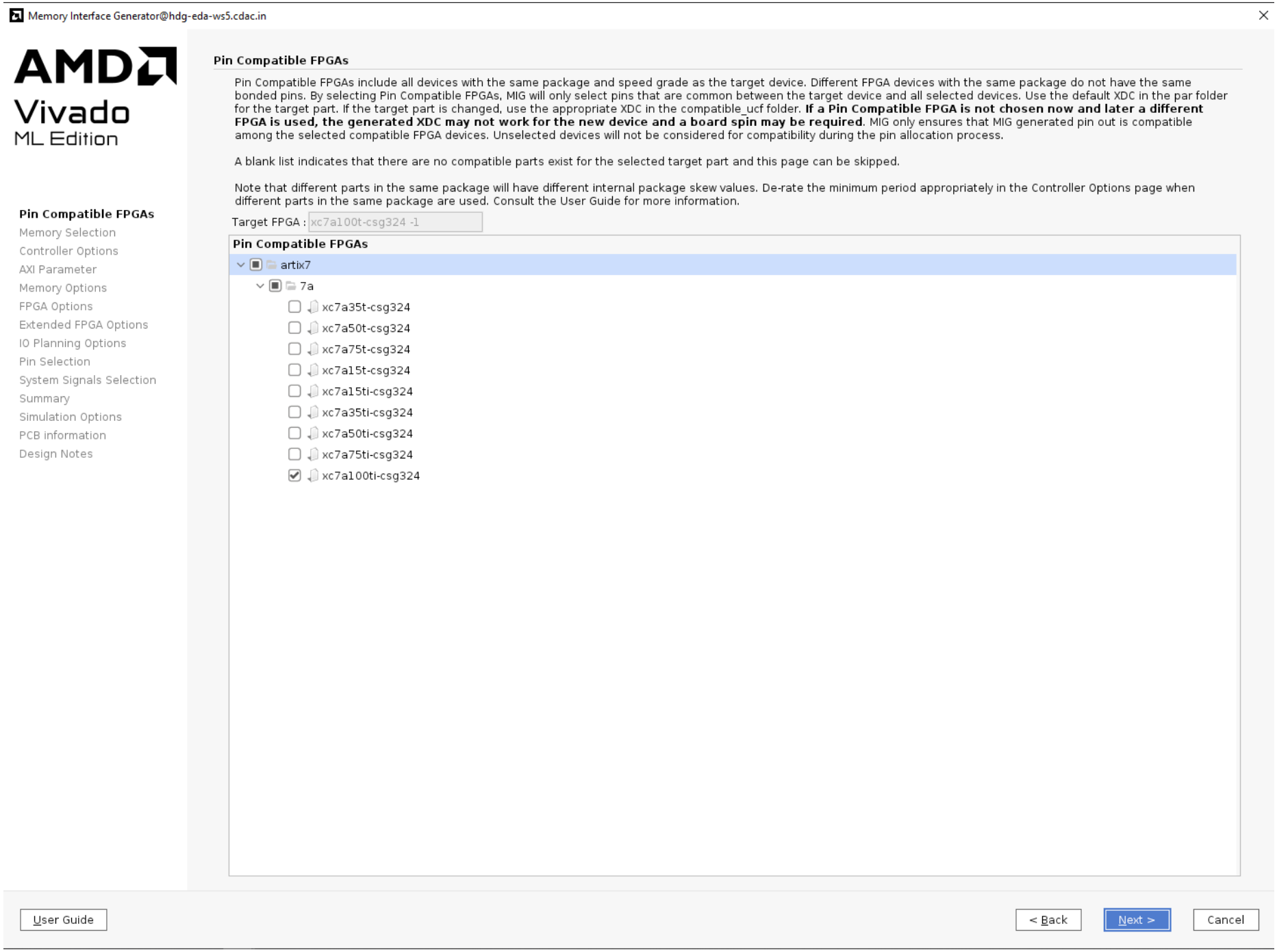
Number of controllers 1

AXI4 Interface

Enables the AXI4 interface. AXI4 interface is supported only for DDR3 SDRAM and DDR2 SDRAM controllers with Verilog design entry.

AXI4 Interface

User Guide | < Back | Next > | Cancel


Memory Interface Generator@hdg-eda-ws5.cdac.in
AMD
Vivado
ML Edition
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Pin Selection
System Signals Selection
Summary
Simulation Options
PCB information
Design Notes
Pin Compatible FPGAs
Pin Compatible FPGAs include all devices with the same package and speed grade as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. Use the default XDC in the par folder for the target part. If the target part is changed, use the appropriate XDC in the compatible_ucf folder. If a Pin Compatible FPGA is not chosen now and later a different FPGA is used, the generated XDC may not work for the new device and a board spin may be required. MIG only ensures that MIG generated pin out is compatible among the selected compatible FPGA devices. Unselected devices will not be considered for compatibility during the pin allocation process.
A blank list indicates that there are no compatible parts exist for the selected target part and this page can be skipped.
Note that different parts in the same package will have different internal package skew values. De-rate the minimum period appropriately in the Controller Options page when different parts in the same package are used. Consult the User Guide for more information.
Target FPGA : xc7a100t-csg324 -1
Pin Compatible FPGAs
artix7
7a
xc7a35t-csg324
xc7a50t-csg324
xc7a75t-csg324
xc7a15t-csg324
xc7a15ti-csg324
xc7a35ti-csg324
xc7a50ti-csg324
xc7a75ti-csg324
xc7a100ti-csg324
User Guide
< Back
Next >
Cancel

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AMD Vivado ML Edition

- Pin Compatible FPGAs
- **Memory Selection**
- Controller Options
- AXI Parameter
- Memory Options
- FPGA Options
- Extended FPGA Options
- IO Planning Options
- Pin Selection
- System Signals Selection
- Summary
- Simulation Options
- PCB information
- Design Notes

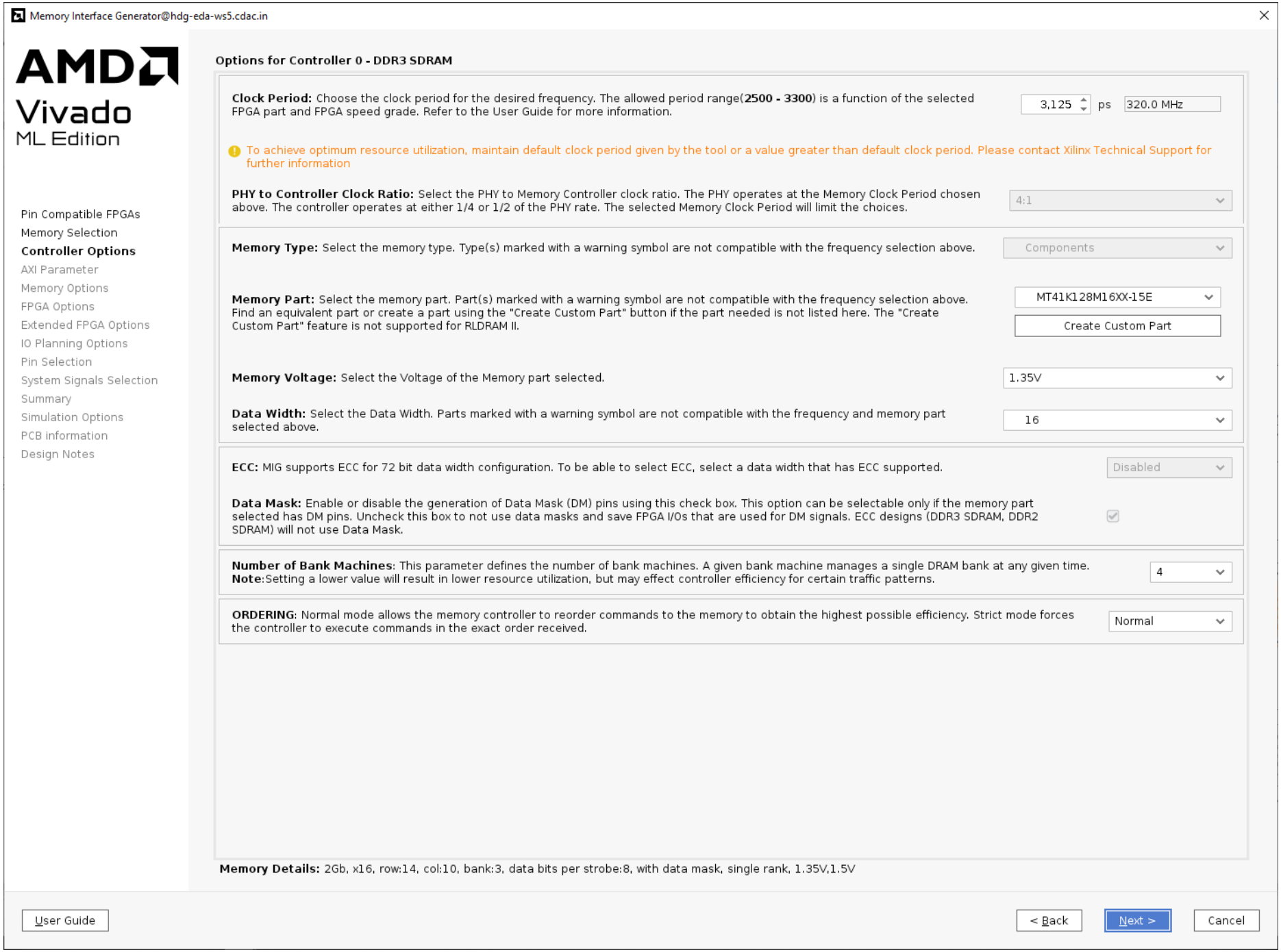
Memory Selection

Select the type of memory interface. Please refer to the User Guide for a detailed list of supported controllers for each FPGA family. The list below shows currently available interface(s) for the specific FPGA, speed grade and design entry chosen.

Select the controller type:

- (●) **DDR3 SDRAM**
- ( ) **DDR2 SDRAM**

User Guide | < Back | Next > | Cancel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AMD
Vivado
ML Edition
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Pin Selection
System Signals Selection
Summary
Simulation Options
PCB information
Design Notes
Options for Controller 0 - DDR3 SDRAM
Clock Period: Choose the clock period for the desired frequency. The allowed period range(2500 - 3300) is a function of the selected FPGA part and FPGA speed grade. Refer to the User Guide for more information.
3,125
ps
320.0 MHz
To achieve optimum resource utilization, maintain default clock period given by the tool or a value greater than default clock period. Please contact Xilinx Technical Support for further information
PHY to Controller Clock Ratio: Select the PHY to Memory Controller clock ratio. The PHY operates at the Memory Clock Period chosen above. The controller operates at either 1/4 or 1/2 of the PHY rate. The selected Memory Clock Period will limit the choices.
4:1
Memory Type: Select the memory type. Type(s) marked with a warning symbol are not compatible with the frequency selection above.
Components
Memory Part: Select the memory part. Part(s) marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part needed is not listed here. The "Create Custom Part" feature is not supported for RLDRAM II.
MT41K128M16XX-15E
Create Custom Part
Memory Voltage: Select the Voltage of the Memory part selected.
1.35V
Data Width: Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above.
16
ECC: MIG supports ECC for 72 bit data width configuration. To be able to select ECC, select a data width that has ECC supported.
Disabled
Data Mask: Enable or disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part selected has DM pins. Uncheck this box to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs (DDR3 SDRAM, DDR2 SDRAM) will not use Data Mask.
Number of Bank Machines: This parameter defines the number of bank machines. A given bank machine manages a single DRAM bank at any given time.
Note:Setting a lower value will result in lower resource utilization, but may effect controller efficiency for certain traffic patterns.
4
ORDERING: Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received.
Normal
Memory Details: 2Gb, x16, row:14, col:10, bank:3, data bits per strobe:8, with data mask, single rank, 1.35V,1.5V
User Guide
< Back
Next >
Cancel

Memory Interface Generator@hdg-eda-ws5.cdac.in

AMD Vivado ML Edition

- Pin Compatible FPGAs
- Memory Selection
- Controller Options
- **AXI Parameter**
- Memory Options
- FPGA Options
- Extended FPGA Options
- IO Planning Options
- Pin Selection
- System Signals Selection
- Summary
- Simulation Options
- PCB information
- Design Notes

Axi Parameter Options C0 - DDR3 SDRAM

Data Width

AXI DATA WIDTH: Data width of AXI read & write channels. The data width is less than or equal to user interface data width with the possible values 32, 64, 128, 256 & 512.

128

Arbitration Scheme

Select the arbitration scheme between the read and write address channels

RD_PRI_REG

Narrow Burst Support

Enables logic to support narrow bursts on the AXI4 slave interface. Can be set to zero if no masters in the system issue narrow bursts and all the data widths are equal. (1-Enable, 0-Disable)

1

Address Width

AXI4 address width of read and write address channels.

28

ID Width

AXI4 ID width for read and write channels. AXI4 ID is used as the identification tag for write or read address group of signals

13

User Guide | < Back | Next > | Cancel

Memory Interface Generator@hdg-eda-ws5.cdac.in

AMD Vivado ML Edition

- Pin Compatible FPGAs
- Memory Selection
- Controller Options
- AXI Parameter
- **Memory Options**
- FPGA Options
- Extended FPGA Options
- IO Planning Options
- Pin Selection
- System Signals Selection
- Summary
- Simulation Options
- PCB information
- Design Notes

Memory Options C0 - DDR3 SDRAM

Input Clock Period: Select the period for the PLL input clock (CLKIN). MIG determines the allowable input clock periods based on the Memory Clock Period entered above and the clocking guidelines listed in the User Guide. The generated design will use the selected Input Clock and Memory Clock Periods to generate the required PLL parameters. If the required input clock period is not available, the Memory Clock Period must be modified.

12500 ps (80 MHz)

☐ Select Additional Clocks (if required)

MIG can generate up to 5 additional clocks to be used in Fabric logic. This will be generated from the same MMCM which is used for generation of UI_CLK. The first clock(Clock 0) has a wider range of choices. All the values in the additional clocks drop downs are calculated considering the MMCM VCO frequency as **1562.5 ps (640 MHz)** Mhz. For complete details on clocking of MIG, refer to MIG User Guide.

Clock 0	NONE	D = 1
Clock 1	NONE	D = 1
Clock 2	NONE	D = 1
Clock 3	NONE	D = 1
Clock 4	NONE	D = 1

Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.

Read Burst Type and Length

The burst type determines the data ordering within a burst. Consult the memory datasheet for more information. Burst length 8 is the only supported value.

Sequential

Output Driver Impedance Control

Programmable impedance for the output buffer.

RZQ/6

RTT (nominal) - On Die Termination (ODT)

Select the nominal value of ODT for the DQ, DQS/DQS# and DM signals on the component or DIMM interface. This must be set to RZQ/6 i(40 ohms) for data rates at 1333 Mbps and above. In 2 slot DIMM configuations this value will be used for the unwritten slot during a write and will also be used for the unselected slot during a read. Use board level simulation to choose the optimum value.

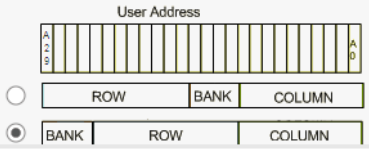
RZQ/6

Controller Chip Select Pin

The Chip Select (CS#) pin can be tied low externally to save one pin in the address/command group when this selection is set to 'Disable'. Disable is only valid for single rank configurations.

Enable

Memory Address Mapping Selection



User Guide | < Back | Next > | Cancel

Memory Interface Generator@hdg-eda-ws5.cdac.in

AMD Vivado ML Edition

- Pin Compatible FPGAs
- Memory Selection
- Controller Options
- AXI Parameter
- Memory Options
- **FPGA Options**
- Extended FPGA Options
- IO Planning Options
- Pin Selection
- System Signals Selection
- Summary
- Simulation Options
- PCB information
- Design Notes

System Clock

Choose the desired input clock configuration. Design clock can be Differential or Single-Ended.

System Clock — No Buffer

Reference Clock

Choose the desired reference clock configuration. Reference clock can be Differential or Single-Ended.

Reference Clock — No Buffer

System Reset Polarity

Choose the desired System Reset Polarity.

System Reset Polarity — ACTIVE HIGH

Internal Vref

Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This option can only be used at 800 Mbps and lower data rates. This can free 2 pins per bank where inputs are used. This setting has no effect on banks with only outputs.

Internal Vref — ☑

IO Power Reduction

Significantly reduces average IO power by automatically disabling DQ/DQS IBUFs and internal terminations during WRITEs and periods of inactivity

IO Power Reduction — ON

XADC Instantiation

The memory interface uses the temperature reading from the XADC block to perform temperature compensation and keep the read DQS centered in the data window. There is one XADC block per device. If the XADC is not currently used anywhere in the design, enable this option to have the block instantiated. If the XADC is already used, disable this MIG option. The user is then required to provide the temperature value to the top level 12-bit device_temp_i input port. Refer to Answer Record 51687 or the UG586 for detailed information.

XADC Instantiation — Enabled

User Guide | < Back | Next > | Cancel

Memory Interface Generator@hdg-eda-ws5.cdac.in

AMD Vivado ML Edition

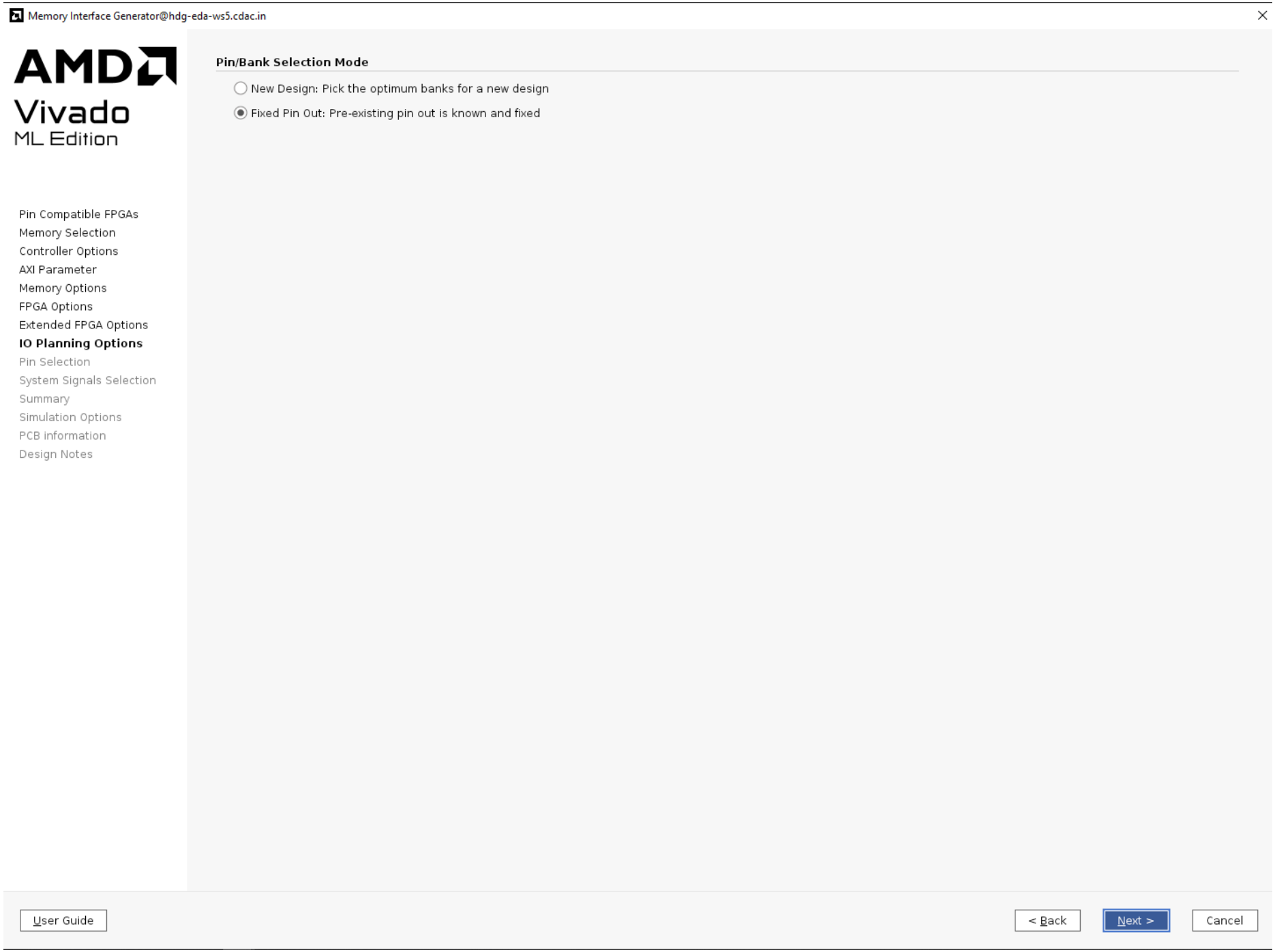
- Pin Compatible FPGAs
- Memory Selection
- Controller Options
- AXI Parameter
- Memory Options
- FPGA Options
- **Extended FPGA Options**
- IO Planning Options
- Pin Selection
- System Signals Selection
- Summary
- Simulation Options
- PCB information
- Design Notes

Internal Termination for High Range Banks

Select the internal termination (IN_TERM) impedance for the High Range (HR) banks. This setting applies **only** to the HR banks used in the interface.

Internal Termination Impedance 50 Ohms

User Guide | < Back | Next > | Cancel


Memory Interface Generator@hdg-eda-ws5.cdac.in
AMD
Vivado
ML Edition
Pin Compatible FPGAs
Memory Selection
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Pin Selection
System Signals Selection
Summary
Simulation Options
PCB information
Design Notes
Pin/Bank Selection Mode
New Design: Pick the optimum banks for a new design
Fixed Pin Out: Pre-existing pin out is known and fixed
User Guide
< Back
Next >
Cancel

Memory Interface Generator@hdg-eda-ws5.cdac.in

AMD Vivado ML Edition

- Pin Compatible FPGAs
- Memory Selection
- Controller Options
- AXI Parameter
- Memory Options
- FPGA Options
- Extended FPGA Options
- IO Planning Options
- **Pin Selection**
- System Signals Selection
- Summary
- Simulation Options
- PCB information
- Design Notes

Pin Selection For Controller 0 - DDR3 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	34	T0	K5	SSTL135
2	ddr3_dq[1]	34	T0	L3	SSTL135
3	ddr3_dq[2]	34	T0	K3	SSTL135
4	ddr3_dq[3]	34	T0	L6	SSTL135
5	ddr3_dq[4]	34	T0	M3	SSTL135
6	ddr3_dq[5]	34	T0	M1	SSTL135
7	ddr3_dq[6]	34	T0	L4	SSTL135
8	ddr3_dq[7]	34	T0	M2	SSTL135
9	ddr3_dq[8]	34	T1	V4	SSTL135
10	ddr3_dq[9]	34	T1	T5	SSTL135
11	ddr3_dq[10]	34	T1	U4	SSTL135
12	ddr3_dq[11]	34	T1	V5	SSTL135
13	ddr3_dq[12]	34	T1	V1	SSTL135
14	ddr3_dq[13]	34	T1	T3	SSTL135
15	ddr3_dq[14]	34	T1	U3	SSTL135
16	ddr3_dq[15]	34	T1	R3	SSTL135
17	ddr3_dm[0]	34	T0	L1	SSTL135
18	ddr3_dm[1]	34	T1	U1	SSTL135
19	ddr3_dqs_p[0]	34	T0	N2	DIFF_SSTL135
20	ddr3_dqs_n[0]	34	T0	N1	DIFF_SSTL135
21	ddr3_dqs_p[1]	34	T1	U2	DIFF_SSTL135
22	ddr3_dqs_n[1]	34	T1	V2	DIFF_SSTL135
23	ddr3_addr[13]	34	T3	T8	SSTL135
24	ddr3_addr[12]	34	T3	T6	SSTL135
25	ddr3_addr[11]	34	T3	U6	SSTL135
26	ddr3_addr[10]	34	T3	R6	SSTL135
27	ddr3_addr[9]	34	T3	V7	SSTL135
28	ddr3_addr[8]	34	T3	R8	SSTL135
29	ddr3_addr[7]	34	T3	U7	SSTL135
30	ddr3_addr[6]	34	T3	V6	SSTL135
31	ddr3_addr[5]	34	T3	R7	SSTL135
32	ddr3_addr[4]	34	T2	N6	SSTL135
33	ddr3_addr[3]	34	T2	T1	SSTL135
34	ddr3_addr[2]	34	T2	N4	SSTL135
35	ddr3_addr[1]	34	T2	M6	SSTL135
36	ddr3_addr[0]	34	T2	R2	SSTL135
37	ddr3_ba[2]	34	T2	P2	SSTL135
38	ddr3_ba[1]	34	T2	P4	SSTL135
39	ddr3_ba[0]	34	T2	R1	SSTL135

INFO: Press **Validate** to proceed.

Validate | Read XDC/UCF | Save Pin Out

User Guide | < Back | Next > | Cancel

Memory Interface Generator@hdg-eda-ws5.cdac.in

AMD Vivado ML Edition

- Pin Compatible FPGAs
- Memory Selection
- Controller Options
- AXI Parameter
- Memory Options
- FPGA Options
- Extended FPGA Options
- IO Planning Options
- **Pin Selection**
- System Signals Selection
- Summary
- Simulation Options
- PCB information
- Design Notes

Pin Selection For Controller 0 - DDR3 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
10	ddr3_dq[9]	34	T1	T5	SSTL135
11	ddr3_dq[10]	34	T1	U4	SSTL135
12	ddr3_dq[11]	34	T1	V5	SSTL135
13	ddr3_dq[12]	34	T1	V1	SSTL135
14	ddr3_dq[13]	34	T1	T3	SSTL135
15	ddr3_dq[14]	34	T1	U3	SSTL135
16	ddr3_dq[15]	34	T1	R3	SSTL135
17	ddr3_dm[0]	34	T0	L1	SSTL135
18	ddr3_dm[1]	34	T1	U1	SSTL135
19	ddr3_dqs_p[0]	34	T0	N2	DIFF_SSTL135
20	ddr3_dqs_n[0]	34	T0	N1	DIFF_SSTL135
21	ddr3_dqs_p[1]	34	T1	U2	DIFF_SSTL135
22	ddr3_dqs_n[1]	34	T1	V2	DIFF_SSTL135
23	ddr3_addr[13]	34	T3	T8	SSTL135
24	ddr3_addr[12]	34	T3	T6	SSTL135
25	ddr3_addr[11]	34	T3	U6	SSTL135
26	ddr3_addr[10]	34	T3	R6	SSTL135
27	ddr3_addr[9]	34	T3	V7	SSTL135
28	ddr3_addr[8]	34	T3	R8	SSTL135
29	ddr3_addr[7]	34	T3	U7	SSTL135
30	ddr3_addr[6]	34	T3	V6	SSTL135
31	ddr3_addr[5]	34	T3	R7	SSTL135
32	ddr3_addr[4]	34	T2	N6	SSTL135
33	ddr3_addr[3]	34	T2	T1	SSTL135
34	ddr3_addr[2]	34	T2	N4	SSTL135
35	ddr3_addr[1]	34	T2	M6	SSTL135
36	ddr3_addr[0]	34	T2	R2	SSTL135
37	ddr3_ba[2]	34	T2	P2	SSTL135
38	ddr3_ba[1]	34	T2	P4	SSTL135
39	ddr3_ba[0]	34	T2	R1	SSTL135
40	ddr3_ck_p[0]	34	T3	U9	DIFF_SSTL135
41	ddr3_ck_n[0]	34	T3	V9	DIFF_SSTL135
42	ddr3_ras_n	34	T2	P3	SSTL135
43	ddr3_cas_n	34	T2	M4	SSTL135
44	ddr3_we_n	34	T2	P5	SSTL135
45	ddr3_reset_n	34	ByteLessPin	K6	SSTL135
46	ddr3_cke[0]	34	T2	N5	SSTL135
47	ddr3_odt[0]	34	T3	R5	SSTL135
48	ddr3_cs_n[0]	34	ByteLessPin	U8	SSTL135

INFO: Press **Validate** to proceed.

Validate | Read XDC/UCF | Save Pin Out

User Guide | < Back | Next > | Cancel

Memory Interface Generator@hdg-eda-ws5.cdac.in

AMD Vivado ML Edition

- Pin Compatible FPGAs
- Memory Selection
- Controller Options
- AXI Parameter
- Memory Options
- FPGA Options
- Extended FPGA Options
- IO Planning Options
- Pin Selection
- **System Signals Selection**
- Summary
- Simulation Options
- PCB information
- Design Notes

System Signals Selection

Select the system pins below appropriately for the interface. Customization of these pins can also be made in the XDC after the design is generated. For more information see UG586 Bank and Pin rules.

System Clock and Reference Clock pin selections will not be visible if the 'No Buffer' option was selected in the FPGA Options page.

System Signals

These signals may be connected internally to other logic or brought out to a pin.

- **sys_rst**: This input signal is used to reset the interface.
- **init_calib_complete**: This signal indicates that the interface has completed calibration and memory initialization and is ready for commands. LOC constraint will be generated in XDC for Example design only based on "Pin Number" selection below.
- **error**: This output signal indicates that the traffic generator in the Example Design has detected a data mismatch. This signal does not exist in the User Design.

Signal Name	Bank Number	Pin Number
sys_rst	Select Bank	No connect
init_calib_complete	Select Bank	No connect
tg_compare_error	Select Bank	No connect

All pins must be constrained to specific locations in order to generate a bit file in the implementation phase (this is not required for simulation).

User Guide | < Back | Next > | Cancel

Memory Interface Generator@hdg-eda-ws5.cdac.in

AMD Vivado ML Edition

- Pin Compatible FPGAs
- Memory Selection
- Controller Options
- AXI Parameter
- Memory Options
- FPGA Options
- Extended FPGA Options
- IO Planning Options
- Pin Selection
- System Signals Selection
- **Summary**
- Simulation Options
- PCB information
- Design Notes

```
Vivado Project Options:
   Target Device              : xc7a100t-csg324
   Speed Grade                : -1
   HDL                        : verilog
   Synthesis Tool             : VIVADO

If any of the above options are incorrect,   please click on "Cancel", change the CORE Generator Project Options, and restart MIG.

MIG Output Options:
   Module Name                : AT1051_SOC_mig_7series_0_1
   No of Controllers          : 1
   Selected Compatible Device(s)   : xc7a100ti-csg324

FPGA Options:
   System Clock Type          : No Buffer
   Reference Clock Type       : No Buffer
   Debug Port                 : OFF
   Internal Vref              : enabled
   IO Power Reduction         : ON
   XADC instantiation in MIG      : Enabled

Extended FPGA Options:
   DCI for DQ,DQS/DQS#,DM         : enabled
   Internal Termination (HR Banks) : 50 Ohms



/************************************************************/
/*               Controller 0                 */
/************************************************************/
Controller Options :
   Memory                     : DDR3_SDRAM
   Interface                  : AXI
   Design Clock Frequency       : 3125 ps (320.00 MHz)
   Phy to Controller Clock Ratio : 4:1
   Input Clock Period         : 12499 ps
   CLKFBOUT_MULT (PLL)          : 16
   DIVCLK_DIVIDE (PLL)          : 1
   VCC_AUX IO                 : 1.8V
   Memory Type                : Components
   Memory Part                : MT41K128M16XX-15E
   Equivalent Part(s)         : --
   Data Width                 : 16
   ECC                        : Disabled
   Data Mask                  : enabled
   ORDERING                   : Normal

AXI Parameters :
   Data Width                 : 128
   Arbitration Scheme           : RD_PRI_REG
```

Print

User Guide | < Back | Next > | Cancel

Memory Interface Generator@hdg-eda-ws5.cdac.in

AMD Vivado ML Edition

- Pin Compatible FPGAs
- Memory Selection
- Controller Options
- AXI Parameter
- Memory Options
- FPGA Options
- Extended FPGA Options
- IO Planning Options
- Pin Selection
- System Signals Selection
- **Summary**
- Simulation Options
- PCB information
- Design Notes

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/*********************************************************/
/*                Controller 0                           */
/*********************************************************/
Controller Options :
   Memory                   : DDR3_SDRAM
   Interface                : AXI
   Design Clock Frequency       : 3125 ps (320.00 MHz)
   Phy to Controller Clock Ratio : 4:1
   Input Clock Period           : 12499 ps
   CLKFBOUT_MULT (PLL)          : 16
   DIVCLK_DIVIDE (PLL)          : 1
   VCC_AUX IO                   : 1.8V
   Memory Type                  : Components
   Memory Part                  : MT41K128M16XX-15E
   Equivalent Part(s)           : --
   Data Width                   : 16
   ECC                      : Disabled
   Data Mask                    : enabled
   ORDERING                     : Normal

AXI Parameters :
   Data Width                   : 128
   Arbitration Scheme           : RD_PRI_REG
   Narrow Burst Support         : 1
   ID Width                     : 13

Memory Options:
   Burst Length (MR0[1:0])         : 8 - Fixed
   Read Burst Type (MR0[3])        : Sequential
   CAS Latency (MR0[6:4])          : 5
   Output Drive Strength (MR1[5,1]) : RZQ/6
   Controller CS option            : Enable
   Rtt_NOM - ODT (MR1[9,6,2])      : RZQ/6
   Rtt_WR - Dynamic ODT (MR2[10:9]) : Dynamic ODT off
   Memory Address Mapping          : BANK_ROW_COLUMN


Bank Selections:
                Bank: 34
                                Byte Group T0:          DQ[0-7]
                                Byte Group T1:          DQ[8-15]
                                Byte Group T2:          Address/Ctrl-0
                                Byte Group T3:          Address/Ctrl-1

System_Control:
                SignalName: sys_rst
                                PadLocation: No connect  Bank: Select Bank
                SignalName: init_calib_complete
                                PadLocation: No connect  Bank: Select Bank
                SignalName: tg_compare_error
                                PadLocation: No connect  Bank: Select Bank
```

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User Guide | < Back | Next > | Cancel