**FAQs for VLSID 2026**

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# Useful Documentation

**Please go through the documents below before start working on tools:**

**> Libero SoC Installation and License Installation Guides:**

[**https://coredocs.s3.amazonaws.com/Libero/2021\_2/Tool/libero\_download\_license\_quickstart.pdf**](https://coredocs.s3.amazonaws.com/Libero/2021_2/Tool/libero_download_license_quickstart.pdf) (Windows)

[**https://coredocs.s3.amazonaws.com/Libero/2021\_2/Tool/linux\_setup\_libero\_soc\_ug.pdf**](https://coredocs.s3.amazonaws.com/Libero/2021_2/Tool/linux_setup_libero_soc_ug.pdf)(Linux)

**> Libero User Guide:**

Latest version as on 15th Oct 2025is Libero2025.1.

<https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/swdocs/libero/libero_ecf_ug_2025_1.pdf>

**> SoftConsole User Guide:**

[**https://ww1.microchip.com/downloads/secure/aemDocuments/documents/FPGA/media-content/FPGA/SoftConsole/v2022-2/Microchip-SoftConsole-v2022.2-RISC-V-747-windows-x64-installer.exe**](https://ww1.microchip.com/downloads/secure/aemDocuments/documents/FPGA/media-content/FPGA/SoftConsole/v2022-2/Microchip-SoftConsole-v2022.2-RISC-V-747-windows-x64-installer.exe) **-> for Windows**

[**https://ww1.microchip.com/downloads/secure/aemDocuments/documents/FPGA/media-content/FPGA/SoftConsole/v2022-2/Microchip-SoftConsole-v2022.2-RISC-V-747-linux-x64-installer.run**](https://ww1.microchip.com/downloads/secure/aemDocuments/documents/FPGA/media-content/FPGA/SoftConsole/v2022-2/Microchip-SoftConsole-v2022.2-RISC-V-747-linux-x64-installer.run) **-> For Linux**

**> Bare metal application development using Softconsole IDE:**

<https://ww1.microchip.com/downloads/aemdocuments/documents/fpga/ProductDocuments/ReleaseNotes/softconsole_v65_releasenotes.pdf> -> This covers complete basics on how to build projects using SoftConsole IDE for Cortex/RISC-V processors etc

[**https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/soc-fpga/softconsole**](https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/soc-fpga/softconsole)->Contains latest SoftConsole IDE (2022.02)

[**https://github.com/polarfire-soc/polarfire-soc-bare-metal-examples**](https://github.com/polarfire-soc/polarfire-soc-bare-metal-examples)-> Bare metal application example for all peripherals support for PFSoC devices

**> PolarFire SoC FPGA product :**

[**https://www.microchip.com/en-us/products/fpgas-and-plds/system-on-chip-fpgas/polarfire-soc-fpgas**](https://www.microchip.com/en-us/products/fpgas-and-plds/system-on-chip-fpgas/polarfire-soc-fpgas)

**> PolarFire SoC MSS configurator User Guide:**

<https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/swdocs/libero/pfsoc_mss_configurator_ug_2025_1.pdf>

**> FlashPro Express Programmer User Guide:**

[**http://coredocs.s3.amazonaws.com/Libero/2024\_1/Tool/flashpro\_express\_ug.pdf**](http://coredocs.s3.amazonaws.com/Libero/2024_1/Tool/flashpro_express_ug.pdf)

**> Programming using Embedded Flashpro Express (eFP6) :**

[**https://github.com/polarfire-soc/polarfire-soc-documentation/blob/master/reference-designs-fpga-and-development-kits/icicle-kit-embedded-software-user-guide.md**](https://github.com/polarfire-soc/polarfire-soc-documentation/blob/master/reference-designs-fpga-and-development-kits/icicle-kit-embedded-software-user-guide.md)

# Licensing FAQs:

**1 Q:** Is a license required to open Libero? If so, which license is necessary to operate the ICICLE kit?

**Answer:** Yes, License is required to execute Libero application.

With the Silver License, users will be able to design and program the Icicle Kit.

Users can generate a Silver License (free) from the following page:<https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/licensing>

**2 Q:** Is a license required to work with SoftConsole?

**Answer:** No License is required for Softconsole which is used for any application development on PFSoC (ex: Icicle kit, MPFS video kit, MPFS Discovery kit etc)

[**https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/soc-fpga/softconsole**](https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/soc-fpga/softconsole)->Contains latest SoftConsole IDE (2022.02)

**3 Q:** Is a license required to use FP Express tool?

**Answer:** No License is required to open FP Express. You can download standalone FP as below:

<https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/programming-and-debug/flashpro-express>

If you don’t have external FlashPro device, another method is programming bitstream with eFP6

[**https://github.com/polarfire-soc/polarfire-soc-documentation/blob/master/reference-designs-fpga-and-development-kits/icicle-kit-embedded-software-user-guide.md**](https://github.com/polarfire-soc/polarfire-soc-documentation/blob/master/reference-designs-fpga-and-development-kits/icicle-kit-embedded-software-user-guide.md)

**NOTE:** for eFP6, both J9 and J24 jumpers are to be shorted. Get jumpers in your Lab.

**4 Q:** Is a license required to open SmartHLS?

**Answer:** To access SmartHLS, a license is mandatory. However, users can obtain a free license by generating it from the designated webpage: <https://www.microchipdirect.com/fpga-software-products>

**5 Q**: NOTE: For some linux machines, you may see issue while running Daemons on Linux machines. In this case, please install the below dependency libraries to support running 32-bit applications on 64-bit x86 machine.

Since “actlmgrd” is a 32-bit application, in order to run this on 64-bit Ubuntu system following packages are required :

**For Ubuntu machine :**

$ sudo apt-get update

$ sudo apt-get install libc6-i386

$ sudo dpkg --add-architecture i386

$ sudo apt-get install libc6:i386 libncurses5:i386 libstdc++6:i386

$ sudo apt-get install multiarch-support

$ sudo apt-get install gcc-multilib

$ sudo apt-get install lsb

**For CentOS machine :**

Please install below libraries to run 32-bit ELF executable on 64-bit machines

$ yum install glibc.i686

$ yum install libXtst.i686

$ yum install glibc.i686

$ yum install libXft.i686

$ yum install libgtk-x11-2.0.so.0

$ yum install libXtst.so.6

$ yum install gtk2-engines.i686

$ yum install libSM.i686

$ yum install libSM.x86\_64

$ yum install libXi

$ yum install libpng

$ yum install libSM

**6 Q**: Do I have to run **lmgrd** command every time after the server restarts?

**Answer**: Yes. It is required to run lmgrd command every after-server restart.

*Command:* Go to daemons download path: lmgrd -c >License\_file\_path> -l <log file path>

**Below is the procedure to set up Libero and run GUI interactively :**

For windows :-

- Download License daemons from the links below :

<https://ww1.microchip.com/downloads/secure/aemDocuments/documents/FPGA/media-content/FPGA/daemons/Windows_Licensing_Daemon_11.19.6.0_64-bit.zip> - Daemons path

unzip and copy daemons to C:\FlexLM path

On cmd prompt :

cd C:\FlexLM

C:\FlexLM: lmgrd -c C:\FlexLM\License.dat -l C:\FlexLM\License.log

For Linux :

- Download License daemons from the links below :

<https://ww1.microchip.com/downloads/secure/aemDocuments/documents/FPGA/media-content/FPGA/daemons/Linux_Licensing_Daemon_11.19.6.0_64-bit.tar.gz> - Daemons path

* copy license.dat file in this folder
* edit license.dat and update daemons local path in it (default port 1702)
* edit <hostname\_of\_server> in it

*In one terminal(On Server):*

$ cd <path\_to\_daemons\_you\_downloaded>

tar -xvf <Linux\_Licensing\_Daemon\_11.19.6.0\_64-bit.tar.gz>

cd <daemons\_folder>

$ chmod 777 \*.\*

$ ./lmgrd -c <path\_to\_License>License.dat -l <path\_to\_log>License.log

.. Hope License server is running (check License.log whether all daemons are running successfully)

NOTE: Please contact Tech support if you face any issue while running Libero license server.

*On another Terminal (from client):*

Export below variables using below commands

$ export LM\_LICENSE\_FILE=1702@<hostname\_of\_server>

$ export SNPSLMD\_LICENSE\_FILE=1702@<hostname\_of\_server>

NOTE: For node-locked, server and client are same.

*How to Start Libero:*

$ export LM\_LICENSE\_FILE=1702@<hostname\_of\_server>

$ cd <Libero\_install\_path>/Libero/bin

$ ./libero

**7 Q**: Unable to run synthesis and getting synthesis failed

**Answer**:

1. Make sure your license is having synplifypro\_actel feature line
2. Make sure snpslmd daemon is running (lmutil lmstat -a -c 1702@<hostname of the server>)
3. Restart the daemons:

lmutil lmdown -c 1702@<hostname of the server>

./lmgrd -c <path\_to\_License>License.dat -l <path\_to\_log>License.log

1. Allow the daemons in the firewall
2. Make sure ports 1702 and 1703 are available for traffic flow (contact your IT for it)

# FAQ for OS Details:

**8 Q: What is the minimum amount of RAM needed to operate Libero?**

**Answer:** A minimum of 16 GB of Random-Access Memory (RAM) is recommended.

**9 Q: Could you please provide information on the compatible operating platforms for using Libero SoC 2023.1?**

**Answer:** Libero SoC Design Suite supports the following 64-bit operating systems:

•Libero SoC Design Suite supports the following 64-bit operating systems:

• Microsoft® Windows 10.0 and Windows 11.0

• Red Hat® Enterprise Linux (RHEL) 8.0-8.10, AlmaLinux® 8.3-8.10

• Ubuntu® 20.04.6 LTS For more information, refer to Libero SoC release notes: <https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/swdocs/libero/libero_soc_v2025_1_release_notes.pdf>

# Tools FAQs:

**10 Q:** **Could you please provide me with the location of the Libero Installation link?**

**Answer:** The Users can download the Libero SoC design suite from the following page: [*https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/libero-software-later-versions*](https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/libero-software-later-versions)

**11 Q: Does the Libero SoC Design suite include all necessary tools or are users required to install additional tools separately?**

**Answer:** The Libero SoC Design Suite comes with all the essential tools except for ***SoftConsole.*** Users must download ***SoftConsole*** separately from the following link: <https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/soc-fpga/softconsole>

**12 Q**: **What should users do if they receive a "Scan chain FAILED" error message while programming?**

A picture containing timeline

Description automatically generated

**Answer**:

1. Make sure that you select right part number for Icicle Kit in Libero design (***MPFS250T\_ES-FCVG484E***)
2. On power up board, both DDR and User LEDs should glow indicates board is working. Else please contact Tech support for assistance.
3. Make sure that you set the right Jumper settings. Refer the following link for Jumper settings: <https://github.com/polarfire-soc/icicle-kit-reference-design/releases>
4. Make sure J9 and J24 closed on Icicle kit for ‘Embedded FP6 programming’
5. J9 and J24 open for external Flashpro programming
6. Make sure that FlashPro/USB-UART drivers are installed properly on your machine

FlashPro drivers (provided along with Libero installations)

(or) Install from Microchip sites

<https://ww1.microchip.com/downloads/secure/aemdocuments/documents/fpga/media-content/fpga/v2024-1/program_debug_v2024.1_win.exe>

(or) Users can install USB-UART drivers from online:

PL2303\_Prolific\_DriverInstaller\_v1200

CP210x\_Universal\_Windows\_Driver

# Precautions while using Kit:

**13 Q**: Could the ICICLE kit be utilized in an environment that is not ESD-compliant?

**Answer:** No, Users **must** operate the ICICLE kit under ESD-compliant environment only. User should not touch with bare hands and must operate at ESD-compliant environment only.

**NOTE:** If device is broken due to mishandling/power fluctuations etc, Microchip is not responsible for it and can’t be replaced.

# Design Examples:

Refer to the following github page for SmartHLS materials and Examples: <https://github.com/MicrochipTech/fpga-hls-examples>

**14 Q:** **What are steps to update a PolarFire SoC Icicle kit to the latest reference design and Linux images?**

**Answer:** The board provided to you is programmed with default factory images.

**Ref design:**

For latest Icicle reference design and. wic image (version 2024.06 as on 24th Sept 2024), please refer below link and program it.

Refer to the following github page for ICICLE Kit reference designs: <https://github.com/polarfire-soc>

Latest Icicle ref design (.Job) : <https://github.com/polarfire-soc/icicle-kit-reference-design/releases/download/v2024.06/MPFS_ICICLE_BASE_DESIGN_2025_07.zip>

Latest Icicle ref design (.design/.tcl): <https://github.com/polarfire-soc/icicle-kit-reference-design/archive/refs/tags/v2025.07.zip>

**Linux (.wic) Image:**

Please refer github link to update Linux image (.wic):

https://github.com/polarfire-soc/polarfire-soc-documentation/blob/master/referencedesigns-fpga-and-development-kits/updating-mpfs-kit.md

Latest Icicle linux BSP image:

<https://github.com/linux4microchip/meta-mchp/releases/download/linux4microchip%2Bfpga-2025.07/mchp-base-image-mpfs-icicle-kit.rootfs-20250725101827.wic.gz>

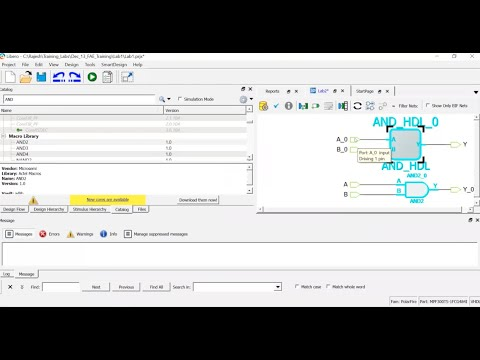
**15 Q:** **Where to download latest linux images for the Icicle kit?**

<https://github.com/polarfire-soc/meta-polarfire-soc-yocto-bsp>

Useful Links & Videos:

Refer the following short videos available on public websites, these videos will help you to understand the Polarfire SoC Design flow and Icicle Reference documentation.

[Libero® Design Flow Using Libero SoC Design Suite v12.3](https://www.youtube.com/watch?v=9anYqUyYMRQ) (Libero® Design Flow Using Libero SoC Design Suite)



<https://github.com/polarfire-soc/icicle-kit-reference-design> (PolarFire® SoC Icicle Kit Reference Design Generation Tcl Scripts - Libero® SoC v2025.07+)

[PolarFire® SoC | Building a Linux Yocto Image and Controlling the MSS GPIOs](https://www.youtube.com/playlist?list=PLtQdQmNK_0DSmjMrldPcwtviwx_JwaOi7) (PFSoC Linux Videos)

<https://www.microchip.com/en-us/products/fpgas-and-plds/system-on-chip-fpgas/polarfire-soc-fpgas> (Generic site for our FPGA’s e.g., PFSoC)

<https://github.com/polarfire-soc/polarfire-soc-documentation> (PFSoC GitHUB documentation)

<https://www.youtube.com/c/MicrochipTech/playlists> - (Public Microchip FPGA Video Training)

<https://mu.microchip.com/page/all-courses> (Search for FPGA training courses)

<https://www.youtube.com/playlist?list=PLtQdQmNK_0DSmjMrldPcwtviwx_JwaOi7> (PolarFire® SoC | Building a Linux Yocto Image and Controlling the MSS GPIOs (PFSoC Linux Videos)

**16 Q:** **Do we have any VectorBlox example for AI/ML development on Icicle kit?**

**Answer:** We do have that (VectorBlox Accelerator Software Development Kit (SDK)):

Please refer to the following user guide for the VectorBlox SDK programmer's guide: <https://www.arrow.de/-/media/arrow/images/research-and-events/articles/0820/microchip-fpga/vectorbloxpg.pdf>

We have good support for VectorBlox for Video kit. However, the support of VBX for Icicle kit very limited.

<https://github.com/polarfire-soc/icicle-kit-reference-design/releases/download/v2024.02/MPFS_ICICLE_VECTORBLOX_2024_02.zip>

Also, we have some tutorials on our github page; please refer to the following page: <https://github.com/Microchip-Vectorblox/VectorBlox-SDK>

**17 Q: Is there a way to communicate with fpga from linux env, as I need the input (image) from linux env loaded into fpga as input. Something like common memory space, if so how can i access that from linux and verilog code?**

**Answer:** This requires Linux driver development and creating a Linux /dev/mem device. A /dev/mem is a character device file that is an image of the memory of the Fabric SRAM or Fabric DDR. Byte addresses in /dev/mem are interpreted as physical memory addresses. mmap() system call reserves a region of the process's virtual address space, it retunes a pointer using which user can do read/write to Fabric SRAM or Fabric DDR.

<https://www.oreilly.com/library/view/linux-device-drivers/0596000081/>

Further, below document describes a demonstration of an FPGA fabric DMA Controller (COREAXIDMACONTROLLER) transferring 32-bit data over an AXI4-Stream interface.  
<https://github.com/polarfire-soc/polarfire-soc-documentation/blob/master/applications-and-demos/mpfs-axi4-stream-demo.md>

Additionally, there is a companion bare-metal project available with the demonstration that initiates the data stream and verifies the data. The bare metal project can be found in the following GitHub repository: <https://github.com/polarfire-soc/polarfire-soc-bare-metal-examples/tree/bbe684720f1eb762d3851ae90592d320b1a03b45/applications/benchmarks/dma_benchmarking/mpfs-dma-benchmarking/src/platform/drivers/fpga_ip/CoreAXI4DMAController>

The bare metal project initiates a dummy AXI4-Stream transfer and reads back all of the streamed values from memory. Messages are printed to UART1, in the event of a data mismatch the incorrect values are flagged.

**18 Q:** **Is there any reference example design on DMA/AXI transfer on Icicle kit?**

**Answer:** pl refer Q18 for more details

**19 Q: How can I control other gpio pins (like rasp header pins) from linux shell/python?**

**Answer:** Control leds from linux scripts by echo ing 1, 0 into gpio16.

PolarFire SoC GPIO Examples you are referring are given here.

<https://github.com/polarfire-soc/polarfire-soc-linux-examples/tree/master/gpio>

There are other methods like UIO to access HW from the user space, e.g., Accessing PolarFire SoC FPGA Fabric LSRAM using UIO

<https://github.com/polarfire-soc/polarfire-soc-linux-examples/tree/d602f23046eadb97b4ff4111495ec0e24965aeb4/fpga-fabric-interfaces/lsram>

Pls make sure you update the Icicle Reference design again in case you make any changes in the PFSoC device GPIO pins allocation using the “PolarFire SoC MSS Configurator”. In Peripherals tab: GPIOs from Bank 2 and Bank 4, OR GPIO from Bank 5.

**20 Q:** **How can I trigger the FPGA signal/execution from Linux env?**

**Answer:** I suggest you use interrupt from fabric to MSS for this purpose. Using GPIO it is easy way to send a control signal from MSS to fabric.

Pls refer Table 6-1. Routing of Interrupts to Processor Cores in PolarFire® SoC MSS Technical Reference Manual

<https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/ProductDocuments/ReferenceManuals/PolarFire_SoC_FPGA_MSS_Technical_Reference_Manual_VC.pdf>

MSS\_INT\_F2M[63:32] 32 [168:137] [181:150] [47:16] — — — — — — —

MSS\_INT\_F2M[31:0] 32 [136:105] [149:118] — [47:16] [47:16] [47:16] [47:16] — — MASKED

**21 Q:** **Are there any bare metal example applications on PFSoC MSS peripherals?**

**Answer:** We have examples available at below github link. Import these projects on Softconsole and build/execute on Icicle kit board. Pl refer Softconsole6.5 (above) on how to import and execute bare metal projects on Softconsole IDE.

[https://github.com/polarfire-soc/polarfire-soc-bare-metal-examples](https://github.com/polarfire-soc/polarfire-soc-bare-metal-examples/)

The example covers on below MSS peripherals :

GPIO

UART

I2C / CAN

MMC

QSPI

MMUART

TIMER

USB

WATCHDOG

PDMA

ETHERNET MAC

**22 Q:** **Are there any examples on how to measure timing on HLS designs?**

**Answer:** <https://github.com/MicrochipTech/fpga-hls-examples>

**23 Q: How do I build yocto BSP on Polarfire SoC for Icicle kit ?**

**Answer:**

For RISC-V architecture, we support 2 ways of building BSP

Yocto build - <https://github.com/linux4microchip/meta-mchp/tree/scarthgap/meta-mchp-common>

Build Root external - <https://github.com/linux4microchip/buildroot-external-microchip>

Use can copy either core-image-minimal (or) mchp-base-image for any linux experiments

NOTE: if Linux is not booting, advise to program latest .wic and .job from github site.

<https://github.com/polarfire-soc/icicle-kit-reference-design/releases/download/v2025.07/MPFS_ICICLE_KIT_ES_2025_07.zip> - Icicle ES .Job

[https://github.com/linux4microchip/meta-mchp/releases/download/linux4microchip%2Bfpga-2025.07/mchp-base-image-mpfs-icicle-kit.rootfs-20250725101827.wic.gz - Icicle ES .wic](https://github.com/linux4microchip/meta-mchp/releases/download/linux4microchip%2Bfpga-2025.07/mchp-base-image-mpfs-icicle-kit.rootfs-20250725101827.wic.gz%20-%20Icicle%20ES%20.wic)

Use eMMC / standard SD cards ex: SanDIsk SD for Linux copy.

NOTE: Since it is generic Linux knowledge on building BSP, User need to familiar with Yocto/Buildroot basics before start building image.

We can’t teach relating to basics of Yocto and Buildroot. Have a look of below yocto Manuals.

<https://docs.yoctoproject.org/dunfell/>

<https://www.yoctoproject.org/pipermail/meta-freescale/2013-March/001742.html>

**24 Q**: **Do PFSoC BSP support python for AI/ML applications on target?**

**Answer:** Yes, our toolchain supports python which can help with the development of AI/ML applications. $ python3 -> on target

**25 Q: How to copy JPEG images from Icicle target to host machine (or) vice versa?**

**Answer:** There are different ways to transfer files from target device to host or vice versa.

-> Connect internet and using WinSCP tool for transfer of files to/from host machine

Where provide IP address / pw: root... as login in WinSCP and drag to /home/<tmpfolder>

**26 Q:** **How to get internet working on Icicle kit?**

**Answer:** Few recommendations

-> Connect to proper ethernet port or switch which has external access for yocto build.

-> $ While booting, you can check MAC, ethernet link up messages on kernel logs.

-> $ifconfig eth0 down/up

NOTE: DHCP is enabled by default. If IP address still not assigned, try static IP.

**27 Q: How to copy application .elf (or) yocto .wic image to eMMC ?**

**Answer:** Please refer below link i.e. with USBDMSC utility from HSS

<https://github.com/polarfire-soc/meta-polarfire-soc-yocto-bsp#Copy-the-created-Disk-Image-to-flash-device>

**-** Ctrl + C while HSS booting

- type mmc

- type ‘usbdmsc’

- Using Win32DiskImager, copy .wic/.elf to eMMC

- type boot

Please refer to the link below for more details about PFSoC software flow:

<https://github.com/polarfire-soc/polarfire-soc-documentation/blob/master/knowledge-base/polarfire-soc-software-tool-flow.md>

<https://github.com/polarfire-soc/polarfire-soc-documentation>

**28 Q: What to do when there are no UART console messages on the Icicle kit?**

**Answer:** As soon as you boot device, you should get both HSS and kernel logs on UART terminals

-> Make sure you installed USB-to-UART driver as suggested Q12.

-> Make sure you open all 4 COM ports using putty/Minicom/Tera term etc @115200 Baud and flow control -> no

-> Suggest to program with latest reference design and .wic image (i.e., latest 2025.07 release)

Please refer below link:

<https://github.com/polarfire-soc/icicle-kit-reference-design/releases/download/v2025.07/MPFS_ICICLE_KIT_ES_2025_07.zip> - Icicle ES .Job

<https://github.com/linux4microchip/meta-mchp/releases/download/linux4microchip%2Bfpga-2025.07/mchp-base-image-mpfs-icicle-kit.rootfs-20250725101827.wic.gz> – Icicle .wic

-> Makre sure J9 and J24 are closed for embedded FP programming of above images

-> Make sure 4 LEDS on (corner of board) are glowing. I.e., 1 DDR and rest User LEDs

NOTE: If still no UART console, it might issue with microUSB port itself. Replace/solder J11 with new microUSB connector in Lab.

Also make sure, you connect USB cable (provided in kit) correctly J11 to board

**29 Q: Are there any bare metal examples available for Icicle kit for testing peripherals ?**

[GitHub - polarfire-soc/polarfire-soc-bare-metal-examples: Bare metal example software projects for PolarFire SoC](https://github.com/polarfire-soc/polarfire-soc-bare-metal-examples)

**30 Q:** **Is there any linux examples available for Icicle kit?**

[GitHub - polarfire-soc/polarfire-soc-linux-examples](https://github.com/polarfire-soc/polarfire-soc-linux-examples)

**31 Q: Is there any linux example to interacts with the PAC193x voltage/current sensor on the board and displays graphs of the readings using a webserver?**

[polarfire-soc-linux-examples/ethernet/iio-http-server/README.md at master · polarfire-soc/polarfire-soc-linux-examples · GitHub](https://github.com/polarfire-soc/polarfire-soc-linux-examples/blob/master/ethernet/iio-http-server/README.md)

**32 Q:** **Is there any example on Transferring Large Blocks of Data between Linux User Space and FPGA Fabric on PolarFire SoC?**

[polarfire-soc-linux-examples/pdma at master · polarfire-soc/polarfire-soc-linux-examples · GitHub](https://github.com/polarfire-soc/polarfire-soc-linux-examples/tree/master/pdma)

**33 Q: Any documentation explaining software development flow on PFSoC ?**

Please refer to the link below for more details about PFSoC software flow:

<https://github.com/polarfire-soc/polarfire-soc-documentation/blob/master/knowledge-base/polarfire-soc-software-tool-flow.md>

<https://github.com/polarfire-soc/polarfire-soc-documentation>

**For any more queries:**

Please contact [Support\_VLSID2026@microchip.com](mailto:Support_VLSID2026@microchip.com) This mail ID is valid during conference period only.