CoreVectorBlox Release Notes

About This Release

This document accompanies the production release of CoreVectorBlox v2.0 IP core. It describes the features and enhancements of CoreVectorBlox v2.0 IP core. It also contains the information on system requirements, supported families, implementations, known limitations and workarounds and resolved issues from the previous version.

Documentation

For more information about Microchip Intellectual Property, see www.microchip.com/en-us/products/fpgas-and-plds/ip-core-tools.

For updates and additional information about Microchip software, FPGAs, and hardware, see www.microchip.com/en-us/products/fpgas-and-plds/fpgas#Design%20Resources.

Release History

The following table lists the release history of CoreVectorBlox IP core.

Table 1. CoreVectorBlox Release History

Version	Date	Changes
2.0	November 2024	TFLite compatible Convolutional Neural Network (CNN) implementation
1.1	January 2021	FPGA resource usage reduction
1.0	November 2020	Performance improvements. Added `output_valid` interrupt signal.
0.9	June 2020	Initial release

Features

CoreVectorBlox is a highly configurable core and has the following features:

- Multiple preset configurations to trade-off performance for resource utilization.
- Overlay design allows multiple networks to run on the same core, even switch dynamically.
- Configurable width (64-bit to 256-bit) AXI4 memory master for data access.
- AXI4-Lite slave for control and status.
- Memory-based; reads inputs from and writes outputs to memory-mapped master.
- Internal vector processor, which can process general neural-network layers.
- Convolutional Neural Network (CNN) accelerator for convolutional layers.

Delivery Types

CoreVectorBlox is licensed as encrypted Register Transfer Level (RTL). Encrypted RTL source code is provided for the core.

Supported Families

This section lists the families supporting CoreVectorBlox v2.0 IP core:

- PolarFire®
- PolarFire SoC

Supported Tool Flows

Libero® System-on-Chip (SoC) v2024.02 or later must be used with this CoreVectorBlox release.

Installation Instructions

The CoreVectorblox CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the Add Core catalog feature. Once the CPZ file is installed in Libero, the core is configured, generated and instantiated within SmartDesign for inclusion in the Libero project.

For further instructions on core instantiation, licensing and general use, see *Libero online help and VectorBlox GitHub documentation*.

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1. What is New?

1.1 New Features and Devices

The following are the new features of v2.0 release:

- Fully TFLite compatible CNN implementation
- Decoupled/parallel Matrix Processor (MXP) and CNN operation with synchronization handshaking for data hand-off

1.2 Known Issues and Workarounds

There are no known issues or workarounds. For latest information, see the SDK documentation.

1.3 Discontinued Features and Devices

The following are the discontinued features in the v2.0 release:

- Internal microprocessor is removed
- Firmware register and firmware file requirement is removed

2. Revision History

Revision	Date	Description
B	11/2024	The following is the list of changes in revision B: • Updated document version from v1.1 to v2.0 • Updated links in Documentation • Updated New Features and Devices • Updated Known Issues and Workarounds • Updated Discontinued Features and Devices
A	01/2021	The following is the list of changes in revision A: • The document was updated to Microchip template and document number was changed from 51300238 to DS50003113A • The version number of CoreVectorblox is increased to v1.1
2.0	11/2020	The following is the list of changes in revision 2.0: • The version number was updated from v0.9 to v1.0 • Table 1 was updated
1.0	06/2020	Revision 1.0 is the first publication of this document

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