Power Consumption Calculation for Two-Stage CMOS OTA

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Objective

This document presents the power consumption calculation for the two-stage Miller-compensated CMOS OTA based on DC operating point simulation results.

Supply Voltage

The OTA operates from symmetric supply rails:

$$V_{DD} = 1.8\,\text{V}, \quad V_{SS} = -1.8\,\text{V}$$

The total supply voltage is:

$$V_{\text{total}} = V_{DD} - V_{SS} = 3.6\,\text{V}$$

Total Bias Current

From DC operating point simulation, the total current drawn is:

$$I_{\text{total}} = 60\,\mu\text{A}$$

This includes contributions from the input stage, bias circuitry, and second gain stage.

Power Consumption

The total power consumption is:

$$P = V_{\text{total}} \times I_{\text{total}}$$

Substituting values:

$$P = 3.6\,\text{V} \times 60\,\mu\text{A}$$

$$\boxed{P = 216\,\mu\text{W}}$$

Conclusion

The OTA consumes 216 µW while meeting gain, bandwidth, and stability requirements.