gm/ID-Based Design Calculations for a Two-Stage Miller-Compensated OTA

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Design Objective

This document presents a logically ordered gm/ID-based hand-calculation flow for a two-stage Miller-compensated Operational Transconductance Amplifier (OTA). The objective is to derive bias currents and transistor dimensions starting from the unity-gain bandwidth requirement.

Given Specifications

- Unity Gain Bandwidth:

$$\mathrm{UGB} = 340\,\mathrm{MHz}$$

- Miller Compensation Capacitor:

$$C_c = 0.1\,\mathrm{pF} = 1 \times 10^{-13}\,\mathrm{F}$$

Unity Gain Bandwidth Relation

For a Miller-compensated two-stage OTA, the unity-gain bandwidth is given by:

$$\mathrm{UGB} = \frac{g_{m1}}{2\pi C_c} \tag{1}$$

Solving for the first-stage transconductance:

$$g_{m1} = 2\pi \cdot \mathrm{UGB} \cdot C_c \tag{2}$$

Substituting numerical values:

$$g_{m1} = 2\pi \cdot (340 \times 10^6) \cdot (1 \times 10^{-13}) \tag{3}$$

$$\boxed{g_{m1} = 0.214\,\mathrm{mS}} \tag{4}$$

Input Differential Pair Transconductance

The input stage consists of a symmetric NMOS differential pair. Hence, the total transconductance is shared equally between the two devices:

$$g_{m,\text{per device}} = \frac{g_{m1}}{2} \tag{5}$$

$$\boxed{g_{m,\text{per device}} = 0.107\,\text{mS}} \tag{6}$$

gm/ID Operating Point Selection

From the NMOS lookup table for $L = 0.5\ \mu$m, the following operating regions are observed:

Region	$\boldsymbol{g_m/I_D}$ (V^{-1})
Weak Inversion	22–25
Moderate Inversion (Chosen)	18–20
Strong Inversion	8–12

For this design, moderate inversion is selected:

$$\boxed{\frac{g_m}{I_D} = 20\ \text{V}^{-1}} \tag{7}$$

Drain Current Calculation

Using the gm/ID relationship:

$$I_D = \frac{g_m}{g_m/I_D} \tag{8}$$

Substituting numerical values:

$$I_D = \frac{0.107 \times 10^{-3}}{20} \tag{9}$$

$$\boxed{I_D = 5.35\,\mu\text{A} \quad \text{(per transistor)}} \tag{10}$$

The tail current of the differential pair is therefore:

$$\boxed{I_{\text{tail}} = 10.7\,\mu\text{A}} \tag{11}$$

Transistor Width Estimation

From the NMOS lookup table at $g_m/I_D \approx 20\ \text{V}^{-1}$:

$$\frac{I_D}{W} \approx 5\,\mu\text{A}\,\mu\text{m}^{-1} \tag{12}$$

Hence, the required transistor width is:

$$W = \frac{I_D}{I_D/W} = \frac{5.35}{5} \tag{13}$$

$$\boxed{W \approx 1.07\,\mu\text{m}} \tag{14}$$

Second-Stage Transconductance Requirement

To ensure adequate phase margin and push the non-dominant pole to higher frequencies, a standard stability guideline is:

$$g_{m2} \geq 3 \cdot g_{m1} \tag{15}$$

$$\boxed{g_{m2} \approx 0.64\,\text{mS}} \tag{16}$$

Practical Design Note

The above calculations provide a first-order gm/ID-based sizing. Final transistor widths were adjusted in `xschem` using AC simulations to account for parasitic capacitances, Miller loading, and short-channel effects, ensuring adequate phase margin and closed-loop stability.

Summary of Transistor Operating Points and Dimensions

Table 1: Summary of OTA Transistor Sizing Using gm/ID Method

Device	**Role**	$\boldsymbol{g_m/I_D}$ (V^{-1})	I_D (μ**A**)	W (μ**m**)
M1, M2	Input differential pair	20	∼5.3	∼1.1
M4, M5	Active PMOS load	18	∼5	∼1.0
M6	Second-stage gain device	15–18	∼10	∼10–12
M3, M9	Tail and bias current devices	10	∼10	∼1.0
M7	Bias device (mirror / startup)	8–10	∼10	∼6.0