

6TLB

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In modern computer systems, the CPU generates virtual addresses, which are then translated into physical addresses before accessing memory. This translation is typically done by the Memory Management Unit (MMU) in conjunction with the TLB.

When the CPU needs to access a memory location, it first checks the TLB to see if the translation from virtual address to physical address is already cached. If the translation is found in the TLB (a TLB hit), the physical address is obtained directly from the TLB, avoiding the need to access the slower main memory for the translation. If the translation is not found in the TLB (a TLB miss), the MMU has to perform a lookup in the page table stored in main memory, which takes more time.