As the flipflop is the boric memory unit. It is used for Storing I bit memory information. The register counists of the set of flip flots which is used for storing a binary word. To store in bit binary word a set of n flipflops in used. There are different types of registers available in MSI circuits. The mostly used of flipflops are used as the registers. and such registers are called shift registers also There are the different modes of operation for the

\* series or serial operation oregisters. \* Parallel operation

gn case of serial operation, digits are putting sequence, one digit for each clock pulse. where as in case of parallel operation all digits get shifted Simultaneously during a ringle clock pulse.

The block diagram for 4 bit register is as shown below

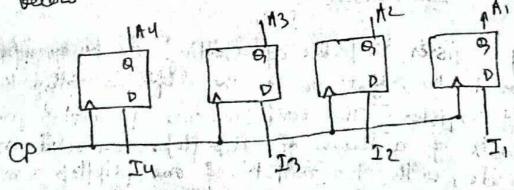


fig:- 4-bit register.

This is the register constructed by the 4-D flipflows

and a common clock puise input that trables all the flipfloter so that the information presently available at the force inputs com be transferred that a bit register. There are different types of exceptions—

Serial in Serial out (SISO) Serial in Parallel out (SIPO) Parallel In Serial out (Piso) Parallel in Parallel out (PIPO)

911 SISO decto Com be Stored Serially one bit at a time and output also transferred 1 bit at a time on SIPO the ofata is stored serially but output is transferred in perellely. Similarly 911 case of PISO the data inputs are provided parallel form of output is transferred in Serdial sequence where as in the PIPO form of register the data are taken in the parallel celso the output is also transferred in parallel return

## Shift Register 1-

Any register capable of estiffind its binary information either to the right or to the left is called the shift rights to the register. The configuration of Shift register consists of a chain of flip-flots connected in cascade, with the output of one flipflots connected to the input of next flipflots. Also all the flipflots in the series receive a common clock pulse which the series receive a common clock pulse which the series the strift from one stage to next. The cause the strift from one stage to next. The

register are the capabilities of these and are given

as A clear control to clear register to o

- A Clock Pulse input for CP to Synchronize all operations

-) Shift right control to enable the shift right operation of the serial input & output associated to shift right

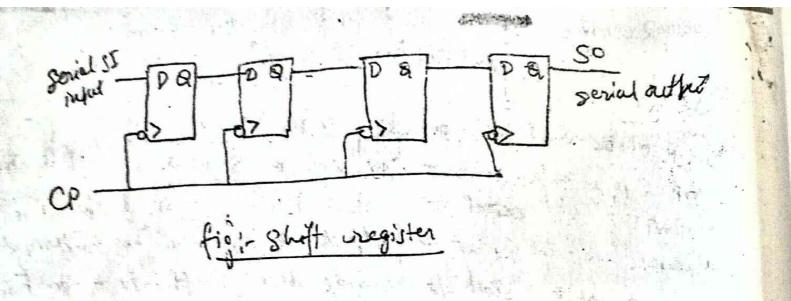
I shift left control to enable the shift left operation of the serial input & output associated to shift left

-) Parallel load central to enable a parallel transfer and the n input associated with the parallel pronfer.

-1 n parallel output lines

in the register unchanged even though clock pulses are continously applied.

Any 8hift orgaister capable of both saight & left shifting of information is called the bidiretimal 8hift only one direction 8hift register and that 8hift register. Also it the in called unidirectional Shift register. Also it the called a shift and parallel load capabilities it is called a shift register with perallel load.



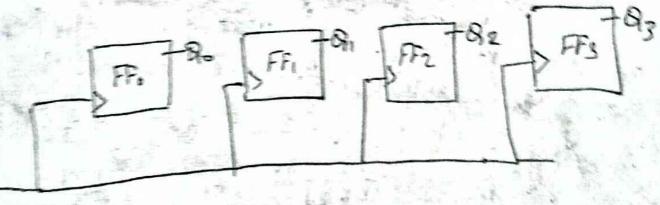
This register shifts its contenents with every clock pulse during negative edge of pulse transition-two is indicated by small circle arrowated with the clock pulse mjut in all flip fleps.

sequential circuits that feet through a prescribed Surveyor of States upon the epithicution of input pulses is called consisten. OR it is a sequential circuit that counts the mo. of input pulses that it decines. Commenty it is constructed by using T or JK flipfly together with other combinational circuits. If we use in full-flaks for commenter them it will count an states and after country completed their the counter resets itself to the original states. There are two types of educates

& STACKNOWILLS CORNER

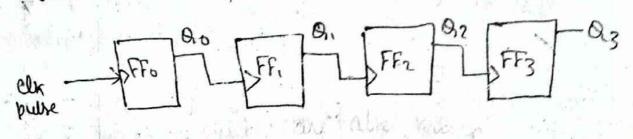
# Keynchronous counter / Riphle Counter

The synchronous enwiews are those to-which the elock input is connected to cell the flip floods individually so that they we simultenously clocked as shown in the figure



fif. The synchronions counter

Asynchronous counters are also known as the right counters and one those in which the right bulks in fiven as input to the first flipflop is flipfloop, the output of the first flipfloop is fed as clock input to the second flip flop as shown in the fisher given below.



fisure: Riphle counter 1 Asynchronous conder.

Binary riphle counter: Binary riphle counter counists of revies of connection of complementing flip flots cither (T flip flot) or JK flip flots) with the output of each flip flots connected to the clock pulse input of each flip flots order flip flots. The flip flots of the next higher order flip flots. The flip flots of the least significent bit receive the holding the least significent bit receive the holding the least pulses. The diagram of binery incoming count pulses. The diagram of binery incoming count pulses. The diagram of binery incoming counter in as follows.

riphee commer in as follows.

As

Clock to the total to the total to next bulse to the stage.

fig: Binery riphle counter

6 Hore all the JK inputs are equals to I

## uses of counter;

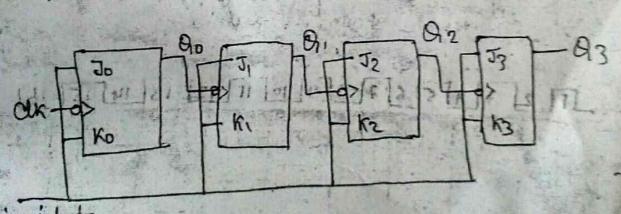
of times that certain event takes place.

in the digital system

\* To generate the clocks of different frequencies. \*
To generate the timing signals.

## 4-Bit Ripple Counter;-

As we know that any n-bit ripple connider can count up to a maximum of 2n states. If we connect four flip floops such that the output connect four flip floops such that the output of first flipflip is fed to the clock whit of of first flipflip is fed to the clock whit of the next as shown below, we get the 4-bit wipple counter.

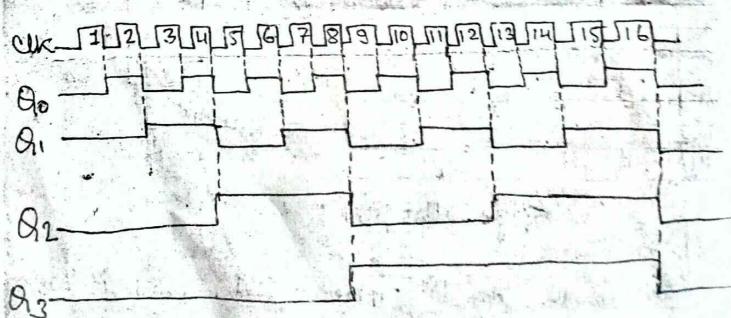


High input

fight. 4 bit viple counter.

This is the four bit riphle counter and it has 24 = 16 states from 0000 to 1111 and then 7

clock bulse	03	92	8,	A <sub>D</sub>	Cour			
Initial	1.0		10-	1	10			
First	0	0_	0	-	1 4			
Second	0	0	17	0	2			
third	0	0	工工	7	3			
fourth	0	1	10	0	4			
fitty	0	4	0	77	- 3			
81xHh	. 0	7	1 7	0	1 6			
seventh	10	F	工工	1	=			
eignith	1	10	0	0	8			
, nuth	1	0		王王	1 9			
tenth	1 1	0		10	10			
eleventy	1 1	1	7	1	1			
twelvoth	1 1	1	- 0	0				
1344	1 1		1 1 0	1 1	11			
1444	4		4.] 4	0	111			
15+4	1 1		1 1	1	1 15			
3) xteenth	0.		0) 0	0	R			
timing diagreem for one cycle for the 4-bit de counter is shown as follows								



Scanned by CamScanner

The part of the computer system that is capable of data storage either tempority or permenently is called the memory unit. Boucially the registers present in the computers have the carpability of Storing data. The registers are either operational or strage. The operational registers are capable of. Storing the binary information in its their flip flop and also these are capable of the data processing task. Means the operational registers are capable of doing both string as well as the operational functions. Similarly the Storage cregisters are only used for Storing the binary information in the temporary form The memory unit of the computer system is the collection of storage registers.

Also the binary cells of registers in memory unit must have the following properties.

- -) It mud have two valiable State for timeny representation
- -1 It must have small size
- -) The cost required for per lit storage should be as low as possible.
- The time of access to memory register should be reasonably fast.

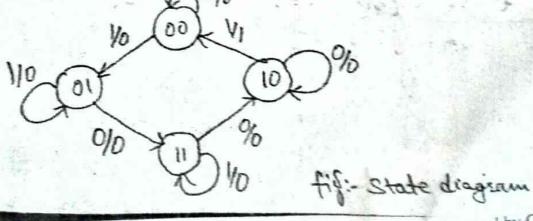
words is the collection of two, Dr four bytes."
Simply it is the collection of binary information.
In terms of groups of bits. It is stored within the memory registers. It may either store some operands, instructions or a group of alphanement characters or may be the binary coded information.

The memory unit is composed of different parts the memory address register (MAR) and memory buffer register (MBR).

The MAR specifies the memory word relected. Each word in memory is assigned a number identification Starting from a up to the maximum number of words available. & The communication been the specific memory word with the individual word the address of the word is transferred to the address register An address register with n bits cam specify upto on meniony words. Computer menory unit can range from 1024 words vegiving an address register of 10 bits to 1048576 = 220 words recruing a 20 bit address register.

The effect of the previous inputs on the output is represented by the state of the circuit of the sequential circuit at any circuit. The output of the sequential circuit at any time depends upon its current state and the input. The next state of the sequential circuit is also determined by the previous inputs and the current state of the circuit. The relationship that exists state of the circuit. The relationship that exists among the inputs, outputs, prevent states and the next states can be sherified by state tables or the next states can be sherified by state tables or the state diagrams.

The state take for the sequential circuit consists of the sections labelled present state, new state of and orether the present state derignates the state of flip flops before the occurance of a clock bulse. The next state shows the states of flip flops after the clock next state shows the states of flip flops after the clock pulse, and the orether section lists the value of the pulse, and the orether during the present state. The flip flops output variables during the present state. The flip flops catholic remarkles during the graphical symbol heaving the different states rather than the only graphical symbol, takes and the equations. The states of symbol, takes and the equations. The states of symbol, takes and the indicates the transition between arrow headed arcs that indicates the transition between arrow headed arcs that indicates the transition between arrow headed arcs that indicates the transition between the different states. Commider the following diagrams.



Here the binary number inside each circle indicary. The state the circle represents. The directed lines are labelled with two binary numbers reparated by a ship. The upper value indicates the import value and the derivation of state to 01 is labelled by 1/0 means if the sequential circuit is in present state and the input is 1 them the next state is 01 and the output is 0. If it is a present state of and the input is 0. If it is remain in that state. A directed line commuting a circle with itself indicates that no change of the state occurs. The state diagram provides exactly same information as the state table and is obtained directly from the state table.

State diagrams for different flipflops

SR flipflop; - S, R = 0,D

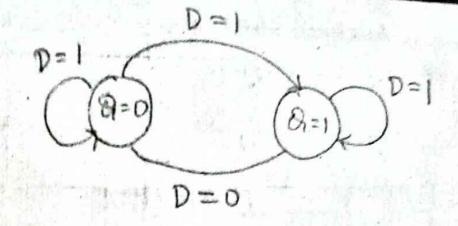
S, R = 1, D

S, R = 0,1

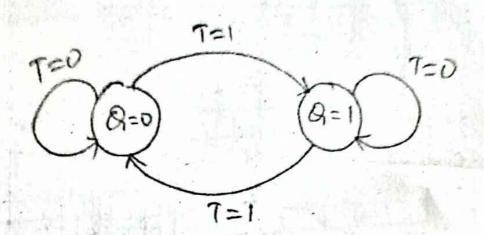
S, R = 0,1

 $\frac{J_{K}-flipflop}{J_{K}-flipflop}; \quad J_{K}=0,0 \qquad \qquad J_{K}=0,0 \qquad J_{K}=0,0 \qquad \qquad J_{K}=0$ 





T-fupflop:-



that all the flip flops have some number of the states and transitions. Each flip flop is in the set state when  $\Omega=1$  and in the reset state when  $\Omega=0$ . Also each flip flop can move from one state to another or it can recenter the same state. The only difference between four types lies state. The only difference between four types lies in the value of input signals that cause there in the value of input signals that cause there transitions. The state diagram is considered very transitions. The state diagram is considered very convenient way to visualise the operations of the flip flop or even of the large sequential the flip flop or even of the large sequential

the design the circuit diagram that convert 4 bit binary number into its 215 emplement

Som

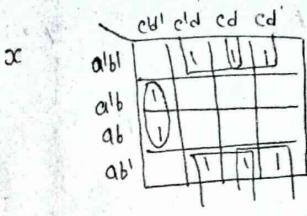
Here the functional table is from by

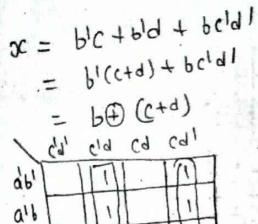
110	buts			0	uth	utz	Š.
Čt.	Ъ	c	d.	w	×	R	2
Ð	0	0	0	0	O.	c	0
0	Ö	Ð	1	k	1	1	l l
0	0	18	0		1	Į.	0
0	0	1	ĵ	Į	ı	٥	1
0	- 1	0	0	4	ı	0	0.
0	Ĭ.	0	1	1	0	1	1
0	1	40	6	1	٥	1	D
O	l l	1		1	0	0	1
8	c-	0	0	1	0	0	0
Ž.	0	0	1	0	1	i	1 -
1	0	1,1	٥	0	1	ŧ	0
1	0	-	1-	0	ı	10	1.
ŧ,	L	0	0	٥	1	0	6
1	- 6	0	1	10	0		
-	i i	į į į	0	٥	0	F	0
1	1	1	100	0	0	0	

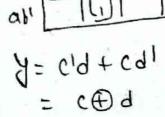
Now, calculating the value of w, x, y, Z on the baris of minterms

2190	7.	الحاط	cld	cd	cyl.	-
صا	ale !				1	-
	a <sup>i</sup> b	T	16	14	11	-
	qb		1_	1	+-	4
	o H		species.	1	+-	د

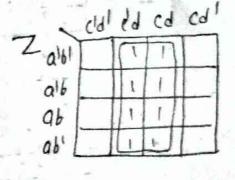
 $\omega = a^{1}d + a^{1}c + a^{1}b + a^{1}b^{1}d^{1}$ =  $a^{1}(b+c+d) + a^{1}b^{1}d^{1}$ =  $a \oplus (b+c+d)$ 



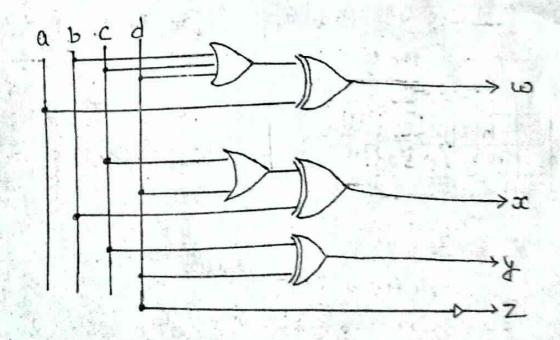




ab



Hence we can draw the circuit as follow-

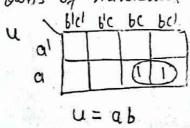


# Design a combinational circuit that accepts a three bit number and generates an output binary number equals to the square of input number.

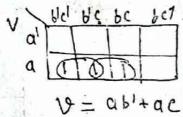
som here the truth table of the operation is

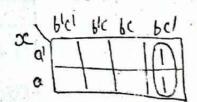
in	putz	3	outputs					
a	b \	c	u	12	w	x	B	2
0	0	0	0	D	0	0	0	0
0	0	1	0	9	0	D	0	1
0	1	0	0	D	0	41	0	0
0	1	1	0	0		0	0	1
1	lo	0	0	1	. 0	0	0	0
Ti	10	1	0	11	Ti	0	0	
1	i	0	1.1	0	0		0	0
1	1		11. 1	11	10	10	0	1

Now calculating the value of u & w x y & Z on the ban's of minterme we get



\	blc!	PIC	βC	bcl
Wai		B	1	
α		1		





Here the output of y all are equal to zero and output of z are as some as the inputs of c. Hence we can write y=0 and Z=C and we draw the circuit as follow—

