Unit-5

→ represent topic
→ represent sub-topic

Basic I/O, Memory R/W and Interrupt Operations:

⊛. Memory mapped I/O	I/O mapped I/O
i) I/O is treated as memory.	i) I/O is treated as I/O.
ii) 16-bit addressing (A_0–A_{15})	ii) 8-bit addressing (A_0–A_7)
iii) It can address $= 2^{16}$ $= 64K$	iii) It can address $= 2^8$ $= 256$
iv) No. of devices = 65536	iv) No of devices = 256
v) More decorder hardware	v) less decorder hardware
vi) Available memory is less.	vi) Available memory is more.
~~vii) Available memory is~~	
vii) $\overline{MERD}$ (Memory read operation) and $\overline{MEWR}$ (Memory write operation) signal with I/O.	vii) $\overline{IOR}$ (Input output read) and $\overline{IOW}$ (Input output write) control signal with I/O.
ix) Instructions used are as following example: LDA XXXX H. STA XXXX H MOV: A,M	ix) Instructions used are as following example. IN XXXXH OUT XXXX H

⊛ → Direct Memory Access (DMA)

- Direct Memory Access (DMA) is a process for data transfer ~~for~~ between memory and I/O, controlled by an external circuit called DMA controller, without involvement of CPU.

Most of data that is input or output from computer is processed by the CPU, but some data does not require processing, or can be processed by another device. In these situations, DMA can save processing time and is a more efficient way to move data from the computer's memory to other devices. For example, a PCI controller and a hard drive controller each have their own set of DMA channels.

Sequence of events that occurs during DMA operation:

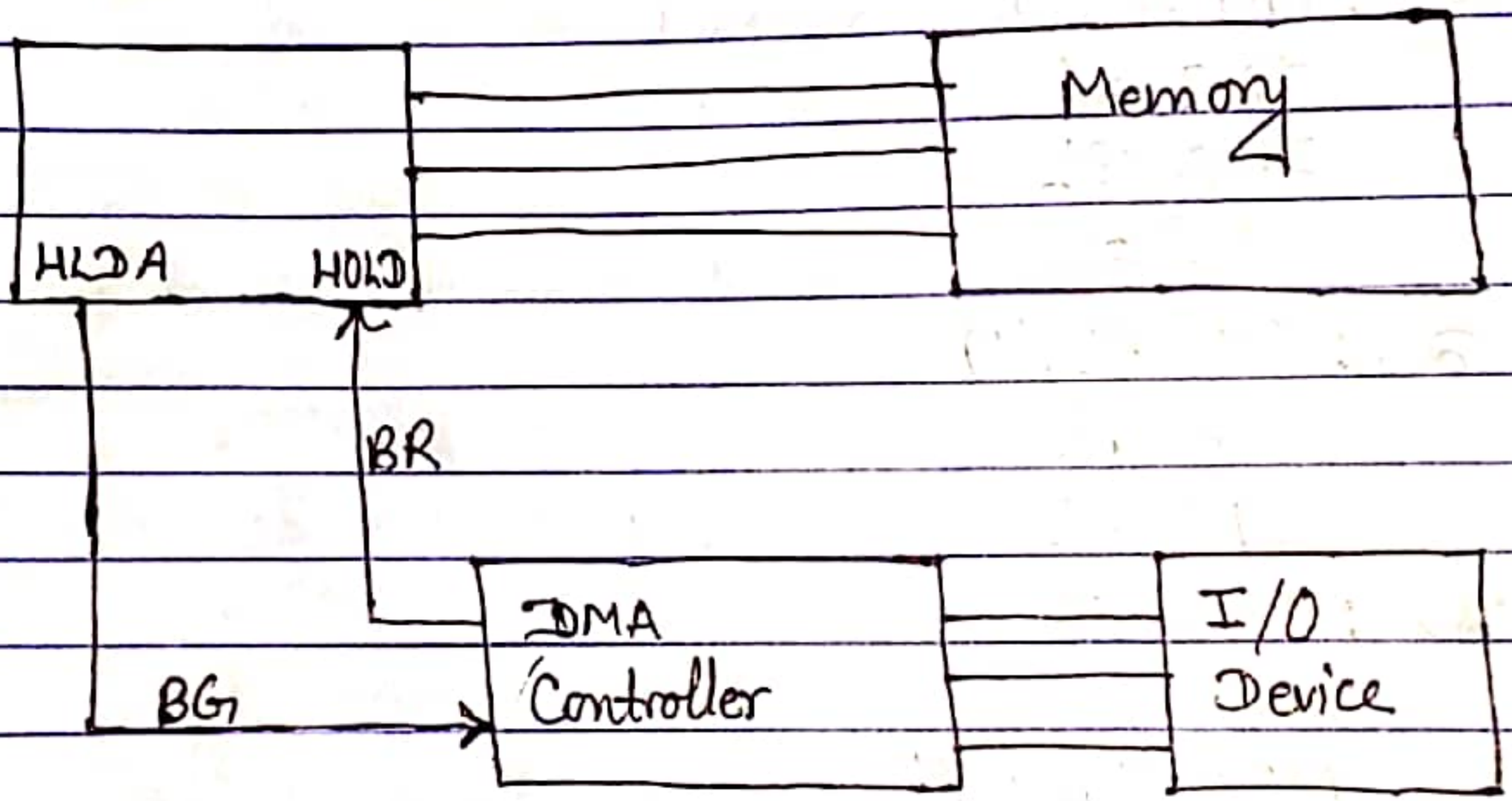

fig. DMA.

8085 MP has two pins HOLD and HLDA which are used for DMA operation. First DMA controller sends a request by making Bus Request (BR) control line high. After receiving HLDA through bus grant (BG) pin of DMA controller, the DMA controller takes control over system bus and transfers data directly between memory and I/O without involvement of CPU.

Advantages of DMA:

i) Fast memory transfer of data.
ii) Fewer CPU cycles for each transfer.
iii) CPU and DMA run concurrently under cache mode.
iv) DMA can trigger an interrupt, which frees the CPU from polling the channel.

Applications of DMA:

i) DMA is useful in real-time computing applications where critical operations must be done concurrently.
ii) Stream processing is another application of DMA, where transfer and data processing are done simultaneously.
iii) Many hardware systems use DMA like floppy disk drive, controllers, graphics cards, network cards, sound cards etc.

8237 DMA Controller and Interfacing:

fig. 8237 DMA Controller and Interfacing.

Date.
Page No.

→ The registers in the DMA are selected by the MP through the address bus by enabling the DS (DMA select) and RS (Register Select) inputs. The RD (read) and WR (write) inputs are bidirectional.

→ When the bus grant (BG) is 0, the MP can communicate with the DMA registers through the data bus to read from or write to the DMA registers. When BG=1, the processor does not have control over the system buses and the DMA can communicate directly with the memory by specifying an address in the address bus and activating the RD or WR control.

→ The DMA controller has three registers: an address register, a word count register and control register.

→ The address register contains an address to specify the desired location in memory.

→ The word count register holds the number of words to be transferred.

→ A control register specifies the mode of transfer.

(*2) Interrupts: (This description about interrupt is not imp. contents inside are imp marked with green)

Interrupt is a process where an external device can get the attention of the microprocessor. The process starts from the I/O device. An interrupt is considered to be an emergency signal that may be serviced. The microprocessor may respond to it as soon as possible.

When the microprocessor receives an interrupt signal, it ~~sus~~ suspends the currently executing program and jumps to an Interrupt Service Routine (ISR) to respond to the incoming interrupt.

Responding to an interrupt may be.

Date.
Page No.

immediate or delayed depending on whether the interrupt is maskable or non-maskable. There are two ways of redirecting the execution to the ISR depending on whether the interrupt is vectored or non-vectored.

Vector Interrupt → In this type of interrupt, Processor ~~can not~~ knows the address of Interrupt. In other word processor knows the address of interrupt service routine.

Example: RST 7.5, RST 6.5, RST 5.5, TRAP.

Non-Vector Interrupt → In this type of interrupt, Processor can not know the address of Interrupt. It should give externally. In the device will have to send the address of interrupt service routine to processor for performing ~~task~~ interrupt.

Example: INTR

Software Interrupt → It is an instruction based Interrupt which is commonly controlled by software. That means programmer can use this instruction to execute interrupt in main program. There are eight software interrupts RST 0 to RST 7 in 8085 microprocessor.

Hardware Interrupt → As name suggests it is an interrupt which can get the interrupt request in hardware pin of microprocessor 8085. There are mainly six pins available in 8085 for hardware interrupt purpose which are TRAP, RST 7.5, RST 6.5, RST 5.5, INTR, INTA.

Date.
Page No.

⊛ 8085 Interrupt pins and Priority:

There are five interrupt pins in 8085 and one interrupt acknowledge (INTA) pin.

Pin No.	Name	Type	Priority
6	TRAP	Vectored	Highest
7	RST 7.5	Vectored	↓
8	RST 6.5	Vectored	
9	RST 5.5	Vectored	
10	INTR	Non-Vectored	Lowest

Pin 6 to pin 10 interrupts have the priorities from highest to lowest in decreasing order. Priority means which interrupt gets the acknowledgement first if more than one are interrupting the microprocessor.

⊛ Maskable and Non-maskable Interrupts.

Maskable interrupts → An interrupt which can be disabled by software that means we can disable the interrupt by sending appropriate instruction, is called a maskable interrupt. RST 7.5, RST 6.5 and RST 5.5 are the examples of Maskable Interrupt.

Non-Maskable interrupts → As name suggests we cannot disable the interrupt by sending any instruction is called non-maskable interrupt. TRAP interrupt is the non-maskable interrupt for 8085. It means that if an interrupt comes via TRAP, 8085 will have to recognize the interrupt we cannot mask it.

Date.
Page No.

⊛ Vectored and Polled Interrupt.

Vectored Interrupt → In a computer, a vectored interrupt is an I/O interrupt that tells the part of the computer that handles I/O interrupts at the hardware level that a request for attention from an I/O device has been received and also identifies the device that sent the request.

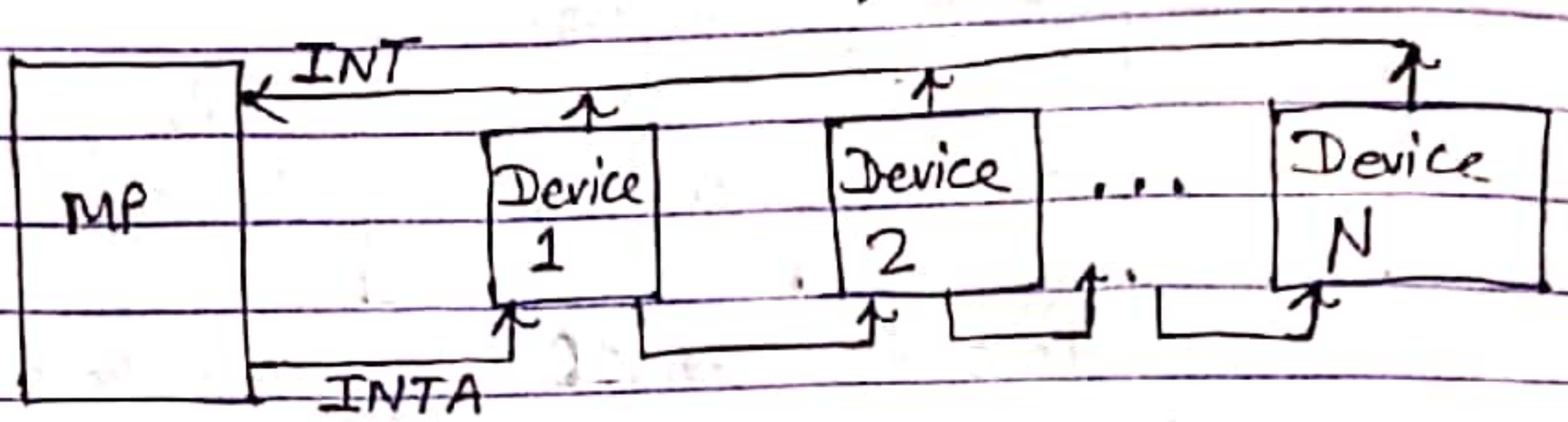

fig Vectored Interrupt.

The device is connected in a chain as shown in fig above for setting up the priority systems. If the device generate interrupt, it will accept the INTA signal from the processor otherwise, it will pass INTA on to the next device until INTA is accepted by the interrupting device.

Polled Interrupt →

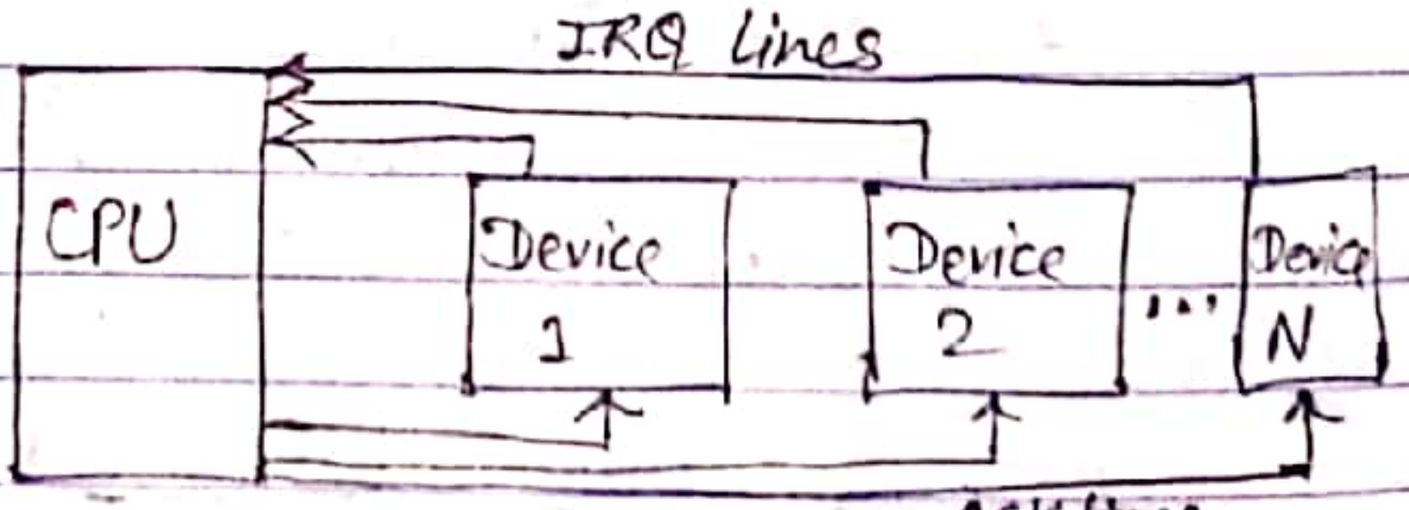

fig. Polled Interrupt

In a computer, a polled interrupt is a specific type of I/O interrupt that notifies the part of the computer containing the I/O interface that a device is ready to be read or ~~art~~ otherwise handled but does not indicate which device. The interrupt controller must

Date.
Page No.

poll (send a signal out to) each device to determine which one made the request. Polled interrupts are handled using software and are therefore slower compared to vectored interrupts.

3) 8259 Interrupt Controller:

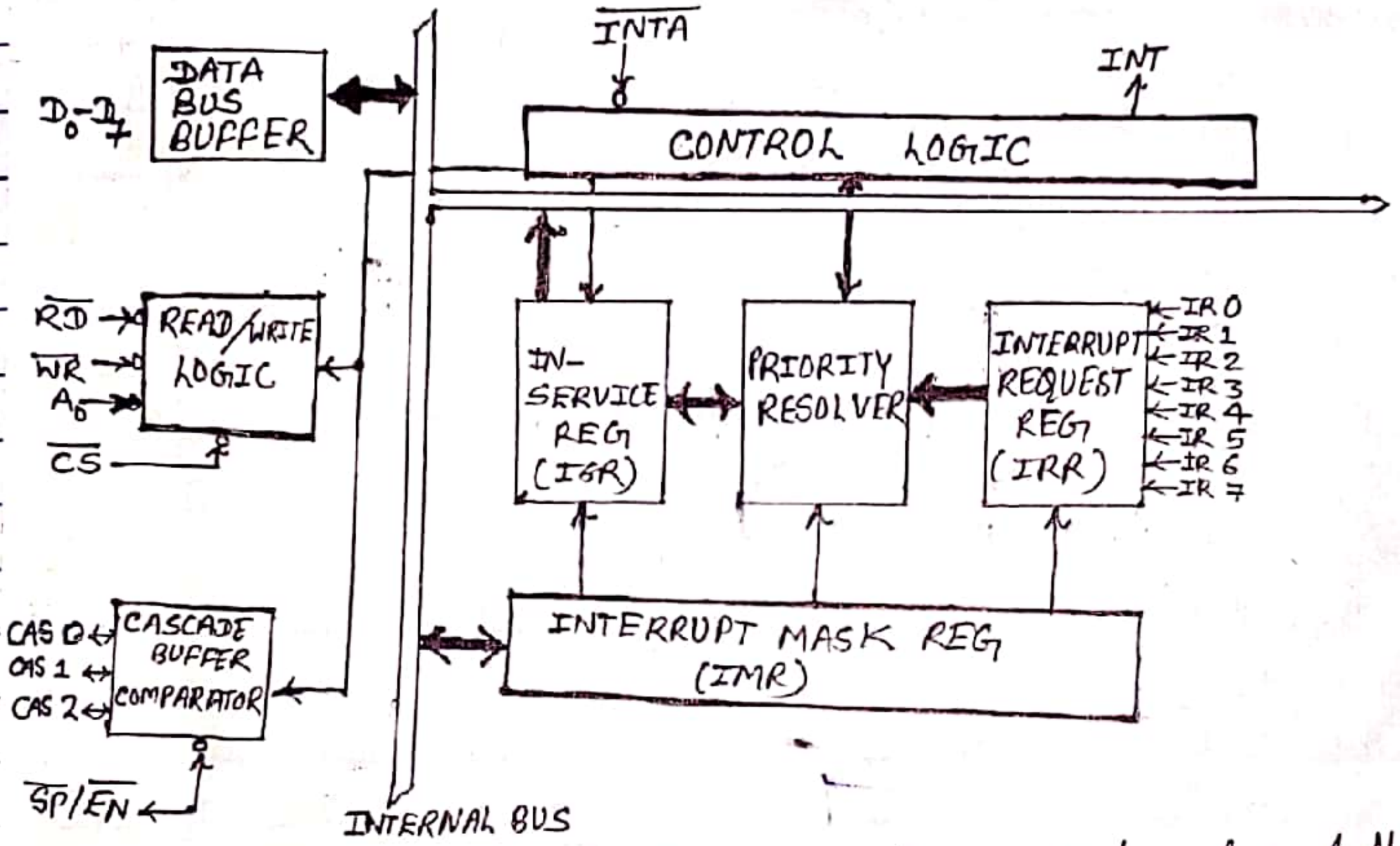

fig. Block Diagram of 8259 Interrupt Controller

The following steps take place during the operation of 8259 A.

i) One or more interrupt request lines go high requesting the service.
ii) The 8259A resolves the priorities and sends an INT signal to the MP.
iii) The MP acknowledges the interrupt by sending INTA (bar).
iv) After the INTA (bar) has been received, the opcode for

Date.
Page No.

the call instruction (CDH) is placed on the data bus.

v) Because of the CALL instruction, the MP sends two or more INTA(bar) signals.

vi) At the first INTA(bar), the 8259A places the low order 8-bit address on the data bus and at the second ~~INTA(bar), the~~ INTA(bar), it places the high order 8-bit address of the interrupt vector. This completes the 3-byte CALL instruction.

vii) The program sequence of the MP is transferred to the memory location specified by the CALL instruction.

Priority modes:

i) Fully Nested mode
→ IR0 has the highest priority and IR1 ... to IR7 have the decreasing priorities.

ii) Automatic rotation mode
→ First priority changes to the last after it's service.

iii) Specific rotation mode
→ This is user selectable or programmable, which means priority can be selected by programming.

Features:

i) It manages 8 interrupt requests.
ii) It can solve 8 levels of interrupt priorities in variety of modes.
iii) It can mask each interrupt request individually.
iv) It can be set up to work with either the 8085 MP mode or the 8086/8088 MP mode.
v) With cascading additional 8259A devices, the priority scheme can be expanded to 64 levels.
vi) The 8259A has the abilities such as reading the status and changing the interrupt mode during a program execution.