Unit6
1

Sequential Circuits

By the name the output of any circuits depends upon the number of sequence means that the previous result also play the role for generating the fresh output. Any circuit in which the result is generated by processing the current inputs as well as the previous output is called the sequential circuit.

In case of the combinational circuits the output completely depends upon the present inputs. There are no any memory element for storing the outputs. Also if we want to store that output for further processing we must use the concept of the memory and this task is only possible by using the concept of the sequential circuits. The sequential circuit consists of combinational circuits along with the memory element and hence the output generated by the sequential circuit are mostly dependent upon the present inputs as well as the previous output of the combinational circuit which is already stored in any memory element. The information stored in memory at any time defines the state of the sequential circuit. These circuits are classified into two types depending upon the timing signals—

(i) Synchronous sequential circuits

(ii) Asynchronous " "

Here the synchronous sequential circuit is the system whose behaviour can be defined from the knowledge of its signals at discrete instants of time. where as the asynchronous sequential circuit depends upon the order in which the input signals change and can be affected at any instant of time. The block diagram for the sequential circuit is given below

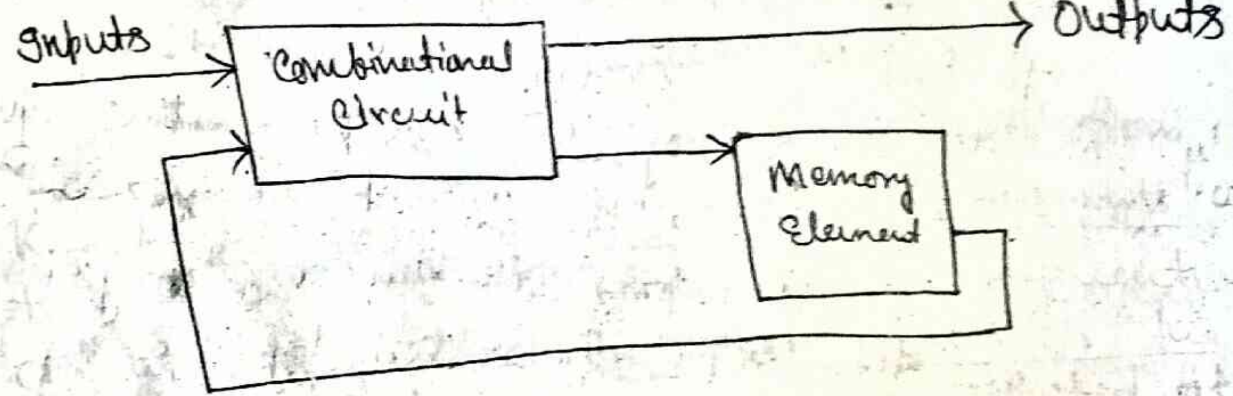


fig:- Block diagram of sequential circuits

The different elements used in the sequential circuits as storing element are also known as the flipflops. we can also state that the flipflops are capable of storing 1 bit information

2

Flip Flop:-

The basic memory element used to store one bit information is called flip flop. we can also defined the flip flop as the sequential circuit having memory device which is capable of storing one bit information. Flip flop has two outputs one the true value and other the complement value. The true value is indicated by Q where complement value is indicated by Q'. A flipflop maintains its binary state until directed by the clock pulse to switch states. Depending upon the number of inputs and state of affection the flip flops are classified into different types. Also the different types of the flip flops posses the following common characteristics.

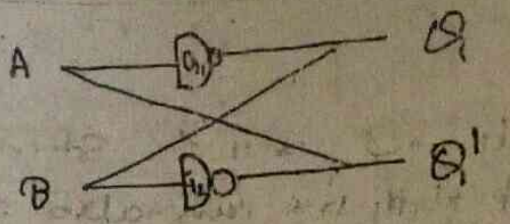
i. The outputs Q & Q' are always complementary to each other.

ii The circuit of flip flop has two stable states set or 1 and reset or 0.

iii If the circuit is in set (1) it continues to remain in this state and similarly if it is in reset (0) it continues to remain in this state until the external signal is changed to change this state

Latch

Latch helps us to understand the operation of flip-flop. It is the circuit diagram having the inverters. The output of one inverter is connected to the input of the second inverter & the output of the second inverter is fed to the input of the first inverter as shown in the figure below-



Latch

Q = 0
Q' = 1 Reset state

Q = 1
Q' = 0 set state

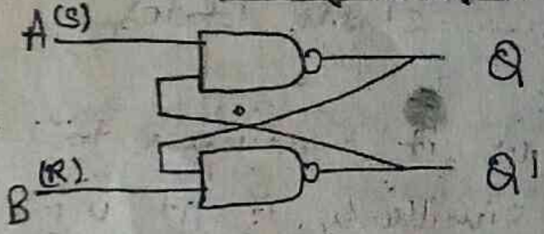
This circuit has two state one is set and other reset.

If output of G1 is 1 ie Q = 1 the input of G2 is 1 and hence output of G2 will be 0 that makes A = 0 and Q = 1 (set state)

If Q = 0 then input of G2 is 0 and hence the output Q' of G2 become 1 (reset state)

The basic flip flops can be designed from either two NAND gates or two NOR gates, the circuit diagrams as as shown below.

FF. using NAND gate

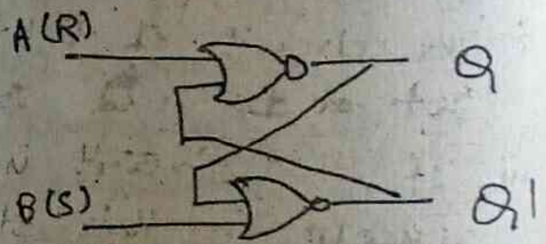


Logic diagram

S	R	Q	Q'	
1	0	0	1	
✓1	1	0	1	after S=1 ,R=0
0	1	1	0	
✓1	1	1	0	after S=0 R=1
0	0	1	1	

Truth table

FF. using NOR gate



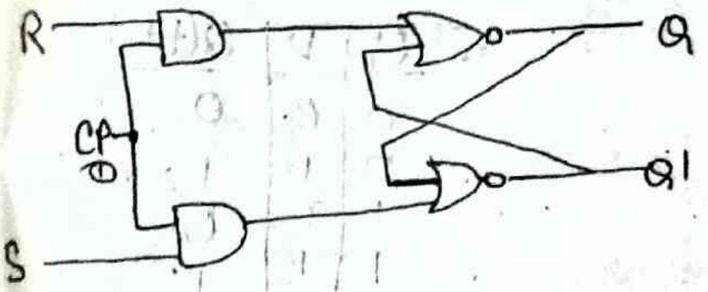
Logic diagram

S	R	Q	Q'	
1	0	1	0	
✓0	0	1	0	after S=1, R=0
0	1	0	1	
✓0	0	0	1	after S=0, R=1
1	1	0	0	

Truth table

RS-Flipflop:-

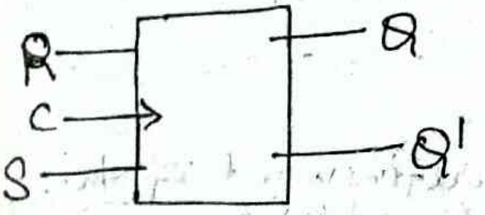
This is the simplest type of flipflop having two inputs S for set and R for reset. Also the two outputs Q for true value and Q' for the complement value. we can design the RS flipflop by using NOR flipflop and AND gates and the clock pulse as shown below



Logic diagram

Q	S	R	Q(t+1)
0	0	0	0 → no change
0	0	1	0 → reset
0	1	0	1 → set
0	1	1	indeterminate
1	0	0	1 → no change
1	0	1	0 → reset
1	1	0	1 → set
1	1	1	indeterminate

Characteristic table

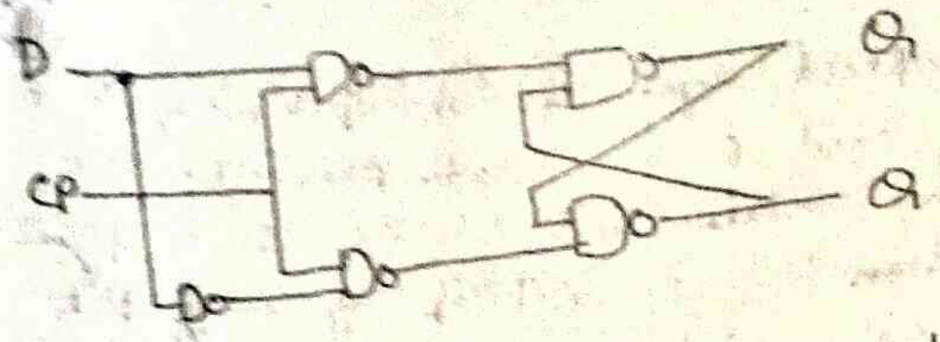


Graphic Symbol

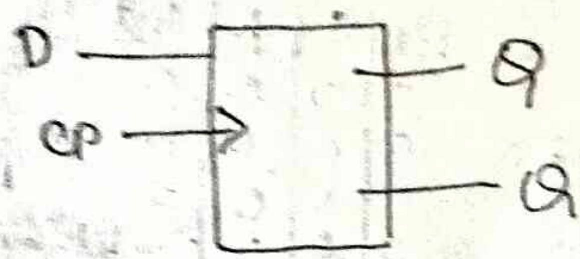
D-flipflop:-

The D-flip flop is the modification of the clocked RS flipflop. Here we use the NAND gate flipflop using ~~three~~ more NAND gates in place of the AND gate and the inputs R & S are replaced by only single input D with true value and the complement value as shown below—

Note:- First P/Z concern Pg no 22 also



Logic diagram with NAND gates



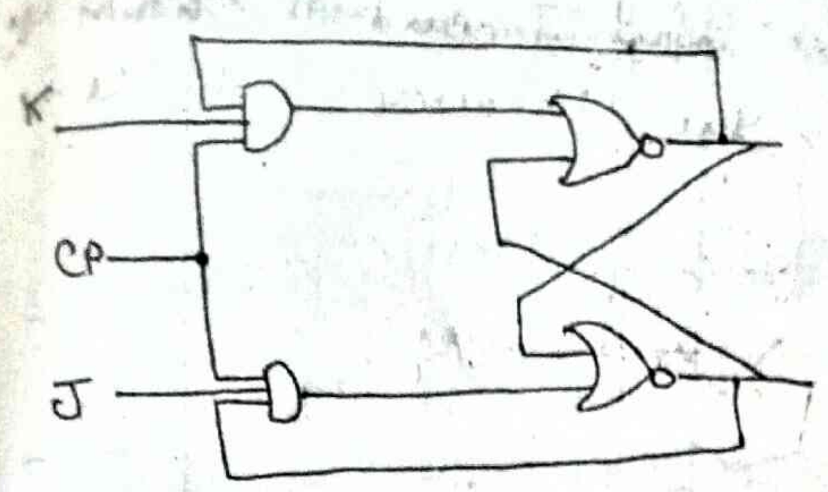
Graphic symbol

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

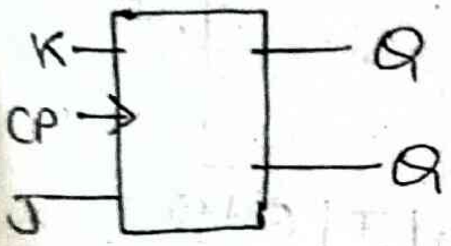
Characteristic table

JK flip flop

This is considered as the refinement of the RS flipflop. The uncertainity of SR flipflop means when S=R=1 is solved by the help of JK flipflop The inputs J & K behaves like inputs S & R to set & clear the flip flop. Just in the case of S R flipflop if Q=1 it switches to Q'=0 & vice versa the diagram alongwith the characteristics table is shown as below. Here we are taking NOR flipflop with two AND gates having the inputs J & K along with Q' and Q respectively with the clock pulse.



Logic diagram



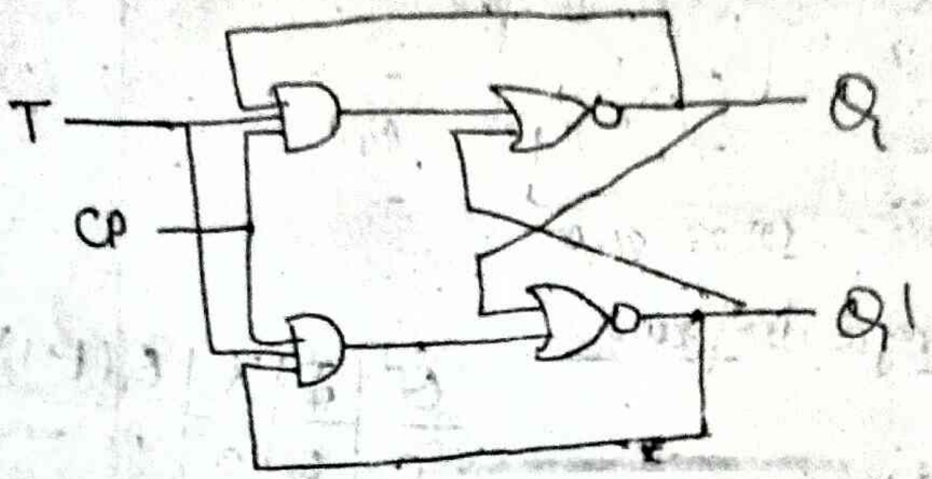
Graphic symbol

Q	J	K	Q(t+1)
0	0	0	0 → no change
0	0	1	0 → no change
0	1	0	1 → set
0	1	1	1 → set
1	0	0	1 → no change
1	0	1	0 → reset
1	1	0	1 → no change
1	1	1	0 → reset

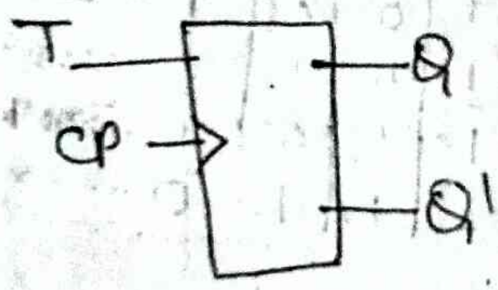
Characteristic table

T flip flop

If the JK flipflop is replaced by only single input form we obtain the T flipflop. Means we take both J & K as a single input. This flipflop just complement the input. Means the output of the flipflop is the complement of the input value and hence it is also known as the toggle flipflop. The logic diagram can be easily obtained by replacing J & K in the JK flipflop by single input T and is shown below alongwith the characteristic table.



Logic Diagram



Graphic Symbol

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic table

Master Slave Flip Flop

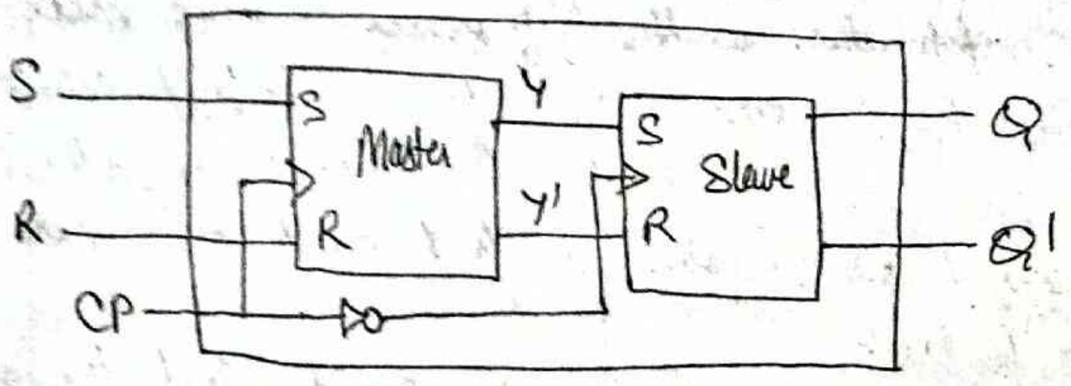
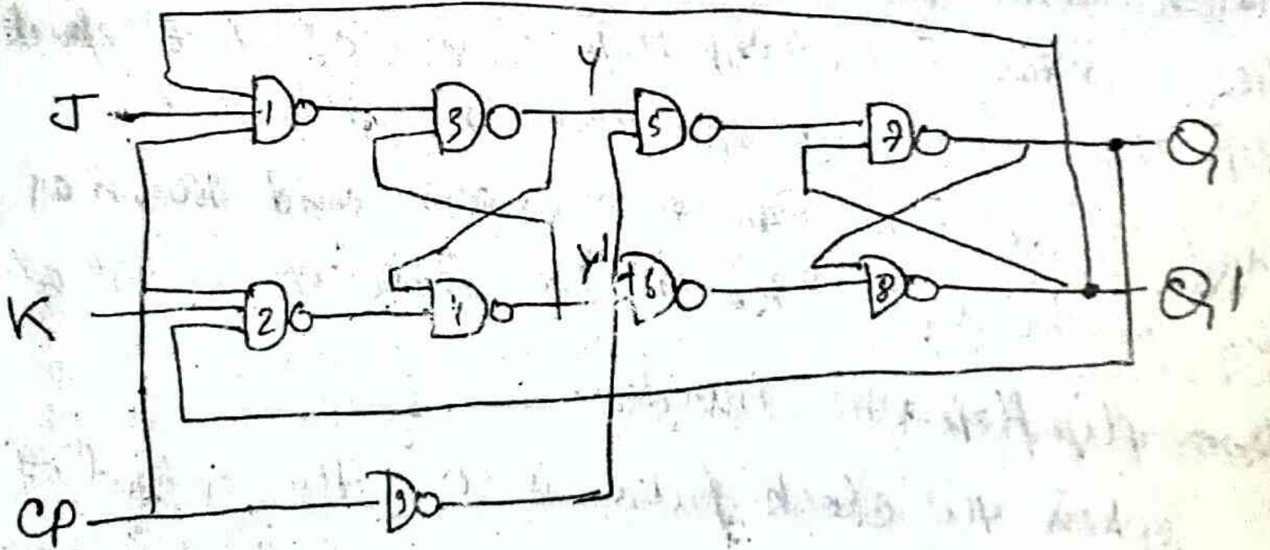


fig:- Master Slave flip flop

Master means the main or superior and slave is the secondary. The flip flop consists of two separat flip flops and out of them one acts as the master and other as the slave and known as the master slave flip flop. The flip flop consists of two flip flop one inverter.

When the clock pulse is 0 the output of inverter become one means the input for the slave become 1 and the flipflop is enabled and the output Q is equal to Y while Q' is equal to Y' when CP is 0 the master flipflop become disabled. Also when CP becomes 1 then the master flipflop is enabled where as the slave flipflop is isolated as long as the pulse is at its 1 level, becaus the output of the inverter is 0. The process of ~~continues~~ enabling and isolating continues. Thus in the master slave flipflop it is possible to switch the outhut of the flipflop and its input information with the same clock pulse. It must be realized that the S input could be come from the output of another master slave flipflop that was switched with the same clock pulse.

Master flipflop also can be constructed by using JK flip flop as well as both the SR and JK flipflop as follow.



Master slave flipflop using JK flip-flop

Triggering of the flip flops

The momentary change in input signals change the state of the flipflop. This change is called the trigger. The transition that cause the change is called triggering the flip flop. The asynchronous flip flops requires an input trigger defined by change of signal level. This level must be returned to its initial value (ie 0 in case of NOR flipflop and 1 in case of NAND flipflop) before a second trigger is applied. The clocked flipflops are trigered by the help of clock pulses. The pulses starts from initial values 0 and go to 1 & after short interval of time returns to its initial value 0.

A clock pulse may be either positive or negative: positive clock remains at 0 during the interval between pulses and goes to 1 during occurance of a pulse. The positive transition is define as the positive edge and the negative transition is known as the negative edge. Both pulses are given as follows

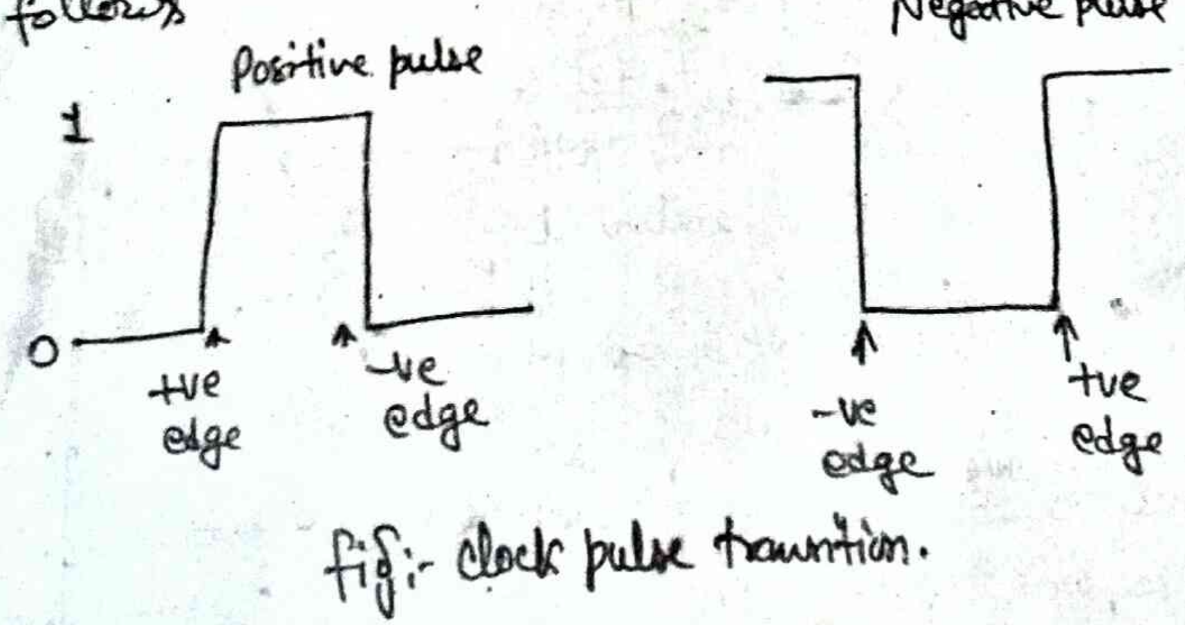


fig:- clock pulse transition.

SR-FF

S	R	Q
0	0	no change
0	1	0 (Reset)
1	0	1 (set)
1	1	? (not allowed)

Clocked-SR·FF

S_n	R_n	Q_{n+1}
0	0	Q_n (nochange)
0	1	0 reset
1	0	1 set
1	1	? (not allowed)

Edge triggered Flipflop:-

The flipflop that synchronises the state changes during the clock pulse transition is the edge triggered flip flop. The output transition occurs at a specific level of the clock pulse. when the pulse input level exceeds this level the inputs are locked out and flipflop is then unresponsive for the changes in inputs until the clock pulse returns 0 and another pulse occurs. Some flipflops cause a transition on the positive edge of the pulse and some cause a transition on the negative edge of the pulse and are known as the positive and negative edge triggered flipflop. The logic circuit for edge triggered flipflop is as follow

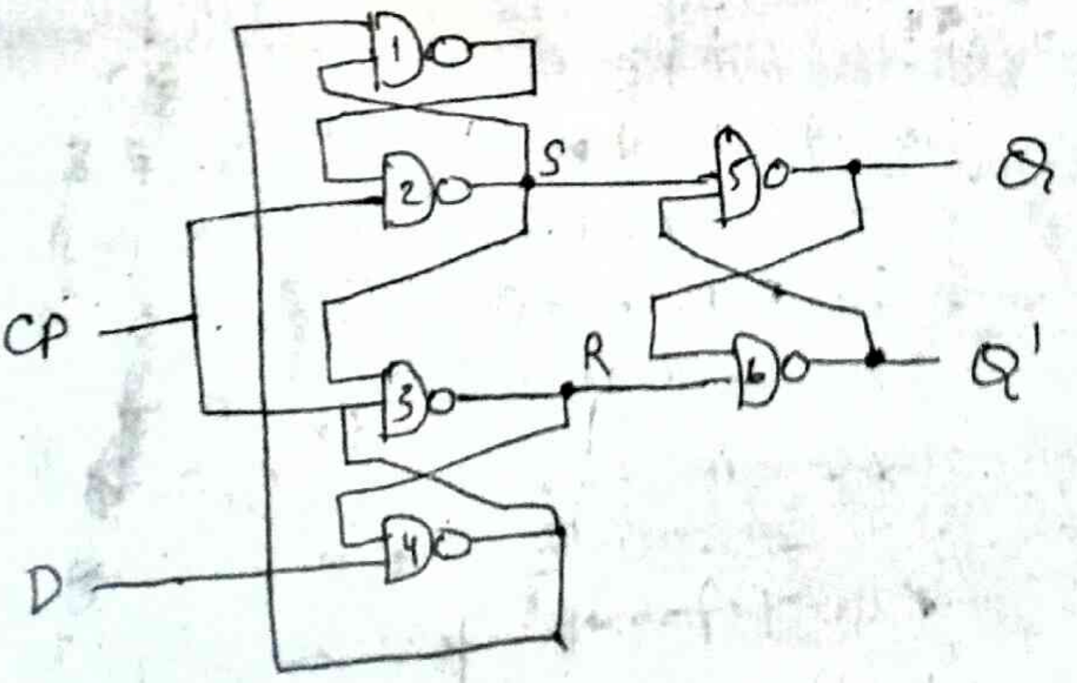


fig:- D-type flip flop with +ve edge

Question Implement a full adder with a decoder and two OR gates.

Soln As we know that the full adder produce sum and carry. Also from the truth table of the ~~truth~~ full adder we can obtain the sum and carry along with the function for the circuit in the form of sum of minterms as follow.

			S	C
a	b	c	Sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Here

$S(x,y,z) = \Sigma(1,2,4,7)$

$C(x,y,z) = \Sigma(3,5,6,7)$

Since here are 8 minterms and so we need 3 to 8 line decoder as follow.

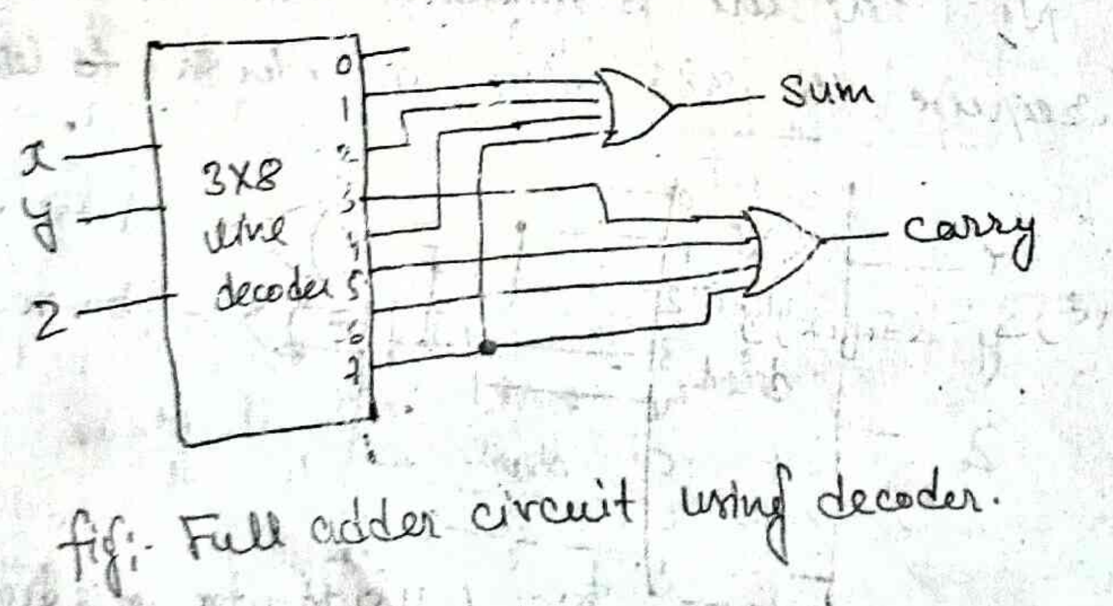


fig:- Full adder circuit using decoder.

Question Implement the full subtractor using the decoder.

Soln As we know that in case of the full subtractor the circuit generates two outputs difference(d) and borrow (b). Also the truth table for the full subtractor as given as follow and according to the full subtractor's tt the functions for the circuits output d and b are as follows

x	y	z	d	b
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
D	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Also the functions for the difference (d) and borrow (b) are as follow in terms of minterms.

$$d(x,y,z) = \Sigma(1,2,4,7)$$
$$b(x,y,z) = \Sigma(1,2,3,7)$$

Now here are 8 minterms and hence we require the 3X8 line decorder as follows

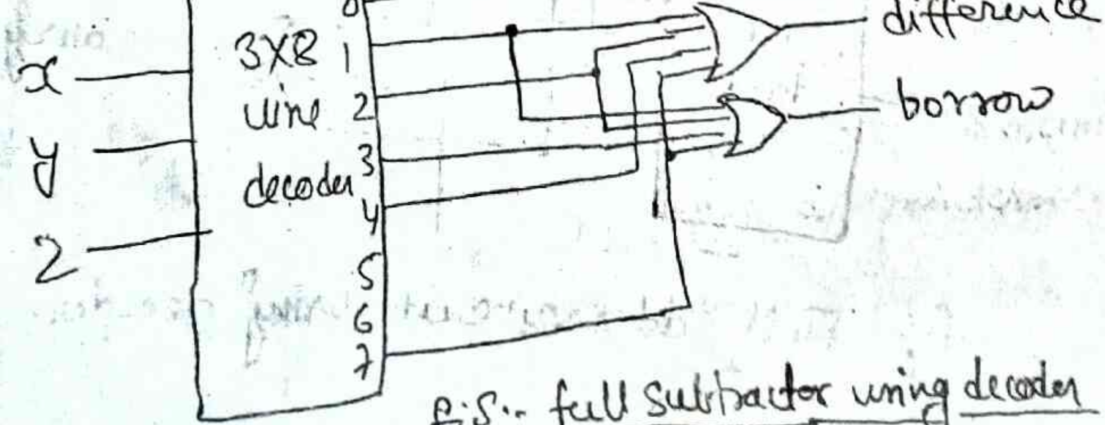


fig:- full subtractor using decoder

NAND decoder looks like this with its inverted truth table.

Hence for NAND gate decoder only one output can be low and equal to logic '0' at any given time with all other output being high at the logic '1'.

Hence the decoder with universal NAND gate is drawn.

Flip flop & applications

- * Flipflop is storing element capable of storing 1 bit information.
- * considered as the sequential circuit can either store 1 or 0. Also known as bistable element.
- * It generate two outputs true value Q & complement value Q'.
- * 1 state of flip flop is the set condition for flip flop
- * 0 State of flip flop in the clear / reset condition for flip flop.
- * It store 0 or 1 within it as long as power is on.

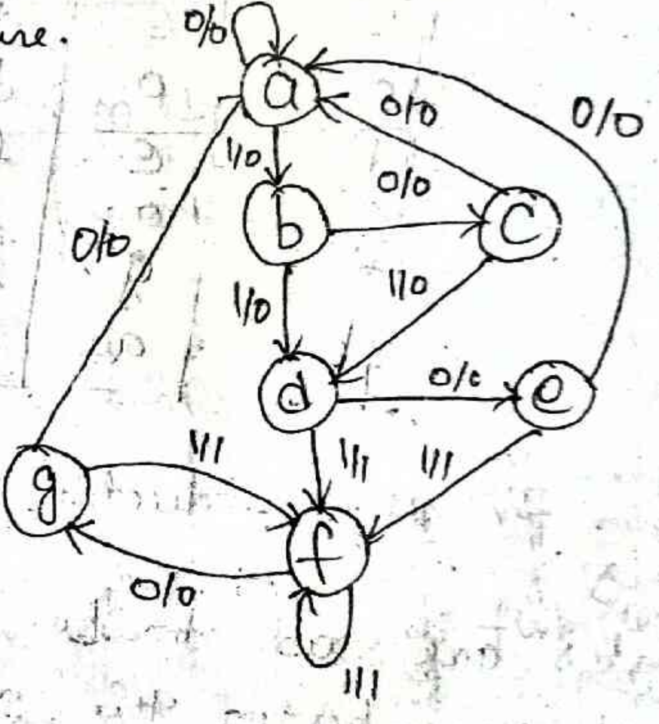
Applications

- * It is used for designing storing elements.
- * Registers are designed by using flipflops
- * Latches can also designed by using flipflop.
- * counter are designed by flipflop
- * FF can be considered as the basic building block of digital electronics.

State Reduction diagram / table

The process of reducing the no of flipflops in any sequential circuit is called the state reduction. These process are concerned with the procedures for reducing the no. of states in the state table while keeping the external input-output unchanged. Since n flipflops produce 2n states. Also a reduction in the number of states may or may not result in a reduction in the number of flip flops.

Consider an example for illustration of the state reduction procedure.



Here we consider the input sequence 01010110100 starting from the initial state (a). Each input of 0 or 1 produces an output of 0 or 1 and causes the circuit go to the next state, the output seqr and the state sequence for the given input sequence as follows.

State	a	a	b	c	d	e	f	f	g	f	g	a
input	0	1	0	1	0	1	1	0	1	0	0	
output	0	0	0	0	0	1	1	0	1	0	0	

we proceed to reduce the no. of state for this example we require the state table as follow

Present State	Next state		output	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

Algorithm for state reduction is given without proof as

Two states are said to be equivalent if, for each member of the set of inputs they give exactly the same output and send the circuit either to the same state or to an equivalent state.

Hence when two states are equivalent one of them can be removed without altering the input output relationships.

∴ Applying this algorithm & going through state table we look for two present states that go to the same next state & having the same output for both input combinations.

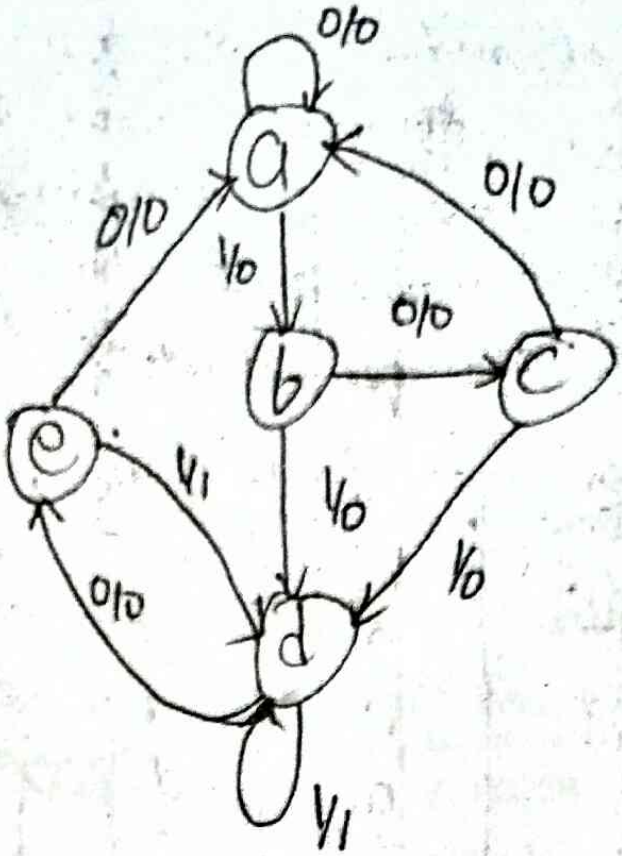
Reducing the state

Present state	Next state		output	
	x = 0	x = 1	x = 0	x = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

Reduced table

Present State	Nextstate		Output	
	x = 0	x = 1	x = 0	x = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

Now the diagram can be represented as follow-



We can represent the state as follow

State	a	a	b	c	d	e	d	d	e	d	e	a
input	0	1	0	1	0	1	1	0	1	0	0	
output	0	0	0	0	0	1	1	0	●	0	0	

Here the States froms seven to five is reduced and hence the circuit consists of the lesser number of the flip flops having simillar functionality.

Mod 6 Synchronous counter!-

Also for mod5, mod, 10 , mod 12 etc etc counters

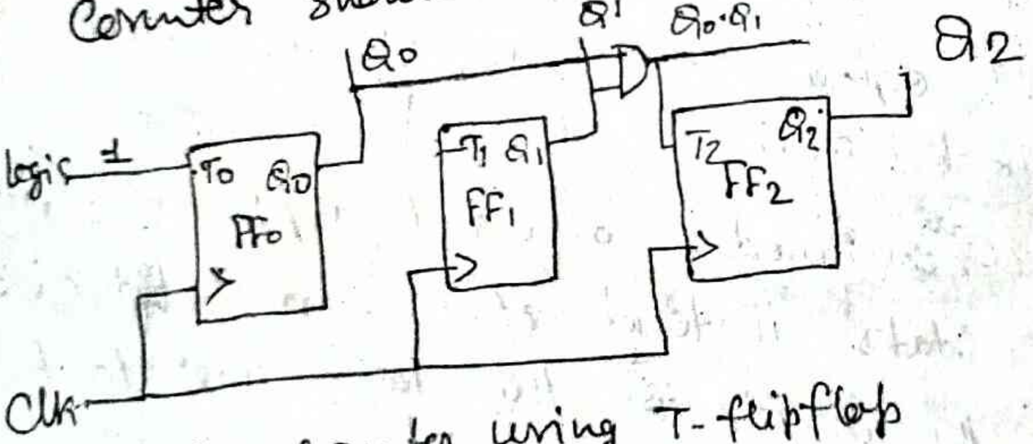
The synchronous counters are considered as the high speed counters in comparision to the counters. In these counters all the flip floks are clocked simultaneously. Also we know that counter having n flip flop is able to count 2^n states. means if we use $n=2, 3, 4, 5$ then the counter is able to count 4, 8, 16 32 states depending upon the value of n. some time we want to count upto desired count say 5, 6, 10 and which is not equal to 4, 8, 16, 32 etc. but in between of these. If we are required to count upto 5 states or 6 states instead of 8 in 3 bit counter then the reset of the states are to be skipped and counter is to get reset. consider the following truth table for 3 bit counter.

Clock pulse	Q_2	Q_1	Q_0	count
Initial	0	0	0	0
1st	0	0	1	1
2nd	0	1	0	2
3rd	0	1	1	3
4th	1	0	0	4
fifth	1	0	1	5
6th	1	1	0	6
7th	1	1	1	7

Reset to 000

Skipped

Here countes with 6 states is called mod 6 counters. mod 6 counts from 000 to 101 and as soon as the count 110 appears the counter should be reset to 000



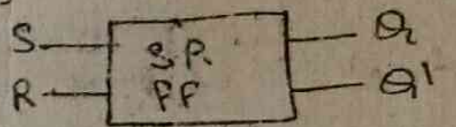
Syn counter using T-flipflop

<u>Procedure for synchronous counter design</u>

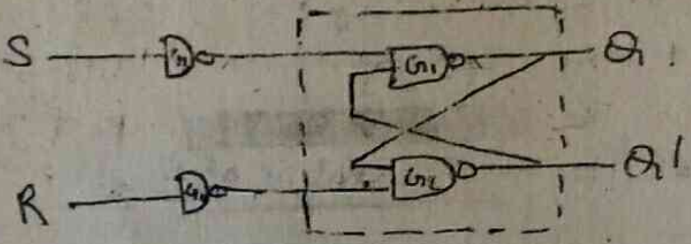
* Find the number of flip flops required.
* write the count sequence in tabular form ie write the desired output
* According to the ~~mod~~ excitation table of ff simplify K map & design the circuit using flipflops & other gates according to the simplified expression.

SR- Flip flop

This is the simple flip flop having two inputs S (set) & R (reset) and two outputs Q & Q'. as shown below



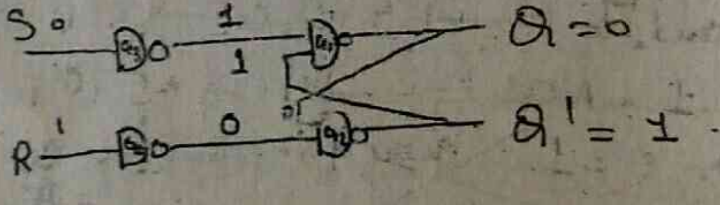
The circuit diagram of SR- ff can be made by the help of latch and two NAND gates as shown below



The output of this circuit at a particular time will depend upon the two inputs S & R also on the state of the latch (Q = 0 & Q = 1)

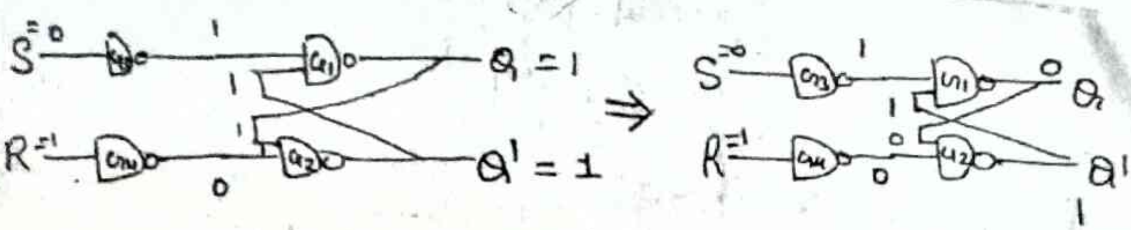
There may be following four cases

<u>Ist case</u> (a) <u>S = 0 R = 1 & Q = 0</u>



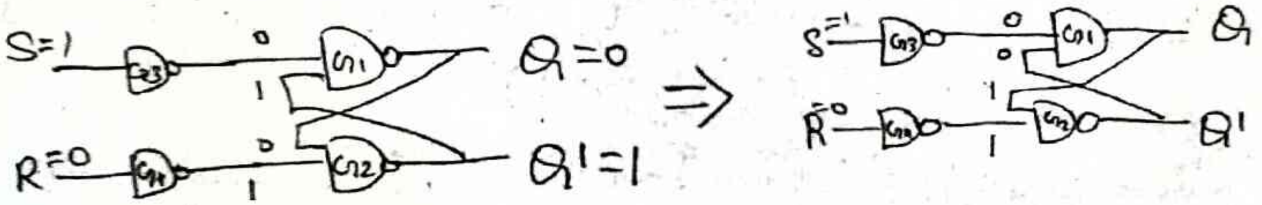
Here when S = 0 O/P of G3 is 1 & when R is 1 the O/P of G4 is 0 since Q = 0, therefore both inputs of G2 are (0,0) which makes Q' = 1. Now both inputs of Gate G1 are (1 1) which makes Q = 0, Hence the conclusion can be given as outputs Q = 0 & Q' = 1 ie the O/P is in reset state.

(b)



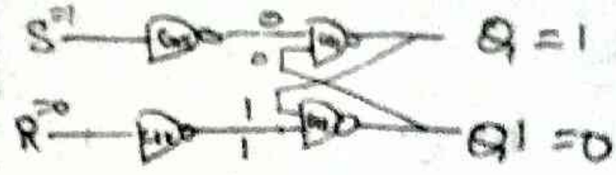
Since $Q=1$ therefore both inputs of gate G_2 are (0,1) which makes $Q'=1$, now both inputs of gate G_1 becomes (1,1) which makes $Q=0$, therefore in this case there is Change In previous output. Again due to change in previous o/p the input of gate G_2 are (0,0) which makes $Q'=1$ and inputs of G_1 are (1,1) which makes $Q=0$. This is the stable state, the state of reset. Hence when $S=0$ & $R=1$ the output is always 0 (reset).

Case II (a) $S=1, R=0, Q=0$



when $S=1$ o/p of of G_3 is 0 & when $R=0$ o/p of $G_4=1$ Since $Q=0$ and hence both inputs of G_2 are (1;0) which make $Q' = 1$. Now both inputs of G_1 are (1,0) which makes $Q=1$. There fore there is Change in previous output. Again due to Change in previous output the input of G_2 are (1,1) which make the output $Q'=0$ & inputs of G_1 are (0,0) which makes $Q=1$. This is the stable state having output $Q=1$ and $Q'=0$ ie the output is Set State.

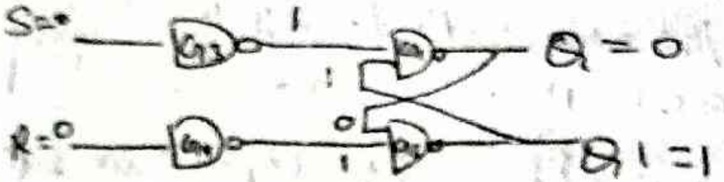
(b) S=1, R=0, Q=1



In this case both inputs of Gate G2 are (1,1) and hence Q'=0 and inputs of G1 are (0,0) and hence Q=1. This is the set state. Hence when S=1 & R=0 the output is always set.

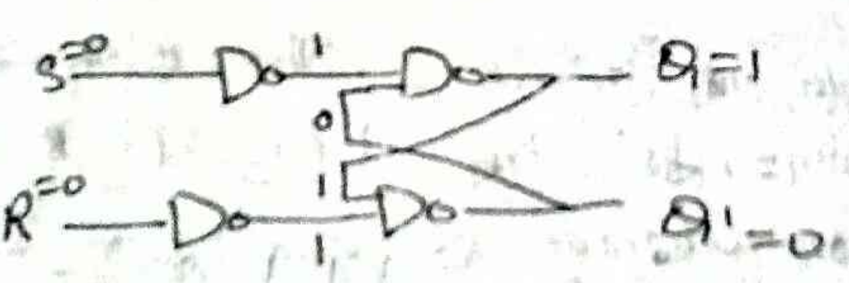
III rd case

(a) S=0, R=0 Q=0



When S=0 the o/p of G3 = 1 & when R=0 OP of G4 is 1 since Q=0 and hence both inputs of G2 are (0,1) and o/p of G2 ie Q'=1. Now both inputs of G1 are (1,1) that makes Q=0 Hence there is no change In the previous output.

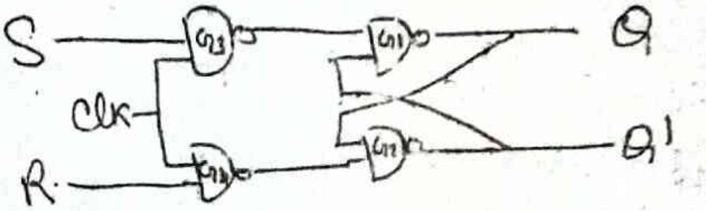
(b) S=0, R=0, Q=1



Here is also no change in the previous output hence when S=0 R=0 there is no change in the previous outputs.

Clocked SR flip flop

If we add a clock input to SR flip flop then it becomes the clocked SR flip flop. The diagram can be shown as follows-



In this circuit if a clock pulse is present (Clk=1) its operation is exactly the same as SR flipflop. On the other hand, when the clock pulse (clk=0) the output of the Gates G3 & G4 are 1 irrespective of the values of S or R. In this case if Q=1 it will remain 1 and if Q=0 it will remain 0. Hence when clk=0, ~~Hence when clk=o~~ there is no change in the flipflop state. Hence the circuit responds to the inputs S and R only when the clock is present (ie clk=1)

The truth table of clocked SR flip flop can be shown as follows when clk=1

Inputs		outputs
S_n	R_n	Q_{n+1}
0	0	Q_n no change
0	1	0 Reset
1	0	1 Set
1	1	? (not allowed)