Unit-3

Instruction Cycle

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Introduction:

Instruction cycle: The time required to execute and fetch an entire instruction is called instruction cycle. An instruction cycle consists of fetch cycle and execute cycle.

In fetch cycle CPU fetches opcode from the memory. The necessary steps which are carried out to fetch an opcode from memory constitute a fetch cycle. In fetch cycle instruction is fetched by the address stored in program counter (PC) and then stored in the instruction register.

The necessary steps which are carried out to ~~fetch an opcode from~~ m get data if any from memory to perform specific operation specified in an instruction constitute an execution cycle. The total time required to execute an instruction given by $IC = F_C + E_C$. The 8085 consists of 1-6 machine cycles or operations.

Machine cycle: The time required by the microprocessor to complete an operation of accessing memory or input/output devices is called machine cycle. This cycle may consists of 3 to 6 T-states.

T-states: One time period of frequency of microprocessor is called t-state OR It is defined as one sub division of the operation performed in one clock period. A t-state is measured from the falling edge of one clock pulse to the falling edge of the next clock pulse. Fetch cycle takes four t-states and execution cycle three t-states.

let address = 2050

higher order address ↑ ↑ lower order address

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Timing diagram: The necessary steps which are carried in a machine cycle can be represented graphically. Such graphical representation is called timing diagram.

Timing diagram consists of following things:-

i) Lower order address → It is the lower bit of address where opcode is stored. Multiplexed address and data bus $AD_0 - AD_7$ are used.

ii) Higher order address → It is higher bit of address where opcode is stored. Multiplexed address and data bus $AD_8 - AD_{15}$ are used.

iii) ALE → It provides signal for multiplexed address and data bus. If signal is high or 1, multiplexed address and data bus will be used as address bus. To fetch lower bit of address, signal is 1 so that multiplexed bus can act as address bus. If signal is low or 0, multiplexed bus will be used as data bus. When lower bit of address is fetched then it will act as data bus as the signal is low.

iv) RD (low active) → If signal is high or 1, no data is read by microprocessor. If signal is low or 0, data is read by microprocessor.

v) WR (low active) → If signal is high or 1, no data is written by microprocessor. If signal is low or 0, data is written by microprocessor.

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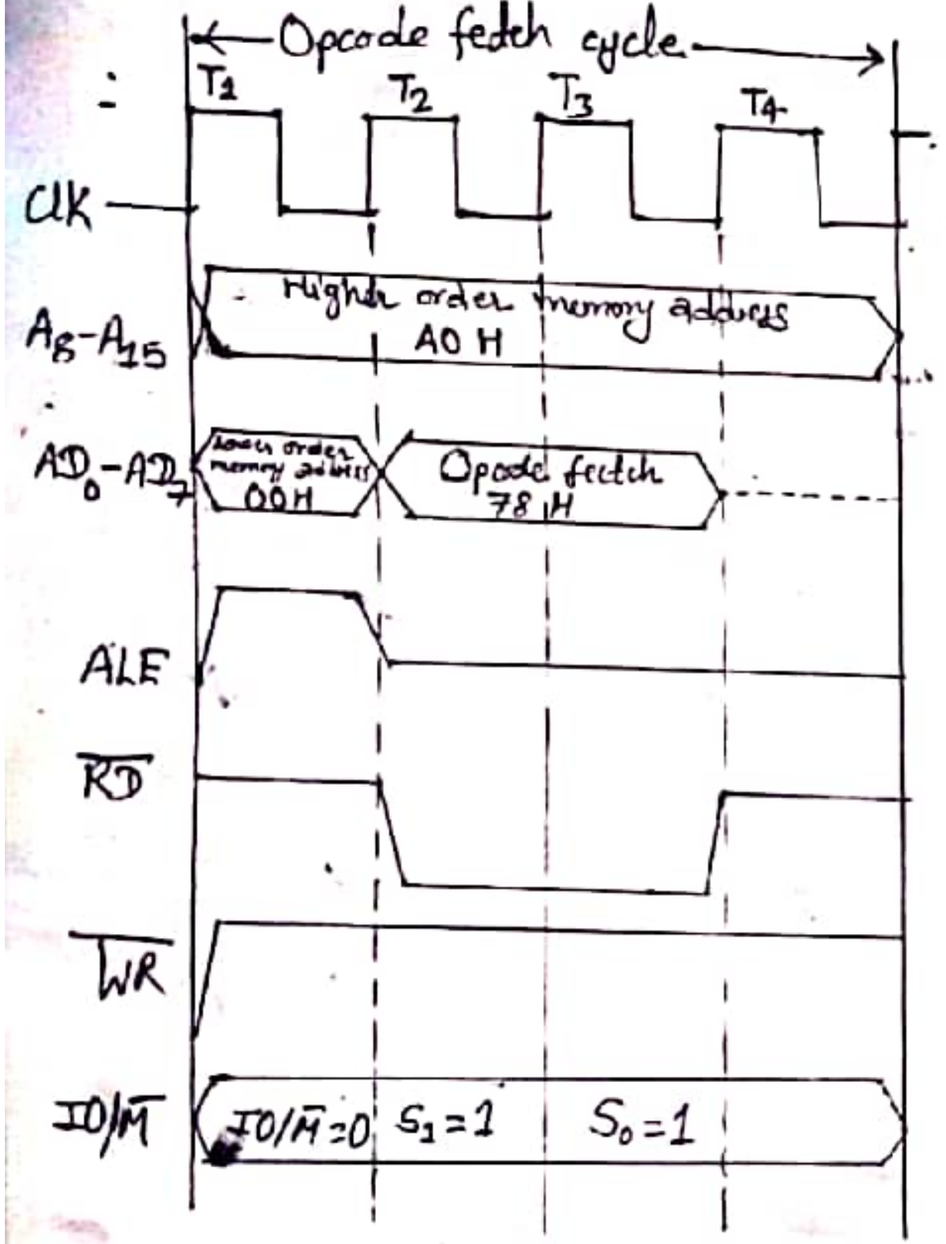
v) IO/M (low active) and S_1, S_0 → If signal is high or 1, operation is performing on input output. If signal is low or 0, operation is performing on memory. for IO/M. IO/M, S_1, S_0 are three status signals used in microprocessor. Below is the truth table for various combinations of status signals.

IO/M	S_1	S_0	Data bus status (Output)
0	0	1	Memory write
0	1	0	Memory read
0	1	1	Opcode fetch
1	0	1	IO write
1	1	0	IO read

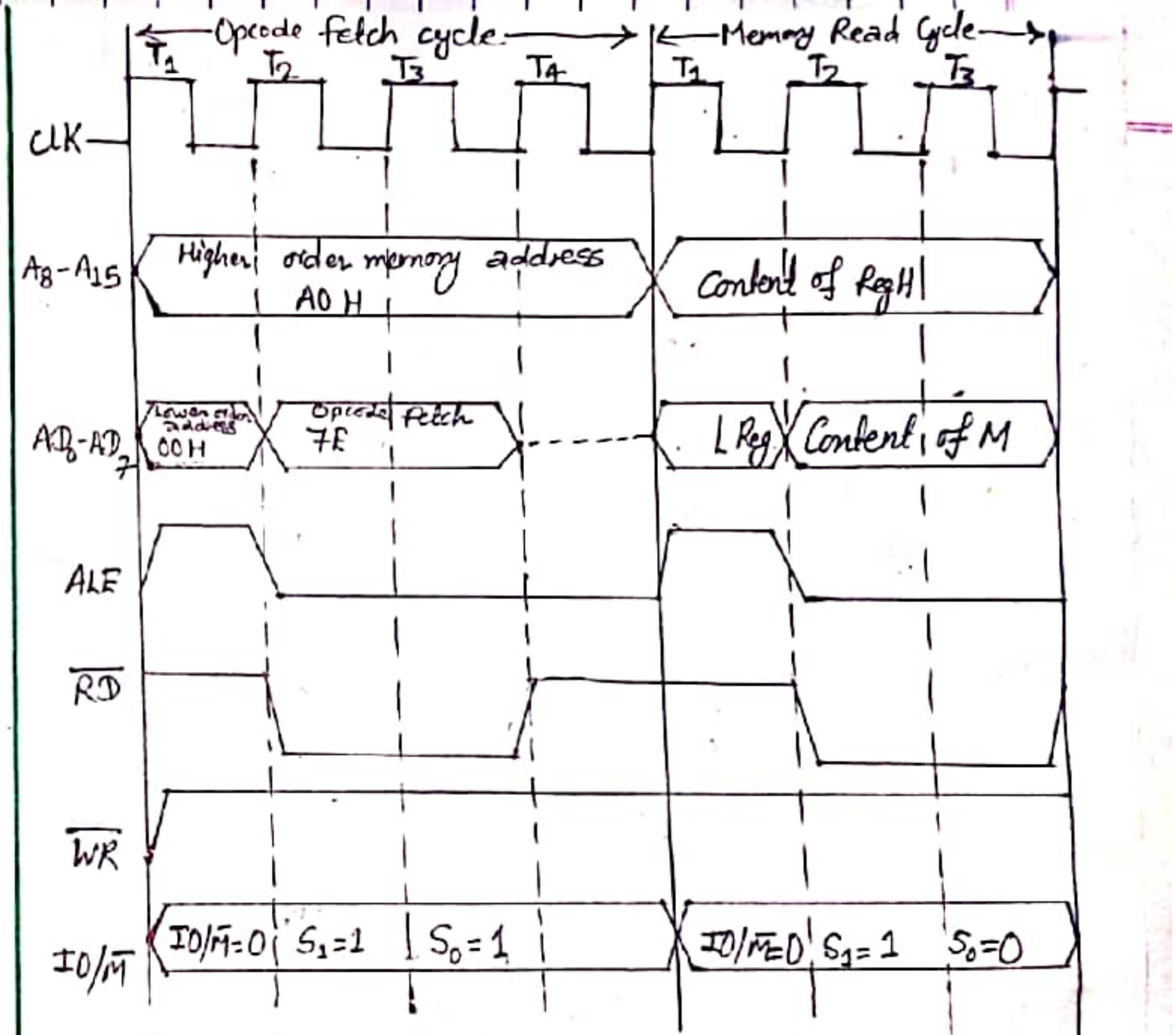
The timing diagrams of:

i) MOV
ii) MVI
iii) IN
iv) OUT
v) LDA
vi) STA

are as follows →

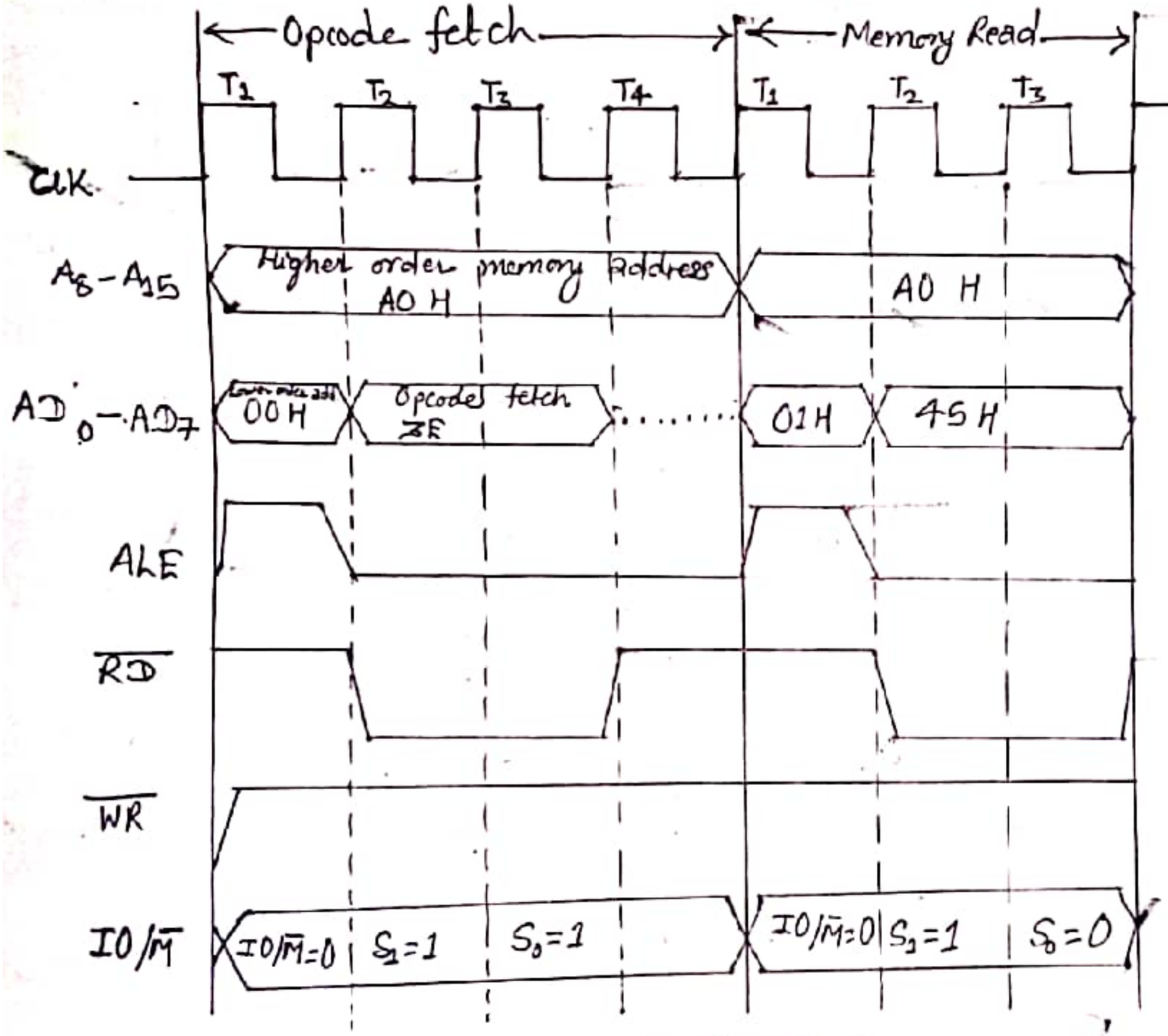


Timing diagram for MOV A, B with instruction A000 H



Timing diagram of MOV A, M with instruction A000 H

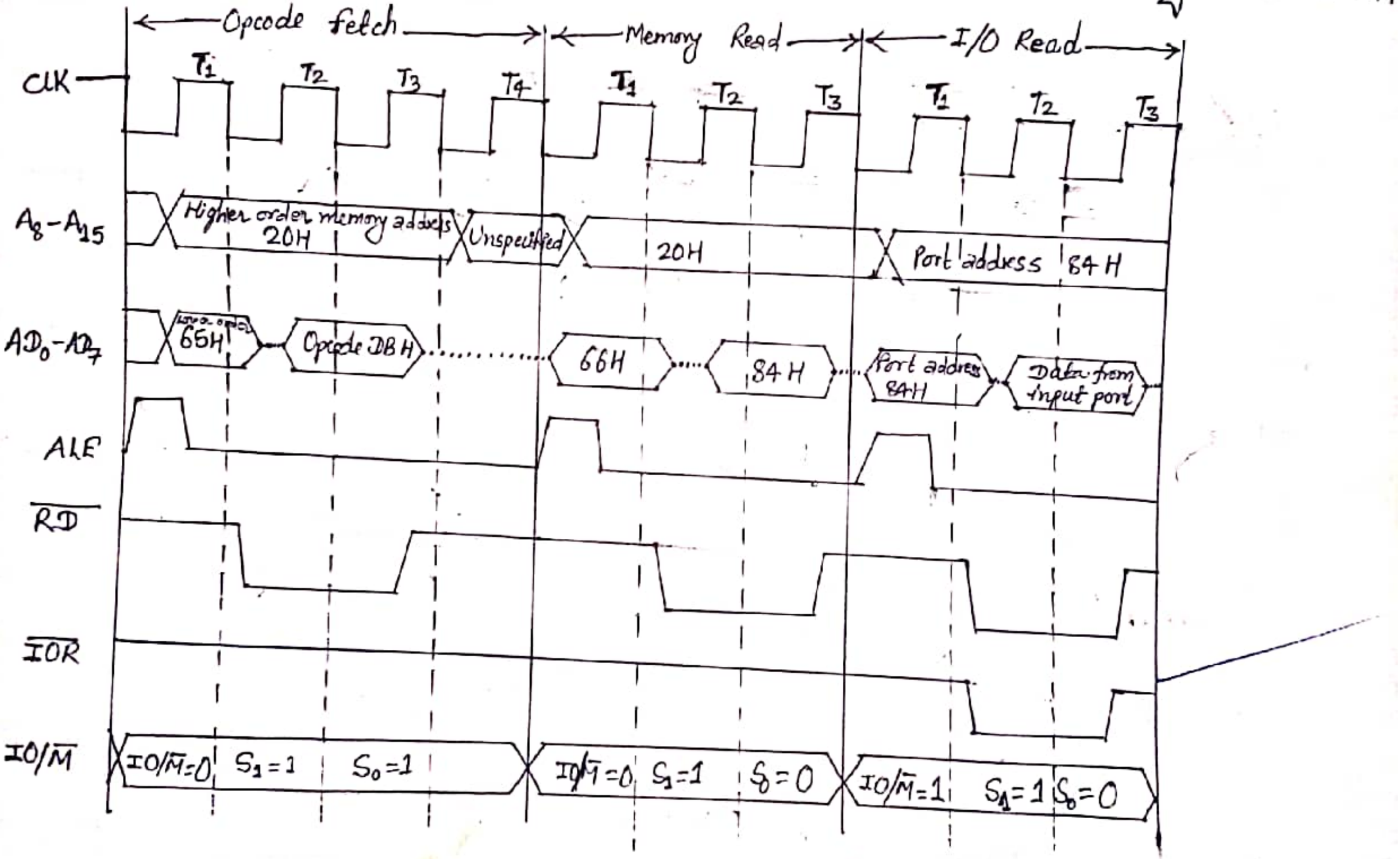
Let we assume that the given Instruction is located in memory address A000 H



Timing diagram of MVI, 45H

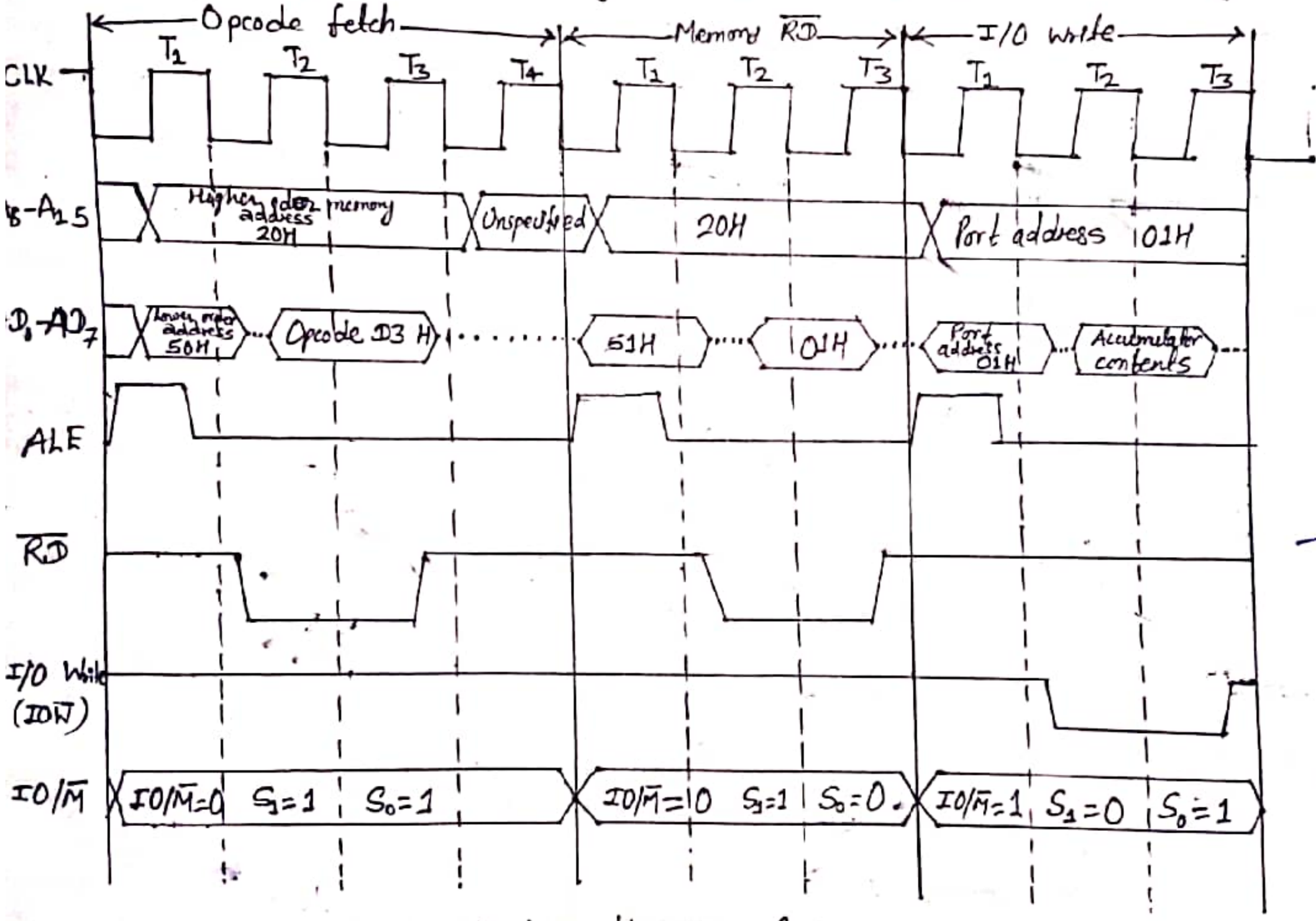
8/15

Let we assume that given instruction is located in memory address 2065H



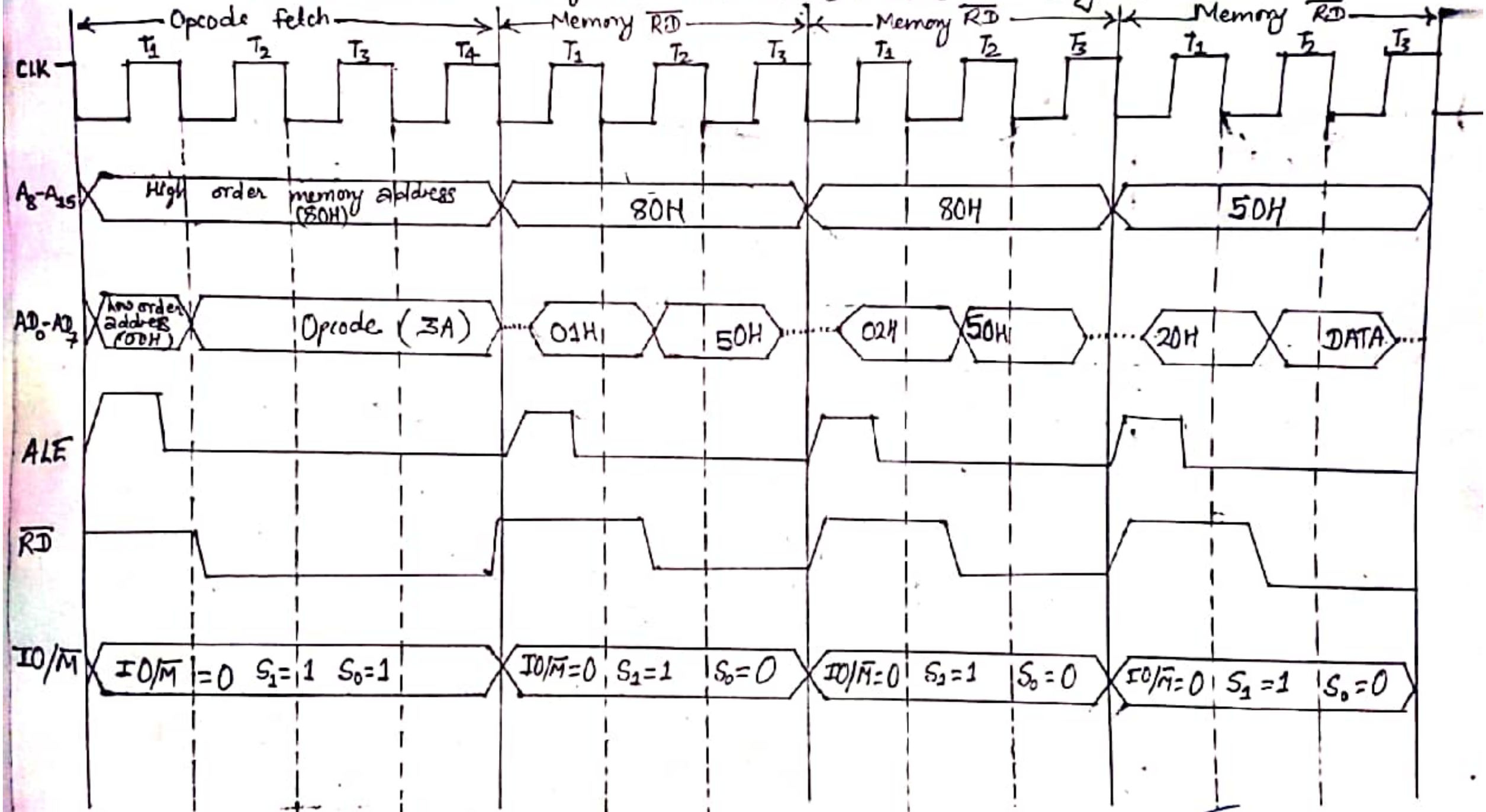
Timing diagram of IN, 84H

Let we assume that given instruction is located in 2050 memory address.



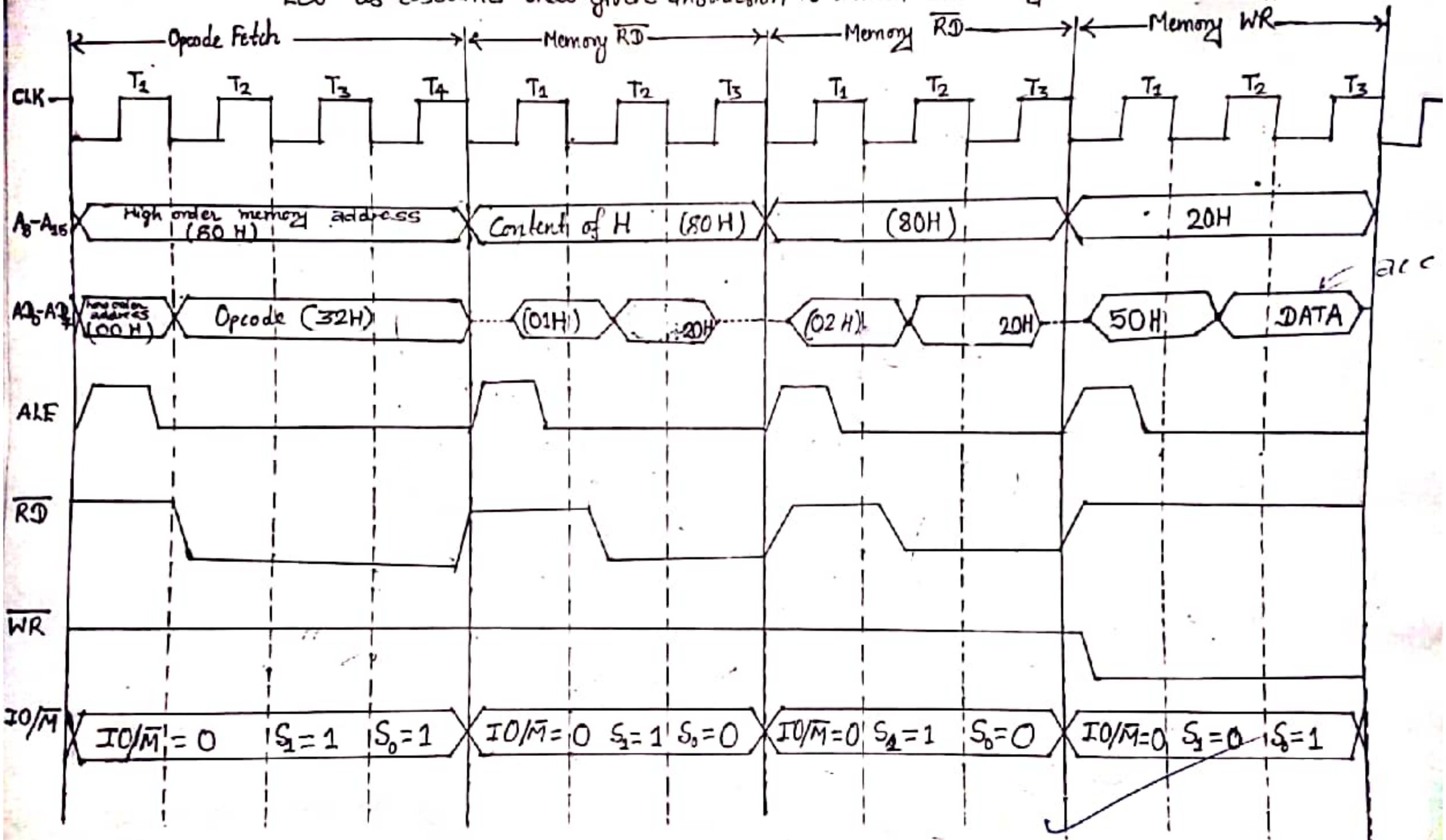
Timing diagram of OUT 01H

Let us assume that given instruction is located in memory address 8000H



Timing diagram for LDA 2050

Let us assume that given instruction is located in memory address 8000H.



Timing diagram for STA (let 2050 location)