Unit → 7

Advanced Microprocessors :

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1> Advanced Microprocessor 80286 :

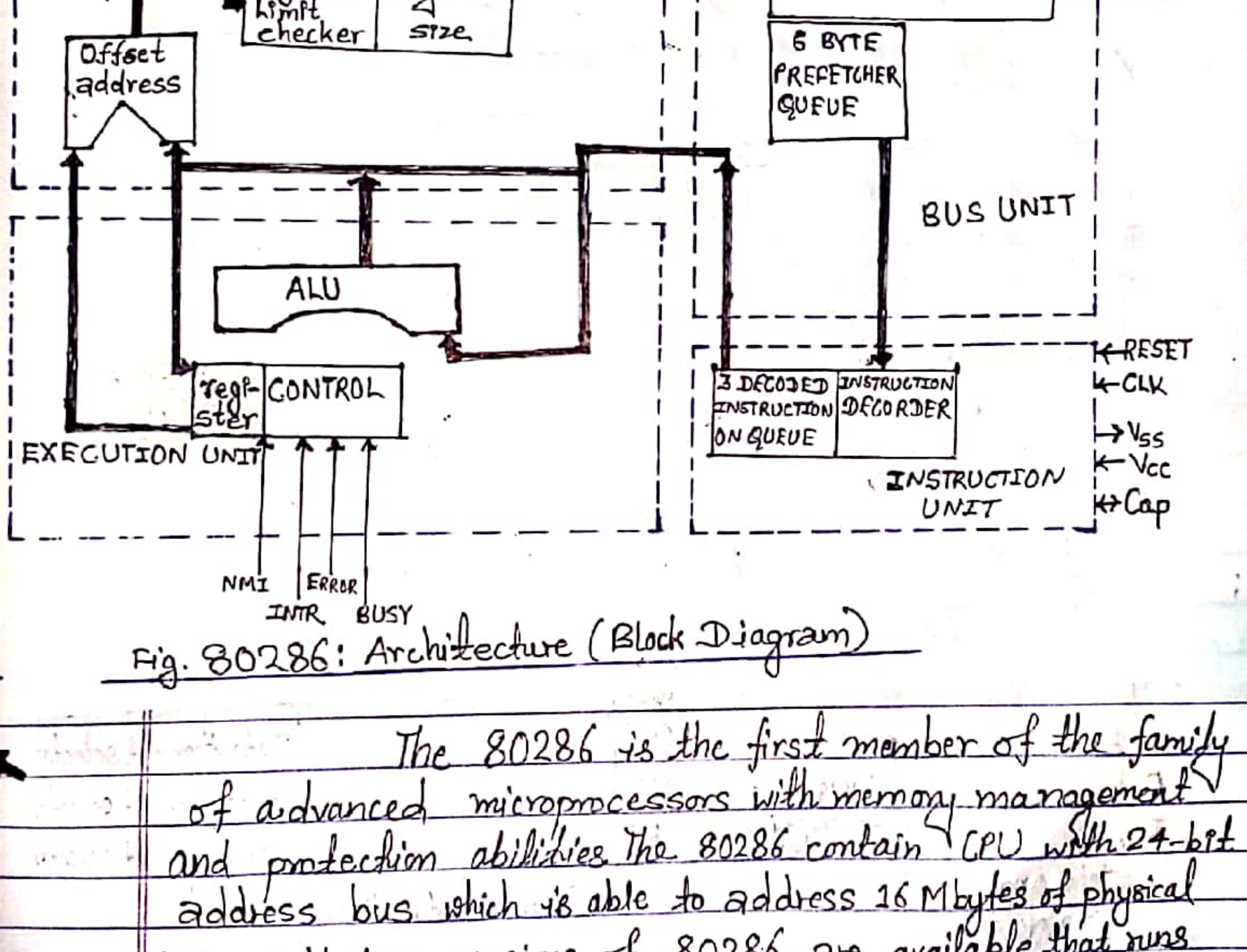

Fig. 80286: Architecture (Block Diagram)

The 80286 is the first member of the family of advanced microprocessors with memory management and protection abilities. The 80286 contain CPU with 24-bit address bus which is able to address 16 Mbytes of physical memory. Various versions of 80286 are available that runs on 12.5MHz, 10 MHz and 8 MHz clock frequencies. 80826 is upwardly compatible with 8086 in terms of instruction set. 80286 includes two operating modes real address mode which can address upto 1Mb and virtual address upto 16 Mb.

Description (only if asked) of 80286

The advanced microprocessor 80286 contain four functional parts which are as follows:

i) **Address Unit (AU)** → It is responsible for calculating the physical addresses of instructions and data that the CPU wants to acess. Also, the address lines derived by this unit maybe used to address different peripherals. This physical address computed by the AU is handed over to the BU of CPU. Address unit provides the memory management and protection services for the 80286.

ii) **Bus Unit (BU)** → It consists of address latches & drivers. One major function of the bus unit is to fetch instruction bytes from the memory. It is responsible for performing all external bus operation. It provide a 16 bit data bus, 24 bit address bus and other signals.

iii) **Instruction Unit (IU)** → It accepts instructions from the prefetch queue and an instruction decorder decodes them one by one. Output of the decoding circuit drives a control unit in the execution unit.

iv) **Execution Unit (EU)** → It is responsible for executing the instructions received from the decoded instruction queue, which sends the data part of the instruction over the data bus. It contains the register bank.

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Register Organization of 80286:

The 80286 CPU contains almost the same set of registers, as in 8086, namely:

i) Eight 16-bit general purpose registers
ii) Four 16-bit segment registers
iii) Status and control registers
iv) Instruction Pointer
v) Two 16-bit register — Flags, MSW
vi) Two 16-bit register — LDTR & TR
vii) Two 48-bit register — GDTR & IDTR

	7	07	0	
AX	AH	AL		} Multiply/Divide I/O instructions.
DX	DH	DL		
CX	CH	CL		} loop/shift/repeat/count
BX	BH	BL		} Base registers
BP				
SI				} Index registers
DI				
SP				} Stack pointer
	15		0	

General Register.

	15	0	
F		Status word	
IP		Instruction pointer	

status and control registers

	15	0	
CS			Code segment selector
DS			Data segment selector
SS			Stack segment selector
ES			Extra segment selector

Segment Registers

Fig. Register set of 80286

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Flag registers:

The flag register reflects the results of logical and arithmetic instructions.

-	NT	IOPL	OF	DF	IF	TF	SF	ZF	-	AF	-	PF	-	CF

Fig. Flag registers

D2, D4, D6, D7 and D11 are called as status flag bits. The bits D8 (TF) and D9 (IF) are used for controlling machine operation and thus they are called control flags. The additional fields available in 80286 flag registers are:-

i) IOPL – I/O Privilege Field (bits D12 and D13).
ii) NT – Nested Task flag (bit D14)
iii) PE – Protection Enable (bit D16)
iv) EM – Processor Extension Emulator (bit D18)
v) MP – Monitor Processor Extension (bit D17)
vi) TS – Task Switch (bit D19)

Machine Status Word (MSW)

The machine status word consists of four flags – PE, MP, EM and TS of the four lower order bits D19 to D16 of the upper word of the flag register. The LMSW and SMSW instructions are available in the instructions are available in the instruction set of 80286 to write and read the MSW in real address mode.

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Privilege levels:

Previlege level is defined as the delegation of authority over computer system.

00 → Kernal level
01 → OS service.
10 → OS extensions
11 → lowest privilege level.

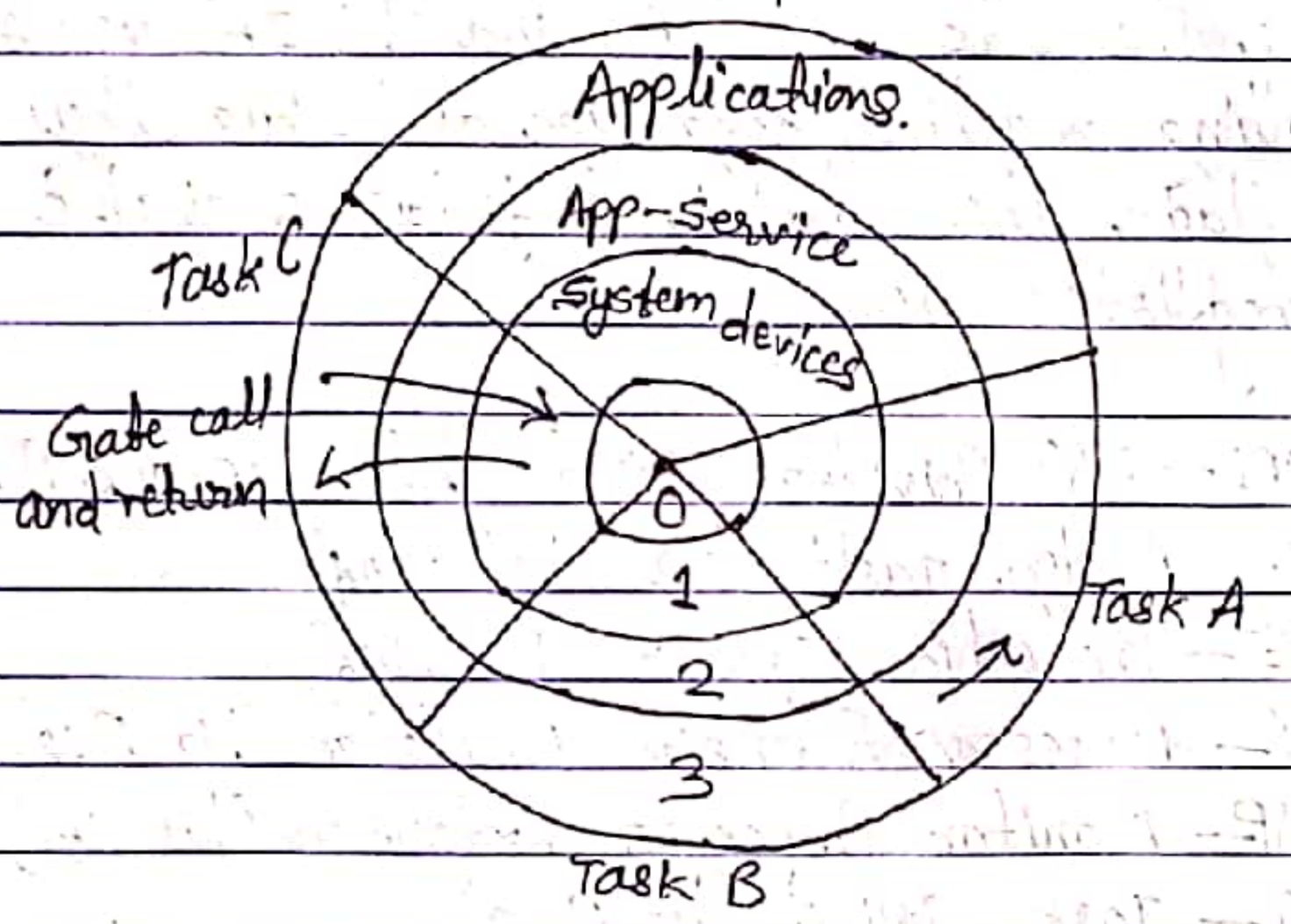

fig. Privilege level

→ Each task assigned a privilege level, which indicates the priority of that task.
→ It can only be changed by transfering the control using gate descriptors, to a new segment.
→ Highest privileged level can access all the data segment defined in GDT & LDT of the task.
→ The least previleged level will have the most limited access of data.
→ The use of ring allows for system software to restrict tasks from accessing data.

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Descriptor cache:

In real or protected mode, the CPU stores the base address of each segment in hidden registers called descriptor cache registers. Each time a segment register is loaded, the segment base address, segment size limit, and access attributes (access rights) are loaded, or "cached", into these hidden registers. To enhance performance, all subsequent memory refrences are made via the descriptor cache registers instead of calculating the physical address, or looking up the base address in the descriptor table.

Memory Access in GDT and LDT:

LDTs are siblings of GDT. LDT (local Descriptor table) is important when we seperate the address space for multiple processes. There will be generally one LDT per user process that describes privately held memory, while GDT (Global Descriptor table) describes shared memory and kernel memory.

When we create any new process the operating system will create new LDT. This new LDT will be in GDT. Sometimes LDTs are useful when we want to give read or write permissions from memory to any process, while memory seperated through GDT will be visible for every process so every process can request for memory. But LDT gives right to read or write for each process.

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Multitasking

In 80286 we improve multitasking capability by adding necessary memory management and task switching in such a way that there is adequate protection:

i) Between the application task and the system and other more privileged task.
ii) For seperating from each other.
iii) Between the code and data module.
iv) Again unwanted accessing or changing the data or code.

The primary key to multitasking in the ability to break the various entities to be processed into part in such a way that the part can easily function together and adequate protection is maintained.

Molecularity make up the task and subtask so that operating system module that include critical code and data table can be protected from application program.

Addressing modes

There are two addressing modes in 80286 which are as follows:-

☆ Real address mode → In real address mode, the 80286 can address upto 1Mb of physical memory address like 8086. In real address mode, the 80286 is object code compatible with 8086.

iii) Virtual address mode → In virtual address mode, it can address up to 16 Mb of physical memory address space and 1 GB of virtual memory address space. In virtual address mode, it is source code compatible with 8086. Virtual address mode is also called protected address mode.

2) Advanced Microprocessor 80386:

Architecture of 80386

The internal architecture of 80386 is divided into 3 sections:-

i) Central processing unit
ii) Memory management unit
iii) Bus interface unit.

Central processing unit is further divided into Execution unit and Instruction unit. Execution unit has 8 General purpose and 8 special purpose registers which are either used for handling data or calculating offset addresses.

The block diagram of 80386 is as follows:

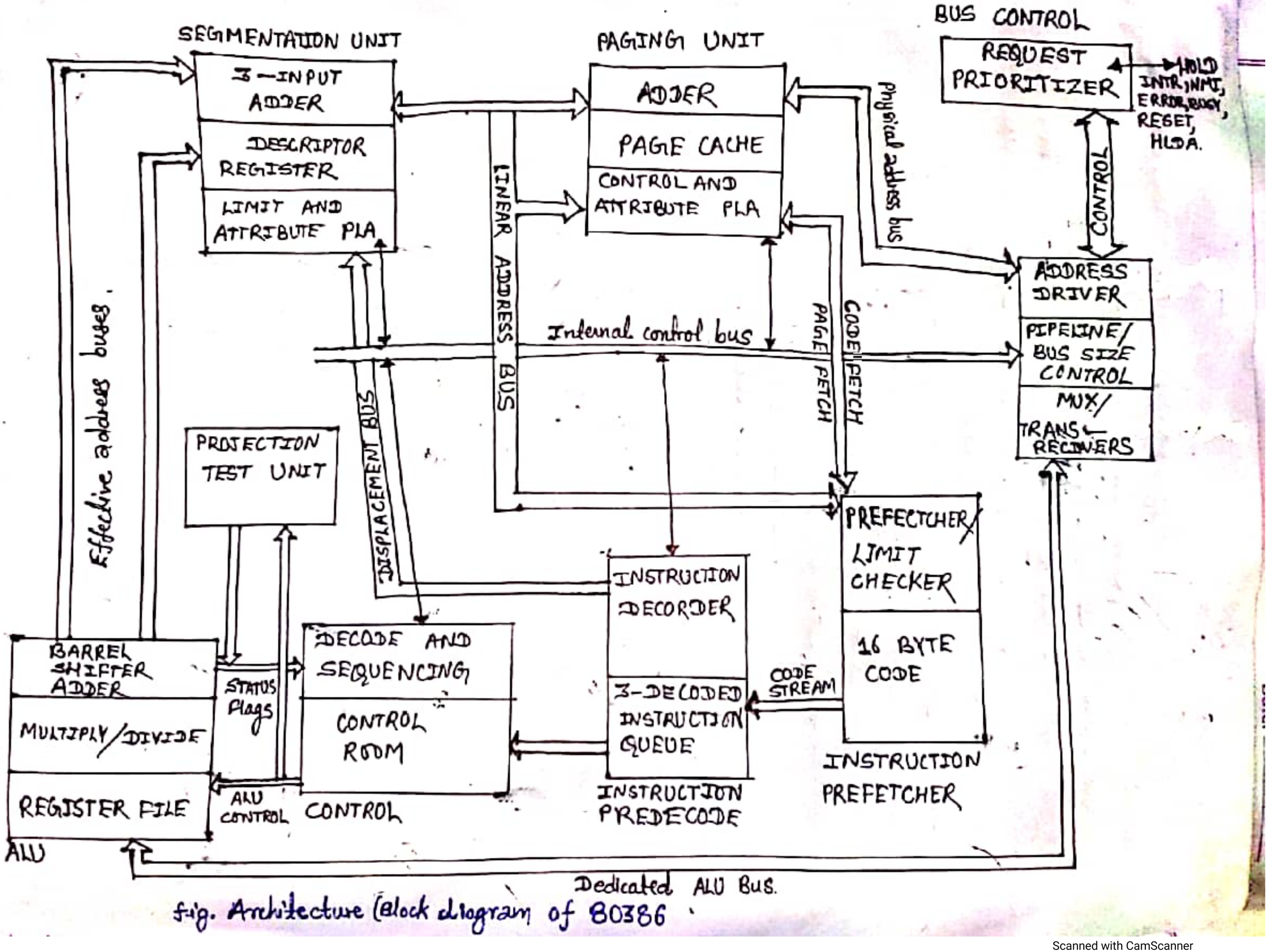

fig. Architecture Block diagram of 80386

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Register Organization:

→ The 80386 has eight 32-bit general purpose registers which may be used as either 8 bit or 16 bit registers.

→ A 32-bit register known as an extended register, is repiesented by the register name with prefix E.
Example: A 32 bit register corresponding to AX is EAX, similarly BX is EBX etc.

→ The 16-bit registers BP, SP, SI and DI in 8086 are now available with their extended size of 32 bit and are names as EBP, ESP, ESI and EDI.

→ AX represents the lower 16-bit of the 32 bit register EAX.

→ BP, SP, SI, DI represents the lower 16 bit of their 32 bit counterparts, and can be used as independent 16 bit registers.

→ The six segment registers available in 80386 are CS, SS, DS, ES, FS and GS.

→ The CS and SS are the code and the stack segment registers respectively, while DS, ES, FS, GS are 4 data segment registers.

→ A 16 bit instruction pointer IP is available along with 32 bit counterpart EIP.

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Memory Access in Protected mode:

In this mode, the contents of segment registers are used as selectors to address descriptors which contain the segment limit, base address and access rights byte of the segment.

The effective address (offset) is added with segment base address to calculate linear address. This linear address is further used as physical address, if the paging unit is disabled, otherwise the paging unit converts the linear address into physical address.

The paging unit is a memory management unit enabled only in protected mode. The paging mechanism allows handling of large segments of memory in terms of pages of 4K byte size.

The paging unit operates under the control of segmentation unit. The paging unit of enabled converts linear addresses into physical address, in protected mode.

Paging

Paging is one of the memory management techniques used for virtual memory multi-tasking operating system. It allows handling of large segments of memory in terms of pages of 4K byte size.

The advantage of paging scheme is that the complete segment of a task need not to be in the physical memory at any time. Only a few pages of the segments, which are currently required

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for the execution need to be available on the physical memory. Thus the memory requirement of the task is reduced, leaving the available memory for other tasks. The paging mechanism provides an effective technique to manage the physical memory for multitasking systems.

THE END

If my notes really helped you,then you can support me on esewa for my hardwork.

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