Roll No. 22EEACY033

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B.TECH. V SEMESTER (NEW SCHEME)
MAIN/BACK EXAMINATION 2024-25
COMPUTER SCIENCE & ENGINEERING

5CS4-02 - Computer Organization and Architecture

5AI4-02, 5AD4-02, 5AM4-02, 5CA4-02, 5CD4-02, 5DS4-02, 5IO4-02, 5IT4-02 5MC4-02, 5CM4-02, 5CY4-02, Common to CS, AI, AD, AM, CA, CD, DS, IO, IT, MC, CM, CY

Time : 3 Hours]

[Max. Marks : 70

[Min. Passing Marks :

Instructions to Candidates :

Part-A : Short Answer Type Questions (up to **25** words) 10 × 2 = 20 marks. All 10 questions are compulsory.

Part-B : Analytical/Problem Solving questions 5 × 4 = 20 marks. Candidates have to answer 5 questions out of 7.

Part-C : Descriptive/Analytical/Problem Solving questions 3 × 10 marks = 30 marks. Candidates have to answer 3 questions out of 5.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.

Use of the following supporting materials is permitted during examination. (Mentioned in form no. 205).

1_____

2_____

Part-A

Q. 1. Write features of RISC processor.

Q. 2. Explain need of I/O processor.

Q. 3. Draw a diagram showing CPU-IOP communication.

Q. 4. What do you mean by SIMD, MIMD, and MISD ?

Q. 5. Discuss the need of virtual memory.

Q. 6. Explain memory operation of the following transfer statements :

(a) $R2 \leftarrow M[AR]$

(b) $M[AR] \leftarrow R3$

(c) $R5 \leftarrow M[R6]$

Q. 7. Differentiate between an isolated I/O and memory mapped I/O.

Q. 8. Explain the terms Tag, Index, and Block in relation to cache memory.

Q. 9. What is stack and what is its role in the operation of computer instructions ?

Q. 10. Differentiate between Bus and memory transfer.

Part-B

Q. 1. What are the differences between direct mapping, associative mapping and set associative mapping ?

Q. 2. Explain general register organization of a computer with suitable diagram.

Q. 3. Describe any *five* addressing modes.

Q. 4. Given the 16 bit value 1001101011001101. What operation must be performed in order to :

(a) Clear to 0(zero) the first eight bits

(b) Complement the middle eight bits

Q. 5. Design a bus system for four 8-bit registers using multiplexers.

Q. 6. A computer has main memory of 512 bytes. The memory is divided into 16 pages of 32 words each. Suppose CUP gives a logical address $(000110011)_2$. Identify the physical address for the given logical address.

Q. 7. Draw a neat diagram of DMA chip and explain its working.

Part-C

Q. 1. Explain Booth's multiplication algorithm for signed 2's complement numbers in detail, with a suitable example.

Q. 2. What do you mean by instruction pipeline ? With a neat diagram explain all the steps involve in instruction pipeline.

Q. 3. Perform the arithmetic operation below with binary numbers and with negative numbers in signed 2's complement representation. Use 7bits registers :

(a) (+35) + (+40)

(b) (-35) + (+40)

Q. 4. What is register transfer language ? Explain basic symbols used in register transfer with examples.

Q. 5. Evaluate the aritmetic statement X = (A + B) * (C + D) using general register computer with three address, two address, one address and zero address instruction format.

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