Do We Still Need Daily Production Target Setting in Fully Automated Fabs?*

Yu-Ting Kao, Chun-Ming Chang, Shi-Chung Chang+
f97546010@ntu.edu.tw, r02921003@ntu.edu.tw, scchangee@ntu.edu.tw,
National Taiwan University
No. 1, Sec. 4, Roosevelt Road, Taipei, 10617 Taiwan (R.O.C)
Phone: +886 -2-3366-3700 ext. 207 Fax: +886-2-2363-8247

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***Abstract*- Fab operations have evolved to full automation along with advancements of automation technologies in material handling, inspection and manufacturing execution and management. A school of practitioners and re-searchers have been arguing that there need only two levels in short-interval production control of a fully automated fab: wafer release (WR) on the top and real time dispatching in the bottom. They have also raised the question: Are the middle two levels of daily production target setting and machine allocation (DPTS&MA) traditionally designed for shop floor operators still necessary? In this paper, we take a first step to address the question by simulation and comparing the performance of the simplest automated dispatching policy, First-In-First-Out (FIFO), and the outperformed dispatching policy in [7], Fluctuation Smoothing Mean Cycle Time and Least Lot Slack-time(FSMCT+LLS), with a traditional DPTS&MA scheme under the same given WR. FIFO serves as a performance lower bound, FSMCT+LLS servers as the representative of good automated dispatching policies and DPTS&MA captures essence adopted by many practitioners of proportional target tracking and detailed dispatching of FIFO. Simulations are over a benchmarking mini-fab of six stages and five tool groups. Preliminary results show that DPTS&MA outperform FSMCT+LLS and FIFO in line balancing and cycle time performance for both high and low variability scenarios. We shall demonstrate how such a foundation may further be exploited to study if DPTS&MA is needed in the short-interval production control hierarchy of a fully automated fab.**

I. FULLY AUTOMATED FAB

During the past decades, the fully automated mode of operation in semiconductor fabs is put into practice due to the improvement of automation technology such as automatic handling of wafer flows and automatic inspection on process conditions [6, 7]. Full automation is common nowadays for raising productivity, especially in 300mm fabs.

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+ Correspondence author: S.-C. Chang, Department of Electrical Engineering, National Taiwan University, Taipei, 10617 Taiwan, ROC. e-mail: scchangee@ntu.edu.tw

In a fully automated fab, production information can be collected much faster and with higher volume and preciseness than before, facilitating comprehensive production control decisions.

As shown in Figure 1, the process flow of a type of wafers through the fab is highly reentrant because the wafers make multiple visits to machine groups as successive circuit layers are added onto the wafer. This reentrant feature poses a unique challenge to production, since wafers of different part types as well as wafers of the same type but at different layers of fabrication may compete for the finite capacity of an equipment group. The complexity of production control is high especially in a foundry fab.

Traditionally, a top-down hierarchical structure is adopted for short-interval production control (Figure 2): planners break the MPS into a executable level and determine the wafer release policy and daily production targets, supervisors guide the machine allocation to achieve the targets and then operator manually dispatch.

With the complete information and the help of decision support software from fab automation, a school of practitioners and re-searchers have been arguing that the complex scheduling decisions could be reduced to two levels [9]: wafer release schedule and real time dispatching of lots and/or machines.

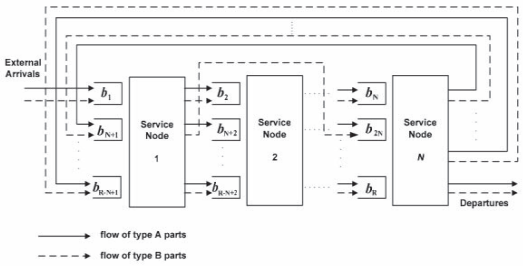

Figure 1. Reentrant process in a fab [8]

Just like in other complex production systems, hierarchical scheduling is widely adopted by fabs based on the time-scale of production flow control (PFC) activities so that the complex scheduling problem can be decomposed into a few levels of simpler but integrated subproblems. Figure 2 depicts a four-level decision hierarchy used by quite a few foundry fabs. The four levels of scheduling functions are (1) wafer release and output scheduling, (2) daily target setting, (3) machine scheduling and (4) lot dispatching. Wafer release and output scheduling aims at controlling the WIP level and

cycle time of the whole fab while meeting delivery requirements. It schedules the quantities of wafer release and output for a fab using a day as a time unit over two to four months. The resultant schedule is also referred to as the Master Production Schedule (MPS). Machine scheduling assigns machines in each equipment group to various production steps requiring the same type of machines. Lot dispatching ranks lot priorities of processing in the same step. Both machine scheduling and lot dispatching are local to individual machines and steps and respond to operation status in real time. For managerial purposes at fab level, a few consecutive production steps are often aggregated into a stage. Daily target setting combines the release/output schedule, present fab production states, and tool capacity forecast to properly set target volumes of daily production for individual part types and steps. These daily targets serve as a guideline for machine scheduling and lot dispatching. Daily target setting bridges between fab wide and local PFC activities. In practice, daily target setting is one of the key review items in the daily production meeting of a fab.

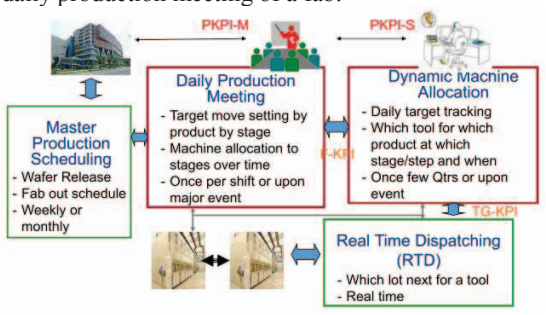

Figure 2. Four-level Fab PFC Hierarchy

Ideally, Flat Management can be reached if there is a good dispatcher who directly considers MPS in its dispatching logic. The supervisors no longer need to allocate the machines, and the production target setting is neither needed. The burden of supervisors and operators are reduced as the dispatching system smartly makes the decisions. Instead of DPTS&MA by the manufacturing supervisors, production control engineers' adjustments of lot priority occur quite often in fully automated fabs, especially for foundry fabs. Here an issue obviously appears: does the interference from the change of priority without the consideration of target setting better than the traditional target-based control? The issue involves both aspects of management and decision support logic about the optimal design of control hierarchy and where to put human intelligence in the control hierarchy. This paper describes a preliminarily design of a simulation environment for comparing different production hierarchy and decision support logics.

II. DAILY PRODUCTION TARGET SETTING

Production target setting is a short-interval production management function that determines for each product type the target number of wafers processed (moves) at each stage during one day. Given the delivery requirements from customers, wafers are released to the production line, which are processed in a serial flow by different tools. In a fab, the fabrication process of each type of wafers may require more than three hundred fabrication steps. For managerial purpose, every few consecutive steps are represented by one key step, which is defined as a stage. Production target setting bridges the fab output requirements such as on-time delivery with the allocation of daily production machines capacity. Therefore, the production target setting is equivalent to properly allocate the tool capacity to different products and stages over time. In practice, the production targets are one of the key review items in the daily production meeting of a fab, which provides direction and serves as a guideline for machine scheduling and lot dispatching [1].In the literature, there has been much research on the target setting problem and the good results are obtained [1-3]. Field applications demonstrated that quality target setting leads to over 20% increase in daily moves and more than 8% decrease of wafers-in-process (WIPs) of a foundry fab case [2] as shown in Figure 3.

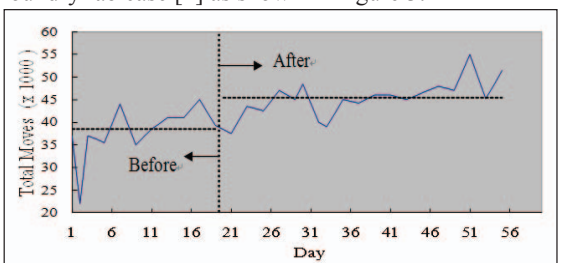

Figure 3a. Improvement in total moves by adopting a target setting system [2]

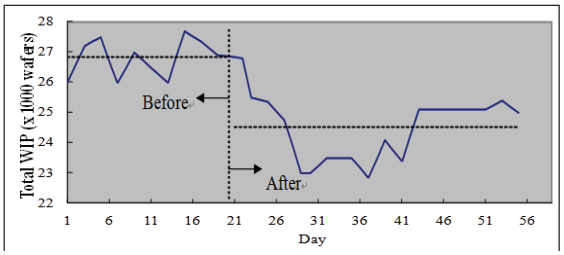

Figure 3b. Reduction in total WIPs over time by adopting a target setting system [2]

III. DPTS SIMULATION DESIGN

Stimulation studies in this section are designed to quantify the effect of target setting under manufacturing uncertainties. The simulation studies are over a 3-station (machine group) and six-step re-entrant semiconductor fabrication from Intel as depicted in Figure 4 [3, 6]. This mini-fab is exemplary but exhibits all of the essential features for fab scheduling. Table 1 lists the process, tool group and WIP parameters, where t and j are station and stage indices respectively. Here the process time is t_e. B_j is the batch size of stage j, and C_t indicates the number of machines in each station. R_t is the maximum

throughput (capacity) per shift of each machine group. The R_{Si} of Station 3 is the smallest among all, which means Station 3 is the capacity bottleneck. Fab and stage cycle times as well as throughputs from the simulator, which tracks the target setting, are collected to evaluate the performance.

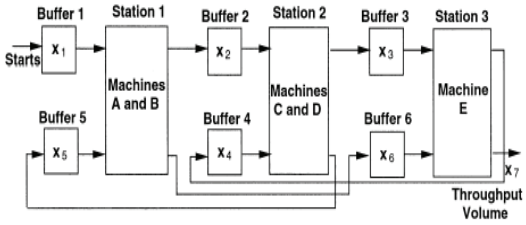

Figure 4. A five-machine six-step mini-Fab [3]

Table 1. Specification of the mini-Fab

t	j	t_{ej}	B_j	C_t	R_t
1	1 5	225 255	3 3	2	6.95
2	2 4	30 50	1 1	2	9.97
3	3 6	55 10	1 1	1	6.38

A. Validation of Mini-Fab

We first validate the implementation of mini-fab model in simulation by comparing the throughput with [5]. There are two validation cases: one with a deterministic release rate of 1 lot per 80 minutes (low release rate) and the other with 1 lot per 75 minutes (high release rate). FIFO is the dispatching rule. The simulation time horizon is 25000 minutes. The results are shown in Table 2. The relative error is less than 2.4%. The minor difference may be caused by implementation of batching rule at stages 1 and 5. The simulation implementation of the mini-fab model is therefore consistent with El [5].

Table 2. Total output lots over 25000 minutes

	(Adl et al 1996)	Simulation in this paper	Relative error
Low release rate	293	300	2.4%
High release rate	290	288	0.7%

B. Proportional to Target Deficit Ratio and FIFO policy (DPTS+FIFO)

In order to investigate the effect posed due to daily production target setting, a control of target integrated with FIFO dispatching rule (DPTS+FIFO) is implemented and compared with FIFO solely, as shown in Figure 5. A deficit ratio to workload is used of each stage for the selection of dispatching. The lower the ratio, the higher the priority of the stage the simulator will dispatch to achieves its targets. For every day t, the fab simulation model receives the targets from an external decision module and faithfully achieves the target based on the dispatching rule. The WIP distribution of the end of day would be recorded. The decision module then set targets based on a given MPS, WIP distribution, and number of finished wafers. Though it is not totally the same as in practice, DPTS+FIFO characterizes the target-tracking feature to compare.

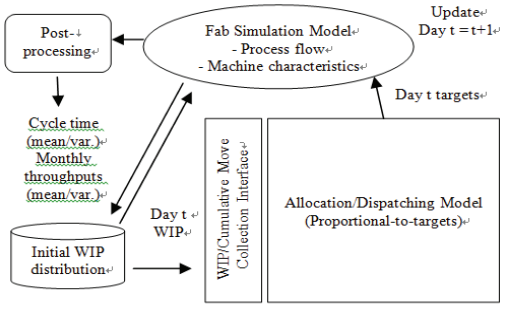

Figure 5. Implementation of DPTS+FIFO

C. Fluctuation Smoothing Mean Cycle Time and Least Lot Slack-time (FSMCT+LLS)

Besides comparison with FIFO, we follow the analyses in [7] and select the top-ranking scheduling policy, which is combined with FSMCT dispatching rule for general machines, and LLS dispatching rule for batching machines. We regard station 2 and 3 in mini-Fab as general machine and station 1 as batching machine. The dispatching rule for general machine, FSMCT, is first proposed by Lu[10], which sets a specific weighting, called slack time, for each lot in each buffer. Slack time is determined by the sequence number of the lot, mean throughput rate, mean cycle time, and the estimation of remaining cycle time from the buffer where the lot is. FSMCT dispatching rule is choosing the lot with least slack time. Dispatching rule for batching machine, LLS, is also a slack time based dispatching policy but LLS chooses the stage of the lot with least slack time to dispatch regardless of full batch or not.

IV. COMPARISON WITH TARGET SETTING

We simulate in two different cases, one case is that the processing time of each stage is uniformly distributed and the other one is exponentially distributed, for analyzing the effects of DPTS under different manufacturing uncertainties. First, we adopt FIFO dispatching rule, which is the simplest automated dispatching policy, as benchmark. Second, we compare DPTS+FIFO with FSMCT+LLS , which is considered as a good dispatching policy.

As Figure 6 and 7, both DPTS+FIFO and FSMCT+LLS reduce 35+% standard deviation of stage moves in both cases, which shows smoother line balance than FIFO. In Table 4, DPTS+FIFO outperforms FSMCT+LLS and FIFO, and reduce at least 20% mean cycle time and 50% cycle time standard deviation in the comparison with FIFO. Compared with FSMCT+LLS, DPTS+FIFO also makes reduction of 7% mean cycle time and 18+% cycle time standard deviation, which implies that DPTS+FIFO provides more intelligent machine allocation and better lot dispatching. In Table 3, DPTS+FIFO performs a little better in throughput, but

due to smaller scale of simulation, the performance differences is not significant, so further comparisons in larger scale simulation may be required. Moreover, FIFO is the simplest automated dispatching policy and provides a lower bound performance for other RTD dispatching policies. Thus, comparisons with other dispatching policies need further research.

Table 3. Throughput performance of DPTS+FIFO, FIFO, FSMCT+LLS in 95% confidence interval

Uni.	DPTS+FIFO	FIFO	FSMCT+LLS
Mean [UB,LB]	534.8 [541.7, 527.9]	530.7 [540.5,520.7]	534.0 [539.2,528.9]
std	18.86	22.49	14.09
Exp.	DPTS+FIFO	FIFO	FSMCT+LLS
Mean [UB,LB]	527.3 [538.6, 516.0]	527.1 [547.6,506.5]	522.3 [529.7,514.9]
std	31.14	46.93	20.18

Table 4. Cycle time performance of DPTS+FIFO, FIFO, FSMCT+LLS in 95% confidence interval

Uni.	DPTS+FIFO	FIFO	FSMCT+LLS
Mean [UB,LB]	3073.1 [3349.6,2796.6]	3944.8 [4618.8,3270.9]	3154.6 [3490.3,2818.9]
std	757.38	1537.80	919.41
Exp.	DPTS+FIFO	FIFO	FSMCT+LLS
Mean [UB,LB]	4123.4 [4504.9,3741.9]	5317.5 [6500.8,4134.3]	4419.7 [5015.9,3823.5]
std	1045.42	2699.84	1632.87

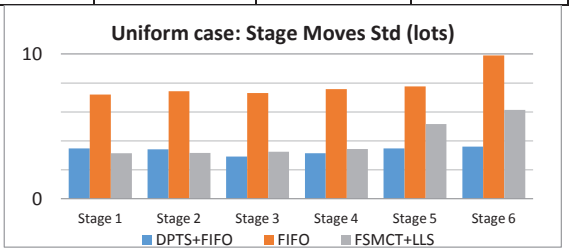

Figure 6. Standard deviation of each stage moves in uniform distribution case

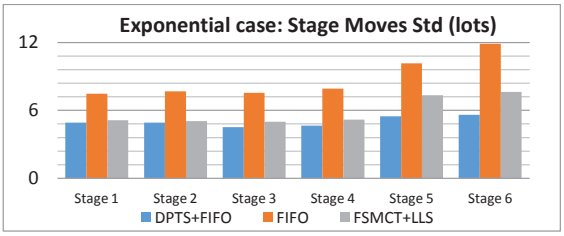

Figure 7. Standard deviation of each stage moves in exponential distribution case

V. CONCLUSIONS

In this research work, a preliminarily study of a simulation-based environment is performed for comparing the performance of FIFO and FSMCT+LLS with a traditional DPTS&MA scheme under the same given wafer release. Simulations are over a benchmarking mini-fab of six stages and five tool groups. In our analysis, both DPTS&MA and FSMCT+LLS help significantly reduce the standard deviations of both cycle time and throughput and also has better line balance in the comparison with FIFO for both high and low variability scenarios. Moreover, DPTS&MA outperforms in cycle time and throughput performances, but throughput performance difference is not significant because of smaller scale of simulation. Therefore, comparisons in larger scale simulation between DPTS&MA and other automated dispatching policies requires further research. In this paper, the comparisons serve as the foundation which may further be exploited to study if DPTS&MA is needed in the short-interval production control hierarchy of a fully automated fab.

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