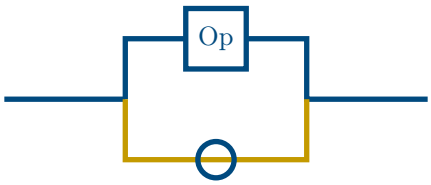
The Art of Electronics

Interactive Circuit Simulator

Comprehensive Development Roadmap

Web Application for Circuit Simulation & Education



AoE Simulator

Project Scope:

A comprehensive web-based circuit simulation platform covering all circuits from *The Art of Electronics* (3rd Edition) and *The X Chapters*

Total Circuits: 150+ unique simulation modules
Estimated Timeline: 18–24 months full development

Version: 1.0

Date: December 1, 2025

Contents

Chapter 1

Executive Summary

▶ Vision Statement

This roadmap outlines the development of a comprehensive web-based circuit simulation platform designed to accompany *The Art of Electronics* by Paul Horowitz and Winfield Hill, including both the main text (3rd Edition) and *The X Chapters*. The platform will provide interactive, browser-based simulations of every circuit covered in the companion laboratory curricula, enabling learners to explore electronics concepts through hands-on virtual experimentation.

1.1 Project Objectives

The AoE Circuit Simulator aims to achieve the following primary objectives:

1. **Comprehensive Coverage:** Simulate all circuits from both the main AoE curriculum (Phases 0–6) and the X Chapters advanced curriculum (Projects A1–A5, D1–D2, E1–E2), totaling over 150 distinct circuit configurations.

2. **Educational Integration:** Align simulations directly with the laboratory curriculum structure, providing guided exercises, measurement challenges, and theoretical verification opportunities.

3. **Accurate Simulation:** Implement SPICE-accurate simulation engines for analog circuits, logic simulation for digital circuits, and hybrid simulation for mixed-signal systems.

4. **Accessible Platform:** Deliver simulations via modern web browsers without requiring software installation, plugin downloads, or high-performance hardware.

5. **Interactive Learning:** Provide virtual oscilloscopes, multimeters, spectrum analyzers, and other measurement tools that mirror real laboratory equipment.

1.2 Source Material Summary

The development roadmap draws from two comprehensive laboratory curricula:

Table 1.1: Source Curriculum Overview

Curriculum	Focus Areas	Circuit Count
AoE Main Curriculum	Phases 0–6: Orientation through Capstone, covering analog foundations, precision instrumentation, power electronics, digital/mixed-signal, and high-speed design	80+ circuits
X Chapters Curriculum	Advanced analog (A1–A5), digital foundations (D1–D2), embedded systems with RTOS (E1–E2)	70+ circuits

1.3 Development Timeline Overview

Table 1.2: High-Level Development Phases

Phase	Deliverables	Duration
Phase I: Foundation	Core simulation engine, basic UI, 20 foundational circuits	4–5 months
Phase II: Analog Core	Op-amp circuits, filters, transistor configurations	3–4 months
Phase III: Precision & Power	Low-noise, instrumentation, power supply circuits	3–4 months
Phase IV: Digital & Mixed	Logic simulators, ADC/DAC, MCU interfaces	3–4 months
Phase V: Advanced	High-speed, RF-lite, X Chapters projects	3–4 months
Phase VI: Integration	Capstone systems, final polish, deployment	2–3 months

Chapter 2

Technical Architecture

2.1 System Architecture Overview

The AoE Circuit Simulator employs a modern web application architecture optimized for computational performance, real-time interactivity, and educational effectiveness.

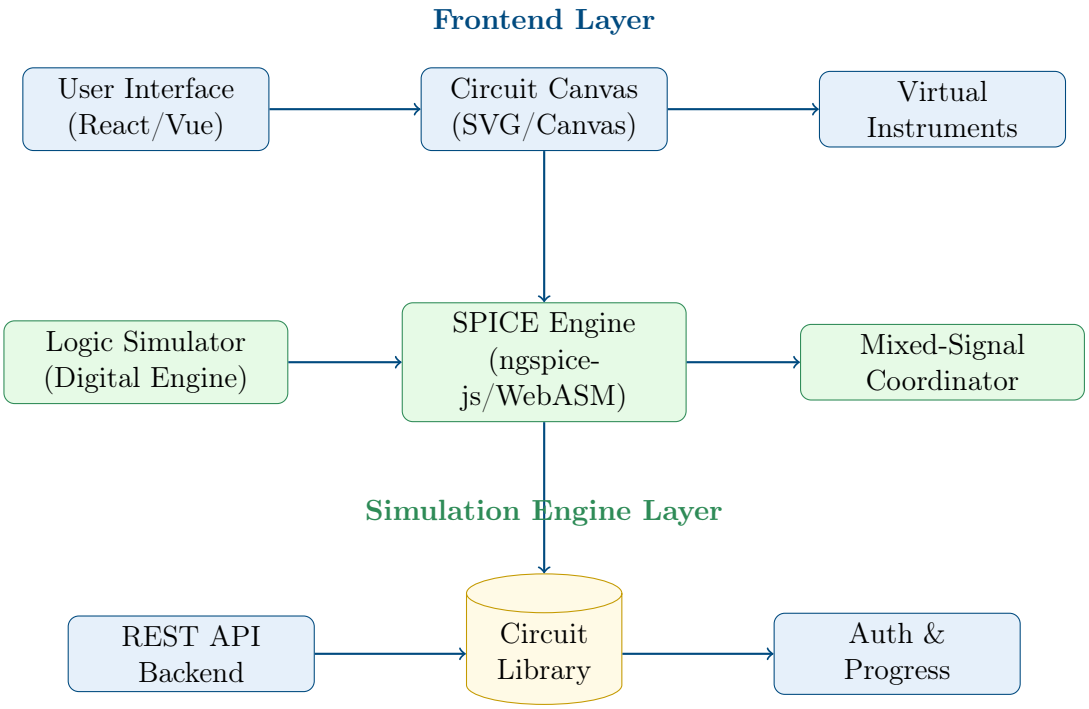


Figure 2.1: High-Level System Architecture

2.2 Simulation Engine Requirements

◇ **Technical Requirements**

The simulation engine must support the following capabilities:

Analog Simulation (SPICE-based):

- DC operating point analysis
- AC frequency response (Bode plots)
- Transient analysis with configurable time steps
- Noise analysis (thermal, shot, 1/f)
- Parameter sweeps and Monte Carlo analysis
- Support for standard component models (resistors, capacitors, inductors, diodes, BJTs, MOSFETs, op-amps)

Digital Simulation:

- Gate-level logic simulation
- Propagation delay modeling
- Setup/hold time checking
- State machine visualization
- Bus timing analysis

Mixed-Signal:

- ADC/DAC behavioral models
- Sample-and-hold dynamics
- Quantization noise representation
- Clock domain interactions

2.3 Technology Stack Recommendations

2.3.1 Frontend Technologies

Table 2.1: Recommended Frontend Stack

Component	Technology	Rationale
UI Framework	React 18+ or Vue 3	Component-based architecture, large ecosystem
State Management	Redux Toolkit / Pinia	Complex simulation state handling
Circuit Rendering	SVG + D3.js	Vector graphics for schematic display
Waveform Display	Chart.js / Plotly.js	High-performance time-domain plotting
Canvas Operations	Fabric.js / Konva.js	Interactive schematic manipulation
Build System	Vite	Fast development builds, ESM native

2.3.2 Simulation Engine Options

Table 2.2: Simulation Engine Comparison

Engine	Advantages	Disadvantages	Use Case
ngspice (WebAssembly)	Full SPICE accuracy, extensive model library	Large binary size (∼5MB), complex integration	Primary analog engine
CircuitJS	Lightweight, educational focus, open source	Limited accuracy for precision circuits	Quick demonstrations
Custom TypeScript	Full control, optimized for web	Development effort, limited models	Digital logic, simple analog
Server-side SPICE	Maximum accuracy, all features	Latency, server costs, scaling challenges	Precision verification

2.3.3 Recommended Hybrid Approach

1. **Client-Side Primary:** Use WebAssembly-compiled ngspice for most analog simulations, running entirely in the browser for responsiveness.

2. **Custom Digital Engine:** Implement a purpose-built TypeScript logic simulator for digital circuits, optimized for the specific needs of the curriculum.

3. **Server-Side Fallback:** Provide server-based simulation for complex circuits (noise analysis, Monte Carlo) where accuracy is paramount.

4. **Progressive Enhancement:** Start with simpler simulations and progressively add complexity based on user hardware capabilities.

2.3.4 Backend Technologies

Table 2.3: Recommended Backend Stack

Component	Technology	Rationale
API Server	Node.js/Express or Python/FastAPI	REST API, WebSocket for real-time
Database	PostgreSQL + Redis	Relational data + caching
Authentication	Auth0 / Firebase Auth	Managed auth, social login
File Storage	AWS S3 / Cloudflare R2	Circuit files, user projects
Server SPICE	ngspice containerized	Accurate simulation fallback
Deployment	Vercel / AWS / GCP	Scalable hosting

2.4 Data Models

2.4.1 Circuit Definition Schema

Circuits will be defined using a JSON-based schema that captures both schematic and simulation parameters:

```
{
  "id": "phase1_opamp_inverting",
  "name": "Inverting Op-Amp Amplifier",
  "curriculum": {
    "source": "aoe_main",
    "phase": 1,
    "section": "1.3.2",
    "aoe_reference": "Chapter 4, Section 4.2"
  },
  "components": [
    {"type": "opamp", "id": "U1", "model": "TL072", ...},
    {"type": "resistor", "id": "R1", "value": "10k", ...}
  ],
  "connections": [...],
  "simulation": {
    "analyses": ["dc", "ac", "transient"],
    "default_params": {...}
  },
  "exercises": [...]
}
```

Chapter 3

Circuit Inventory: AoE Main Curriculum

This chapter provides a comprehensive inventory of all circuits from the main *The Art of Electronics* laboratory curriculum that must be implemented in the simulator.

3.1 Phase 0: Orientation & Laboratory Setup

Phase 0 Circuits — Foundation & Measurement

Duration: 1–2 weeks **Circuit Count:** 8 circuits
This phase establishes measurement fundamentals and basic circuit behavior verification.

○ Phase 0 Circuit List

1. **7805 Linear Voltage Regulator**
   - Basic 12V to 5V regulation with input/output capacitors
   - Simulations: Line regulation, load regulation, ripple rejection, thermal behavior
   - Measurements: V_{out} vs V_{in}, V_{out} vs I_{load}, dropout voltage
2. **RC Low-Pass Filter (First-Order)**
   - Simple RC network for frequency response fundamentals
   - Simulations: Bode plot (magnitude/phase), step response, square wave response
   - Cutoff frequency calculation and verification
3. **RC High-Pass Filter (First-Order)**
   - Complementary to low-pass for complete filter understanding
   - AC coupling behavior demonstration
4. **Voltage Divider Networks**
   - Basic resistive dividers with loading effects
   - Source impedance and load impedance interactions
5. **Diode Rectifier (Half-Wave)**
   - Basic rectification with 1N400x diodes
   - Peak detection, ripple analysis

6. **Diode Rectifier (Full-Wave Bridge)**
   - Bridge rectifier with filter capacitor
   - Ripple voltage calculation, capacitor sizing
7. **Zener Diode Regulator**
   - Simple shunt regulation
   - Line and load regulation characteristics
8. **LED Current Limiting**
   - Basic LED driver with series resistor
   - Forward voltage drop, current calculation

3.2 Phase 1: Analog Foundations & Building Blocks

Phase 1 Circuits — Analog Core

Duration: 3–4 weeks **Circuit Count:** 25 circuits

Core analog building blocks including op-amp configurations, filters, and transistor circuits.

3.2.1 Op-Amp Configurations

○ Op-Amp Circuits

1. **Inverting Amplifier**
   - Configurable gain (1, 10, 100)
   - Virtual ground concept demonstration
   - Simulations: DC gain, bandwidth, slew rate, input/output impedance
2. **Non-Inverting Amplifier**
   - High input impedance configuration
   - Gain-bandwidth product demonstration
3. **Unity-Gain Buffer (Voltage Follower)**
   - Impedance transformation
   - Loading effect elimination
4. **Summing Amplifier**
   - Multiple input weighted summation
   - Audio mixer application
5. **Difference Amplifier**
   - Basic differential measurement
   - CMRR demonstration
6. **Integrator**
   - Op-amp with capacitive feedback
   - Square-to-triangle conversion
   - DC offset management
7. **Differentiator**

- High-frequency noise amplification issue
- Practical differentiator with limiting resistor

8. **Comparator**
   - Open-loop op-amp operation
   - Hysteresis (Schmitt trigger) addition

3.2.2 Active Filters

○ Active Filter Circuits

1. **Sallen-Key Low-Pass Filter (2nd Order)**
   - Butterworth response (Q = 0.707)
   - Selectable cutoff: 1kHz, 10kHz
   - 40 dB/decade rolloff demonstration
2. **Sallen-Key High-Pass Filter (2nd Order)**
   - Complementary high-pass design
   - Audio applications (DC blocking)
3. **Multiple Feedback (MFB) Bandpass Filter**
   - Center frequency and Q selection
   - Audio tone detection
4. **State-Variable Filter**
   - Simultaneous LP, HP, BP outputs
   - Independent Q and frequency control
5. **Twin-T Notch Filter**
   - 50/60 Hz hum rejection
   - Deep null at target frequency

3.2.3 Transistor Circuits

○ Transistor Circuits

1. **BJT Switch (NPN)**
   - 2N3904/2N2222 saturation switching
   - Base resistor calculation for hard saturation
   - LED driver, relay driver applications
2. **BJT Switch (PNP)**
   - High-side switching configuration
   - Complementary to NPN designs
3. **MOSFET Switch (N-Channel)**
   - 2N7000/BS170 logic-level switching
   - Gate threshold and $R_{DS(on)}$ demonstration
4. **Emitter Follower (Common Collector)**
   - Unity voltage gain buffer
   - High input impedance, low output impedance

- Current gain demonstration

5. **Source Follower (Common Drain)**
   - JFET-based high-impedance buffer
   - Very high input impedance ($> 10^{12}\Omega$)
6. **Common Emitter Amplifier**
   - Basic voltage amplifier stage
   - Biasing, gain, bandwidth trade-offs
7. **Darlington Pair**
   - High current gain (β^2)
   - Buffer applications
8. **Current Mirror**
   - Basic BJT current mirror
   - Wilson and Widlar variations

3.3 Phase 2: Precision & Low-Noise Instrumentation

Phase 2 Circuits — Precision & Noise

Duration: 4–5 weeks **Circuit Count:** 18 circuits

Precision measurement circuits with noise analysis capabilities.

○ Precision Circuits

1. **Three-Op-Amp Instrumentation Amplifier**
   - High CMRR (>100 dB) differential amplifier
   - Single resistor gain setting
   - Bridge sensor interface (strain gauge, load cell)
2. **Integrated Instrumentation Amplifier (INA128/AD620)**
   - Commercial in-amp behavior modeling
   - CMRR vs frequency, gain accuracy
3. **Transimpedance Amplifier (Photodiode Front-End)**
   - Current-to-voltage conversion
   - Photodiode capacitance compensation
   - Noise analysis: voltage noise, current noise, thermal noise
4. **Low-Noise Preamplifier**
   - Optimized for minimum noise figure
   - Input-referred noise calculation
5. **Chopper-Stabilized Amplifier**
   - Auto-zero offset cancellation
   - 1/f noise elimination
6. **Precision Voltage Reference**
   - Bandgap reference behavior (REF5050, LM4040)

- Temperature coefficient, load regulation

7. **Kelvin (4-Wire) Resistance Measurement**
   - Lead resistance elimination
   - RTD temperature sensing
8. **Wheatstone Bridge**
   - Bridge excitation and balance
   - Strain gauge signal conditioning
9. **Active Guard Driver**
   - Leakage current elimination
   - High-impedance node protection
10. **Sample-and-Hold Circuit**
    - Acquisition time, droop rate
    - ADC front-end application

3.3.1 Noise Analysis Features

The Phase 2 simulations must include comprehensive noise analysis capabilities:

- **Noise Spectral Density:** Display nV/$\sqrt{\text{Hz}}$ or pA/$\sqrt{\text{Hz}}$ vs frequency
- **Integrated Noise:** Calculate RMS noise over specified bandwidth
- **Noise Budget Tool:** Interactive calculator showing contributions from each component
- **1/f Corner Frequency:** Identification of flicker noise corner
- **Signal-to-Noise Ratio:** SNR calculation for given signal levels

3.4 Phase 3: Power Electronics & Protection

Phase 3 Circuits — Power

Duration: 4–5 weeks **Circuit Count:** 15 circuits

Power supply design, switching regulators, and protection circuits.

○ Power Supply Circuits

1. **LM317 Adjustable Regulator**
   - Adjustable output voltage design
   - Current limiting, thermal protection
2. **Discrete Linear Regulator (Pass Transistor)**
   - Op-amp + pass transistor topology
   - Feedback loop compensation
   - Foldback current limiting

3. **Buck Converter (Step-Down)**
   - Basic switching topology
   - Inductor sizing, ripple calculation
   - Continuous vs discontinuous conduction
4. **Boost Converter (Step-Up)**
   - Voltage step-up from lower input
   - Duty cycle vs output voltage relationship
5. **Buck-Boost Converter**
   - Inverting topology
   - Input voltage range flexibility
6. **Synchronous Buck Converter**
   - High-efficiency design with active rectification
   - Dead-time control, shoot-through prevention
7. **Flyback Converter**
   - Isolated power supply topology
   - Transformer design considerations
8. **Current Limiting Circuit**
   - Constant current, foldback limiting
   - Pass device protection
9. **Crowbar Overvoltage Protection**
   - SCR-based protection
   - Fuse coordination
10. **Soft-Start Circuit**
    - Inrush current limiting
    - Capacitor-controlled ramp
11. **Reverse Polarity Protection**
    - Diode vs P-FET protection
    - Voltage drop considerations

3.5 Phase 4: Digital Logic & Mixed-Signal

Phase 4 Circuits — Digital & Mixed

Duration: 4–5 weeks **Circuit Count:** 20 circuits

Digital logic, data conversion, and mixed-signal integration.

○ Digital & Mixed-Signal Circuits

1. **Level Shifter (5V to 3.3V)**
   - Resistor divider, dedicated IC approaches
   - Bidirectional level shifting

2. **Logic Gate Fundamentals**
   - AND, OR, NAND, NOR, XOR gates
   - Propagation delay, fan-out
3. **D Flip-Flop**
   - Setup/hold time demonstration
   - Metastability visualization
4. **Binary Counter**
   - Ripple vs synchronous
   - Timing analysis
5. **Shift Register**
   - Serial-to-parallel conversion
   - SPI interface fundamentals
6. **R-2R DAC**
   - Basic digital-to-analog conversion
   - Monotonicity, DNL, INL
7. **Flash ADC (3-bit)**
   - Parallel comparator architecture
   - Speed vs resolution trade-off
8. **Successive Approximation ADC**
   - SAR algorithm visualization
   - Conversion timing
9. **Delta-Sigma Modulator**
   - Oversampling concept
   - Noise shaping demonstration
10. **Anti-Aliasing Filter**
    - Nyquist frequency considerations
    - Filter order vs aliasing
11. **PWM Generation**
    - Timer-based PWM
    - Analog reconstruction
12. **Button Debouncing**
    - Hardware RC debounce
    - Software debounce algorithm
13. **I2C Interface**
    - Pull-up resistor selection
    - Bus timing, clock stretching
14. **SPI Interface**
    - Clock polarity/phase modes
    - Multi-device bus

3.6 Phase 5: High-Speed & RF-Lite

Phase 5 Circuits — High-Speed

Duration: 4–6 weeks **Circuit Count:** 12 circuits
High-frequency design, transmission lines, and signal integrity.

○ High-Speed Circuits

1. **Transmission Line (50Ω)**
   - Reflection visualization with various terminations
   - Open, short, matched, and mismatched loads
   - TDR-style analysis
2. **50Ω Line Driver**
   - High-speed buffer design
   - Output impedance matching
3. **Current-Feedback Amplifier**
   - CFB vs VFB comparison
   - Bandwidth independence from gain
4. **Video Buffer**
   - Wide bandwidth, low distortion
   - Back-termination techniques
5. **Crystal Oscillator**
   - Pierce oscillator topology
   - Load capacitance selection
   - Start-up behavior
6. **Phase-Locked Loop (Basic)**
   - Phase detector, loop filter, VCO
   - Lock acquisition visualization
7. **RF Amplifier (Low-Noise)**
   - Input/output matching
   - Noise figure optimization

Chapter 4

Circuit Inventory: X Chapters Curriculum

The X Chapters curriculum represents advanced topics requiring sophisticated simulation capabilities.

4.1 Phase 1: Advanced Analog & Power Core

4.1.1 Project A1: Multi-Output Lab Power Supply

○ A1 Power Supply Circuits

Complete multi-rail laboratory power supply with the following subsystems:

1. **5V/3A Digital Rail**
   - Fixed output with tight regulation
   - Overcurrent protection
2. **3.3V/3A Digital Rail**
   - Modern logic/MCU supply
   - Low-noise design for sensitive digital
3. **Adjustable 0–24V/3A Rail**
   - Wide output range with constant regulation
   - Pre-regulator + linear post-regulator topology
   - Foldback current limiting visualization
4. **±12V/1A Symmetric Rails**
   - Op-amp supply rails
   - Tracking behavior demonstration
   - Start-up sequencing
5. **Protection Circuits**
   - SOA (Safe Operating Area) visualization
   - Thermal shutdown modeling
   - Reverse current protection

6. **Loop Compensation**
   - Bode plot analysis
   - Phase margin, gain margin visualization
   - Step load transient response

4.1.2 Project A2: Precision Transresistance Amplifier

○ A2 TIA Circuits

Low-noise photodiode amplifier with femtoampere sensitivity:

1. **Ultra-Low-Noise TIA (Slow)**
   - Bandwidth: 1–10 kHz
   - Input-referred noise: <10 fA/$\sqrt{\text{Hz}}$
   - FET-input op-amp (OPA627, AD549)
2. **Fast TIA**
   - Bandwidth: 100 kHz – 1 MHz
   - Noise-bandwidth trade-off demonstration
3. **Noise Analysis Features**
   - Johnson-Nyquist noise visualization
   - Op-amp voltage/current noise
   - Noise bandwidth calculation
4. **Stability Compensation**
   - Photodiode capacitance effect
   - Feedback capacitor sizing
   - Phase margin optimization

4.1.3 Project A3: High-Speed Op-Amp Circuit

○ A3 High-Speed Circuits

High-frequency amplifier designs (50+ MHz bandwidth):

1. **Gain-of-10 VFB Amplifier**
   - Voltage-feedback topology
   - GBW product verification
2. **Gain-of-10 CFB Amplifier**
   - Current-feedback topology comparison
   - Bandwidth vs gain behavior
3. **Differential Amplifier**
   - Single-ended to differential conversion
   - Matched delay paths
4. **PCB Parasitic Effects**
   - Trace inductance modeling
   - Ground plane effects
   - Decoupling effectiveness

4.1.4 Project A4: High-Energy Pulser / Coil Driver

○ A4 Power Switching Circuits

High-current switching circuits with protection:

1. **Fast LED Driver**
   - Nanosecond pulse generation
   - 10A peak current capability
2. **Inductive Coil Driver**
   - Solenoid actuation
   - Flyback voltage demonstration
3. **MOSFET Gate Drive**
   - Gate charge calculation
   - Miller plateau visualization
   - Gate driver IC behavior
4. **Snubber Design**
   - RC snubber optimization
   - RCD clamp circuits
   - dV/dt and dI/dt control
5. **Inductive Kickback**
   - $V = L \cdot di/dt$ visualization
   - Clamp diode operation
   - Energy dissipation

4.1.5 Project A5: Precision Measurement Instrument

○ A5 Measurement Circuits

Complete measurement front-end integration:

1. **Precision DC Voltmeter Front-End**
   - $\pm 10\mu$V to $\pm$10V range
   - Input impedance >1GΩ
   - 1μV resolution
2. **Low-Noise AC Probe**
   - 1 Hz – 100 kHz bandwidth
   - <10 nV/$\sqrt{\text{Hz}}$ noise floor
   - Differential input, high CMRR
3. **Simple Impedance Probe**
   - R, L, C measurement at fixed frequencies
   - Phase detection
   - Component verification
4. **Error Budget Analysis**
   - Interactive error source tracking
   - Offset, gain, linearity errors
   - Temperature coefficient effects

4.2 Phase 2: Digital & Embedded Foundations

4.2.1 Project D1: Breadboard Computer

○ D1 CPU Building Blocks

Discrete logic implementation of a minimal processor:

1. **Clock Generator**
   - Crystal oscillator or 555-based
   - Single-step mode for debugging
2. **Program Counter**
   - 8-bit counter with load capability
   - Jump instruction support
3. **Register File**
   - 4–8 general-purpose registers
   - Read/write port timing
4. **ALU (Arithmetic Logic Unit)**
   - ADD, AND, OR, XOR operations
   - Carry/overflow flag generation
5. **Instruction Decoder**
   - ROM-based microcode or hardwired
   - Control signal generation
6. **Memory Interface**
   - Address decoding
   - Read/write cycle timing
   - Memory-mapped I/O
7. **Bus Architecture**
   - Tristate buffer control
   - Bus contention detection

4.2.2 Project D2: FPGA-Based System

○ D2 FPGA Circuits

HDL-based digital system with analog interfaces:

1. **Simple Processor Core**
   - Behavioral simulation of instruction execution
   - Register transfer level visualization
2. **SPI Master Controller**
   - Configurable clock rate
   - Multiple device support
3. **UART Transmitter/Receiver**
   - Baud rate generation
   - Start/stop bit framing
4. **PWM Controller**

- Variable frequency and duty cycle
- Dead-time insertion

5. **ADC Interface**
   - SPI-based ADC control
   - Sample timing coordination
6. **Clock Domain Crossing**
   - Two-flip-flop synchronizer
   - Gray code counter crossing
   - Async FIFO

4.3 Phase 3: Embedded Systems with RTOS

4.3.1 Project E1: ARM MCU + RTOS Platform

○ E1 Embedded Circuits

MCU peripheral interface circuits:

1. **MCU Power Supply Filtering**
   - Decoupling capacitor placement
   - Ferrite bead usage
2. **Crystal Oscillator Interface**
   - Load capacitor selection
   - Start-up reliability
3. **Reset Circuit**
   - Brown-out detection
   - Manual reset debouncing
4. **Debug Interface (SWD)**
   - Connector pinout
   - Series resistor protection
5. **GPIO Protection**
   - ESD protection
   - Current limiting

4.3.2 Project E2: Embedded Instrument / Controller

○ E2 System Integration Circuits

Complete system integration simulations:

1. **Digitally-Controlled Power Supply**
   - DAC/PWM setpoint control
   - ADC voltage/current monitoring
   - Closed-loop regulation
2. **Data Acquisition System**
   - Multi-channel ADC sampling

- Triggering and capture
- SD card interface

3. **Function Generator**
   - DDS waveform synthesis
   - DAC reconstruction
   - Output conditioning
4. **Mixed-Signal Grounding**
   - Ground plane partitioning
   - Star grounding
   - Digital noise isolation

Chapter 5

User Interface Design

5.1 Core UI Components

5.1.1 Circuit Canvas

The primary interaction surface for circuit manipulation:

- **Schematic View:** Traditional electronics schematic representation with standard symbols
- **Component Palette:** Drag-and-drop component library organized by category
- **Wire Routing:** Automatic orthogonal routing with manual override capability
- **Node Highlighting:** Visual indication of connected nodes
- **Zoom/Pan:** Smooth navigation for complex circuits
- **Grid Snap:** Configurable grid for neat layouts

5.1.2 Virtual Instruments

Table 5.1: Virtual Instrument Requirements

Instrument	Features	Priority
Digital Multimeter	DC/AC voltage, current, resistance, continuity	P0
Oscilloscope	2–4 channels, triggering, cursors, FFT, XY mode	P0
Function Generator	Sine, square, triangle, arbitrary waveforms	P0
Bode Plotter	Magnitude/phase vs frequency, log/linear scales	P0
Power Supply	Adjustable voltage/current, display, limiting	P1
Spectrum Analyzer	FFT-based frequency domain display	P1
Logic Analyzer	Multi-channel digital capture, protocol decode	P2
Curve Tracer	I-V characteristic plotting for semiconductors	P2

5.1.3 Simulation Controls

- **Analysis Selection:** DC operating point, AC sweep, transient, noise
- **Parameter Entry:** Time range, frequency range, sweep points
- **Run Controls:** Start, stop, pause, single-step
- **Progress Indication:** Simulation progress for long analyses
- **Results Management:** Save, load, export simulation data

5.2 Educational Features

5.2.1 Guided Exercises

Each circuit includes structured learning activities:

1. **Objective Statement:** Clear learning goal
2. **Step-by-Step Instructions:** Guided procedure
3. **Measurement Challenges:** Specific values to measure
4. **Calculation Verification:** Compare calculated vs simulated
5. **"What If" Explorations:** Guided parameter variations
6. **Troubleshooting Scenarios:** Diagnose intentionally faulty circuits

5.2.2 AoE Reference Integration

- **Section Links:** Direct references to AoE book sections
- **Rule-of-Thumb Display:** Relevant rules shown in context
- **Equation Reference:** Key formulas with variable highlighting
- **Design Guidelines:** Practical advice from the text

5.2.3 Progress Tracking

- **Curriculum Map:** Visual overview of all phases and circuits
- **Completion Status:** Track completed exercises
- **Achievement Badges:** Gamification elements for motivation
- **Lab Notebook:** Save notes, screenshots, measurement data

5.3 Responsive Design

The application must support multiple form factors:

Table 5.2: Platform Support Requirements

Platform	**Primary Use Case**	**Constraints**
Desktop (1920×1080+)	Full simulation environment	None
Laptop (1366×768)	Portable learning	Reduced canvas size
Tablet (iPad)	Touch-based interaction	No hover states
Mobile (phone)	Quick reference, simple circuits	Very limited space

Chapter 6

Development Roadmap

6.1 Phase I: Foundation (Months 1–5)

⋆ Phase I: Core Infrastructure

Goal: Establish fundamental architecture and demonstrate feasibility with 20 foundational circuits.

Deliverables:

1. Core simulation engine integration (ngspice-WebAssembly)
2. Basic schematic editor with component library
3. Virtual oscilloscope and multimeter
4. Phase 0 circuits complete (8 circuits)
5. Basic op-amp circuits (12 circuits)
6. User authentication and progress tracking

Technical Milestones:

- Week 4: WebAssembly SPICE engine running in browser
- Week 8: Schematic editor MVP with 20 components
- Week 12: Oscilloscope displaying transient simulation results
- Week 16: First 10 circuits fully functional
- Week 20: Phase I complete, internal alpha release

6.1.1 Sprint Breakdown: Phase I

Table 6.1: Phase I Sprint Plan

Sprint	Duration	Focus
1–2	4 weeks	Project setup, SPICE engine evaluation and integration
3–4	4 weeks	Schematic editor core: canvas, components, wiring
5–6	4 weeks	Simulation pipeline: netlist generation, SPICE execution
7–8	4 weeks	Virtual instruments: oscilloscope, DMM
9–10	4 weeks	Circuit library: Phase 0 + basic op-amps

6.2 Phase II: Analog Core (Months 6–9)

⋆ Phase II: Analog Expansion

Goal: Complete Phase 1 curriculum circuits and add advanced analysis capabilities.
Deliverables:
1. Complete op-amp circuit library (all configurations)
2. Active filter circuits (Sallen-Key, MFB, state-variable)
3. Transistor circuits (BJT/MOSFET switches, amplifiers)
4. Bode plotter for frequency response
5. AC analysis integration
6. Parameter sweep functionality

Circuit Count: 25 additional circuits (Total: 45)

6.3 Phase III: Precision & Power (Months 10–13)

⋆ Phase III: Precision & Power Electronics

Goal: Add precision instrumentation circuits and power supply simulations.
Deliverables:
1. Noise analysis engine and visualization
2. Instrumentation amplifier circuits
3. Transimpedance amplifier with noise budget tool
4. Linear regulator circuits (7805, LM317, discrete)
5. Switching regulator simulations (buck, boost, buck-boost)
6. Protection circuit demonstrations
7. Thermal modeling for power devices

Circuit Count: 33 additional circuits (Total: 78)

6.4 Phase IV: Digital & Mixed-Signal (Months 14–17)

⋆ Phase IV: Digital Integration

Goal: Add digital logic simulation and mixed-signal capabilities.
Deliverables:
1. Digital logic simulation engine
2. Logic analyzer virtual instrument
3. ADC/DAC behavioral models
4. Level shifter and interface circuits
5. D1 Breadboard Computer simulation

6. D2 FPGA module simulations
7. Mixed-signal co-simulation

Circuit Count: 35 additional circuits (Total: 113)

6.5 Phase V: Advanced Topics (Months 18–21)

⋆ Phase V: Advanced & High-Speed

Goal: Complete X Chapters advanced projects and high-speed simulations.
Deliverables:
1. Transmission line simulation with reflections
2. High-speed amplifier circuits (VFB/CFB)
3. A1–A5 project complete circuits
4. E1–E2 embedded system interfaces
5. PLL and oscillator circuits
6. RF-lite simulations

Circuit Count: 30 additional circuits (Total: 143)

6.6 Phase VI: Integration & Polish (Months 22–24)

⋆ Phase VI: Production Ready

Goal: Final integration, polish, and production deployment.
Deliverables:
1. Capstone project simulations
2. Complete curriculum integration
3. Performance optimization
4. Mobile responsiveness refinement
5. Documentation and help system
6. Production deployment
7. User feedback integration

Final Circuit Count: 150+ circuits

6.7 Milestone Summary

Table 6.2: Complete Milestone Timeline

Month	Phase	Circuits	Key Milestone
5	I Complete	20	Alpha release, core functionality
9	II Complete	45	Full analog simulation
13	III Complete	78	Precision & power circuits
17	IV Complete	113	Digital & mixed-signal
21	V Complete	143	Advanced topics
24	VI Complete	150+	Production launch

Chapter 7

Risk Analysis & Mitigation

7.1 Technical Risks

△ Critical Consideration

Risk 1: WebAssembly SPICE Performance
Description: ngspice compiled to WebAssembly may not achieve adequate performance for complex circuits or long transient simulations.
Impact: High — Core functionality depends on simulation speed.
Mitigation Strategies:
- Implement simulation timeouts with graceful degradation
- Offer server-side simulation fallback for complex circuits
- Optimize netlists to reduce simulation complexity
- Use adaptive time-stepping aggressively
- Consider Web Workers for non-blocking simulation

△ Critical Consideration

Risk 2: Mixed-Signal Simulation Accuracy
Description: Combining analog SPICE simulation with digital logic simulation while maintaining timing accuracy is challenging.
Impact: Medium — Affects Phase IV and V circuits.
Mitigation Strategies:
- Use behavioral models for ADC/DAC interfaces
- Accept some timing approximation for educational purposes
- Document accuracy limitations for users
- Implement event-driven digital simulation with analog checkpoints

△ Critical Consideration

Risk 3: Browser Compatibility
Description: WebAssembly and advanced JavaScript features may not work consistently across all browsers.

Impact: Medium — Affects user reach.
Mitigation Strategies:
- Target modern browsers only (Chrome, Firefox, Safari, Edge)
- Implement feature detection with clear error messages
- Provide system requirements documentation
- Test extensively on target platforms

7.2 Educational Risks

△ Critical Consideration

Risk 4: Simulation vs Reality Gap
Description: Students may develop unrealistic expectations from simulations that don't capture real-world parasitics, component variations, and environmental factors.
Impact: Medium — Affects educational effectiveness.
Mitigation Strategies:
- Include explicit "simulation limitations" notes with each circuit
- Add Monte Carlo analysis for component tolerance
- Include parasitic models where significant
- Encourage real hardware construction alongside simulation
- Document common "gotchas" when moving from simulation to hardware

7.3 Project Risks

△ Critical Consideration

Risk 5: Scope Creep
Description: The comprehensive nature of the curriculum (150+ circuits) creates risk of never-ending feature additions.
Impact: High — Affects schedule and budget.
Mitigation Strategies:
- Strict prioritization with P0/P1/P2 classification
- Time-boxed phases with hard deadlines
- MVP mindset: functional before perfect
- Regular scope reviews with stakeholders
- "Version 2" parking lot for future features

Chapter 8

Testing & Validation Strategy

8.1 Simulation Accuracy Validation

8.1.1 Reference Comparison

All circuit simulations must be validated against desktop SPICE results:

1. **LTspice Reference:** Export circuit to LTspice, compare DC, AC, and transient results
2. **Tolerance Definition:** Accept ±1% for DC, ±2% for AC, ±5% for transient
3. **Automated Regression:** CI/CD pipeline runs comparison tests on each commit
4. **Edge Case Coverage:** Test extreme component values, high frequencies, fast transients

8.1.2 Educational Verification

1. **AoE Rule-of-Thumb Verification:** Each circuit must demonstrate the relevant AoE principles
2. **Expected Behavior:** Document expected results for each exercise
3. **Common Mistakes:** Ensure simulator correctly shows incorrect circuit behavior
4. **Beta Testing:** Electronics students test curriculum flow

8.2 Performance Testing

Table 8.1: Performance Targets

Metric	Target	Measurement
Initial Load Time	<5 seconds on broadband	Lighthouse
Simple DC Analysis	<100 ms	Performance.now()
10ms Transient (simple)	<1 second	Performance.now()
AC Sweep (1Hz–1MHz)	<2 seconds	Performance.now()
Complex Circuit Load	<500 ms	Performance.now()
Memory Usage	<200 MB typical	DevTools

8.3 Usability Testing

1. **User Studies:** Observe students completing exercises
2. **Task Completion:** Measure time to complete standard tasks
3. **Error Rates:** Track common user mistakes
4. **Satisfaction Surveys:** Net Promoter Score tracking
5. **Accessibility:** WCAG 2.1 AA compliance testing

Chapter 9

Resource Requirements

9.1 Team Composition

Table 9.1: Recommended Team Structure

Role	Responsibilities	FTE
Project Lead	Architecture, technical decisions, stakeholder management	1.0
Frontend Developer(s)	React/Vue development, UI/UX implementation	2.0
Simulation Engineer	SPICE integration, numerical methods, accuracy	1.0
Backend Developer	API, authentication, data management	1.0
Electronics SME	Circuit design review, educational content	0.5
QA Engineer	Testing, automation, validation	1.0
UX Designer	Interface design, user research	0.5
Total		**7.0 FTE**

9.2 Infrastructure Costs

Table 9.2: Estimated Monthly Infrastructure Costs

Service	Purpose	Monthly Cost
Cloud Hosting (AWS/GCP)	Application servers, CDN	$500–1,500
Database (PostgreSQL)	User data, circuits, progress	$100–300
Redis Cache	Session management, caching	$50–100
Storage (S3/R2)	Circuit files, user projects	$50–100
Authentication (Auth0)	User management	$100–500
Monitoring (Datadog/etc)	Performance, errors	$100–300
CI/CD (GitHub Actions)	Build, test, deploy	$100–200
Total (Development)		**$1,000–3,000/mo**
Total (Production)		**$2,000–5,000/mo**

9.3 Development Tools

- **IDE:** VS Code with relevant extensions
- **Version Control:** GitHub with branch protection
- **Project Management:** Jira, Linear, or GitHub Projects
- **Design:** Figma for UI mockups
- **Documentation:** Notion or Confluence
- **Communication:** Slack or Discord

Appendix A

Complete Circuit Inventory

A.1 AoE Main Curriculum Circuits

Table A.1: Complete AoE Main Curriculum Circuit List

ID	Circuit Name	Phase	Priority
P0-01	7805 Linear Voltage Regulator	Phase 0	P0
P0-02	RC Low-Pass Filter	Phase 0	P0
P0-03	RC High-Pass Filter	Phase 0	P0
P0-04	Voltage Divider Network	Phase 0	P0
P0-05	Half-Wave Rectifier	Phase 0	P0
P0-06	Full-Wave Bridge Rectifier	Phase 0	P0
P0-07	Zener Diode Regulator	Phase 0	P1
P0-08	LED Current Limiting	Phase 0	P0
P1-01	Inverting Amplifier	Phase 1	P0
P1-02	Non-Inverting Amplifier	Phase 1	P0
P1-03	Unity-Gain Buffer	Phase 1	P0
P1-04	Summing Amplifier	Phase 1	P1
P1-05	Difference Amplifier	Phase 1	P0
P1-06	Integrator	Phase 1	P1
P1-07	Differentiator	Phase 1	P1
P1-08	Comparator with Hysteresis	Phase 1	P0
P1-09	Sallen-Key Low-Pass (2nd Order)	Phase 1	P0
P1-10	Sallen-Key High-Pass (2nd Order)	Phase 1	P1
P1-11	MFB Bandpass Filter	Phase 1	P1
P1-12	State-Variable Filter	Phase 1	P2
P1-13	Twin-T Notch Filter	Phase 1	P2
P1-14	BJT Switch (NPN)	Phase 1	P0
P1-15	BJT Switch (PNP)	Phase 1	P1
P1-16	MOSFET Switch (N-Channel)	Phase 1	P0
P1-17	Emitter Follower	Phase 1	P0

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Table A.1 – continued

ID	Circuit Name	Phase	Priority
P1-18	Source Follower	Phase 1	P1
P1-19	Common Emitter Amplifier	Phase 1	P1
P1-20	Darlington Pair	Phase 1	P1
P1-21	Current Mirror	Phase 1	P1
P2-01	Three-Op-Amp Instrumentation Amplifier	Phase 2	P0
P2-02	Integrated In-Amp (INA128)	Phase 2	P0
P2-03	Transimpedance Amplifier	Phase 2	P0
P2-04	Low-Noise Preamplifier	Phase 2	P1
P2-05	Chopper-Stabilized Amplifier	Phase 2	P2
P2-06	Precision Voltage Reference	Phase 2	P0
P2-07	4-Wire Kelvin Measurement	Phase 2	P1
P2-08	Wheatstone Bridge	Phase 2	P0
P2-09	Active Guard Driver	Phase 2	P2
P2-10	Sample-and-Hold Circuit	Phase 2	P1
P3-01	LM317 Adjustable Regulator	Phase 3	P0
P3-02	Discrete Linear Regulator	Phase 3	P0
P3-03	Buck Converter	Phase 3	P0
P3-04	Boost Converter	Phase 3	P0
P3-05	Buck-Boost Converter	Phase 3	P1
P3-06	Synchronous Buck Converter	Phase 3	P1
P3-07	Flyback Converter	Phase 3	P2
P3-08	Foldback Current Limiter	Phase 3	P0
P3-09	Crowbar OVP	Phase 3	P1
P3-10	Soft-Start Circuit	Phase 3	P1
P3-11	Reverse Polarity Protection	Phase 3	P0
P4-01	Level Shifter (5V/3.3V)	Phase 4	P0
P4-02	Logic Gates (AND/OR/NAND/NOR)	Phase 4	P0
P4-03	D Flip-Flop	Phase 4	P0
P4-04	Binary Counter	Phase 4	P0
P4-05	Shift Register	Phase 4	P1
P4-06	R-2R DAC	Phase 4	P0
P4-07	Flash ADC (3-bit)	Phase 4	P1
P4-08	SAR ADC	Phase 4	P0
P4-09	Delta-Sigma Modulator	Phase 4	P2
P4-10	Anti-Aliasing Filter	Phase 4	P0
P4-11	PWM Generator	Phase 4	P0
P4-12	Button Debounce	Phase 4	P0
P4-13	I2C Interface	Phase 4	P1
P4-14	SPI Interface	Phase 4	P1
P5-01	50Ω Transmission Line	Phase 5	P0
P5-02	50Ω Line Driver	Phase 5	P1
P5-03	Current-Feedback Amplifier	Phase 5	P1

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Table A.1 – continued

ID	Circuit Name	Phase	Priority
P5-04	Video Buffer	Phase 5	P2
P5-05	Crystal Oscillator	Phase 5	P1
P5-06	Basic PLL	Phase 5	P2
P5-07	RF LNA	Phase 5	P2

A.2 X Chapters Curriculum Circuits

Table A.2: Complete X Chapters Circuit List

ID	Circuit Name	Project	Priority
A1-01	5V/3A Digital Supply Rail	A1	P0
A1-02	3.3V/3A Digital Supply Rail	A1	P0
A1-03	0-24V Adjustable Rail	A1	P0
A1-04	+12V Symmetric Rail	A1	P0
A1-05	-12V Symmetric Rail	A1	P0
A1-06	SOA Protection Circuit	A1	P1
A1-07	Thermal Shutdown	A1	P1
A1-08	Loop Compensation Demo	A1	P0
A2-01	Ultra-Low-Noise TIA (Slow)	A2	P0
A2-02	Fast TIA	A2	P0
A2-03	TIA Noise Analysis	A2	P0
A2-04	TIA Stability Compensation	A2	P0
A3-01	Gain-of-10 VFB Amplifier	A3	P0
A3-02	Gain-of-10 CFB Amplifier	A3	P0
A3-03	Differential Amplifier (High-Speed)	A3	P1
A3-04	PCB Parasitic Effects Demo	A3	P1
A4-01	Fast LED Driver	A4	P0
A4-02	Inductive Coil Driver	A4	P0
A4-03	MOSFET Gate Drive Circuit	A4	P0
A4-04	RC/RCD Snubber	A4	P0
A4-05	Inductive Kickback Demo	A4	P0
A5-01	Precision DC Voltmeter Front-End	A5	P0
A5-02	Low-Noise AC Probe	A5	P1
A5-03	Simple Impedance Probe	A5	P2
A5-04	Error Budget Analysis Tool	A5	P1
D1-01	Clock Generator	D1	P0
D1-02	Program Counter	D1	P0
D1-03	Register File	D1	P0
D1-04	ALU	D1	P0
D1-05	Instruction Decoder	D1	P1
D1-06	Memory Interface	D1	P1
D1-07	Bus Architecture	D1	P0

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Table A.2 – continued

ID	**Circuit Name**	**Project**	**Priority**
D2-01	Simple Processor Core	D2	P1
D2-02	SPI Master Controller	D2	P0
D2-03	UART TX/RX	D2	P0
D2-04	PWM Controller	D2	P0
D2-05	ADC Interface	D2	P1
D2-06	Clock Domain Crossing	D2	P1
E1-01	MCU Power Supply Filtering	E1	P0
E1-02	Crystal Oscillator Interface	E1	P0
E1-03	Reset Circuit	E1	P0
E1-04	Debug Interface (SWD)	E1	P1
E1-05	GPIO Protection	E1	P0
E2-01	Digitally-Controlled PSU	E2	P1
E2-02	Data Acquisition System	E2	P1
E2-03	Function Generator	E2	P2
E2-04	Mixed-Signal Grounding	E2	P0

Appendix B

Glossary

AC Analysis
: Frequency-domain simulation showing gain and phase vs frequency (Bode plot).

ADC
: Analog-to-Digital Converter; converts continuous analog signals to discrete digital values.

Bode Plot
: Graph showing magnitude and phase response of a circuit vs frequency.

CFB
: Current-Feedback (op-amp topology with bandwidth nearly independent of gain).

CMRR
: Common-Mode Rejection Ratio; measure of differential amplifier's ability to reject common-mode signals.

DAC
: Digital-to-Analog Converter; converts digital values to analog voltages or currents.

DC Operating Point
: Steady-state analysis showing all node voltages and branch currents with no time-varying inputs.

ENOB
: Effective Number of Bits; actual resolution of an ADC considering noise and distortion.

GBW
: Gain-Bandwidth Product; constant for voltage-feedback op-amps relating gain to bandwidth.

HDL
: Hardware Description Language (Verilog, VHDL); used to describe digital circuits.

In-Amp
: Instrumentation Amplifier; precision differential amplifier with high CMRR.

Monte Carlo
: Statistical analysis varying component values to assess circuit tolerance.

Noise Analysis
: Simulation calculating noise contributions from all circuit elements.

RTOS
: Real-Time Operating System; OS designed for deterministic timing behavior.

SAR
: Successive Approximation Register (ADC architecture).

SPICE Simulation Program with Integrated Circuit Emphasis; industry-standard circuit simulator.

TDR Time-Domain Reflectometry; technique for analyzing transmission line discontinuities.

TIA Transimpedance Amplifier; converts input current to output voltage.

Transient Analysis
Time-domain simulation showing circuit response over time.

VFB Voltage-Feedback (traditional op-amp topology with constant GBW product).

WebAssembly
Binary instruction format enabling near-native code execution in web browsers.

"The best way to learn electronics is to build things. The second best way is to simulate them first."

— Adapted from Horowitz & Hill

Document Summary

Total Circuits:	150+
Development Phases:	6
Estimated Timeline:	18–24 months
Primary Sources:	AoE 3rd Edition, X Chapters