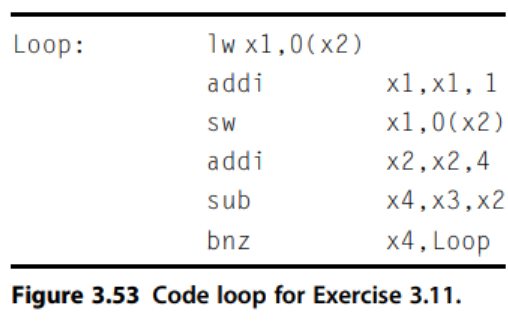
**2st Homework for Computer Architecture**

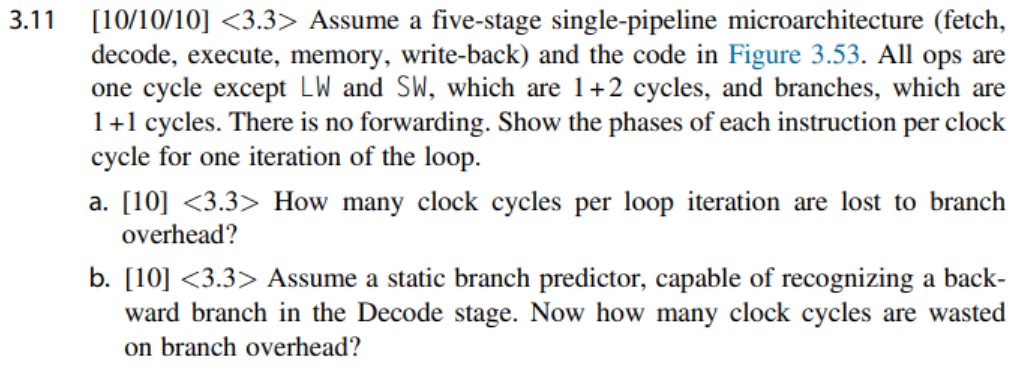
**Read Chapter 3 Appendix C then do the following problems.**

**(Total 105 points)**

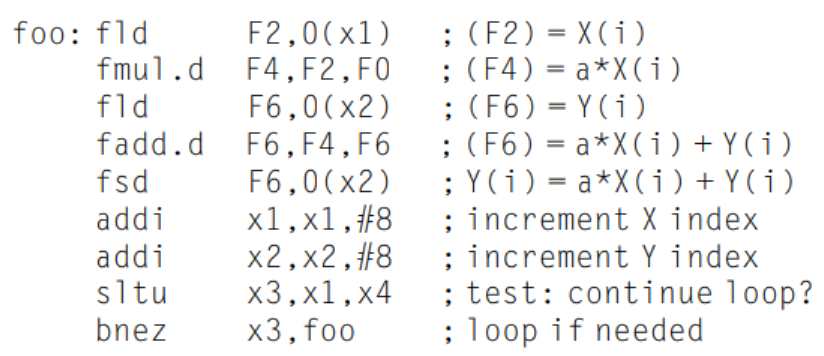
**In 6th Edition**

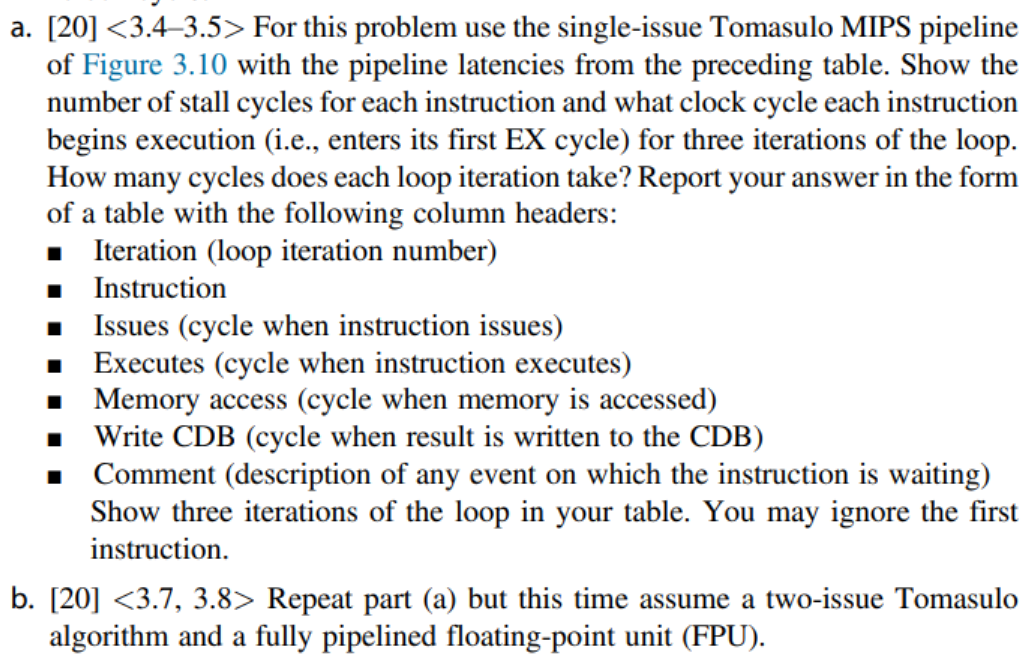
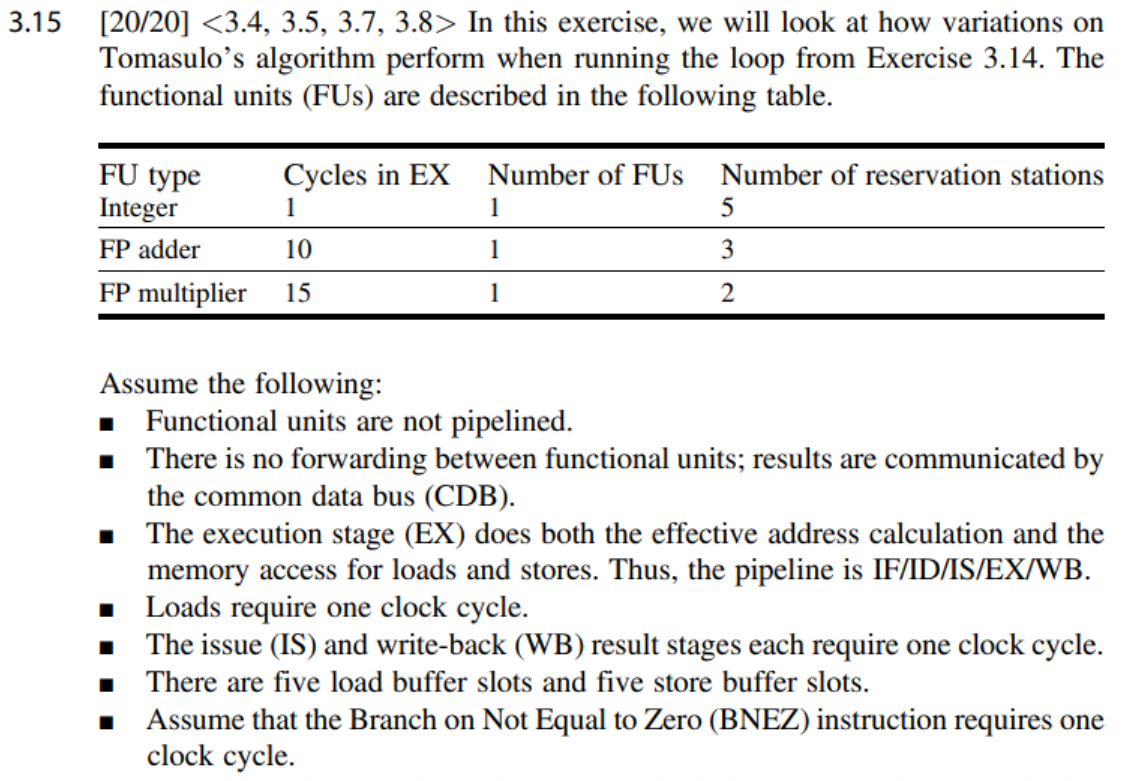
**3.11 3.15 3.16 3.17(不做要求，建议自己推一下) C.10**





|  |  |
| --- | --- |
| **Answer** | |
| **a** | 5 clock cycles per loop iteration are lost to branch overhead. 如果没有overhead下一个迭代的F应该在bnz的D状态下面，由于bnz需要执行完E后lw才能够读入，那么sub和bnz的数据冲突导致D执行3个周期，之后题干说bnz的E是2个周期。注意：其中如果发生数据冲突，在有double bump的情况下同一个周期的上一条指令的W能够在下降沿将寄存器传到下一条指令的D状态。 |
| **b** | 1 cycle lost with static predictor.（说法合理即可）如果偏移地址能够在D阶段被计算，那么D的下一个周期能够fetch下一轮的instruction（lw）所以相比之下只需要停1个周期。 |
| **c** | 0 cycle lost. 因为动态预测器能够记录上次迭代bnz指令跳转的地址，直接去取，不用停顿。 |



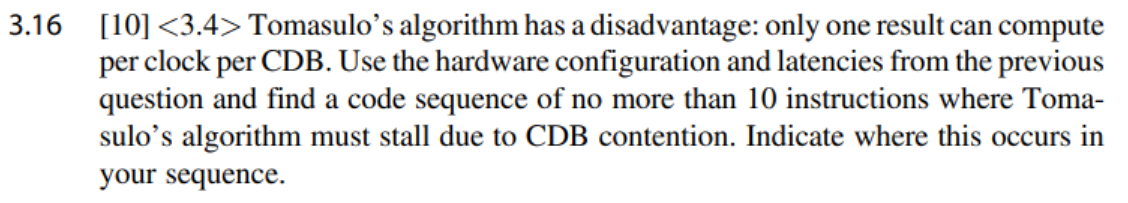


**(a)**

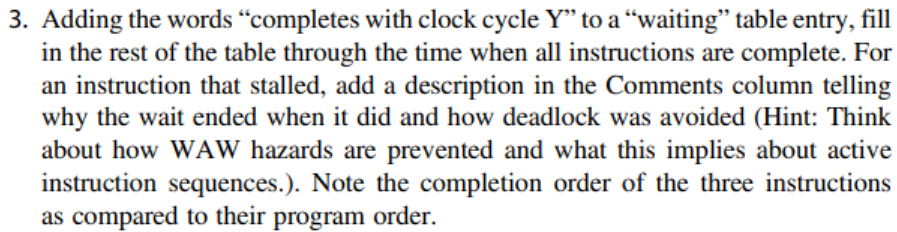
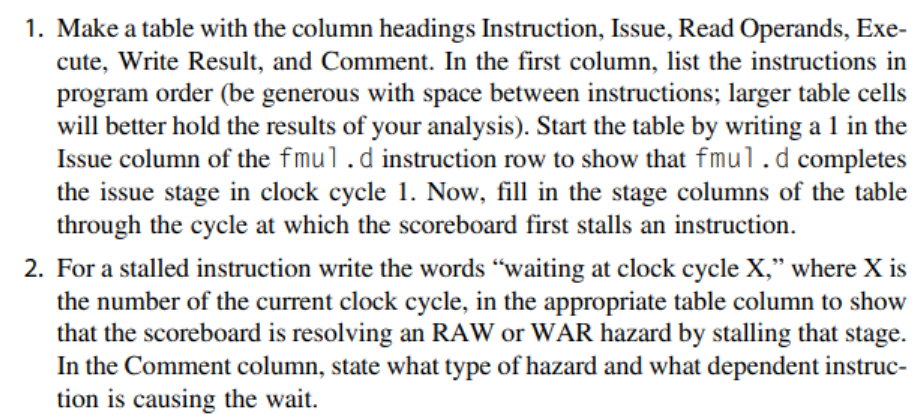
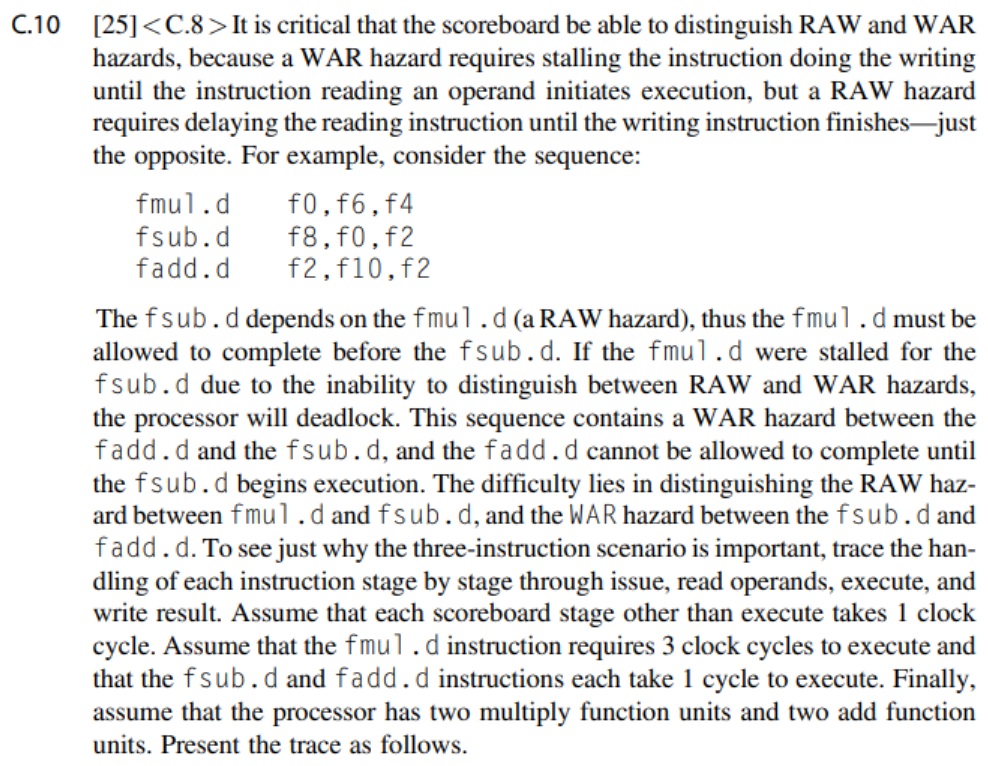
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| No. | Iter. | Inst. | Issue | Execute  /Memory | Write  CDB | Comment |
| 1 | 1 | fld F2, 0(x1) | 1 | 2 | 3 |  |
| 2 | 1 | fmul.d F4, F2, F0 | 2 | 4 | 19 | 等指令1的F2 |
| 3 | 1 | fld F6, 0(x2) | 3 | 4 | 5 |  |
| 4 | 1 | fadd.d F6, F4, F6 | 4 | 20 | 30 | 等指令2的F4 |
| 5 | 1 | fsd F6, 0(x2) | 5 | 31 |  | 等指令4的F6 |
| 6 | 1 | addi x1, x1, #8 | 6 | 7 | 8 |  |
| 7 | 1 | addi x2, x2, #8 | 7 | 8 | 9 |  |
| 8 | 1 | sltu x3, x1, x4 | 8 | 9 | 10 |  |
| 9 | 1 | bnez x3, foo | 9 | 11 |  | 等指令8的x3 |
| 10 | 2 | fld F2, 0(x1) | 10 | 12 | 13 | 等指令bnez |
| 11 | 2 | fmul.d F4, F2, F0 | 11 | 14（19） | 34 | 等指令10的F2，之后等指令2的Mul FU |
| 12 | 2 | fld F6, 0(x2) | 12 | 13 | 14 |  |
| 13 | 2 | fadd.d F6, F4, F6 | 13 | 35 | 45 | 等指令11的F4 |
| 14 | 2 | fsd F6, 0(x2) | 14 | 46 |  | 等指令13的F6 |
| 15 | 2 | addi x1, x1, #8 | 15 | 16 | 17 |  |
| 16 | 2 | addi x2, x2, #8 | 16 | 17 | 18 |  |
| 17 | 2 | sltu x3, x1, x4 | 17 | 18 | 20 |  |
| 18 | 2 | bnez x3, foo | 18 | 20 |  | 等指令17的x3 |
| 19 | 3 | fld F2, 0(x1) | 19 | 21 | 22 | 等指令bnez |
| 20 | 3 | fmul.d F4, F2, F0 | 20 | 23（34） | 49 | 等指令19的F2，之后等指令11的Mul FU |
| 21 | 3 | fld F6, 0(x2) | 21 | 22 | 23 |  |
| 22 | 3 | fadd.d F6, F4, F6 | 22 | 50 | 60 | 等指令20的F4 |
| 23 | 3 | fsd F6, 0(x2) | 23 | 61 |  | 等指令22的F6 |
| 24 | 3 | addi x1, x1, #8 | 24 | 25 | 26 |  |
| 25 | 3 | addi x2, x2, #8 | 25 | 26 | 27 |  |
| 26 | 3 | sltu x3, x1, x4 | 26 | 27 | 28 |  |
| 27 | 3 | bnez x3, foo | 27 | 29 |  | 等指令26的x3 |

**(b)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| No. | Iter. | Inst. | Issue | Execute/  Memory | Write  CDB | Comment |
| 1 | 1 | fld F2, 0(x1) | 1 | 2 | 3 |  |
| 2 | 1 | fmul.d F4, F2, F0 | 1 | 4 | 19 | 等指令1的F2 |
| 3 | 1 | fld F6, 0(x2) | 2 | 3 | 4 |  |
| 4 | 1 | fadd.d F6, F4, F6 | 2 | 20 | 30 | 等指令2的F4 |
| 5 | 1 | fsd F6, 0(x2) | 3 | 31 |  | 等指令4的F6 |
| 6 | 1 | addi x1, x1, #8 | 3 | 4 | 5 |  |
| 7 | 1 | addi x2, x2, #8 | 4 | 5 | 6 |  |
| 8 | 1 | sltu x3, x1, x4 | 4 | 6 | 7 | 等指令7的Int FU |
| 9 | 1 | bnez x3, foo | 5 | 7 |  | 等指令8的x3 |
| 10 | 2 | fld F2, 0(x1) | 6 | 8 | 9 | 指令9为跳转，发射在下一周期。等指令9的Int FU |
| 11 | 2 | fmul.d F4, F2, F0 | 6 | 10 | 25 | 等待指令10的F2，全流水，Mul FU不冲突 |
| 12 | 2 | fld F6, 0(x2) | 7 | 9 | 10 | 等指令10的Int FU |
| 13 | 2 | fadd.d F6, F4, F6 | 7 | 26 | 36 | 等指令11的F4 |
| 14 | 2 | fsd F6, 0(x2) | 8 | 37 |  | 等指令13的F6 |
| 15 | 2 | addi x1, x1, #8 | 8 | 10 | 11 | 等指令12的Int FU |
| 16 | 2 | addi x2, x2, #8 | 9 | 11 | 12 | 等指令15的Int FU |
| 17 | 2 | sltu x3, x1, x4 | 9 | 12 | 13 | 等指令16的Int FU |
| 18 | 2 | bnez x3, foo | 10 | 14 |  | 等指令17的x3 |
| 19 | 3 | fld F2, 0(x1) | 11 | 15 | 16 | 等指令bnez |
| 20 | 3 | fmul.d F4, F2, F0 | 20 | 21 | 36 | 等待指令2退出保留站，否则结构冲突不能发射 |
| 21 | 3 | fld F6, 0(x2) | 20 | 21 | 22 |  |
| 22 | 3 | fadd.d F6, F4, F6 | 21 | 37 | 47 | 等指令20的F4 |
| 23 | 3 | fsd F6, 0(x2) | 21 | 48 |  | 等指令22的F6 |
| 24 | 3 | addi x1, x1, #8 | 22 | 23 | 24 |  |
| 25 | 3 | addi x2, x2, #8 | 22 | 24 | 25 | 等指令24的Int FU |
| 26 | 3 | sltu x3, x1, x4 | 23 | 25 | 26 | 等指令24的x1，等指令25的Int FU |
| 27 | 3 | bnez x3, foo | 23 | 27 |  | 等指令26的x3 |



|  |  |
| --- | --- |
| **Answer** | |
| **a** |  |



**Ans:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Instruction | Issue | Read Operands | Execute | Write Result | Comment |
| fmul.d f0, f6, f4 | 1 | 2 | 3 | 6 |  |
| fsub.d f8, f0, f2 | 2 | waiting at clock cycle 2, completes at clock cycle 7 | 8 | 9 | Wait for f0. RAW |
| fadd.d f2, f10, f2 | 3 | 4 | 5 | waiting at clock cycle 6, complete at clock cycle 8 | wait for f2 to be read. WAW |

**Completion order: fmul.d, fadd.d, fsub.d**