

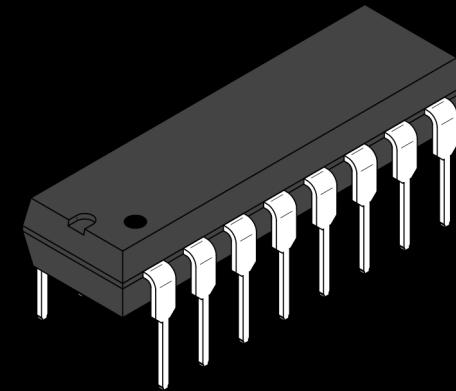
# Hardwarepraktikum II

Erstellt von Nour Hashem & Nouralrahman Hussain

Versuch: 6

Matrikelnummer: 81575

Matrikelnummer: 79968



# Benötigte Bauelemente

Würfelanzeige

Diverse Grundgatter

2.1 DM74LS08N

2.2 DM74LS14N

2.3 DM74LS32N

2.3 SN74LS00N

DL193D 4-Bit Zähler

Gal16v8d

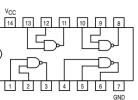
# Diverse Grundgatter

## SN74LS00N



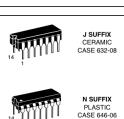
### QUAD 2-INPUT NAND GATE

• ESD > 3500 Vols



### SN54/74LS00

#### QUAD 2-INPUT NAND GATE LOW POWER SCHOTTKY



#### ORDERING INFORMATION

SN40LS00J Ceramic

SN74LS00J Plastic

SN74LS00DO SOIC

#### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	54	4.5	5.5	V
		74	4.75	5.0	
				5.25	
$T_A$	Operating Ambient Temperature Range	54	-55	25	°C
		74	0	25	
				70	
$I_{OH}$	Output Current — High	54, 74		-0.4	mA
$I_{OL}$	Output Current — Low	54		4.0	mA
		74		8.0	

FAST AND LS TTL DATA

## DM74LS32N



### 54LS32/DM54LS32/DM74LS32 Quad 2-Input OR Gates

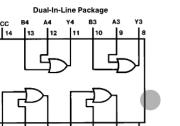
#### General Description

This device contains four independent gates each of which performs the logic OR function.

#### Features

■ Alternate Military/Aerospace device (54LS32) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

#### Connection Diagram



May 1989

Order Number: DM74LS32N  
DM54LS32J, DM74LS32W, DM74LS33M or DM74LS33N  
See NS Package Number E20A, J14A, M14A, N14A or W14B

#### Function Table

Y = A + B		
Inputs	Output	
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level  
L = Low Logic Level

## DM74LS14N



### DM74LS14 Hex Inverter with Schmitt Trigger Inputs

#### General Description

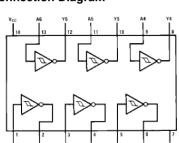
This device contains six independent inverter gates each of which performs the logic NOT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

#### Ordering Code:

Order Number	Package Number	Package Description
DM74LS14M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS14S	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

August 1986  
Revised March 2000

#### Connection Diagram



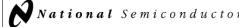
Device also available in Tape and Reel. Specify by appending the suffix letter "T" to the ordering code.

#### Function Table

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level  
L = LOW Logic Level

## DM74LS08N



### 54LS08/DM54LS08/DM74LS08 Quad 2-Input AND Gates

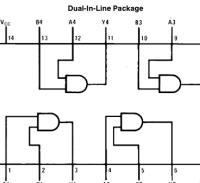
#### General Description

This device contains four independent gates each of which performs the logic AND function.

#### Features

This device contains four independent gates each of which performs the logic AND function.

#### Connection Diagram



June 1989

Order Number 54LS08DM08, 54LS08FM08, 54LS08LMB, DM54LS08J, DM54LS08W, DM74LS08W or DM74LS08N  
See NS Package Number E20A, J14A, M14A, N14A or W14B

#### Function Table

Y = AB		
Inputs	Output	
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level  
L = Low Logic Level

# 4.1) Wahrheit

	$Q_C$	$Q_B$	$Q_A$	$D$	$C$	$B$	$A$
0	0	0	0	0	1	1	1
1	0	0	1	1	1	0	1
2	0	1	0	0	1	0	1
3	0	1	1	1	0	0	1
4	1	0	0	0	0	0	1
5	1	0	1	1	0	0	0
6	1	1	0	X	X	X	X Reset

Würfel
1
2
3
4
5
6 Reset

# Minimierung & Logik

D)

		$a$			
		0	1	1	0
		$\sqrt{0}$	$\sqrt{1}$	$\sqrt{5}$	$\sqrt{9}$
b	0	0	1	$\times$	$\times$
	1	$\sqrt{2}$	$\sqrt{3}$	$\sqrt{7}$	$\sqrt{6}$

$$D = a$$

c

c)

		$a$			
		1	1	0	0
		$\sqrt{0}$	$\sqrt{1}$	$\sqrt{5}$	$\sqrt{9}$
b	0	1	$\sqrt{2}$	$\times$	$\times$
	1	$\sqrt{0}$	$\sqrt{3}$	$\sqrt{7}$	$\sqrt{6}$

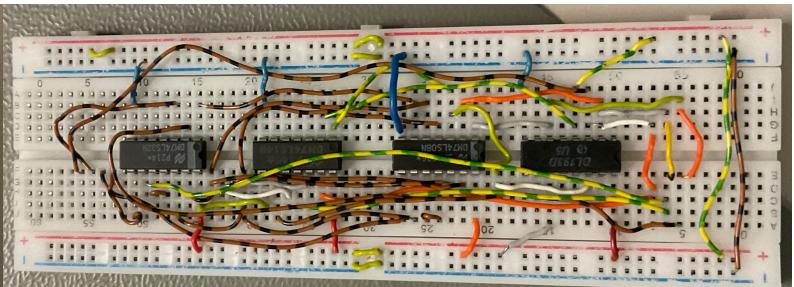
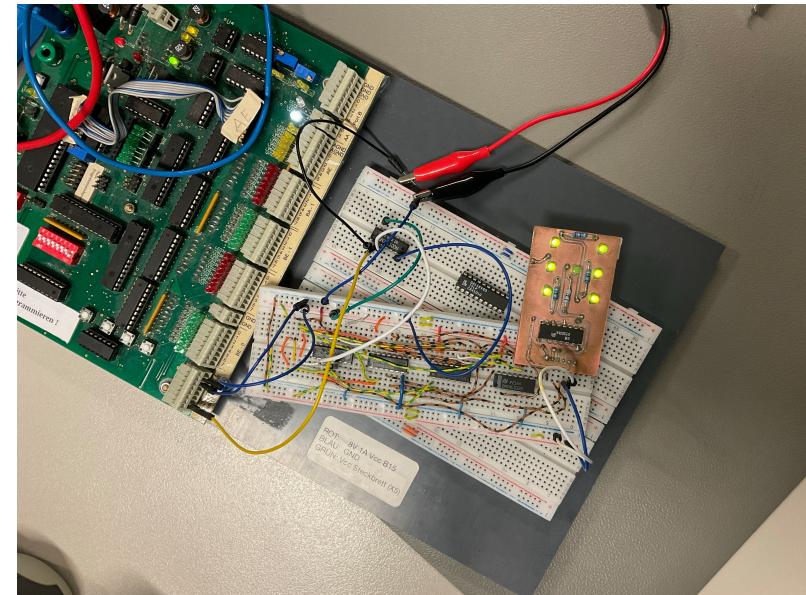
$$C = (\bar{b} \bar{c}) \vee (\bar{a} \bar{c})$$

b)

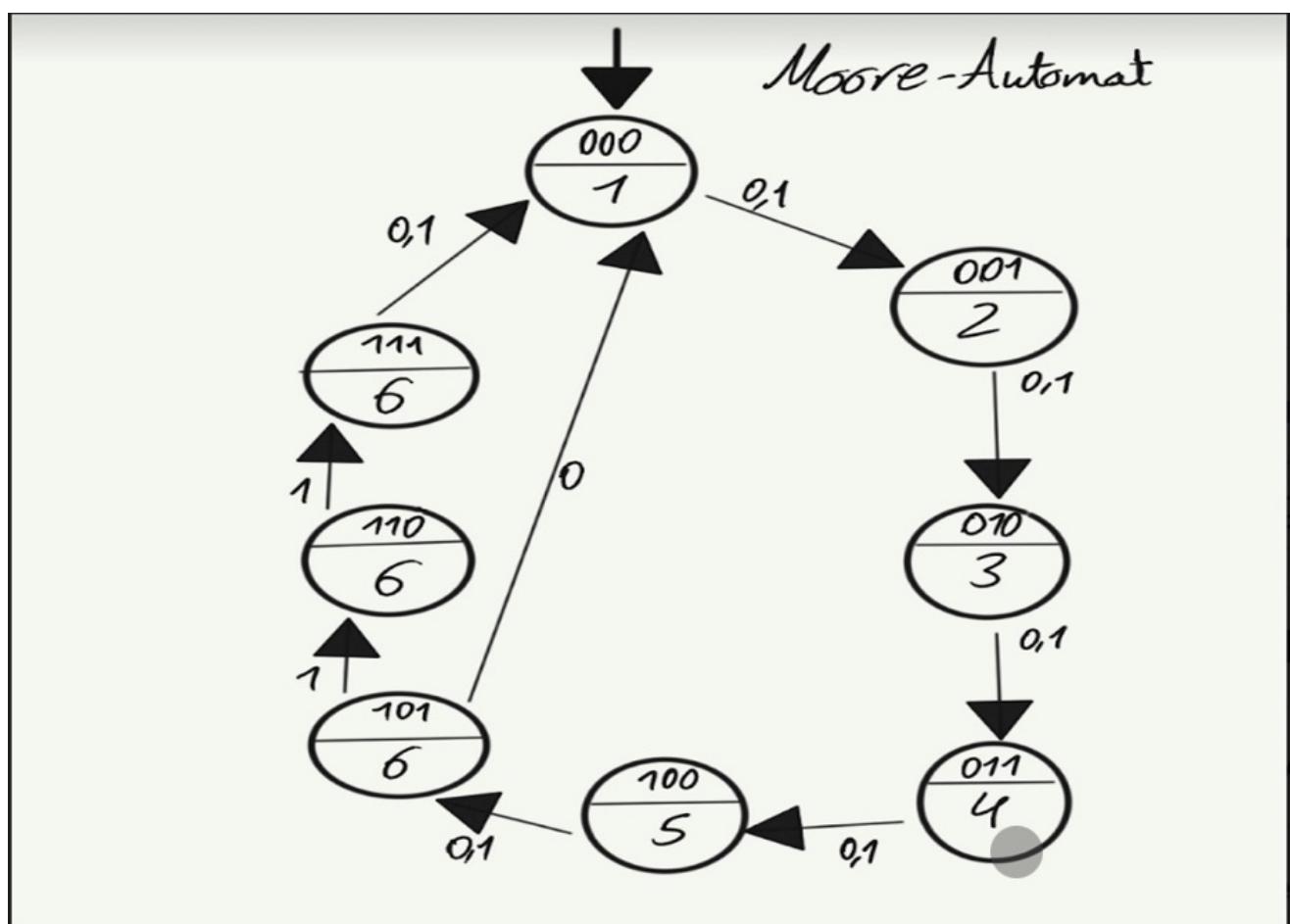
		$a$			
		1	0	0	0
		$\sqrt{0}$	$\sqrt{1}$	$\sqrt{5}$	$\sqrt{9}$
b	0	0	$\sqrt{3}$	$\times$	$\times$
	1	$\sqrt{2}$	$\sqrt{3}$	$\sqrt{7}$	$\sqrt{6}$

c

$$b = \bar{a} \bar{b} \bar{c}$$



## 5.1) Automat



# 3 Bits Zähler

Die Zustände {000, 001....111} werden mit Hilfe von 3 Flip-Flops gemacht.

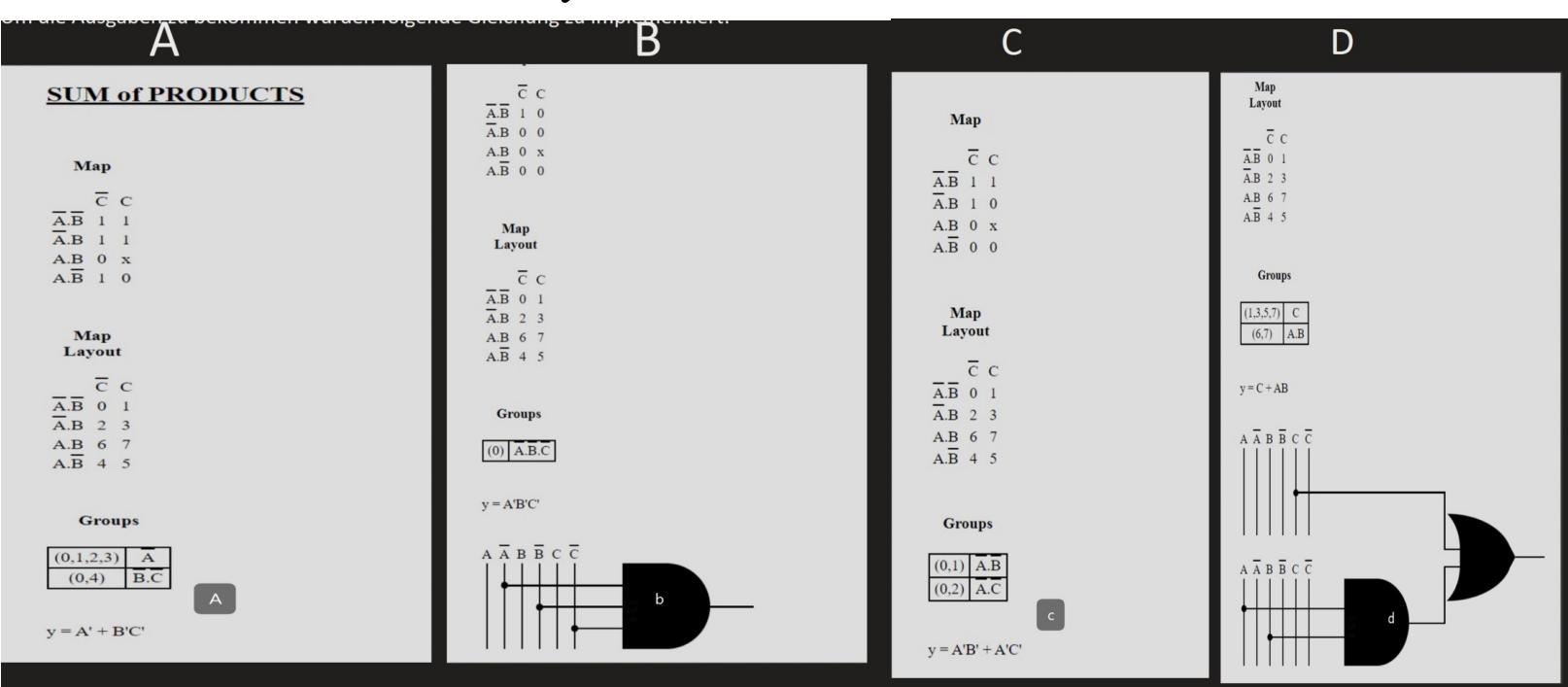
/\*8Bit Zaehler Fuer die Zustände\*/

- PIN 12 = q0 ;//qc
- PIN 13 = q1 ;//qb
- PIN 14 = q2 ;//qa
- PIN 19 = res; // Fue Beschränkung und umschalten auf anderen Zustand (mehrere 6en)
- res.d = (q2 & ! q1 & ! q0 & ! x); // Beschränk die Anzahl der Zustände auf 6 wenn die Eingabe x nicht aktiv
- q0.d = ! res & ( ! q0); //
- q1.d = ! res & ( q1 \$ q0); // \$=XOR
- q2.d = ! res & (q2 \$(q1 & q0));//

Und somit haben wir die 8 Zuständen.

Um die Ausgaben zu bekommen wurden folgende Gleichung zu implementiert:

## Minimierung / Automaten Gleichung



Im Programm sehen sie so aus:

```
/*Gatter fuer die Ausgaben */
PIN 15 = a ; //A Wuefel
PIN 16 = b ; //B Wuefel
PIN 17 = c ; //C Wuefel
PIN 18 = d ; //D Wuefel

a.d = (! q2 # ( ! q1 & ! q0)); //Gleichung fuer A
b.d = (! q2 & ! q1 & ! q0) ; //Gleichung fuer B
c.d = ((! q2 & ! q1) # (!q2 & !q0)); //Gleichung fuer C
d.d = (q0 # (q2 & q1)); //Gleichung fuer D
```

