

Computer Architecture , project B

Title: Car Parking System

Section: 4C2

Group number: 2

| No. | Name | Academic No. | Academic email | Work |
|-----|-----------------|--------------|----------------|-----------|
| 1 | نورة علي القاسم | | 442@pnu.edu.sa | Team work |

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The project aim:

We want to create a private parking that allows certain people to enter through the gate which has an entrance sensor that is activated by cars approaching the gate, the gate will ask for a password, afterwards if the LED light turns green it indicates that the password was entered correctly so the gate will open. However if the LED light turns red it refers to that the password was entered incorrectly so the gate will refuse to open. After the car enters the exit sensor will detect it and the gate will be locked, At the end the password monitor will reset to its main screen for the next car.

The input:

LockSignal, ResetSignal, EntranceSensor, ExitSensor and Password

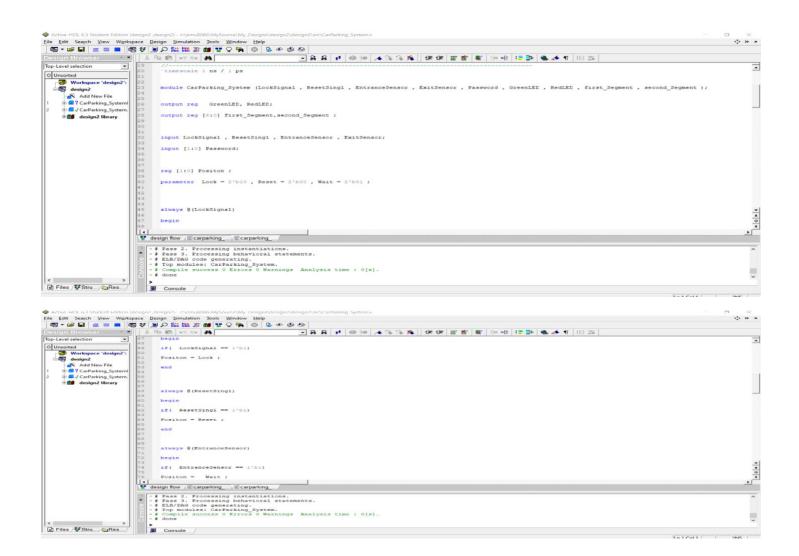
The output:

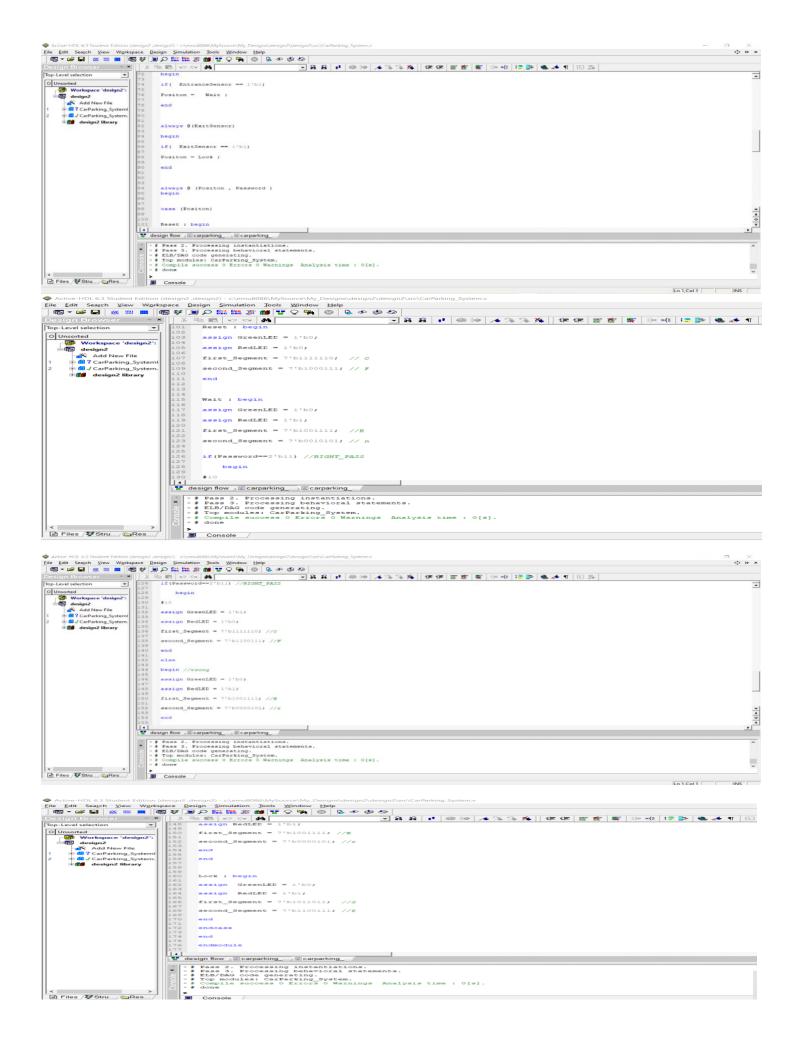
first_Segment,second_Segment, RedLED and GreenLED

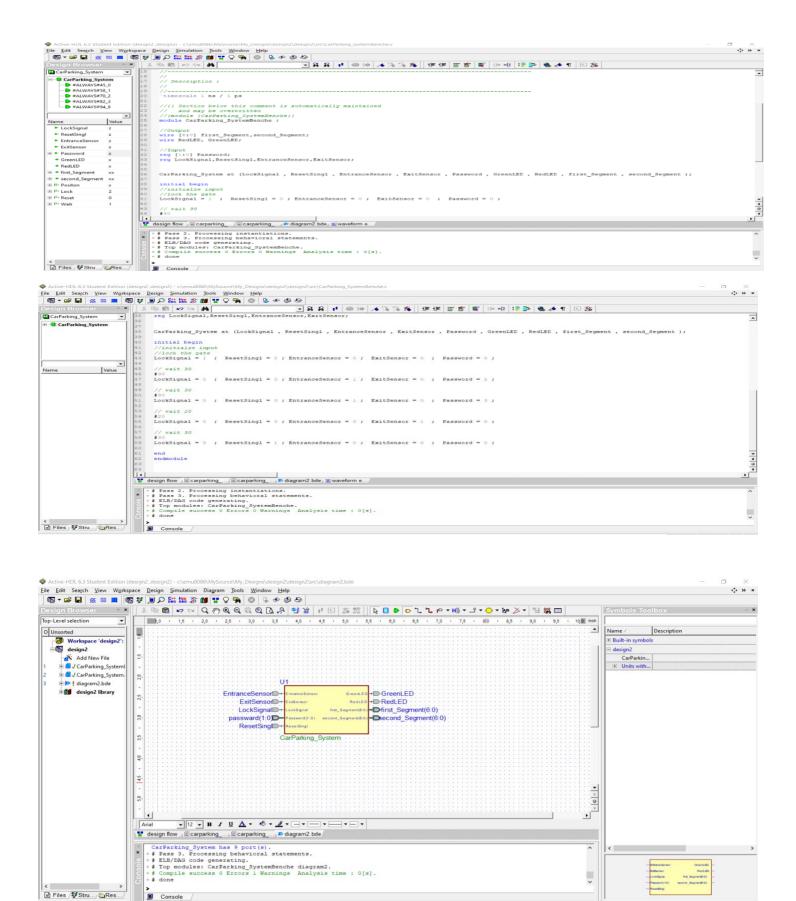
The problem solution:

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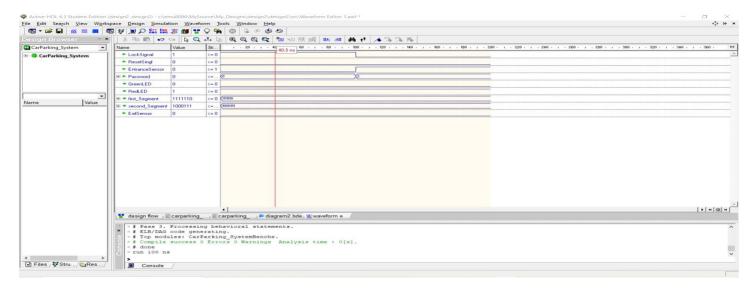
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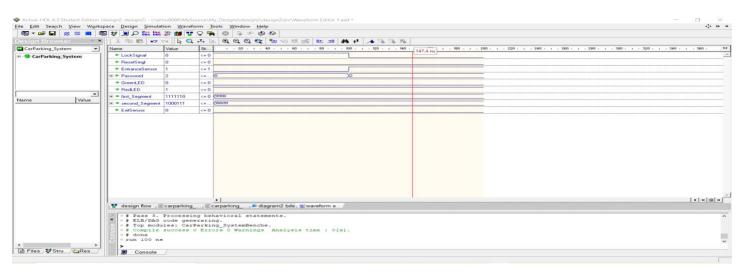


The first scenario:



When the Lock_Signal equals one then the GreenLED will equal zero and the RedLED will equal one and the first segment will equal 1111110 and the second segment will equal 1000111

The second scenario:



When the Lock_Signal equals zero then the GreenLED will equal zero and the RedLED will equal one and the first segment will equal 1111110 and the second segment will equal 1000111

Solution code:

begin

```
// group number :2 , 4C2 , maram almousa 442000723@pnu.edu.sa , wateen alzamel 442000928@pnu.edu.sa ,noura ali alqasem
442001119@pnu.edu.sa
//, taif alsadoon 442000762@pnu.edu.sa ,jomanh almanaa 442004948@pnu.edu.sa, mzoon alrubaish 442007363@pnu.edu.sa
module CarParking_System (LockSignal, ResetSingl, EntranceSensor, ExitSensor, Password, GreenLED, RedLED, first_Segment,
second_Segment);
output reg GreenLED, RedLED;
output reg [6:0] first_Segment,second_Segment;
input LockSignal, ResetSingl, EntranceSensor, ExitSensor;
input [1:0] Password;
reg [1:0] Positon;
parameter Lock = 2'b10, Reset = 2'b00, Wait = 2'b01;
always @(LockSignal)
begin
if( LockSignal == 1'b1)
Positon = Lock;
end
always @(ResetSingl)
begin
if( ResetSingl == 1'b1)
Positon = Reset;
end
always @(EntranceSensor)
begin
if( EntranceSensor == 1'b1)
Positon = Wait;
end
always @(ExitSensor)
begin
if( ExitSensor == 1'b1)
Positon = Lock;
end
always @ (Positon, Password)
```

```
case (Positon)
Reset: begin
assign GreenLED = 1'b0;
assign RedLED = 1'b0;
first_Segment = 7'b1111110; // O
second_Segment = 7'b1000111; // F
end
Wait: begin
assign GreenLED = 1'b0;
assign RedLED = 1'b1;
first_Segment = 7'b1001111; //E
second_Segment = 7'b0010101; // n
if(Password==2'b11) //RIGHT_PASS
                                         begin
                                                    #10
assign GreenLED = 1'b1;
assign RedLED = 1'b0;
first_Segment = 7'b1111110; //O
second_Segment = 7'b1100111; //F
end
else
begin //wrong
assign GreenLED = 1'b0;
assign RedLED = 1'b1;
first_Segment = 7'b1001111;
                                 //E
second_Segment = 7'b0000101; //r
end
end
Lock : begin
assign GreenLED = 1'b0;
assign RedLED = 1'b1;
first_Segment = 7'b1011011;
                                 //S
second_Segment = 7'b1100111; //P
end
endcase
               end
endmodule
```

the testbenches code:

```
module CarParking_SystemBenche
//Output
wire [6:0] first_Segment, second_Segment;
wire RedLED, GreenLED;
//Input
reg [1:0] Password;
reg LockSignal,ResetSingl,EntranceSensor,ExitSensor;
CarParking_System at (LockSignal, ResetSingl, EntranceSensor, ExitSensor, Password, GreenLED, RedLED, first_Segment,
second_Segment);
initial begin
//initialze input
//lock the gate
LockSignal = 1; ResetSingl = 0; EntranceSensor = 0; ExitSensor = 0; Password = 0;
// wait 30
#30
LockSignal = 0; ResetSingl = 0; EntranceSensor = 1; ExitSensor = 0; Password = 2;
// wait 30
#30
LockSignal = 0; ResetSingl = 0; EntranceSensor = 1; ExitSensor = 0; Password = 3;
// wait 20
#20
LockSignal = 0; ResetSingl = 0; EntranceSensor = 0; ExitSensor = 1; Password = 0;
// wait 30
#30
LockSignal = 0; ResetSingl = 1; EntranceSensor = 0; ExitSensor = 0; Password = 0;
end
endmodule
```

References:

The fifth edition of computer organization and design

Computer Organization and Architecture

https://verificationguide.com/systemverilog/systemverilog-program-block/