Tutorial 3

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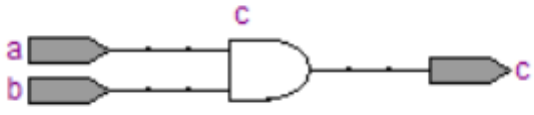
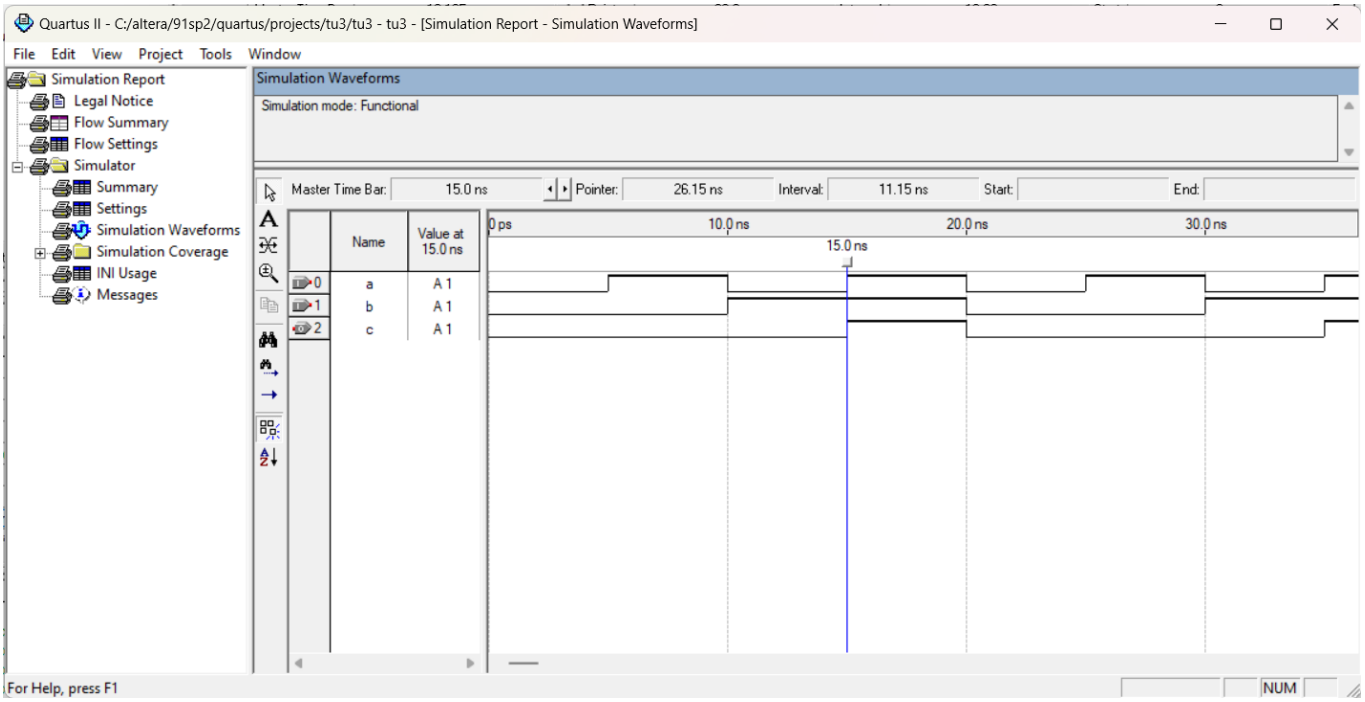
AND gate

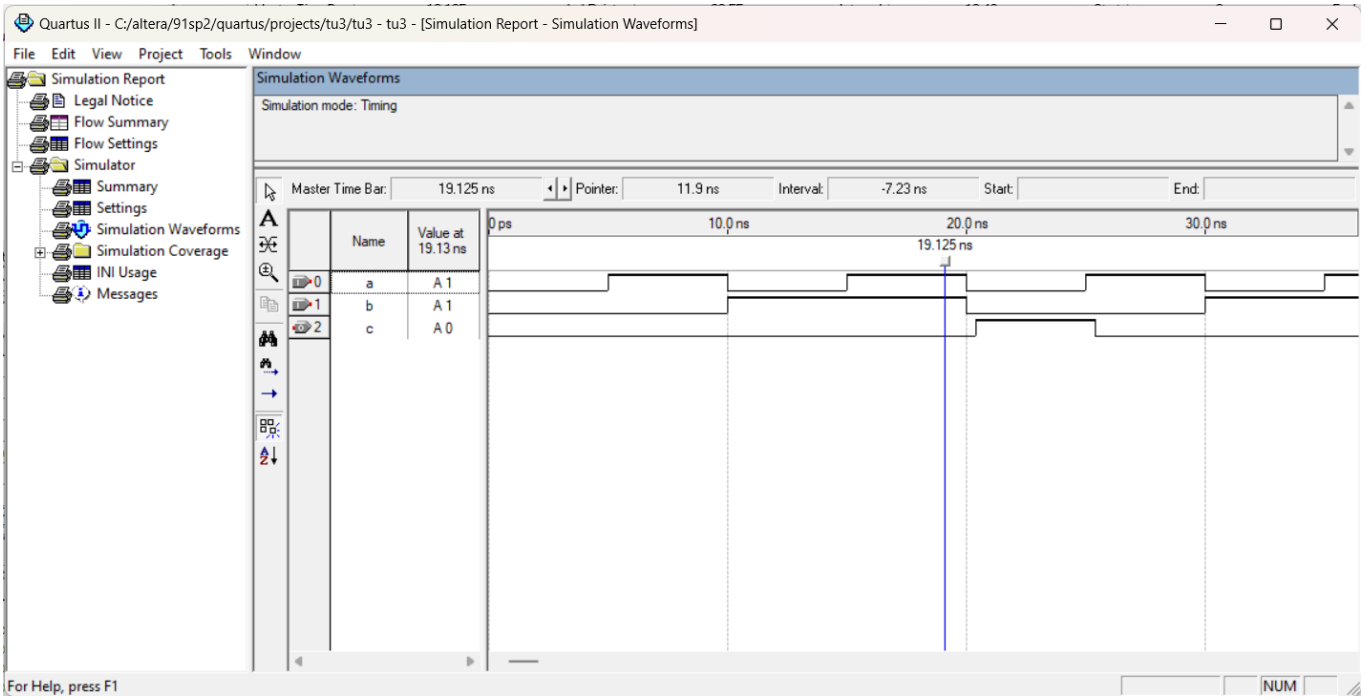
```
library ieee;
use ieee.std_logic_1164.all;

entity tu3 is
port(
          a,b : in std_logic;
          c : out std_logic
          );

end tu3;

architecture behave of tu3 is

begin

c <= a and b;

end behave;
```



simulation mood: functional



simulation mood: timing



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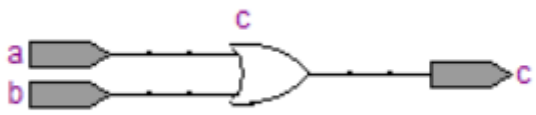
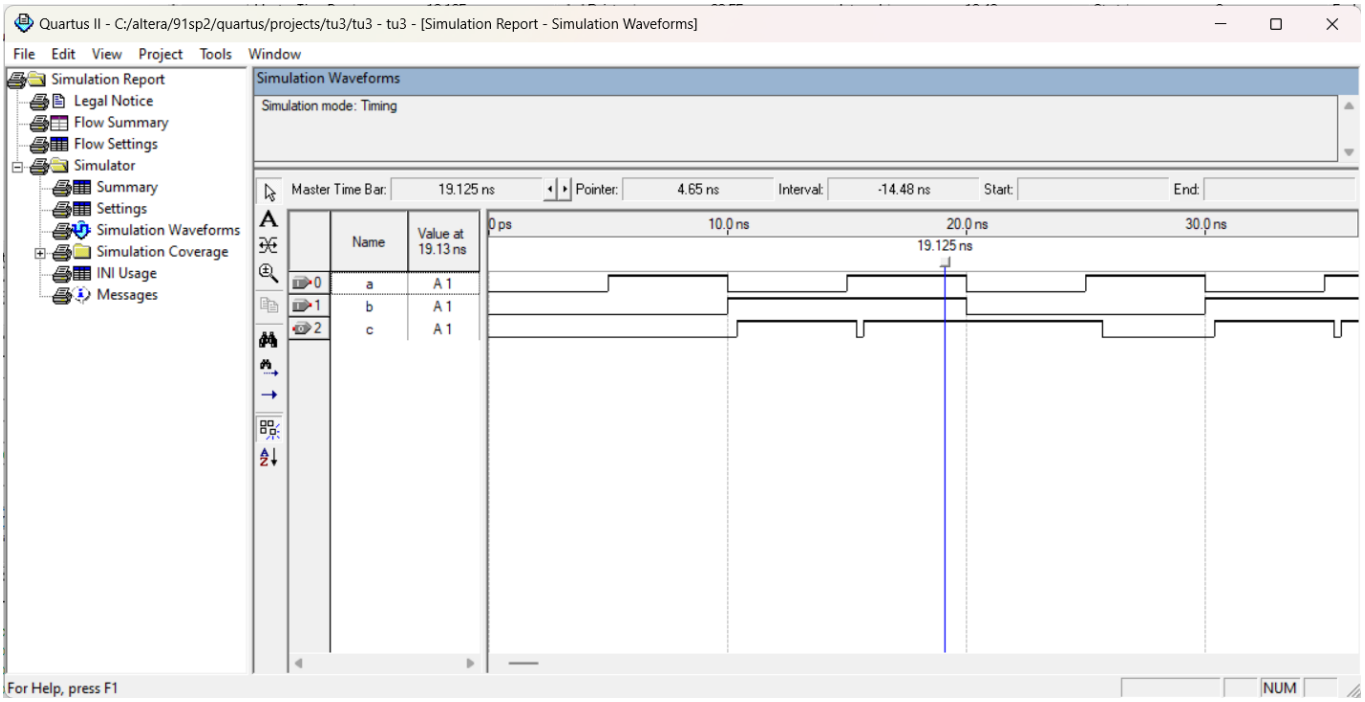
OR gate

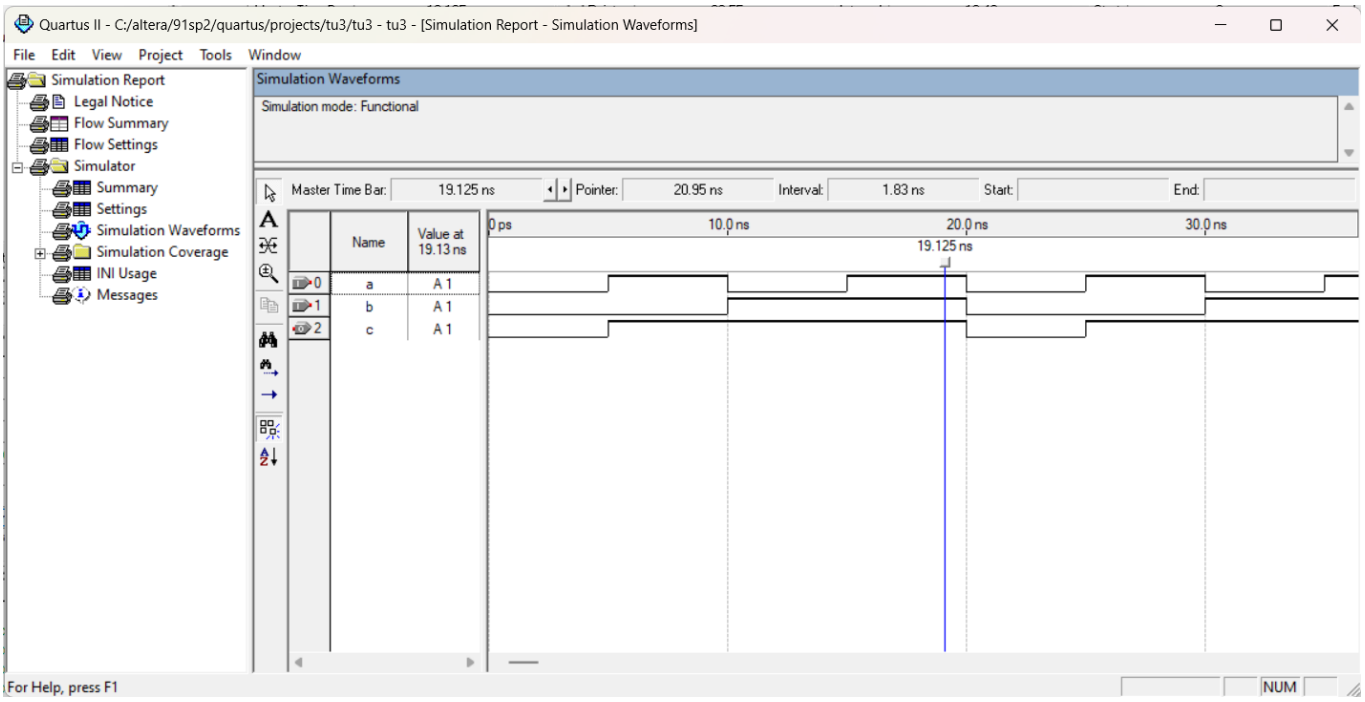
```
library ieee;
use ieee.std_logic_1164.all;

entity tu3 is
port(
          a,b : in std_logic;
          c : out std_logic
          );

end tu3;

architecture behave of tu3 is

begin

c <= a or b;

end behave;
```



simulation mood: timing



simulation mood: functional



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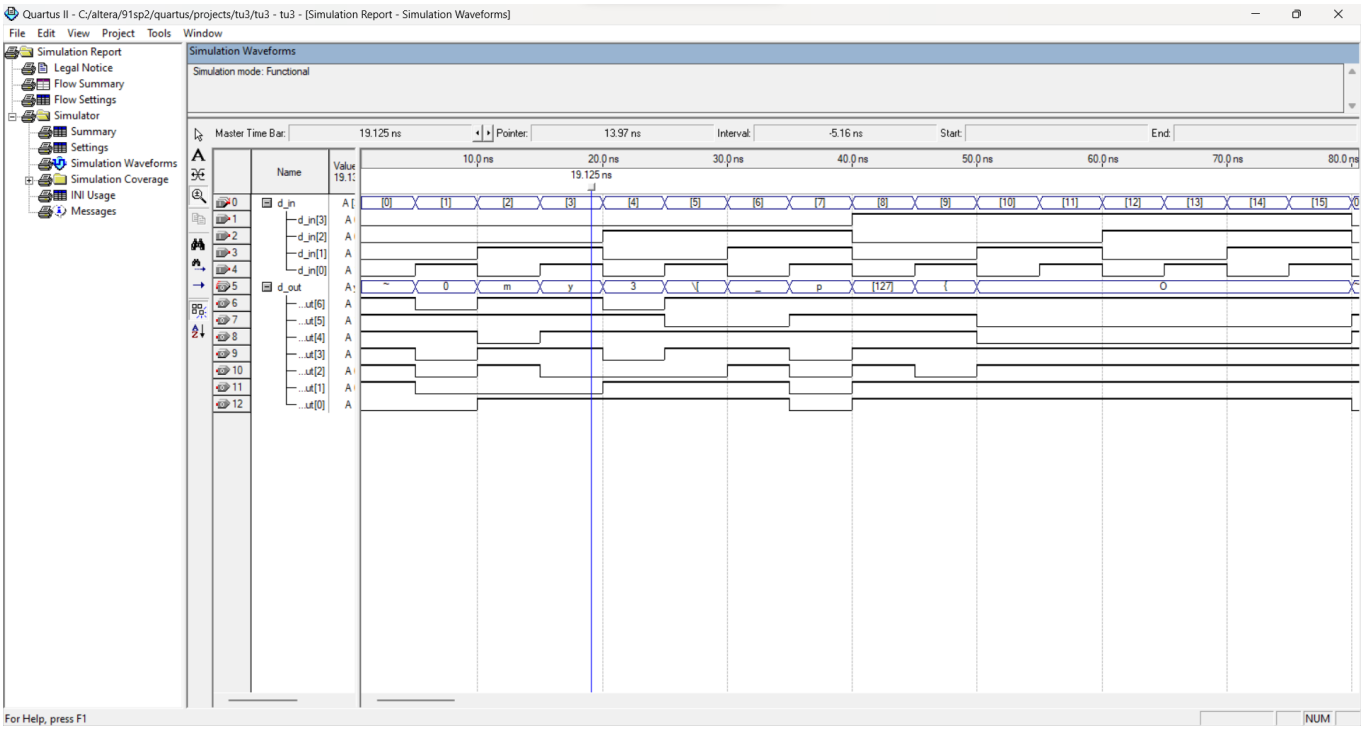
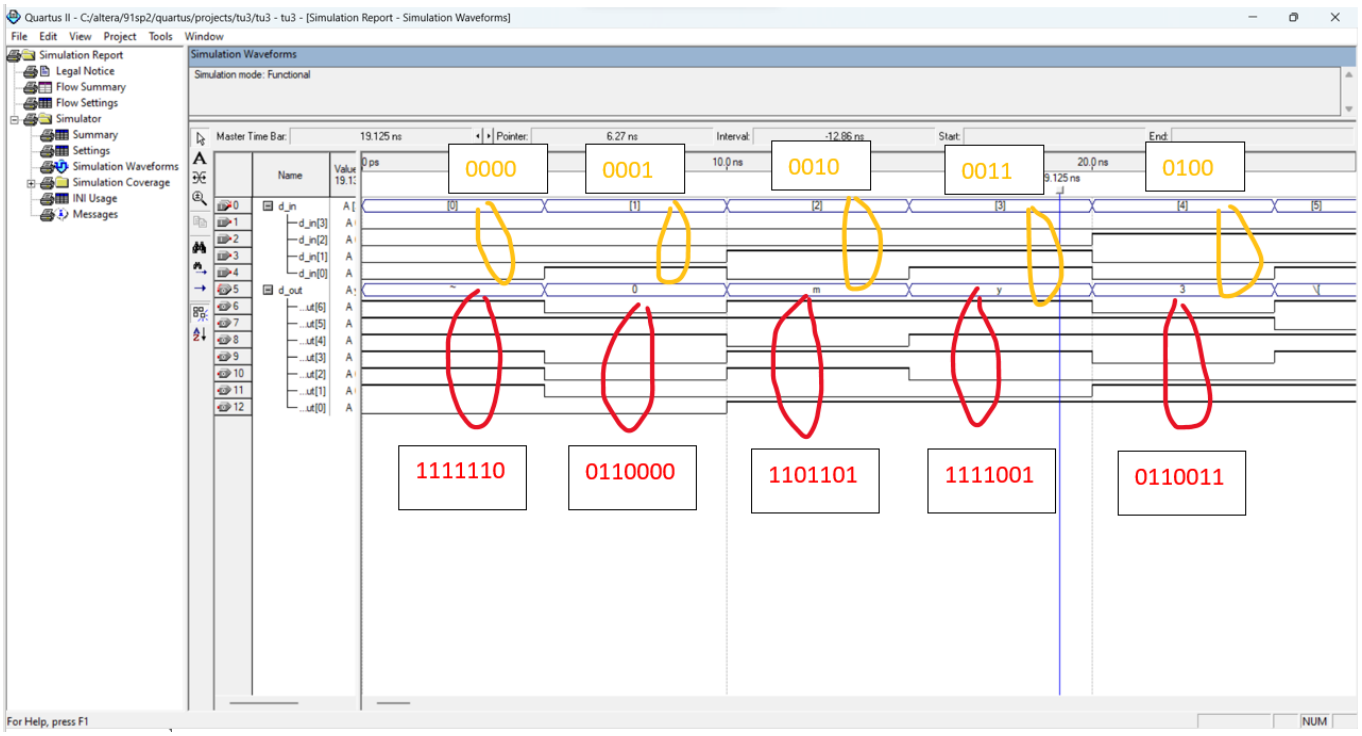
7 segment

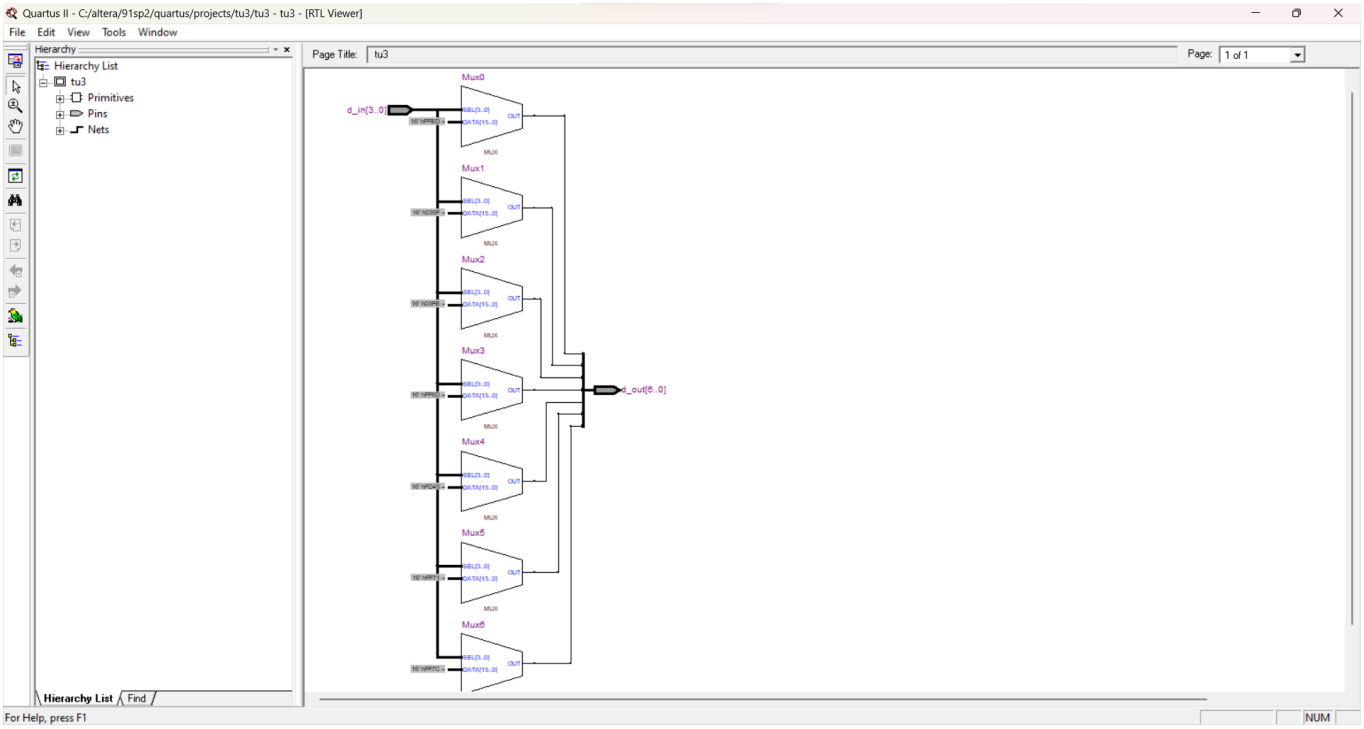
```
library ieee;
use ieee.std_logic_1164.all;
entity tu3 is
port(
        d_in : in std_logic_vector(3 downto 0);
        d_out : out std_logic_vector(6 downto 0) );
        end tu3;

architecture behave of tu3 is
begin
        process (d_in)
        begin
                case d_in is
                        when "0000" => --0
                                d_out <= "1111110";
                        when "0001" => --1
                                d_out <= "0110000";
                        when "0010" => --2
                                d_out <= "1101101";
                        when "0011" => --3
                                d_out <= "1111001";
                        when "0100" => --4
                                d_out <= "0110011";
                        when "0101" => --5
                                d_out <= "1011011";
                        when "0110" => --6
                                d_out <= "1011111";
                        when "0111" => --7
                                d_out <= "1110000";
                        when "1000" => --8
                                d_out <= "1111111";
                        when "1001" => --9
                                d_out <= "1111011";
                        when others =>
                                d_out <= "1001111";
                end case;
        end process;
end behave;
```

simulation mood: functional





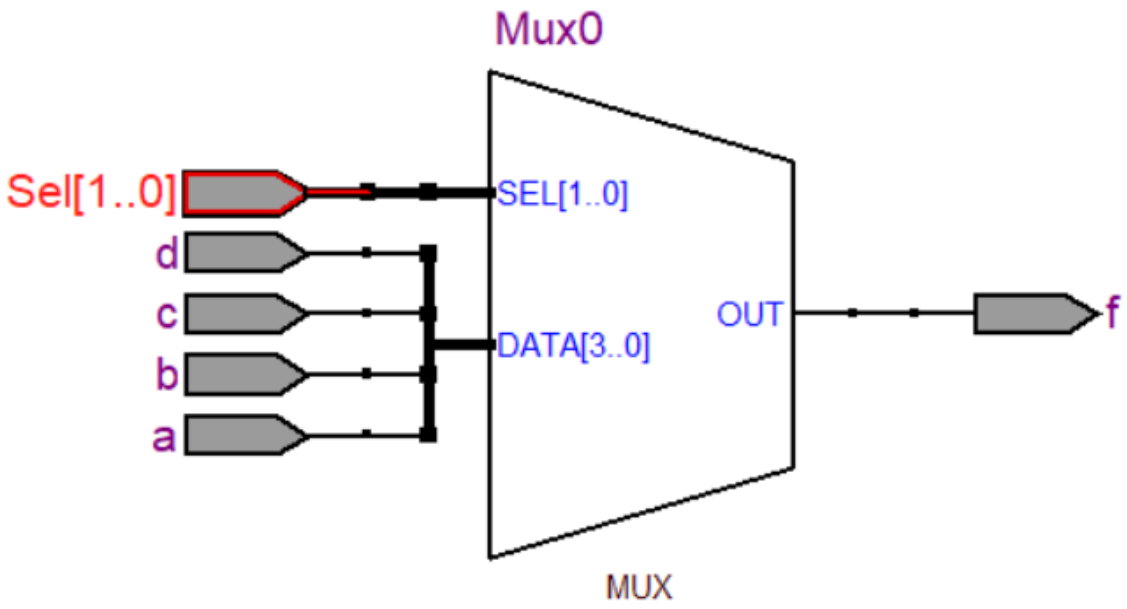

Quartus II - C:/altera/91sp2/quartus/projects/tu3/tu3 - tu3 - [RTL Viewer]
File Edit View Tools Window
Hierarchy
Hierarchy List
tu3
Primitives
Pins
Nets
Page Title: tu3
Page: 1 of 1
Mux0
Mux1
Mux2
Mux3
Mux4
Mux5
Mux6
d_in[3..0]
d_out[6..0]
MUX
Hierarchy List
Find
For Help, press F1
NUM

MUX

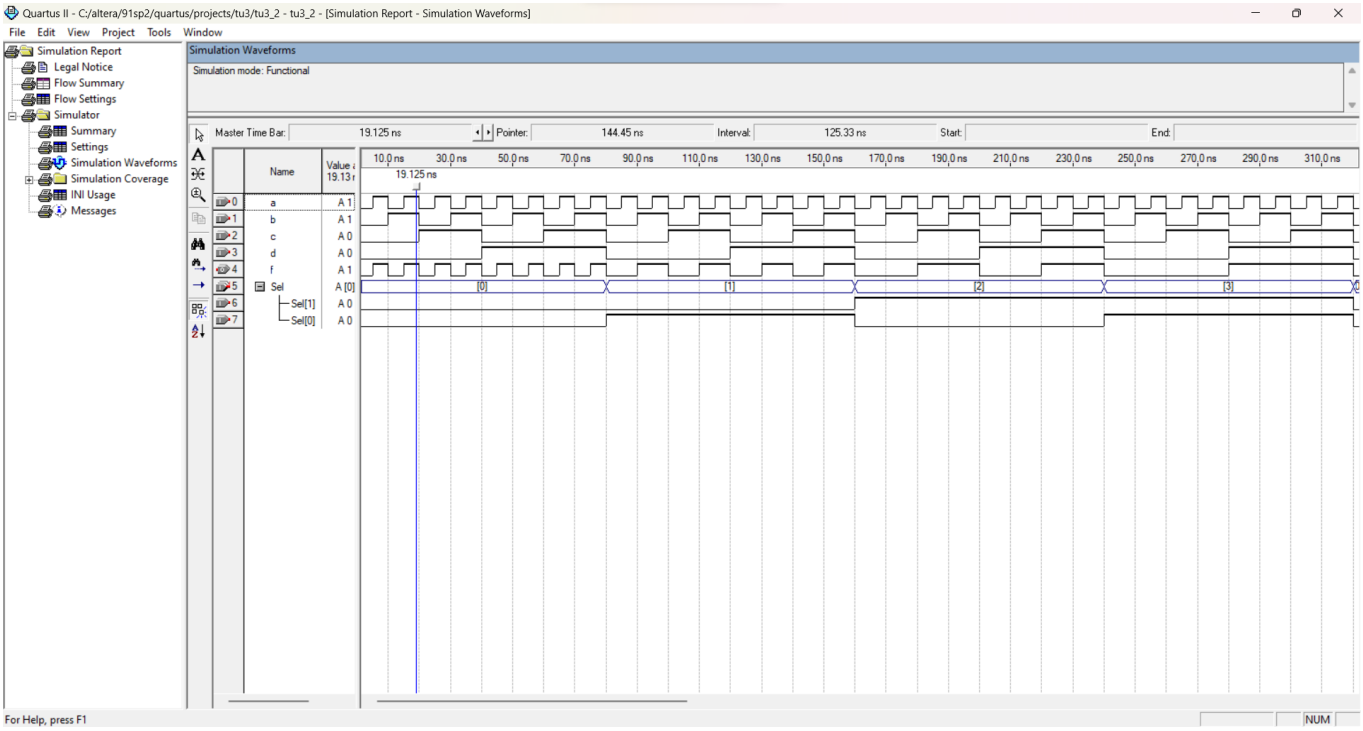
```
library ieee;
use ieee.std_logic_1164.all;

ENTITY tu3_2 IS
        port(
                        a, b,c,d : in std_logic;
                        Sel: in std_logic_vector (1 downto 0);
                        f : out std_logic);
END ENTITY;

ARCHITECTURE behave OF tu3_2 IS
BEGIN
process (a, b,c,d,sel)
begin
        Case sel is
                When "00" =>
                f <= a;
                When "01" =>
                f <= b;
                When "10" =>
                f <= c;
                When "11" =>
                f <= d;
        End case;
End process;
End architecture;
```



simulation mood: functional



the output **F** depends on the selection line:
when the selection lines values were both zeros **"00"**
the output was same as the input **A**.
and the values **"01"** gives the output same as **B**.
"10" gives **C**.
"11" gives **D**.