Tutorial 1

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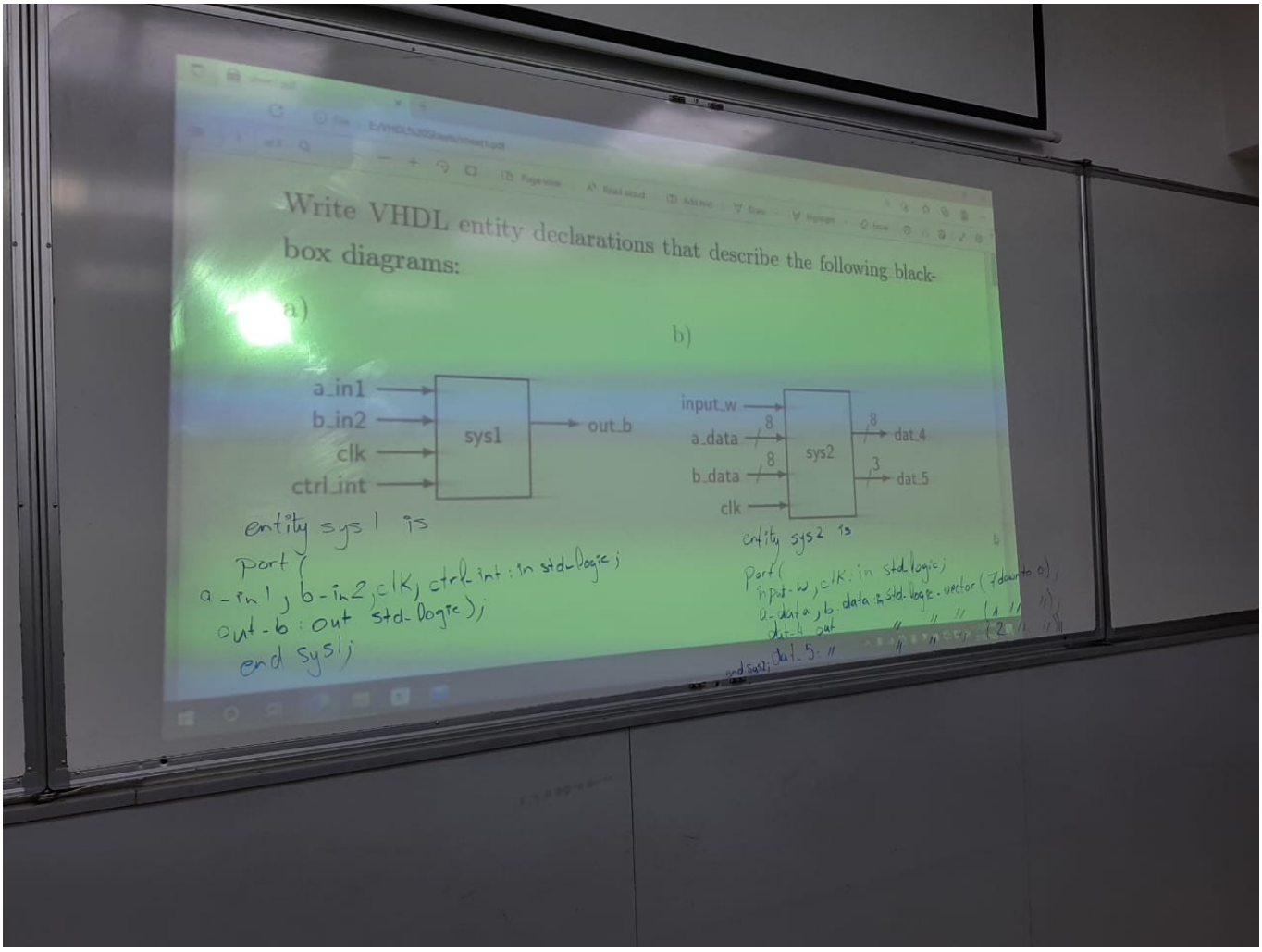
Q1)



a)

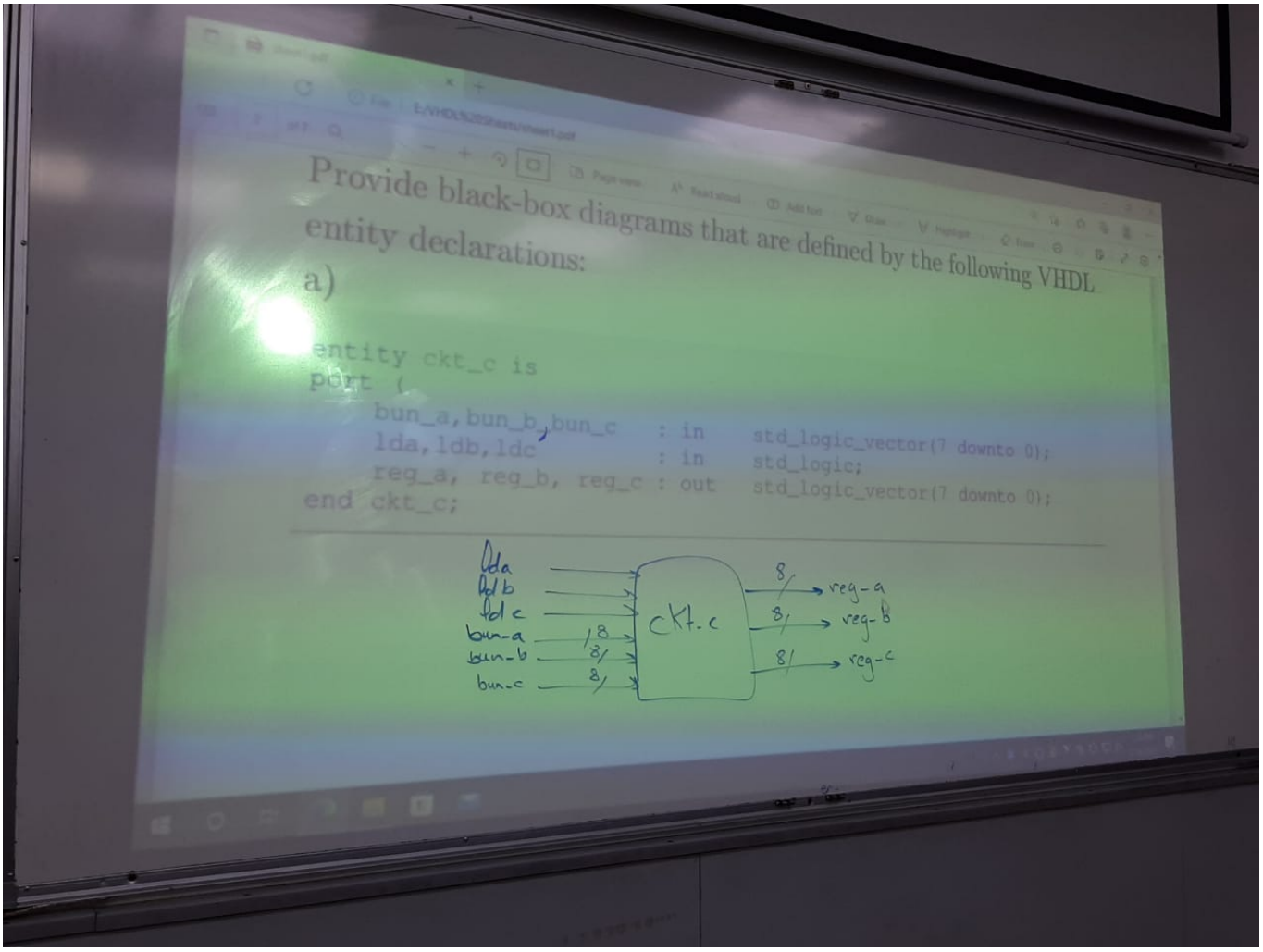
```
entity sys1 is
port(
a_in1, b_in2, clk, ctrl_int: in std_logic;
out_b: out std_logic
);
end sys1;
```

b)

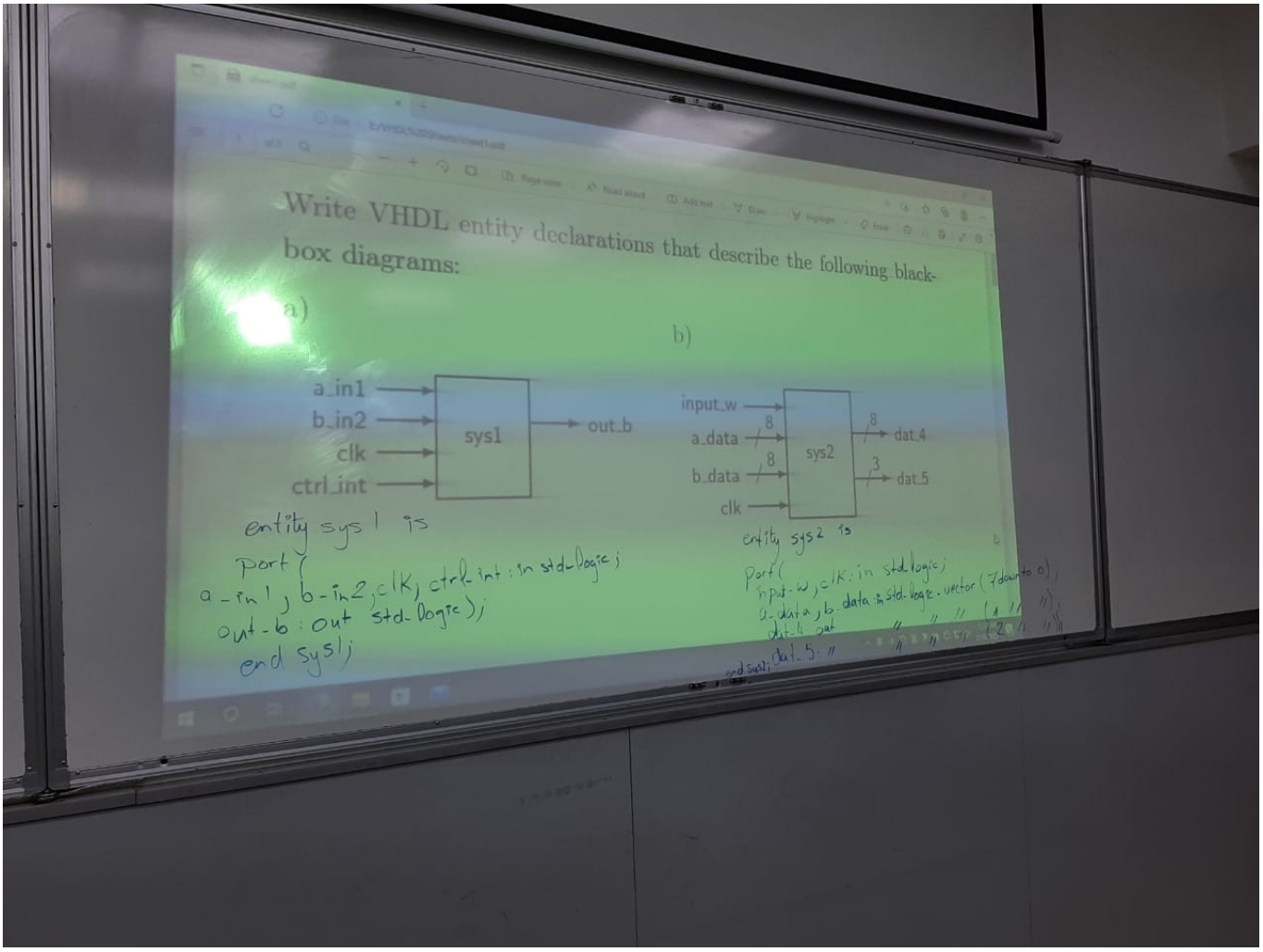
```
entity sys2 is
port(
input_w, clk: in std_logic;
a_data, b_data: in std_logic_vector(7 downto 0);
dat_4: out std_logic_vector(7 downto 0);
dat_5: out std_logic_vector(2 downto 0)
);
end sys2;
```

Q2)

a)



Q3)



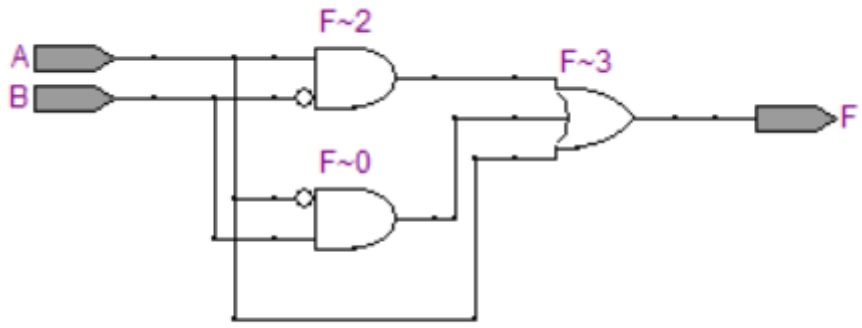
Q4)

a) F(A,B)= !A B + A + A !B

```
Library IEEE;
use ieee.std_logic_1164.all;


entity tutorial1 is
port(
A,B: in std_logic;
F: out Std_logic
);
end tutorial1;
```

```
architecture behave of tutorial1 is
begin
F <= ( (not A) and B) or (A) or (A and (not B) );
end architecture;
```

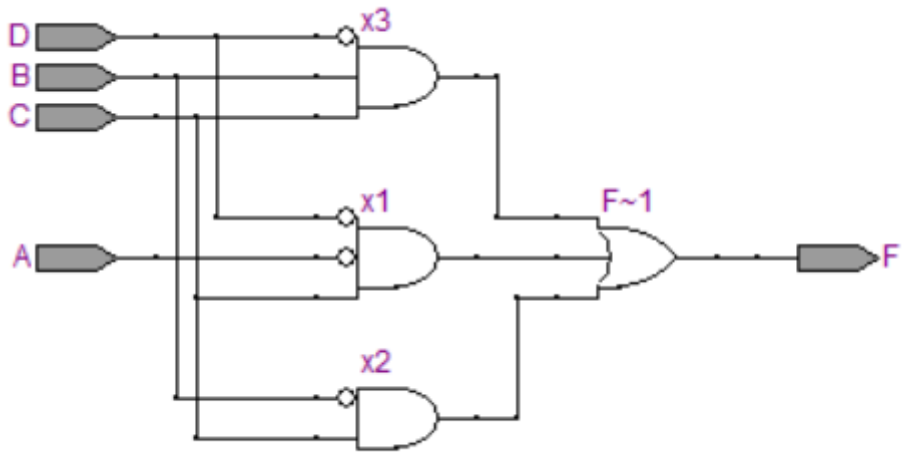


b) F(A,B,C,D)= !A C !D + !B C + B C !D

```
Library IEEE;
use ieee.std_logic_1164.all;


entity tutorial1 is
port(
A,B,C,D: in std_logic;
F: out Std_logic
);
end tutorial1;

architecture behave of tutorial1 is
signal x1, x2, x3: std_logic;
begin
x1 <= (not A) and C and (not D);
x2 <= (not B) and C;
x3 <= B and C and (not D);
F <= ( x1 ) or ( x2 ) or ( x3 );
end architecture;
```

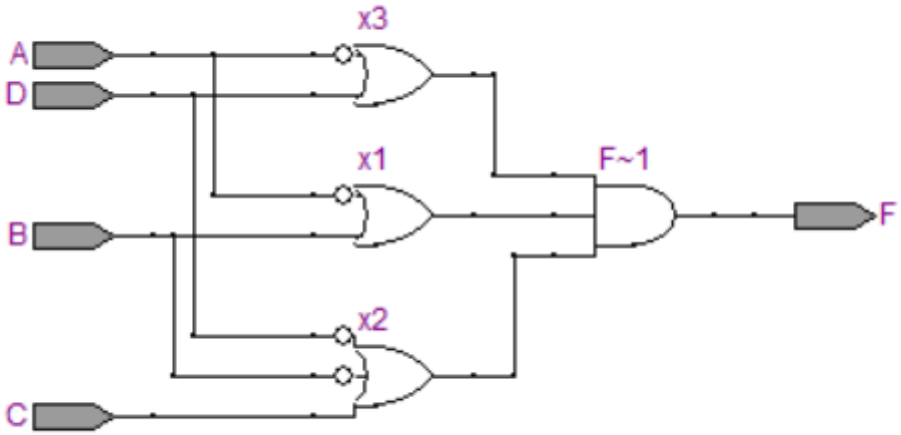


c) F(A,B,C,D)= (!A + B) . (!B + C + !D) . (!A + D)

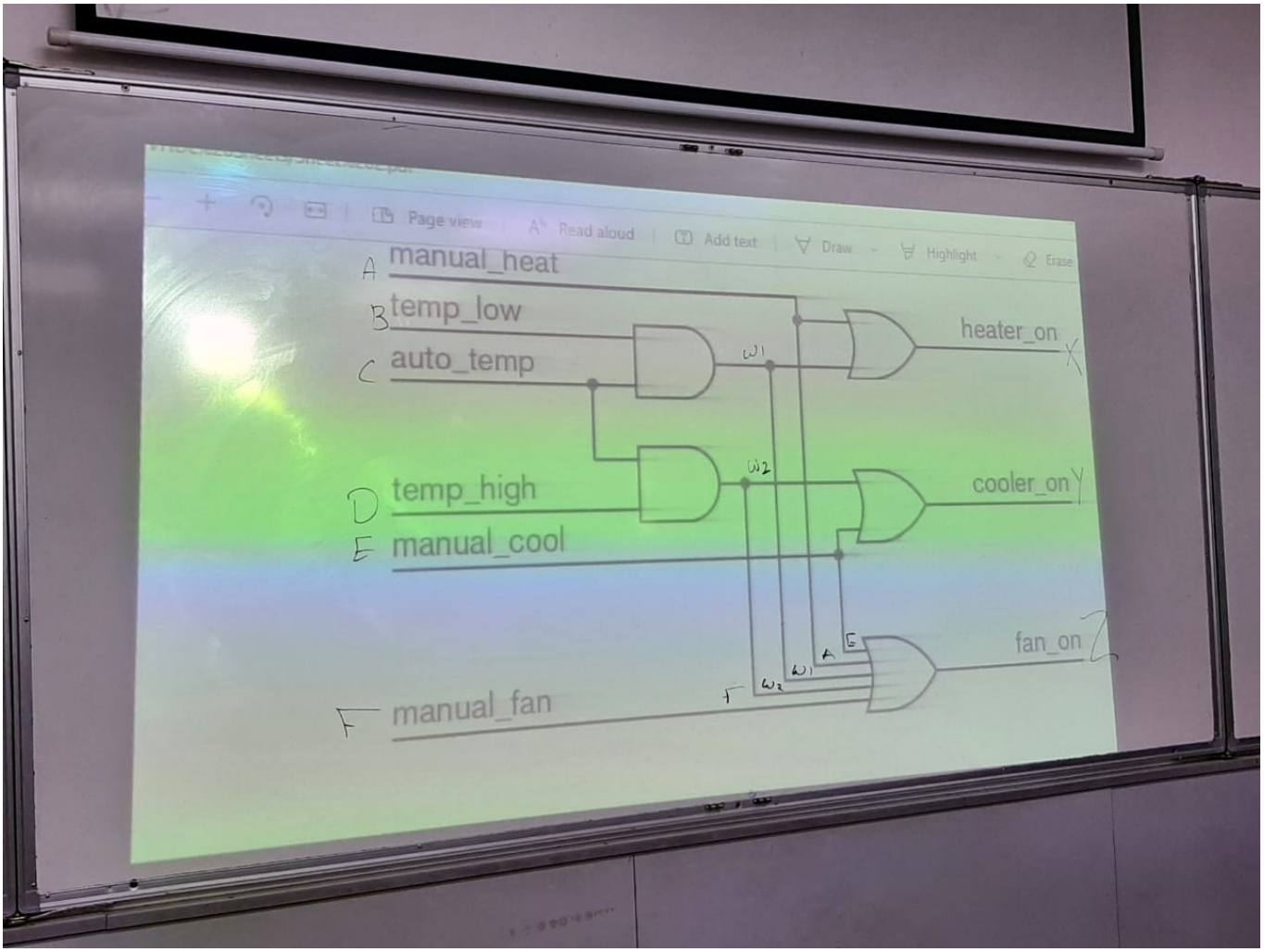
```
Library IEEE;
use ieee.std_logic_1164.all;


entity tutorial1 is
port(
A,B,C,D: in std_logic;
F: out Std_logic
);
end tutorial1;

architecture behave of tutorial1 is
signal x1, x2, x3: std_logic;
begin
x1 <= (not A) or B;
x2 <= (not B) or C or (not D);
x3 <= (not A) or D;
F <= ( x1 ) and ( x2 ) and ( x3 );
end architecture;
```



Q5)




```
Library IEEE;
use ieee.std_logic_1164.all;
```

```
entity tutorial1 is
port(
A,B,C,D,E,F: in std_logic;
X,Y,Z: out Std_logic
);
end tutorial1;

architecture behave of tutorial1 is
signal w1, w2 : std_logic;
begin
w1 <= C and B;
w2 <= C and D;
X <= A or w1 ;
Y <= w2 or E;
Z <= E or A or w1 or w2 or F;
end architecture;
```