# Misr International University
# Electronics and Communication Engineering
# ECE 542 (VLSI Lab)
# Spring 2023

# Lab 1:
# Inverter Gate

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| Name | ID |
|---|---|
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# Contents

# Table of Figures:

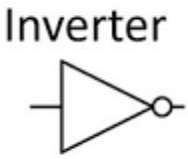
## Aim:

The aim of this report is to present the design process of an inverter gate using the Cadence tool. The design process consists of the following steps:

- Defining the specifications of the inverter gate
- Developing a behavioral model of the inverter gate
- Creating a schematic diagram of the inverter gate
- Testing the functionality and performance of the schematic design
- Designing a layout of the inverter gate
- Testing the layout design for any errors or violations
- Performing a post-layout simulation and verification

## Introduction:

An inverter gate is a basic logic gate that produces an output that is the opposite of its input. For example, if the input is 1, the output is 0, and vice versa. Inverter gates are widely used in digital circuits and systems, such as computers, calculators, and communication devices. In this report, we will describe how we designed an inverter gate using the Cadence tool, which is a software platform for electronic design automation. We will explain the steps we followed to create a schematic diagram, a layout design, and a post-layout simulation of the inverter gate. We will also present the results of our testing and verification of the design, and discuss the challenges and limitations we faced during the design process.




| Input | Output |
|---|---|
| 0 | 1 |
| 1 | 0 |

*Figure 1: Inverter Truth Table*

## Run Cadence

- Launch VMware and access the CentOS virtual machine.

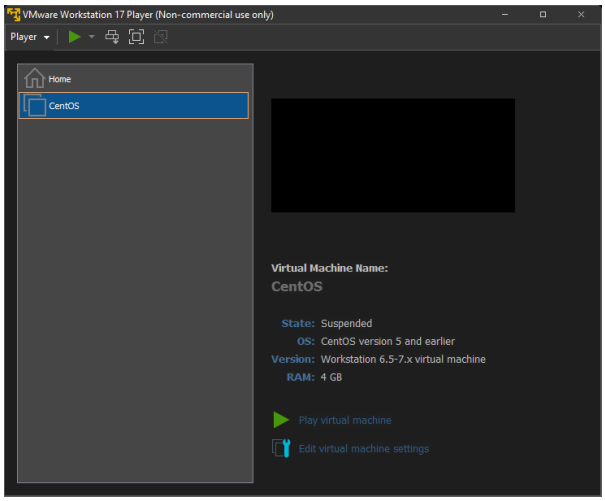



*Figure 2: Run The VMware*

- Log in as root user with the password elc411.

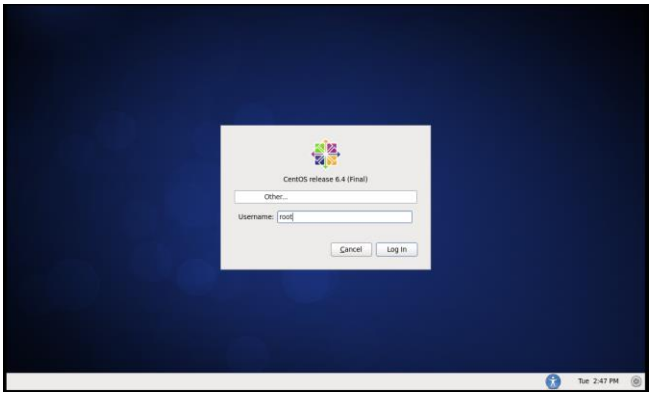



*Figure 3: Log in*

- Open a terminal window and enter “cadence 1”.

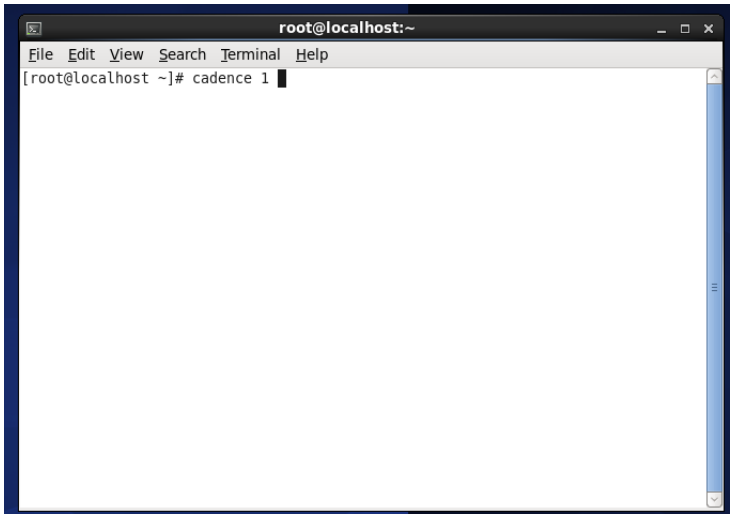



*Figure 4: open Cadence*

- Then enter “virtuoso &” and wait for cadence to open.

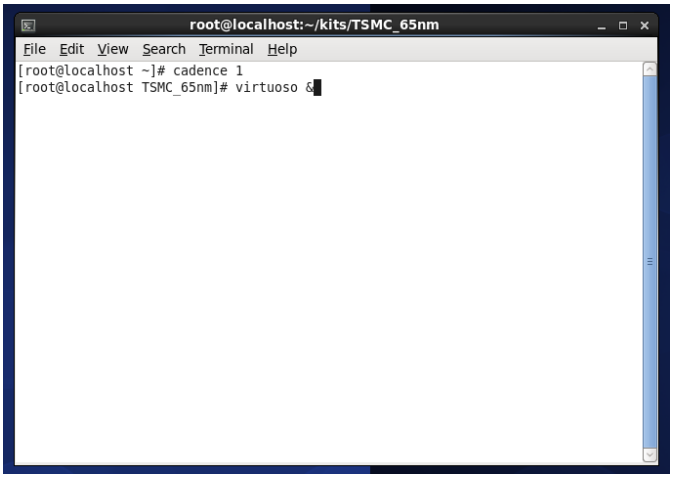



*Figure 5: open virtuoso*

- Make a new library with a name of your choice.
- Make a new cell named “Inverter”.

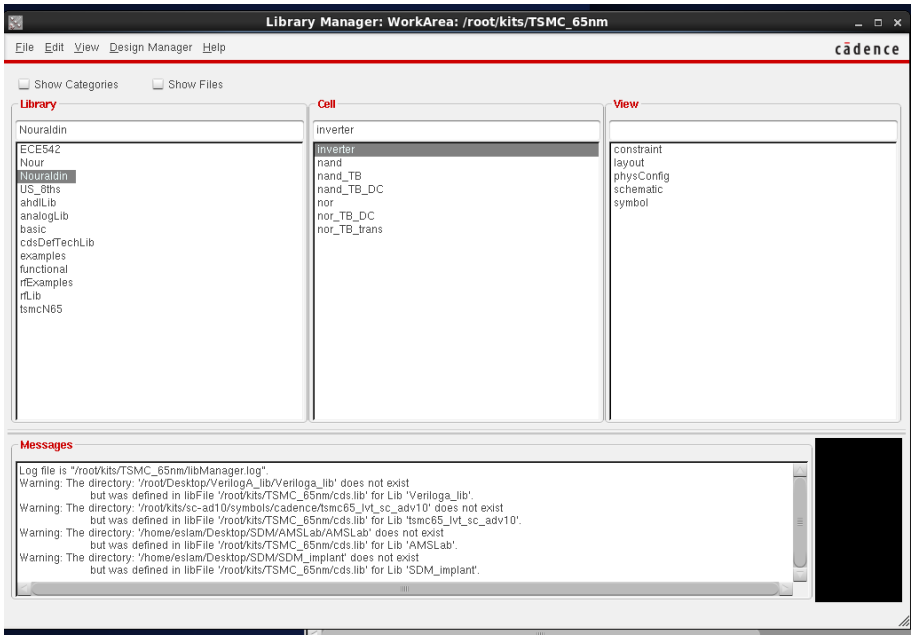



*Figure 6: Creating New Library and cell*

## Inverter Gate Schematic Design

- Press ‘I’ to insert the components required for the schematic.
- From the “TSMC65” technology library, insert a pmos “pch” and a nmos “nch”.
- Change the pch parameters to W = 2u.
- change the nch parameters to W = 1u.
- From the “analoglib” library, insert vdd and gnd.
- Make your Vin and Vout ports.
- Press ‘W’ to start connecting the components.

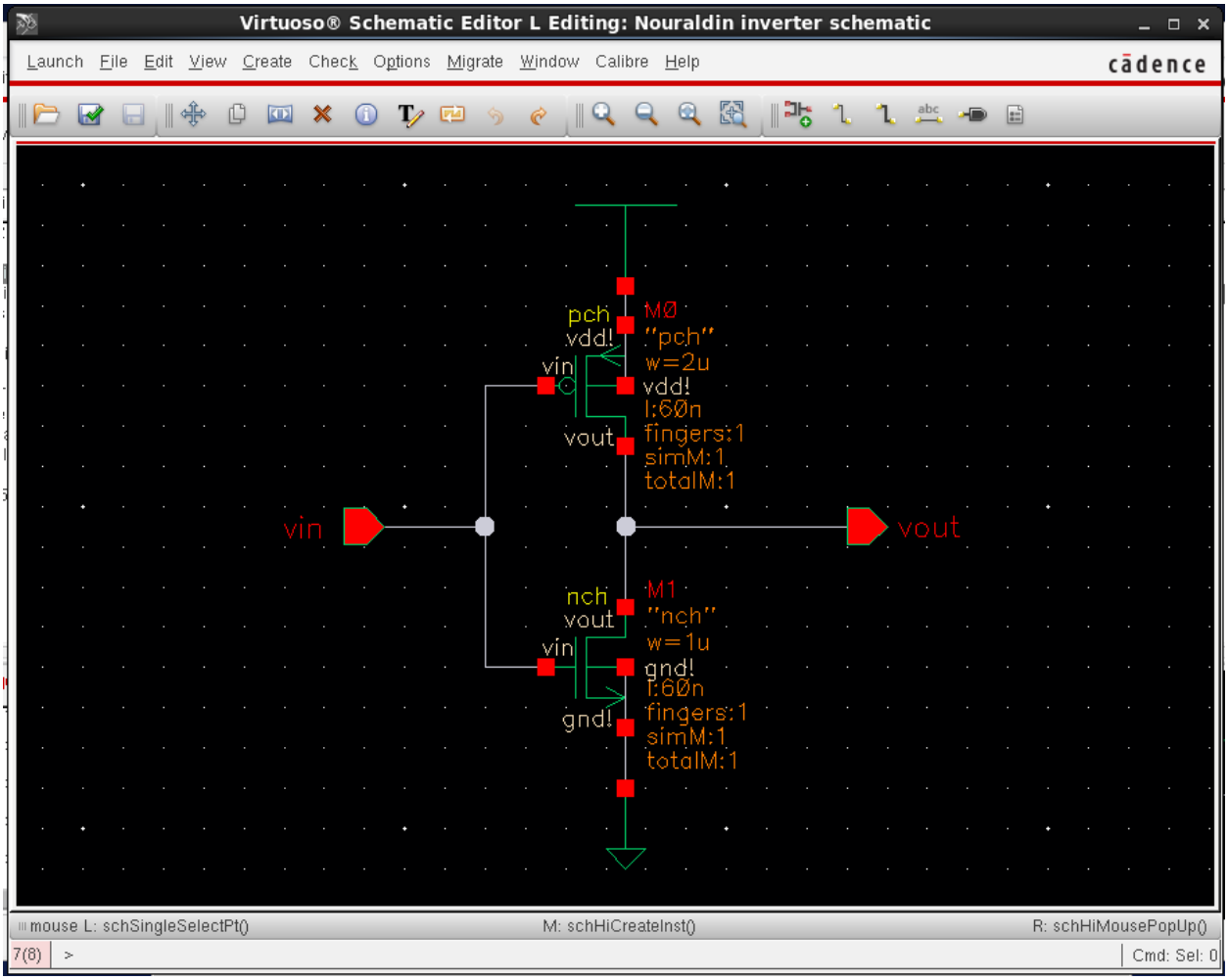



*Figure 7: Inverter Schematic*

# Inverter Gate Testbench

- We need to create a cell view

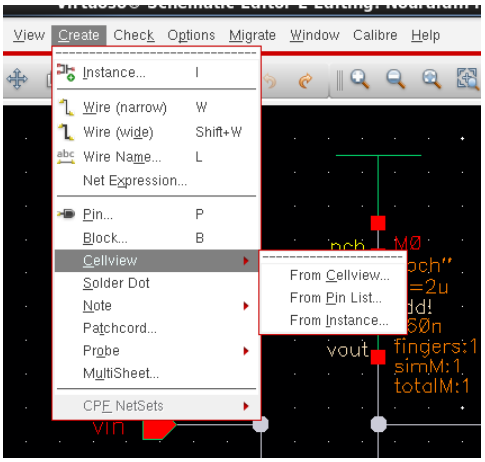



*Figure 9: Create New Cell View*

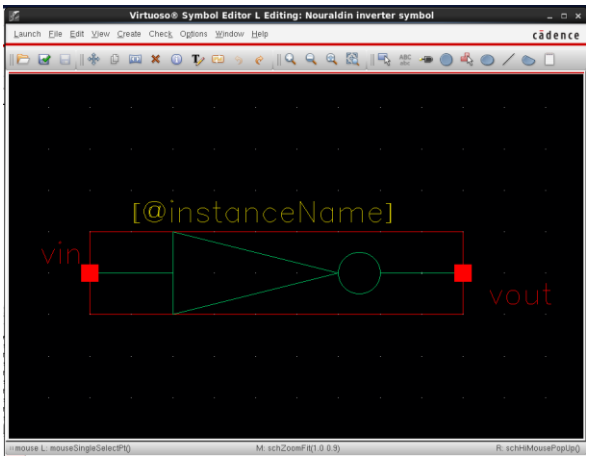



*Figure 8: Inverter Symbol*

- Then we create a new cell called “Inverter_TB_DC” for DC analysis and “Inverter_TB_trans” for transient analysis.


*Figure 10: files of inverter testbench*

## DC analysis

### schematic:

We used a DC voltage source with value = vb as an input.

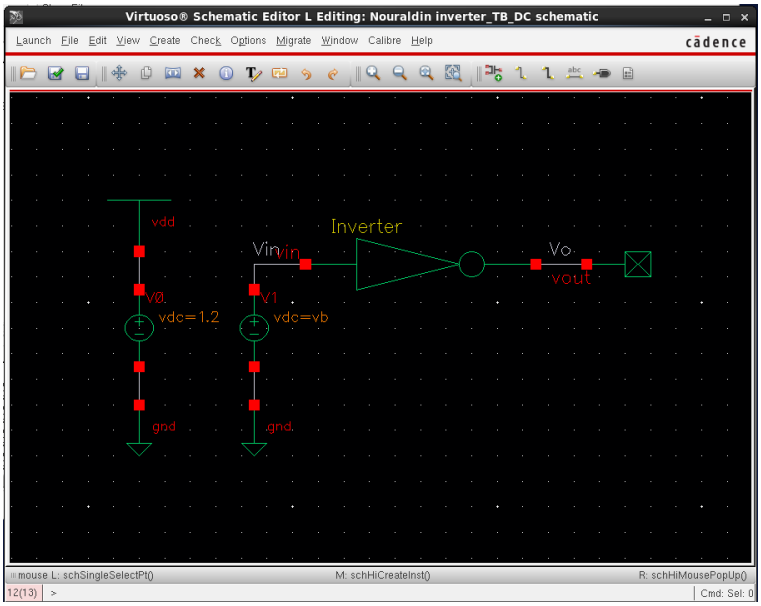



*Figure 11: DC analysis Schematic*

### simulation Output:

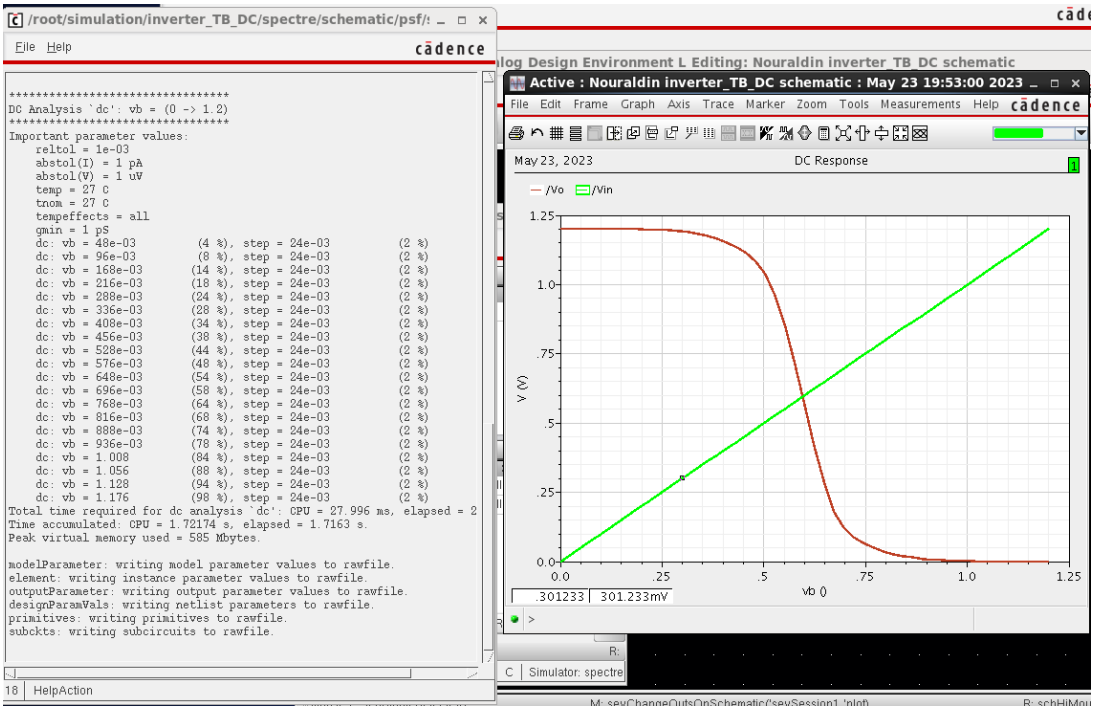



*Figure 12: DC analysis Output*

The parametric analysis investigates how the circuit performance varies with the width of the pmos transistor

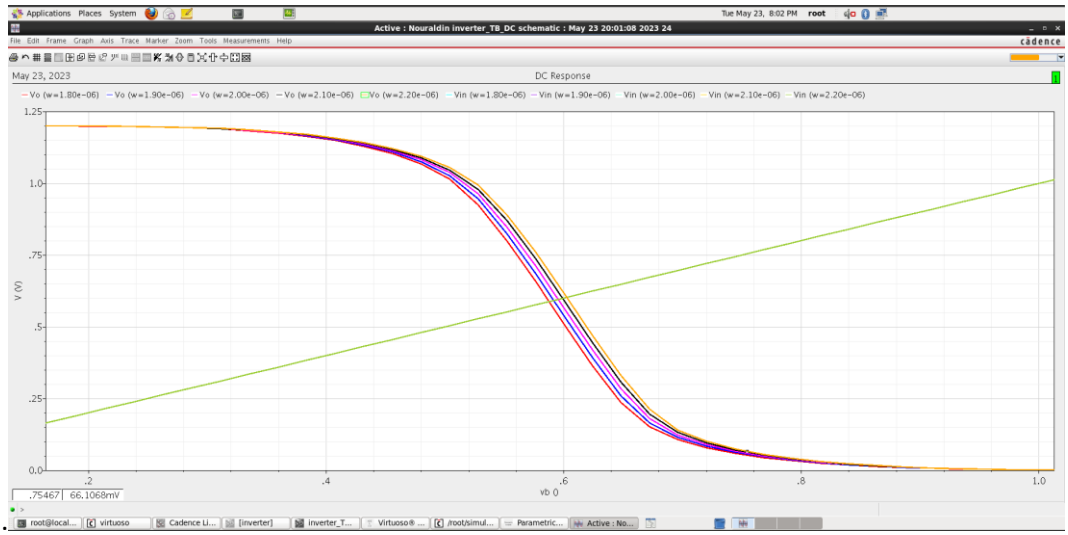



*Figure 13: DC analysis output with variation in W*

## Transient Response analysis

### schematic:

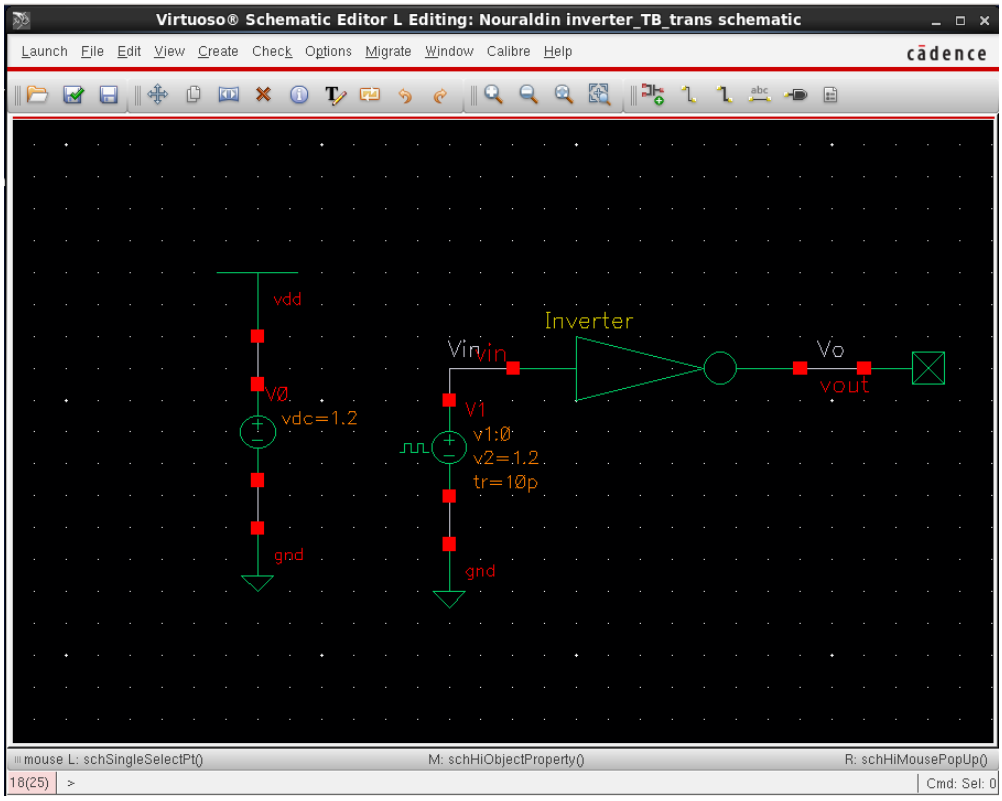
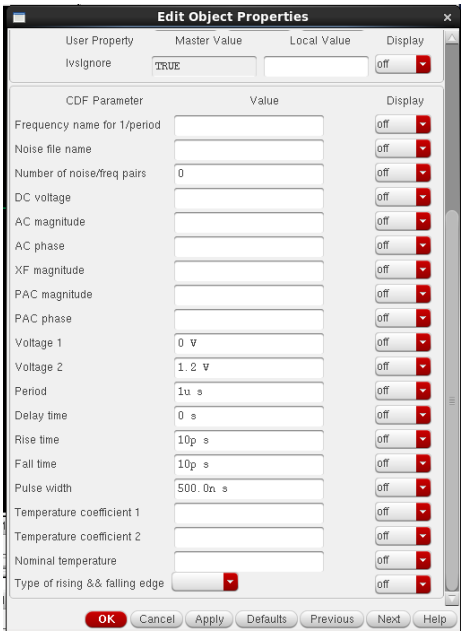



*Figure 14: Transient Analysis Schematic*

Vpulse voltage source was used to provide the input signal.



## simulation Output:

The simulation shows that the output is the opposite of the input, which confirms the correct functioning of the inverter.

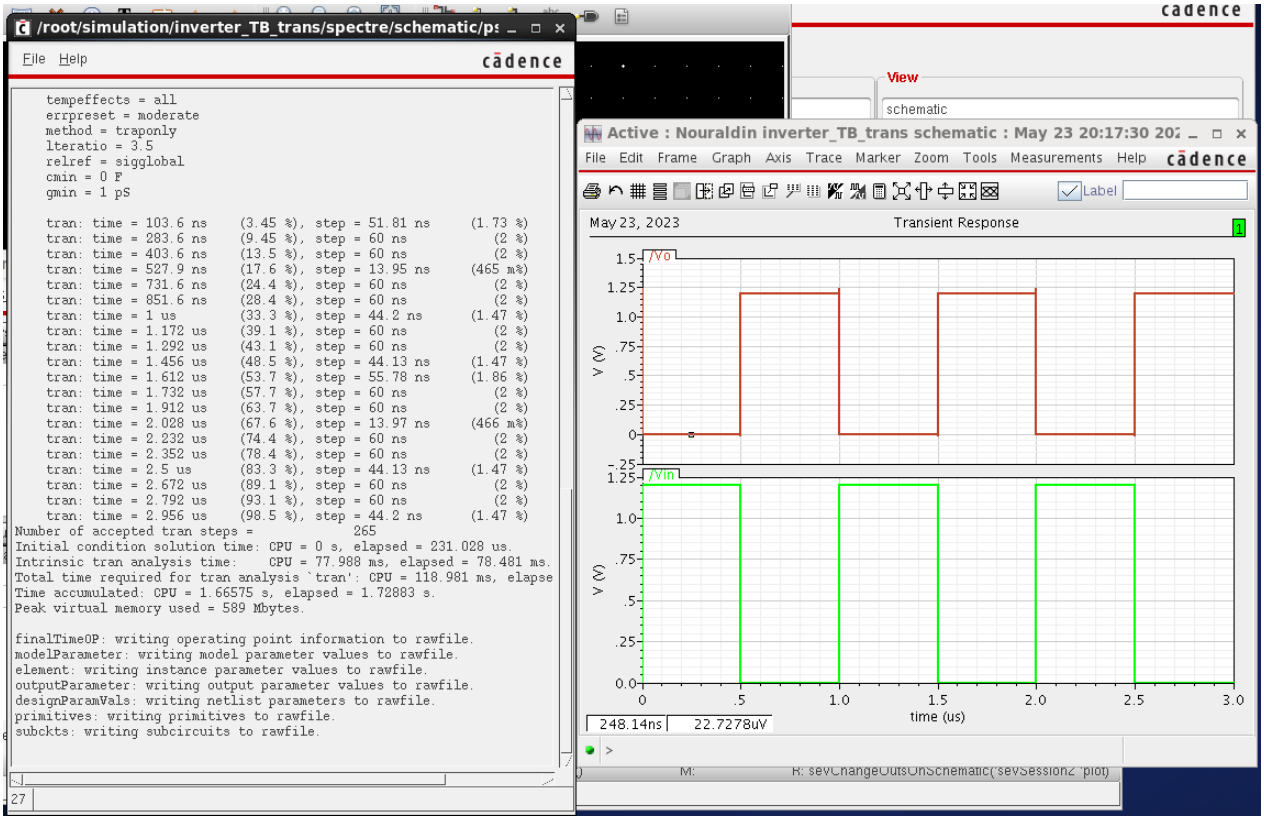



*Figure 15: Transient Analysis Simulation Output*

# Inverter Gate Layout:

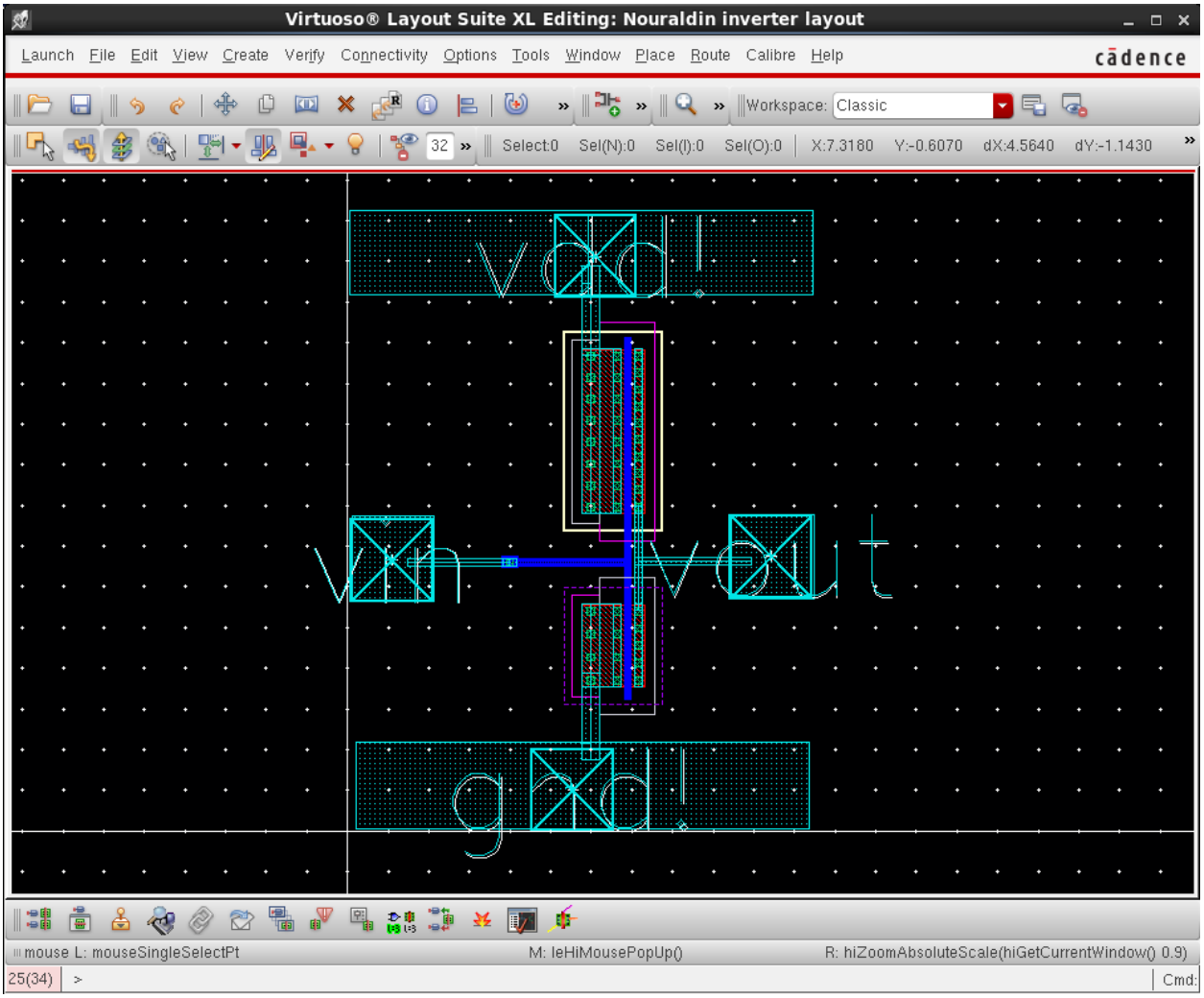



*Figure 16: Inverter Layout*

# Testing

## Design Rule Check Simulation ( DRC ):

There is No Mx.S or A or W.

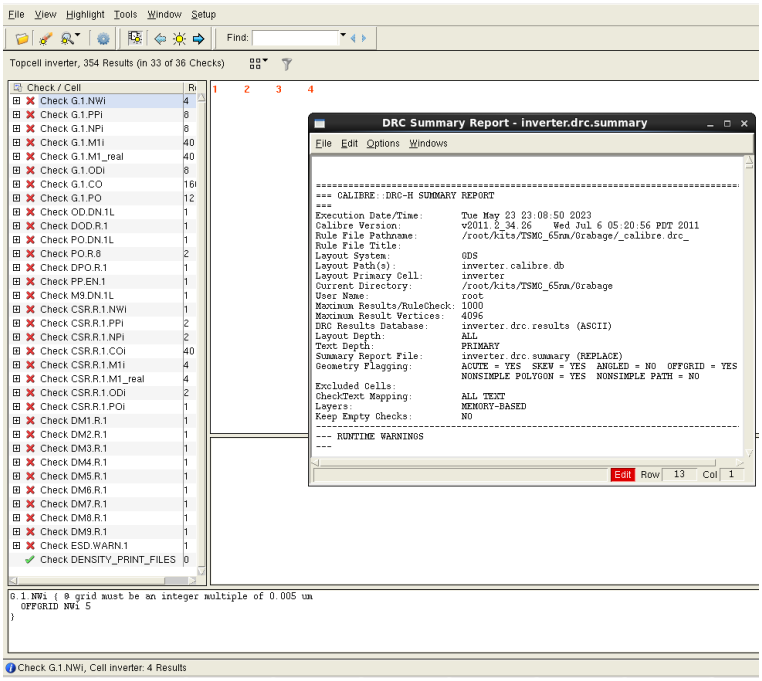



*Figure 17: DRC*

## Layout Versus Schematic ( LVS )

We have the smiley face 😊

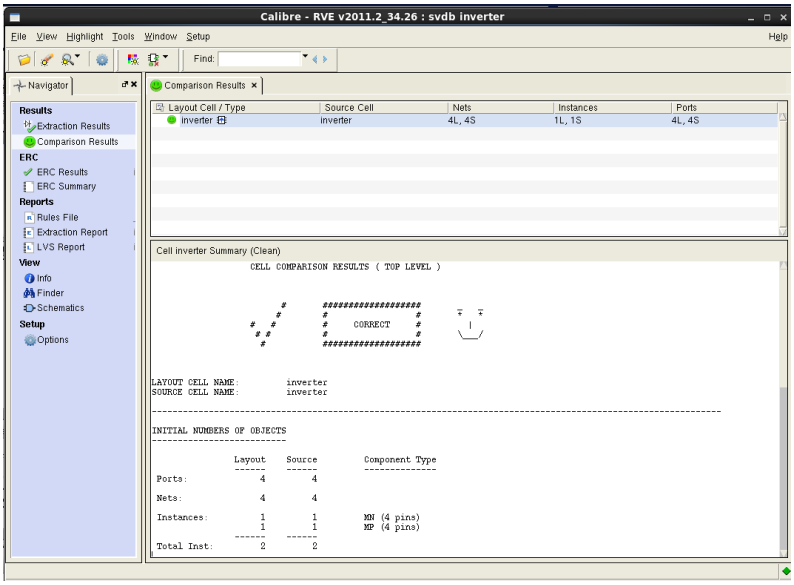



*Figure 18: LVS*

## Parasitic Extraction ( PEX )

Parasitic Extraction (PEX) is a process of calculating the unwanted effects of parasitic components, such as resistances, capacitances, and inductances, in an electronic circuit. PEX is used to create an accurate model of the circuit for simulation and verification purposes.

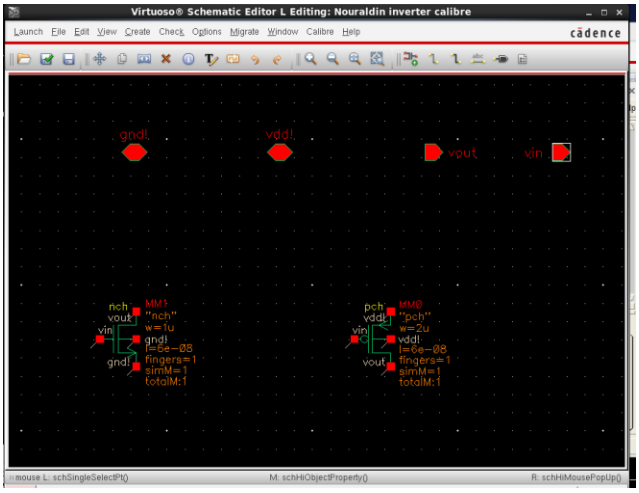



*Figure 20*

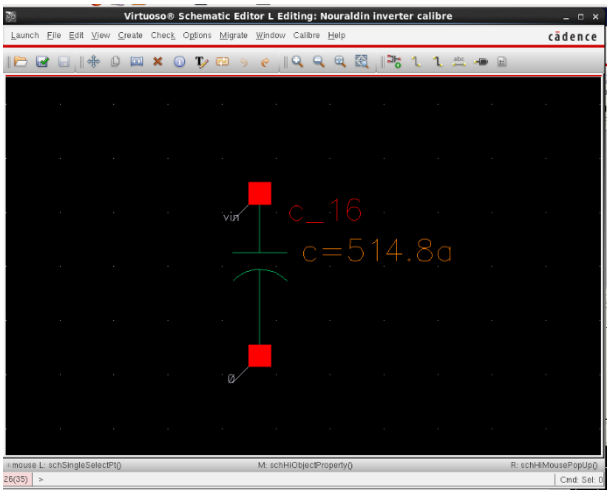



*Figure 19*

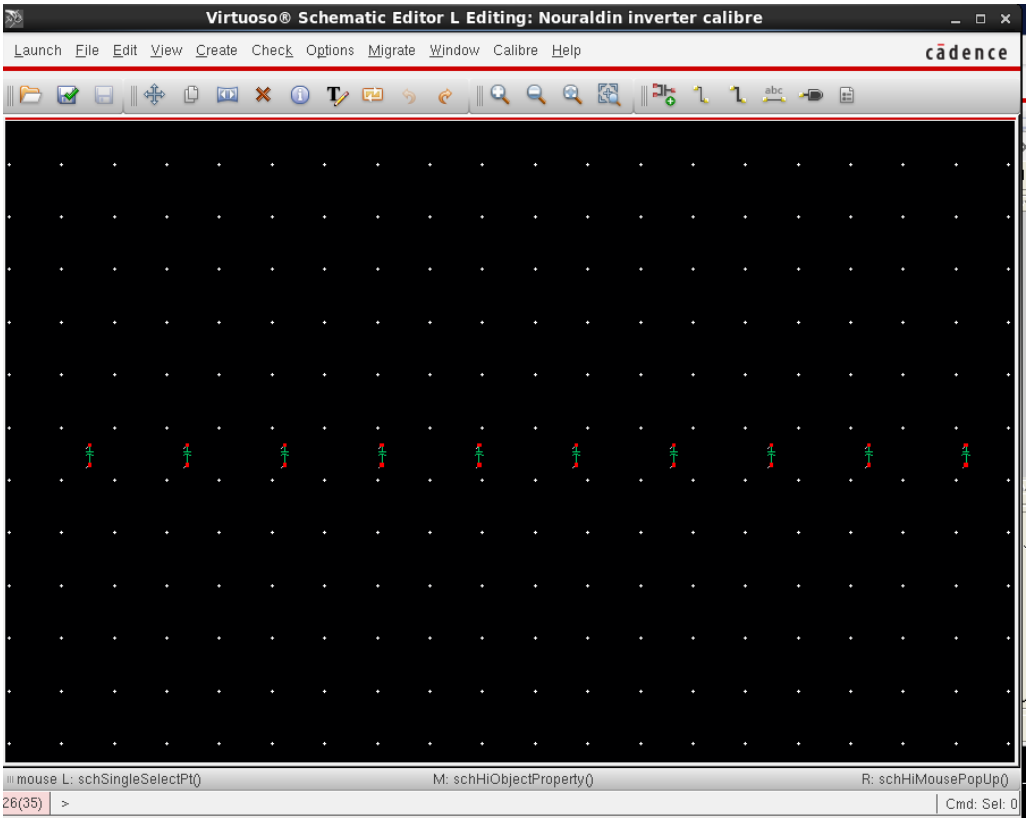



*Figure 21: Parasitic Components*

# Post Layout Simulation

The delay, which is 1.59ps as seen in the following figure, is within the acceptable range.

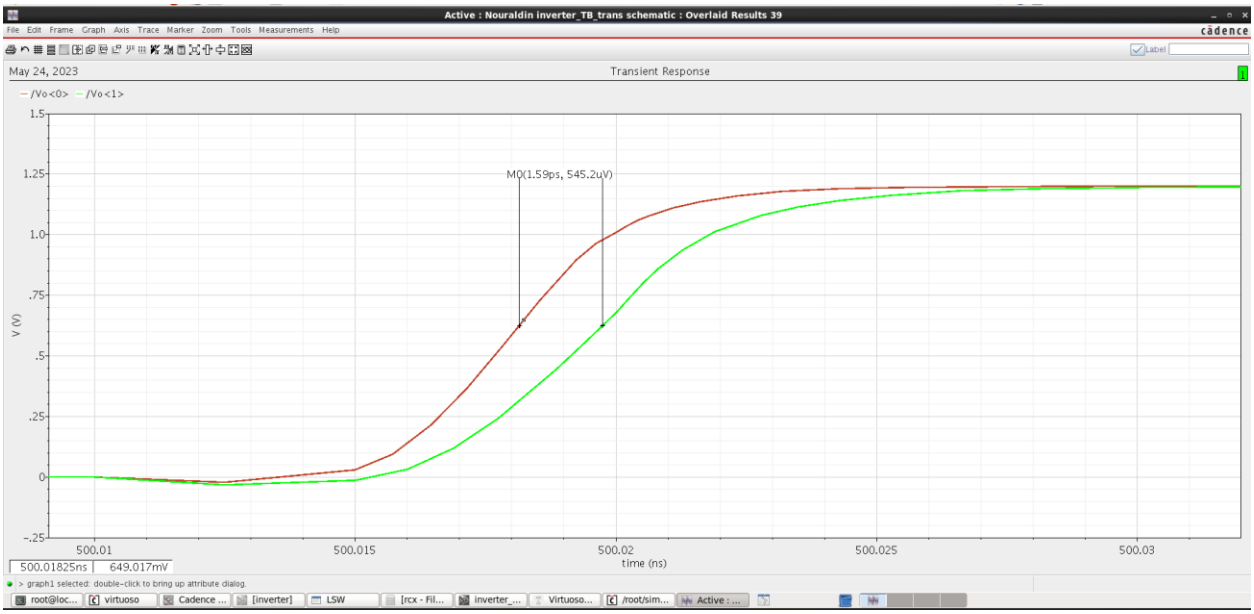



*Figure 22: Post Layout Simulation Output*

## Conclusion:

In this report, we have presented the design process of an inverter gate using the Cadence tool. We have successfully completed the following steps:

- Defined the specifications of the inverter gate
- Created a schematic diagram of the inverter gate
- Tested the functionality and performance of the schematic design
- Designed a layout of the inverter gate
- Tested the layout design for any errors or violations
- Performed a post-layout simulation and verification

We have demonstrated that our design meets the requirements and specifications of an inverter gate. We have also learned how to use the Cadence tool for electronic design automation, and gained valuable experience and skills in digital circuit design. We have encountered some challenges and limitations during the design process, such as choosing the appropriate parameters, optimizing the layout area, and ensuring the reliability and robustness of the design. We have overcome these challenges by applying the relevant concepts, methods, and tools that we have learned in this course. We hope that this report has provided a clear and comprehensive overview of our design process and results.

## Reference:

All the references are from the lab manual and from the Lecture by Dr. Ghazal Attia and Eng. Habiba Mohamed