Assignment 4

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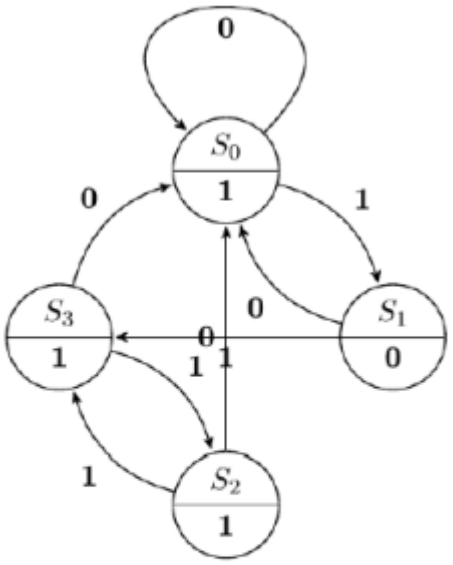
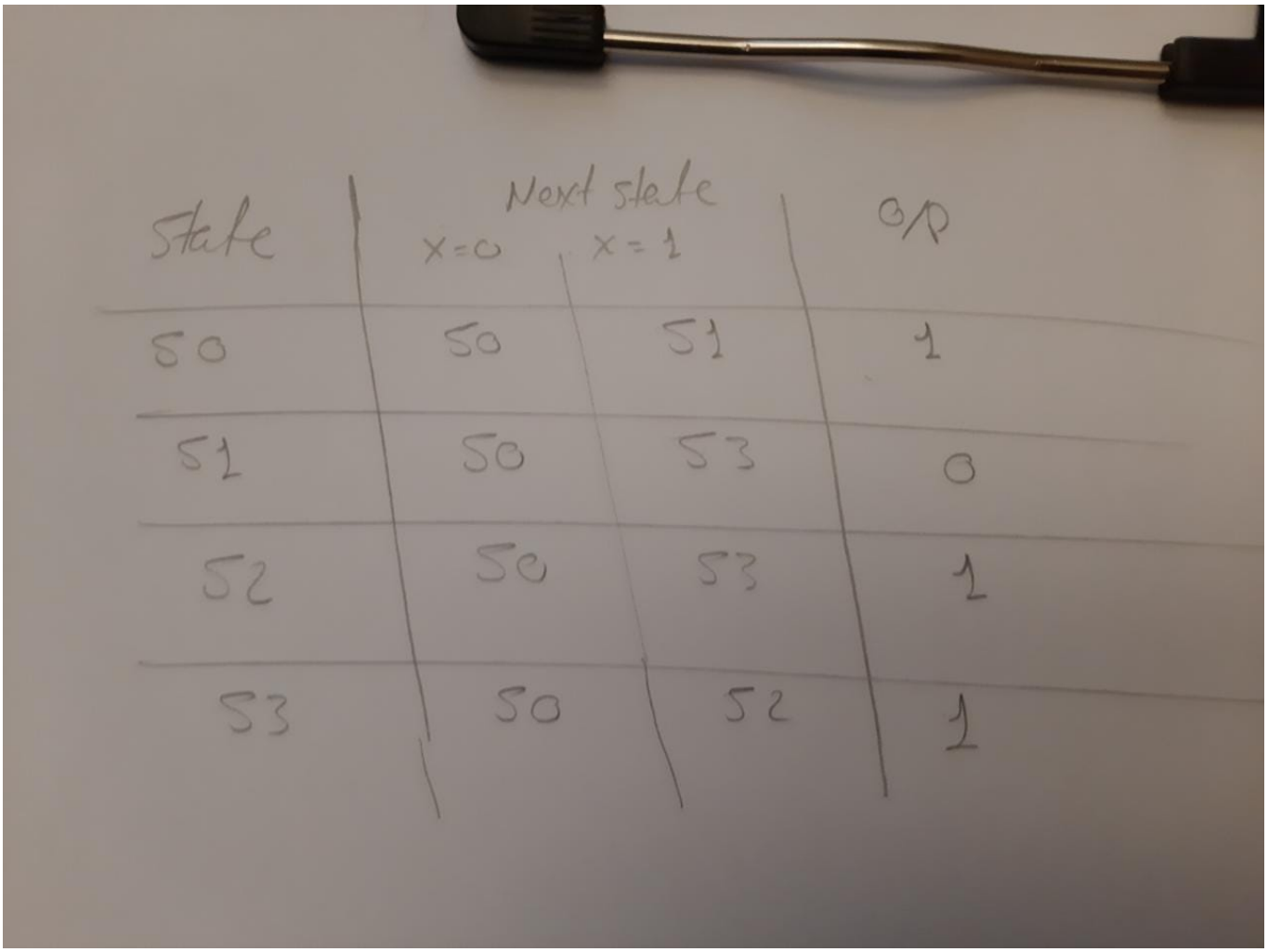
Q3)



a) Analyze this FSM and minimize it if possible

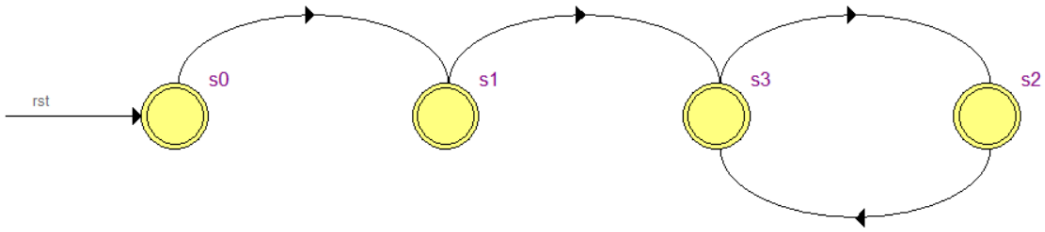
b) Write a VHDL code to describe that minimized state diagram.




```
library ieee;
use ieee.std_logic_1164.all;

entity sheet5 is
        port(
                clk,rst,x : in std_logic;
                z : out std_logic
        );
end entity;

architecture behave of sheet5 is
        type state is(s0,s1,s2,s3);
        signal ns,ps : state;
begin
        present_state : process(clk,rst)
        begin
                if rst='1' then
                        ps <= s0;
                elsif rising_edge(clk) then
```

```
                        ps <= ns;
                end if;
        end process;

        next_state : process(ps,x)
        begin
                case ps is
                        when s0 =>
                                if x = '0' then
                                        ns <= s0;
                                elsif x = '1'
                                        then ns <= s1;
                                end if;
                        when s1 =>
                                if x = '0'
                                        then ns <= s0;
                                elsif x = '1'
                                        then ns <= s3;
                                end if;
                        when s2 =>
                                if x = '0'
                                        then ns <= s0;
                                elsif x = '1'
                                        then ns <= s3;
                                end if;
                        when s3 =>
                                if x = '0'
                                        then ns <= s0;
                                elsif x = '1'
                                        then ns <= s2;
                                end if;
                end case;
        end process;
        z<='0' when ps<=s1 else '1';
end behave;
```

State Machine: |sheet5|ps



	Source State	Destination State	Condition
1	s0	s1	(x)
2	s1	s3	(x)
3	s2	s3	(x)
4	s3	s2	(x)

Transitions | Encoding