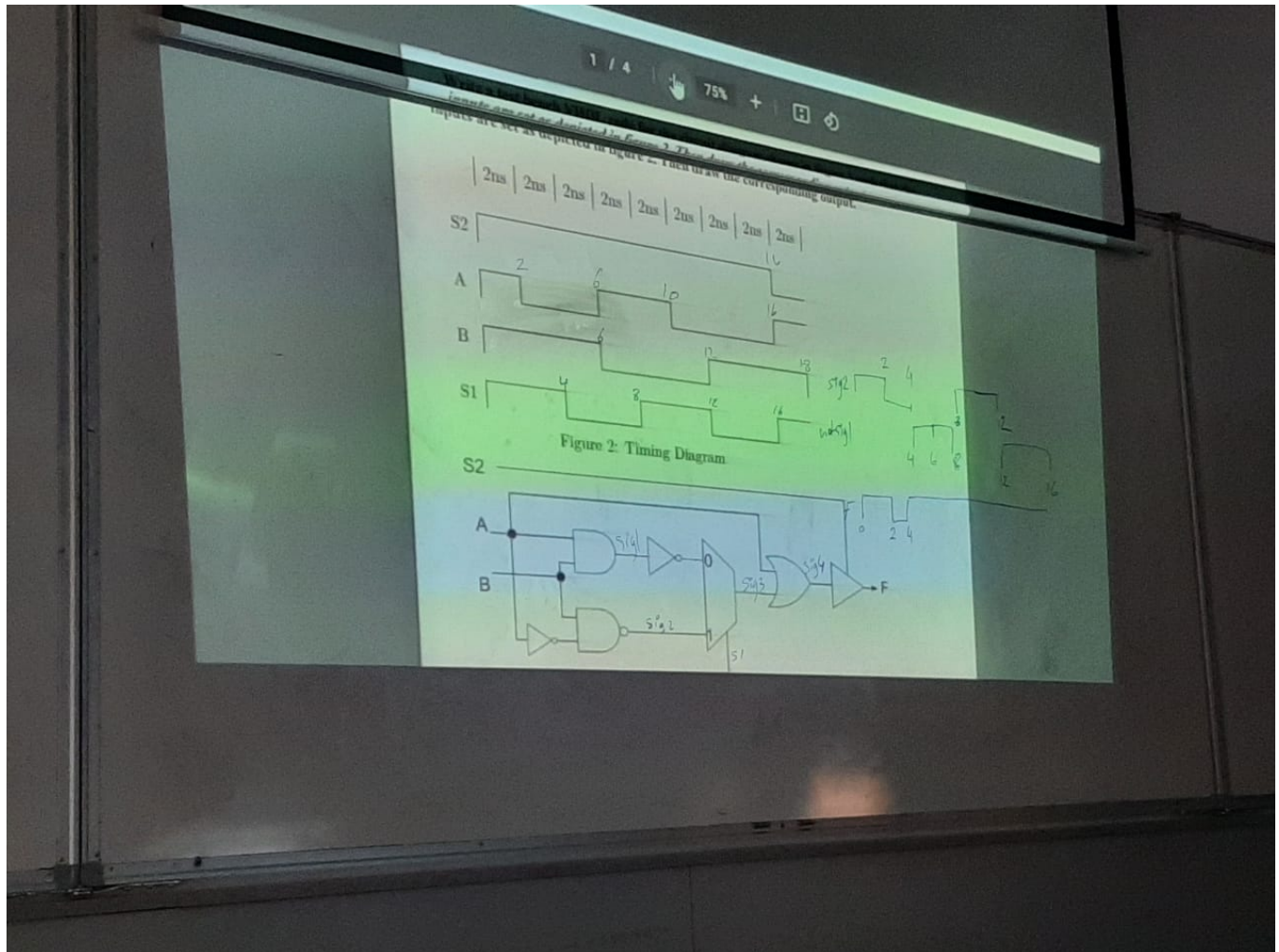


Tutorial 4

sheet 3

Q1



```
library ieee;
use ieee.std_logic_1164.all;

entity tu4 is
port(
    a, b, s1, s2: in std_logic;

    f: out std_logic
);

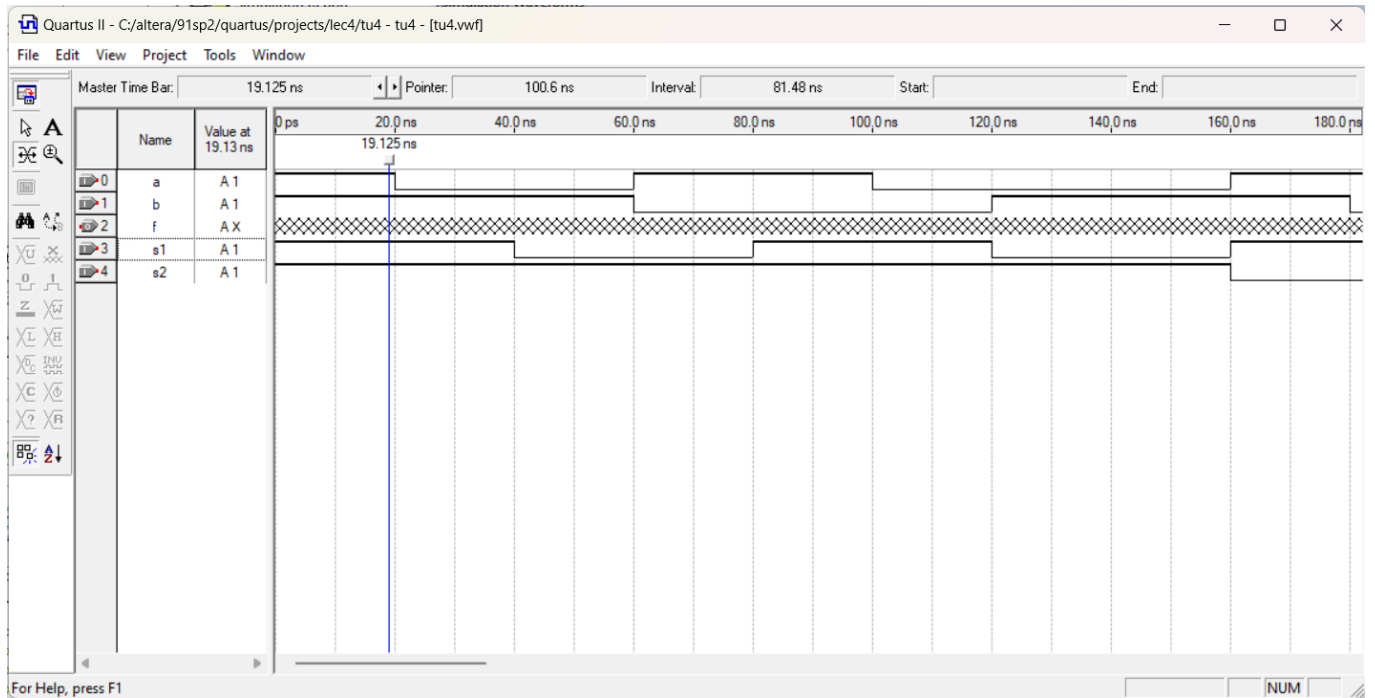
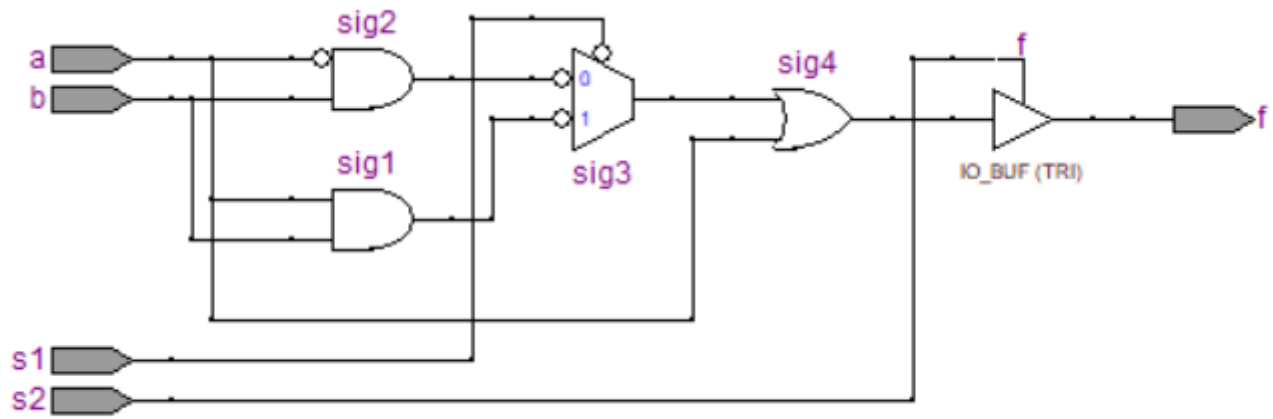
end tu4;
```

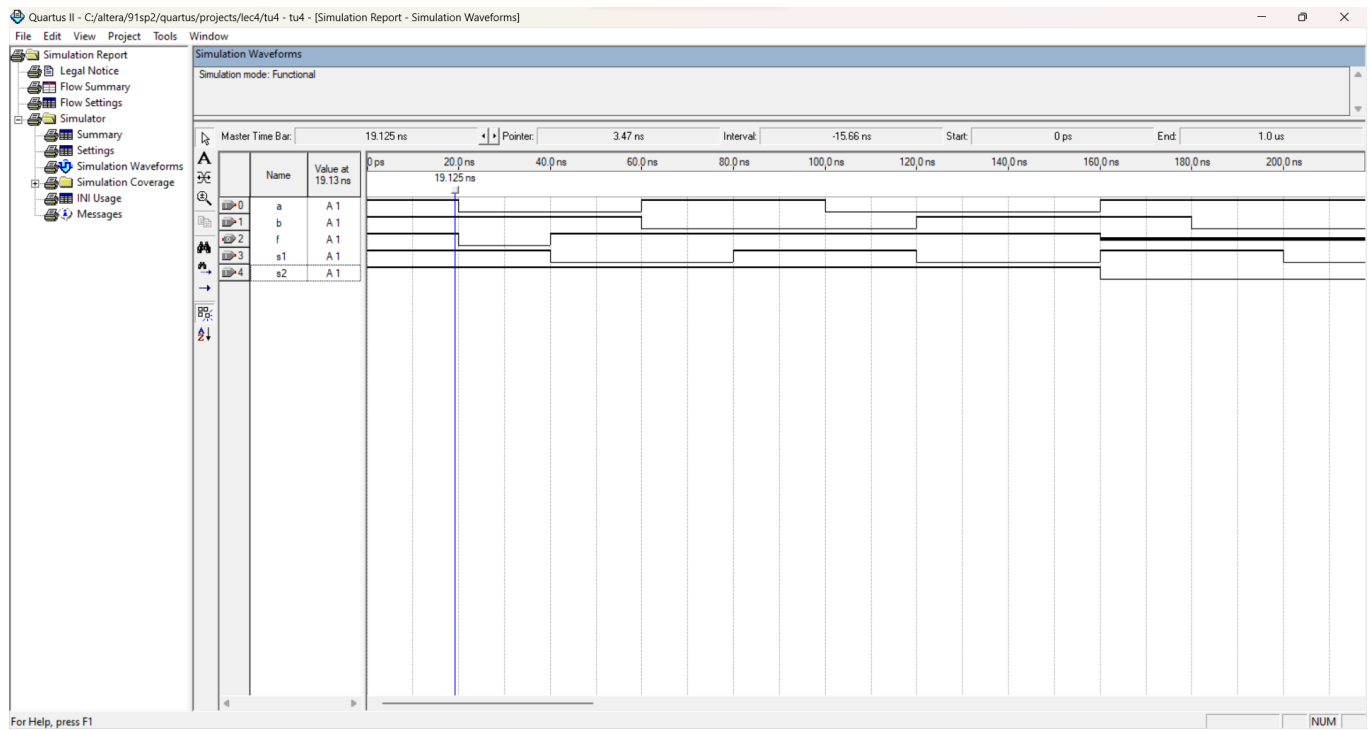
```
architecture behave of tu4 is

    signal sig1, sig2, sig3, sig4: std_logic;

begin
    sig1 <= not( a and b );
    sig2 <= not( not a and b );
    process (s1)
        begin
            case s1 is
                when '0' =>
                    sig3 <= sig1;
                when '1' =>
                    sig3 <= sig2;
            end case;
        end process;
    sig4 <= sig3 or a;

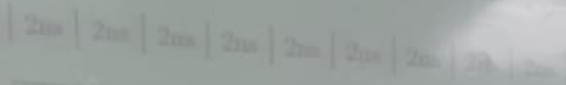
    f <= sig4 when(s2='1') else 'Z';
end behave;
```





Q2

Write a test bench VHDL code for the circuit diagram shown in figure 1 such that the inputs are set as depicted in figure 2. Then draw the corresponding output.



$out1 \leftarrow sig5(0)$
 $out2 \leftarrow sig5(1)$
 $out3 \leftarrow sig5(2)$
 $out4 \leftarrow sig5(3)$

$sig5;$
 $sig5 \leftarrow "0001" \text{ when } 00;$
 $"0010"$
 $"0100"$
 $"1000"$

