Tutorial 6

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Q1

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-- PROGRAM		"Quartus II"
-- VERSION		"Version 9.1 Build 350 03/24/2010 Service Pack 2 SJ Web
Edition"
-- CREATED		"Wed Apr 26 15:34:12 2023"

LIBRARY ieee;
USE ieee.std_logic_1164.all;

LIBRARY work;

ENTITY aftermid IS
	PORT
	(
		A :  IN  STD_LOGIC;
		B :  IN  STD_LOGIC;
		C :  IN  STD_LOGIC;
		D :  IN  STD_LOGIC;
		F :  OUT  STD_LOGIC
	);
```

```
END aftermid;

ARCHITECTURE bdf_type OF aftermid IS

SIGNAL  SYNTHESIZED_WIRE_0 :  STD_LOGIC;
SIGNAL  SYNTHESIZED_WIRE_1 :  STD_LOGIC;


BEGIN

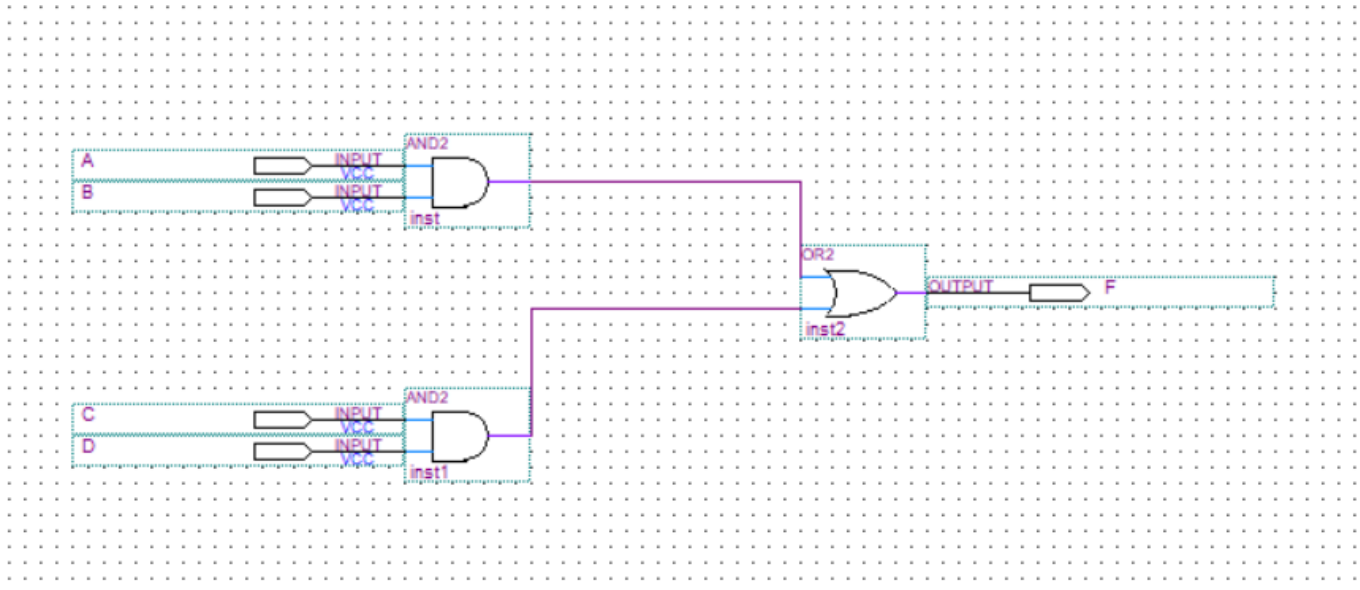


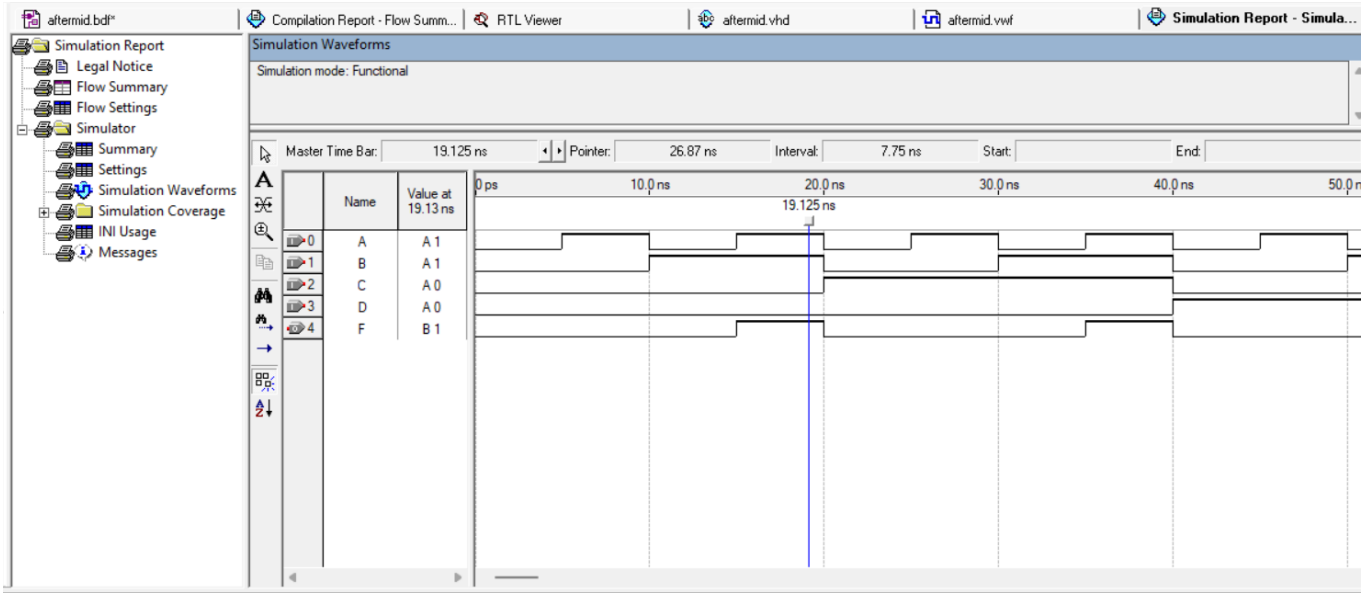
SYNTHESIZED_WIRE_1 <= A AND B;


SYNTHESIZED_WIRE_0 <= C AND D;

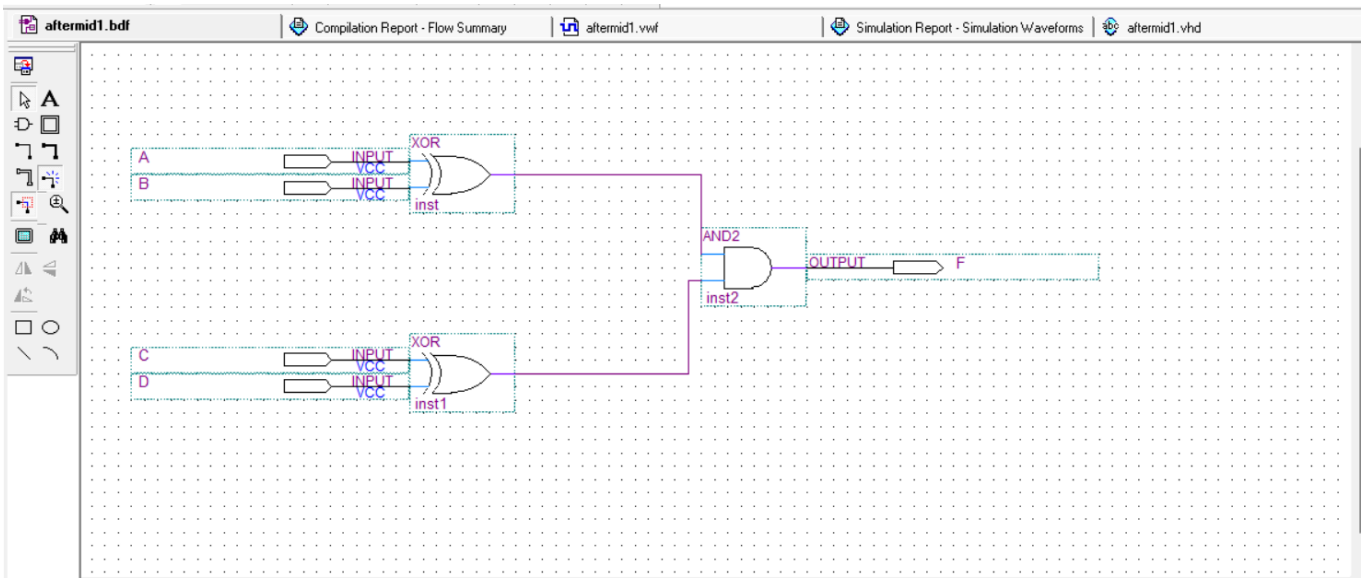

F <= SYNTHESIZED_WIRE_0 OR SYNTHESIZED_WIRE_1;


END bdf_type;
```


A
B
INPUT
VCC
AND2
inst
OR2
OUTPUT
F
inst2
C
D
inst1


aftermid.bdf*
Compilation Report - Flow Summ...
RTL Viewer
aftermid.vhd
aftermid.vwf
Simulation Report - Simula...
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Waveforms
Simulation Coverage
INI Usage
Messages
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 19.125 ns
Pointer: 26.87 ns
Interval: 7.75 ns
Start:
End:
Name
Value at 19.13 ns
0 A A 1
1 B A 1
2 C A 0
3 D A 0
4 F B 1
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
19.125 ns

Q2

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-- PROGRAM		"Quartus II"
-- VERSION		"Version 9.1 Build 350 03/24/2010 Service Pack 2 SJ Web
Edition"
-- CREATED		"Wed Apr 26 15:49:53 2023"

LIBRARY ieee;
USE ieee.std_logic_1164.all;

LIBRARY work;

ENTITY aftermid1 IS
	PORT
```
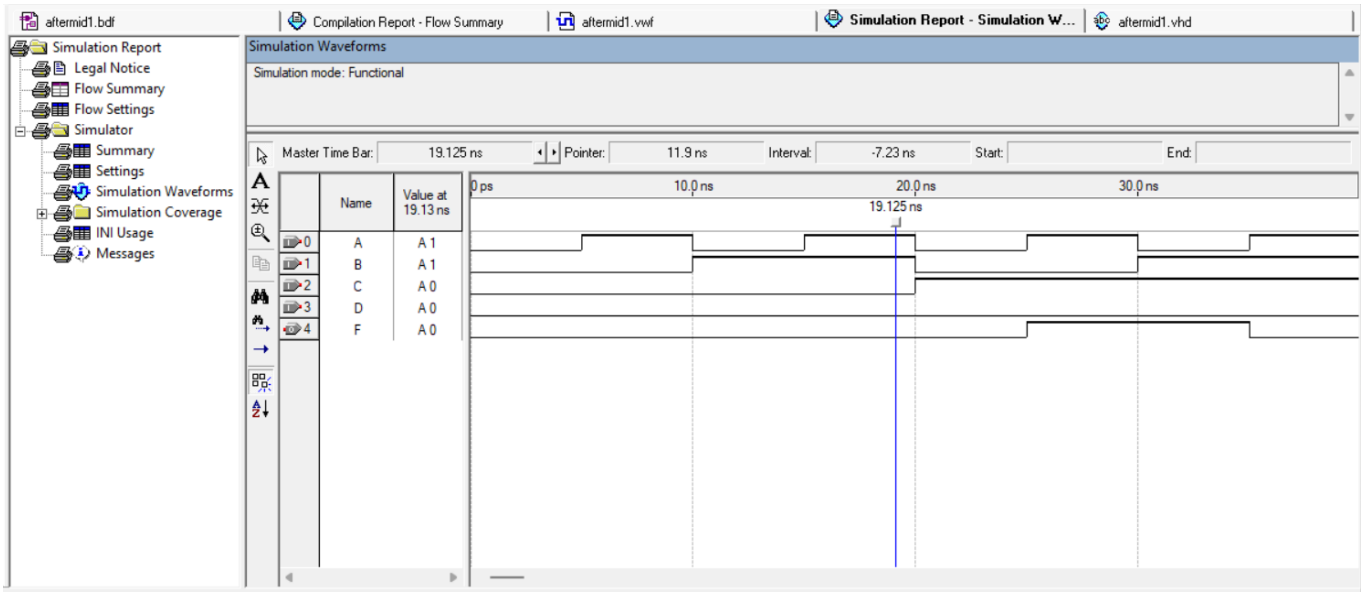

```
        (
                A :  IN  STD_LOGIC;
                B :  IN  STD_LOGIC;
                C :  IN  STD_LOGIC;
                D :  IN  STD_LOGIC;
                F :  OUT  STD_LOGIC
        );
END aftermid1;

ARCHITECTURE bdf_type OF aftermid1 IS

SIGNAL  SYNTHESIZED_WIRE_0 :  STD_LOGIC;
SIGNAL  SYNTHESIZED_WIRE_1 :  STD_LOGIC;


BEGIN



SYNTHESIZED_WIRE_0 <= A XOR B;


SYNTHESIZED_WIRE_1 <= C XOR D;


F <= SYNTHESIZED_WIRE_0 AND SYNTHESIZED_WIRE_1;


END bdf_type;
```



Q3

```
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-- PROGRAM		"Quartus II"
-- VERSION		"Version 9.1 Build 350 03/24/2010 Service Pack 2 SJ Web
Edition"
-- CREATED		"Wed Apr 26 16:11:36 2023"

LIBRARY ieee;
USE ieee.std_logic_1164.all;

LIBRARY work;

ENTITY aftermid11 IS
	PORT
	(
		a :  IN  STD_LOGIC;
		b :  IN  STD_LOGIC;
		c :  IN  STD_LOGIC;
		d :  IN  STD_LOGIC;
		e :  IN  STD_LOGIC;
		f :  IN  STD_LOGIC;
		x :  OUT  STD_LOGIC;
		y :  OUT  STD_LOGIC
	);
END aftermid11;

ARCHITECTURE bdf_type OF aftermid11 IS
```
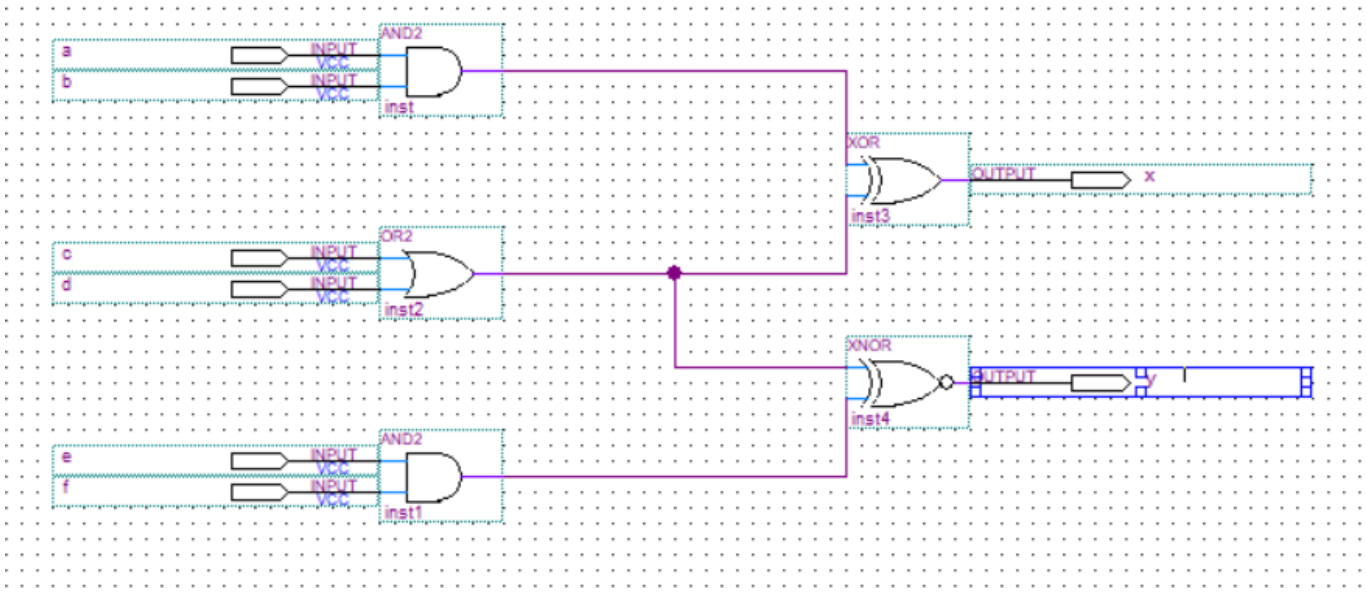
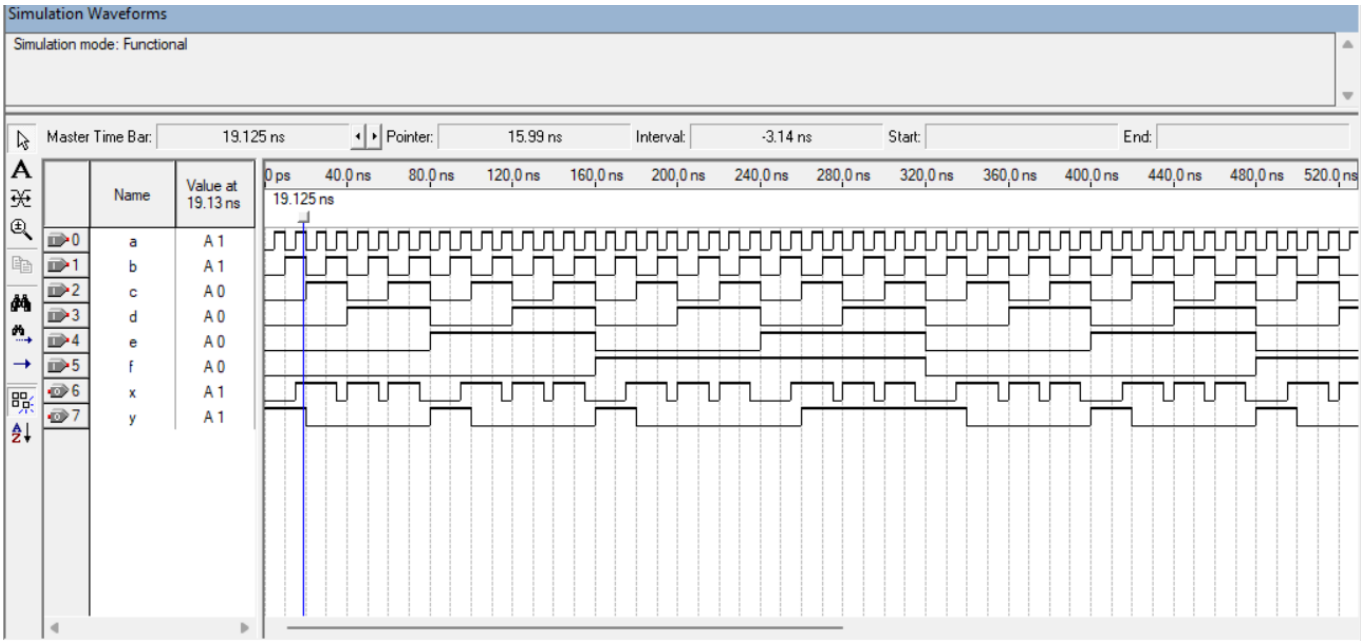

```
SIGNAL  SYNTHESIZED_WIRE_0 :  STD_LOGIC;
SIGNAL  SYNTHESIZED_WIRE_4 :  STD_LOGIC;
SIGNAL  SYNTHESIZED_WIRE_3 :  STD_LOGIC;


BEGIN


SYNTHESIZED_WIRE_0 <= a AND b;


SYNTHESIZED_WIRE_3 <= e AND f;


SYNTHESIZED_WIRE_4 <= d OR c;


x <= SYNTHESIZED_WIRE_0 XOR SYNTHESIZED_WIRE_4;


y <= NOT(SYNTHESIZED_WIRE_4 XOR SYNTHESIZED_WIRE_3);


END bdf_type;
```




Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 19.125 ns
Pointer: 15.99 ns
Interval: -3.14 ns
Start:
End:
Name
Value at 19.13 ns
0 a A 1
1 b A 1
2 c A 0
3 d A 0
4 e A 0
5 f A 0
6 x A 1
7 y A 1
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns
240.0 ns
280.0 ns
320.0 ns
360.0 ns
400.0 ns
440.0 ns
480.0 ns
520.0 ns
19.125 ns