Misr International University
Electronics and Communication Engineering
ECE 542 (VLSI Lab)
Spring 2023

Lab 2:
NAND Gate

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Contents

Table of Figures:

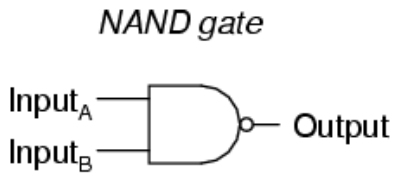
Aim:

The aim of this report is to explain the design process of a NAND gate using the Cadence tool. The design process consists of the following steps:

- Defining the specifications of the NAND gate
- Developing a behavioral model of the NAND gate
- Creating a schematic diagram of the NAND gate
- Testing the functionality and performance of the schematic design
- Designing a layout of the NAND gate
- Testing the layout design for any errors or violations
- Performing a post-layout simulation and verification

Introduction:

A NAND gate is a basic logic gate that produces an output that is 0 only when both of its inputs are 1, and 1 otherwise. For example, if the inputs are 1 and 0, the output is 1, and if the inputs are 0 and 0, the output is 1. NAND gates are essential components of digital circuits and systems, such as microprocessors, memory devices, and logic controllers. In this report, we will show how we designed a NAND gate using the Cadence tool, which is a software suite for electronic design automation. We will describe the steps we took to create a behavioral model, a schematic diagram, a layout design, and a post-layout simulation of the NAND gate. We will also report the results of our testing and verification of the design and discuss the difficulties and constraints we encountered during the design process.



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Figure 2: NAND truth Table

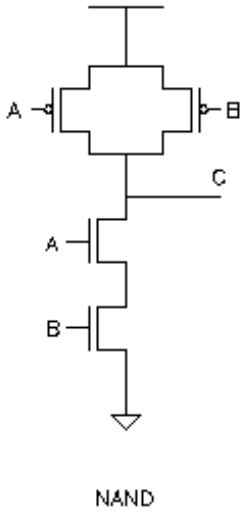


Figure 1: NAND Schematic

NAND Gate Schematic Design

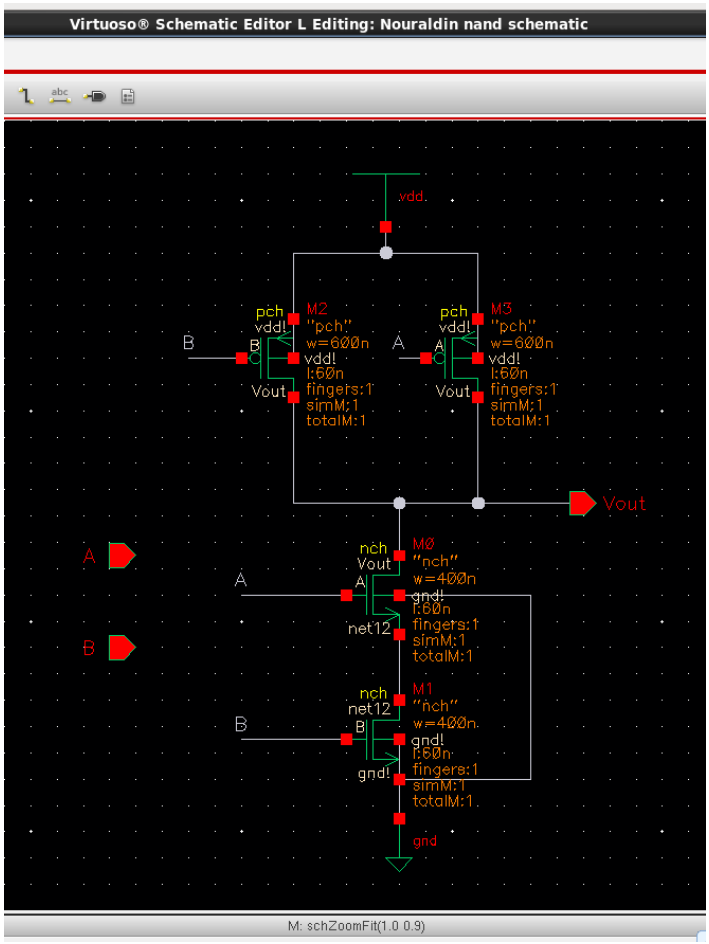


Figure 3: NAND Schematic

- The figure above shows the circuit schematic
- The circuit consists of:
  - Two PMOS transistors with L = 60nm and W = 600nm
  - Two NMOS transistors with L = 60nm and W = 400nm
- The inputs A and B are connected to:
  - The gate terminals of one PMOS and one NMOS transistor each

NAND Gate Testbench

- We need to create a cell view

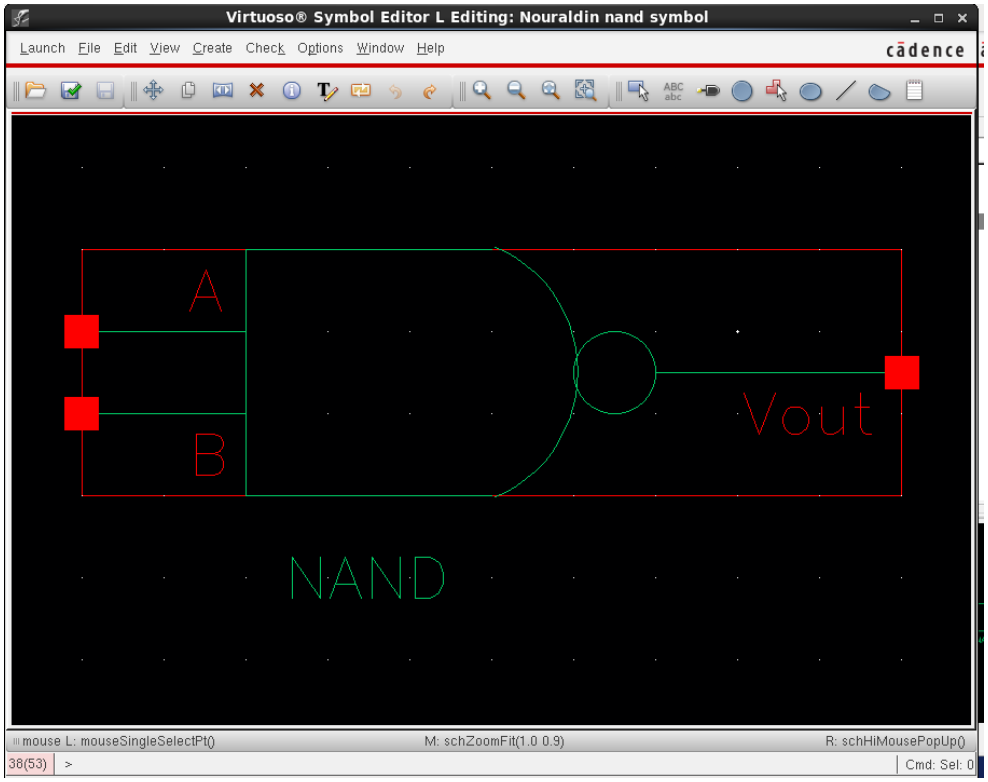


Figure 4: NAND Symbol

- Then we create a new cell called “NAND_TB_DC” for DC analysis and “NAND_TB_trans” for transient analysis.

Figure 5: files of NAND testbench

DC analysis

schematic:

We used a DC voltage source with value = vb as an input.

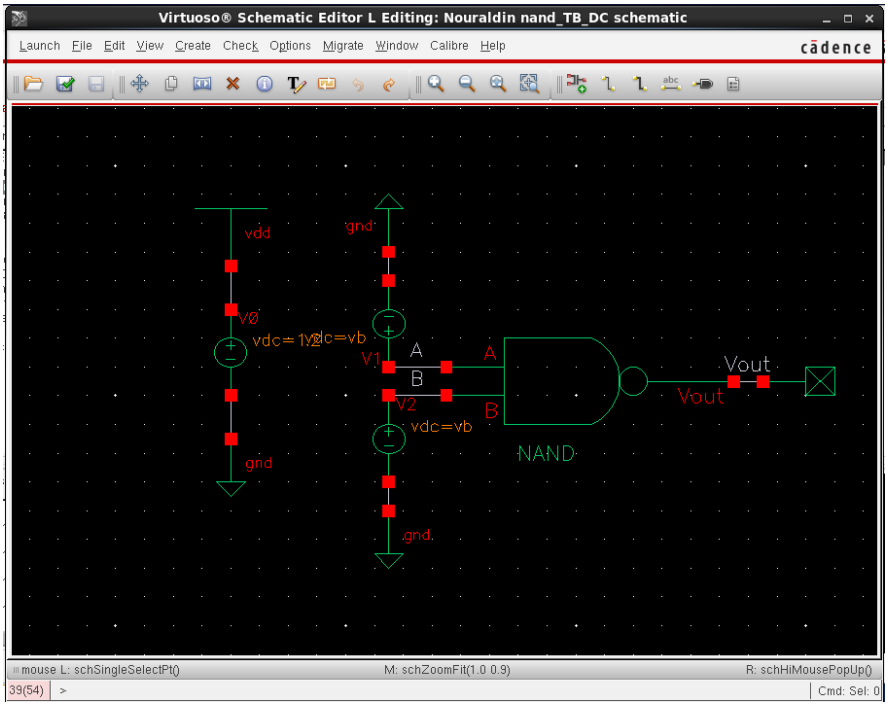


Figure 6: DC analysis Schematic

simulation Output:

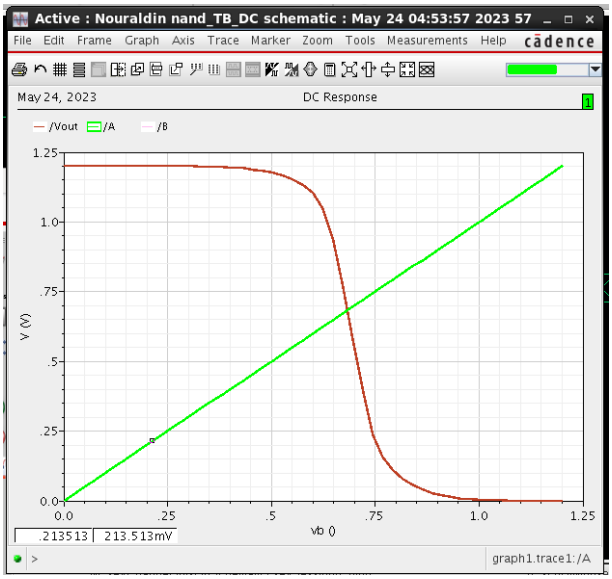


Figure 7: DC analysis Output

Transient Response analysis

schematic:

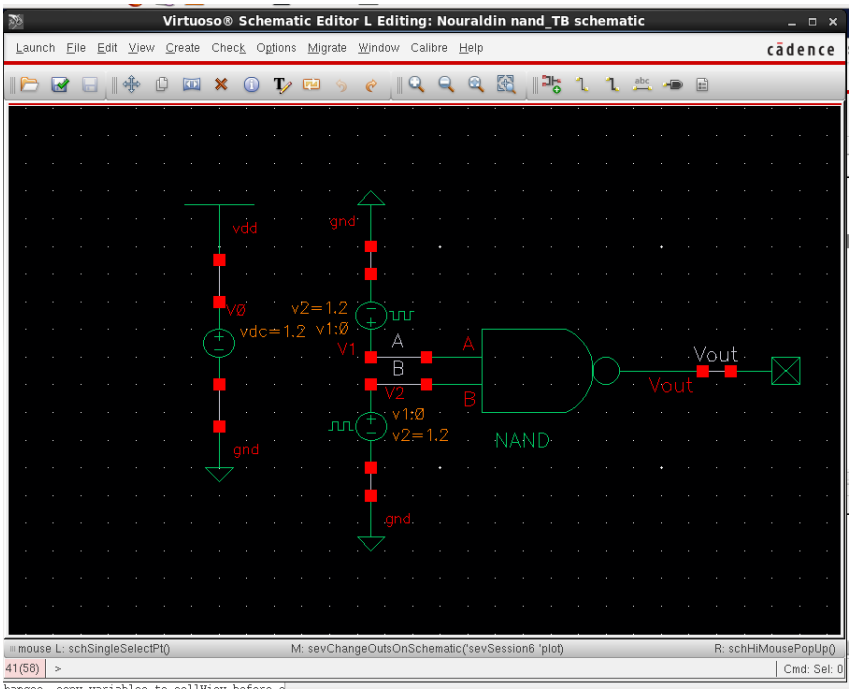


Figure 8: Transient Analysis Schematic

Vpulse voltage source was used to provide the input signal.

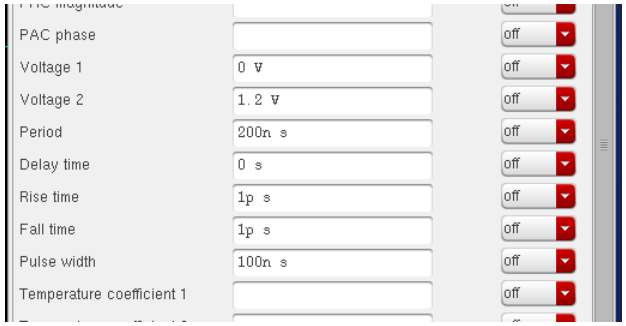


Figure 9: Vpulse 1

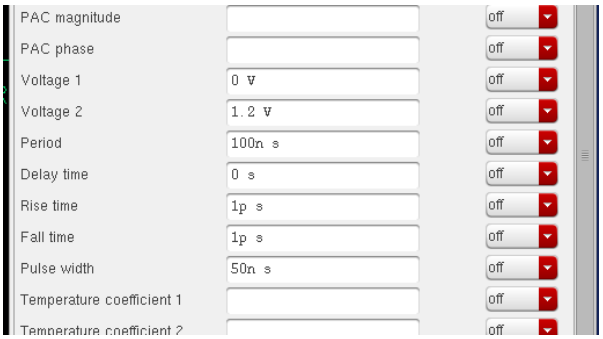


Figure 10: Vpulse 2

simulation Output:

The simulation shows that the output is 0 when Both A and B are 1, which confirms the correct functioning of the NAND.

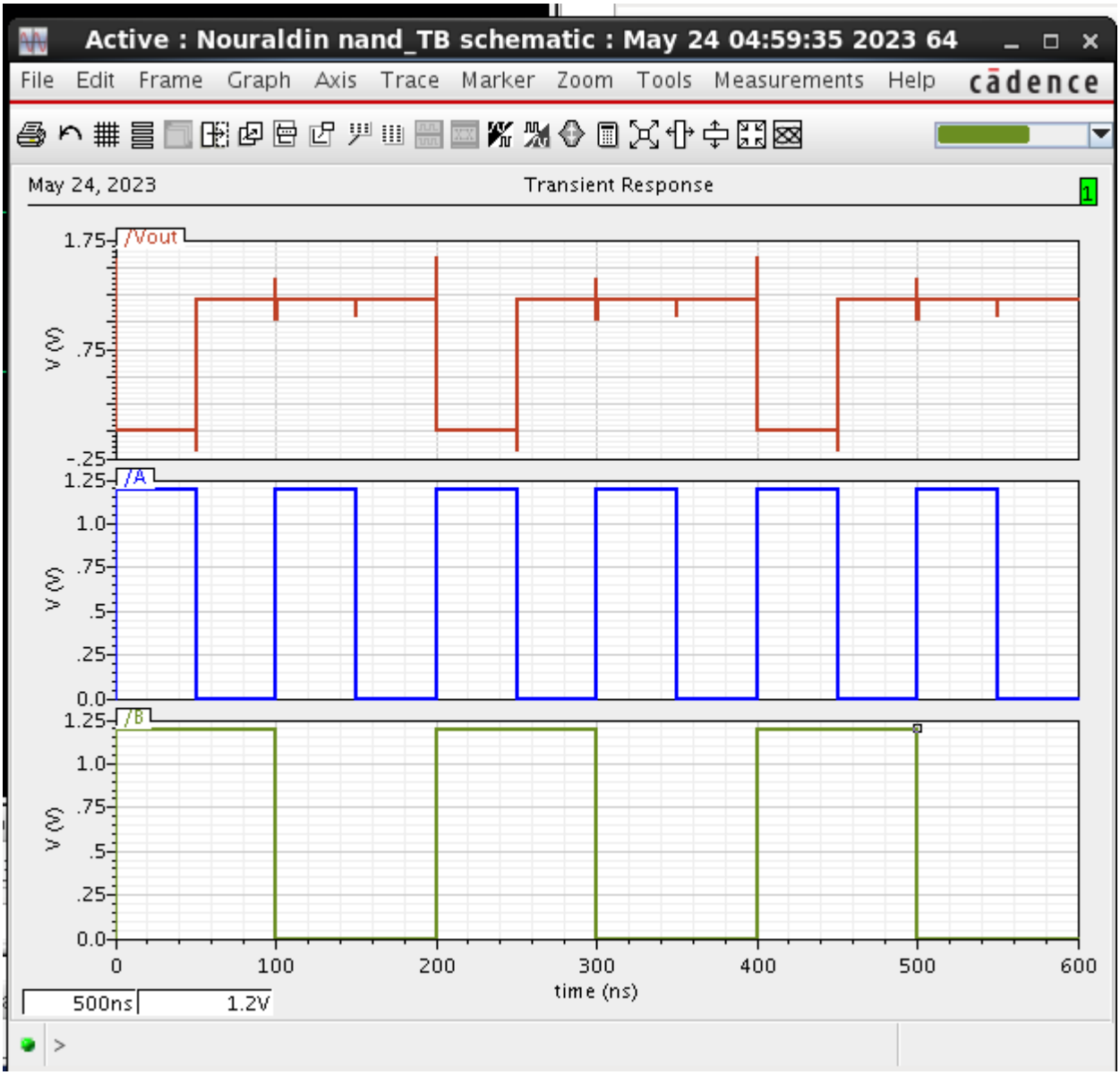


Figure 11: Transient Analysis Simulation Output

NAND Gate Layout:

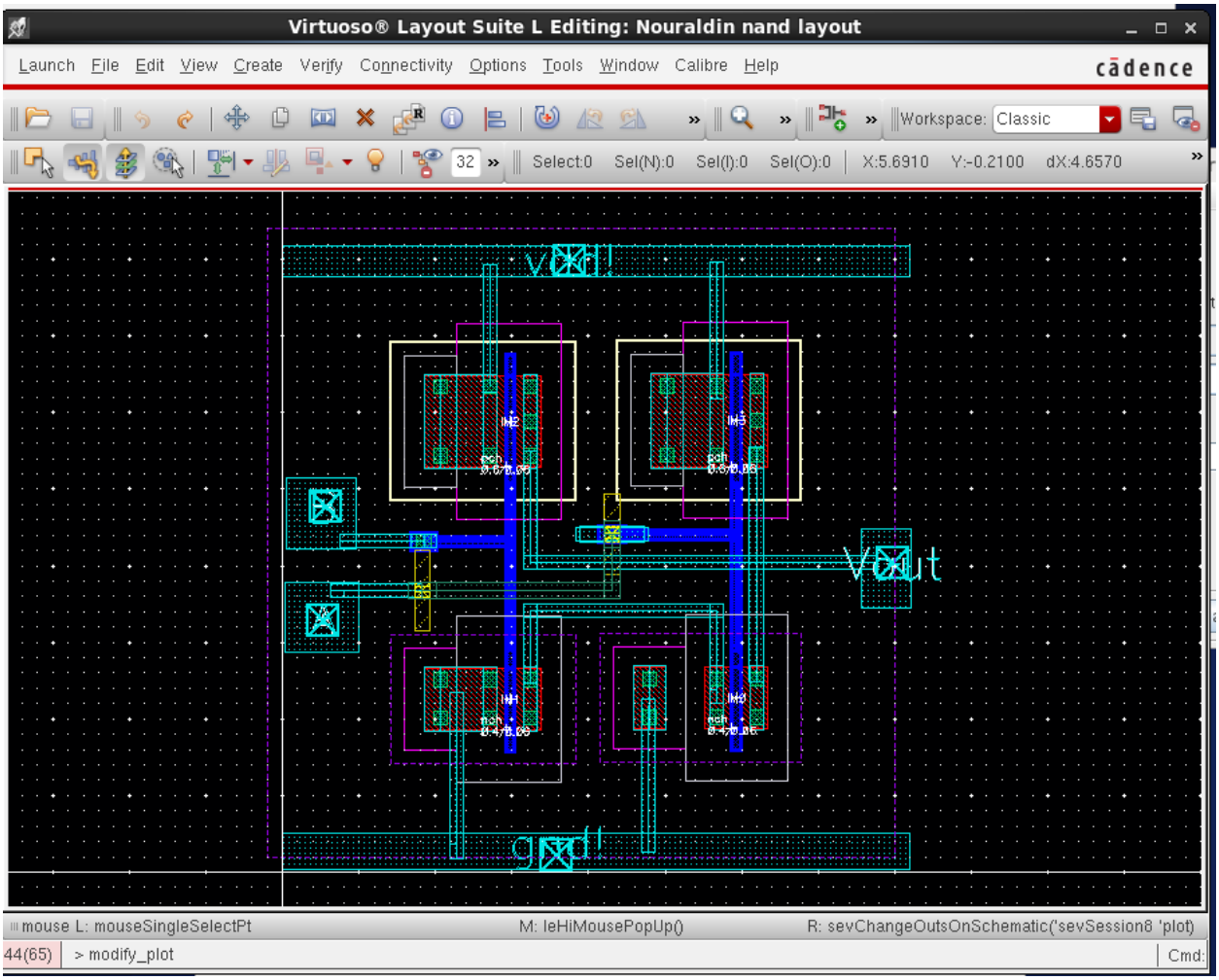


Figure 12: NAND Layout

Testing

Design Rule Check Simulation (DRC):

There is No Mx.S or A or W.

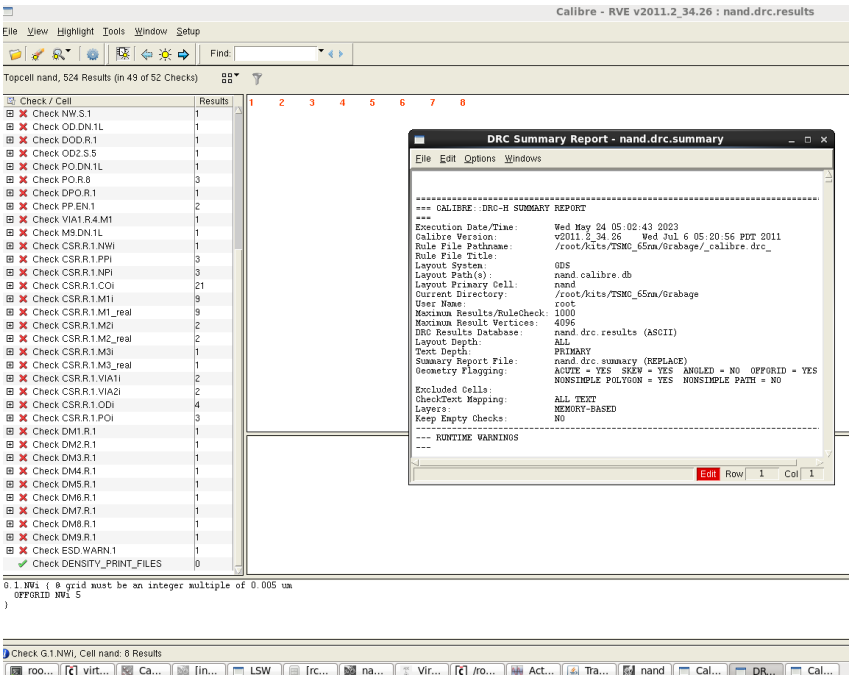


Figure 13: DRC

Layout Versus Schematic (LVS)

We have the smiley face 😊

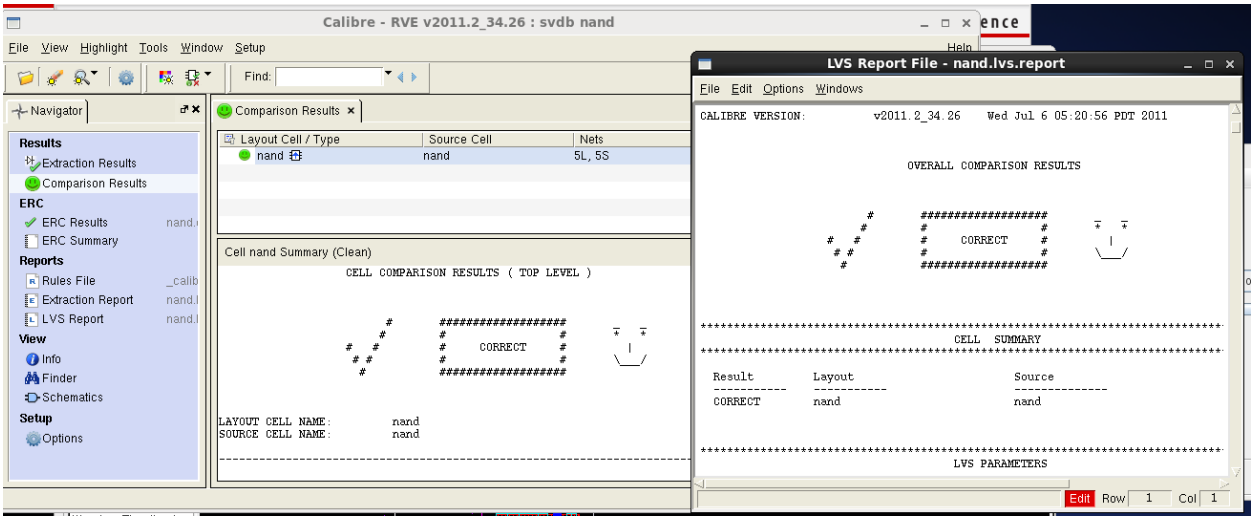


Figure 14: LVS

Parasitic Extraction (PEX)

Parasitic Extraction (PEX) is a process of calculating the unwanted effects of parasitic components, such as resistances, capacitances, and inductances, in an electronic circuit. PEX is used to create an accurate model of the circuit for simulation and verification purposes.

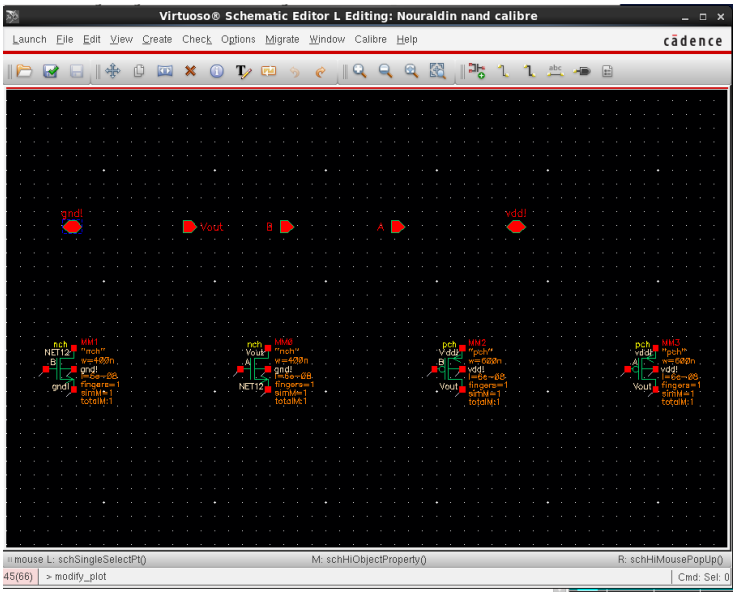


Figure 15

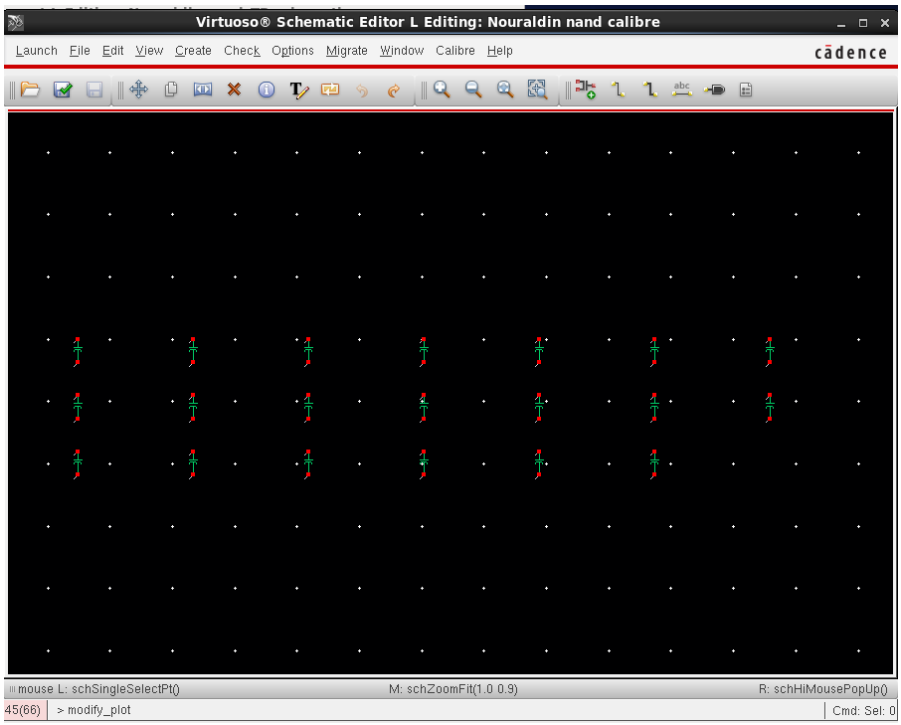


Figure 16: Parasitic Components

Post Layout Simulation

The delay, which is 3.535ps as seen in the following figure, is within the acceptable range.

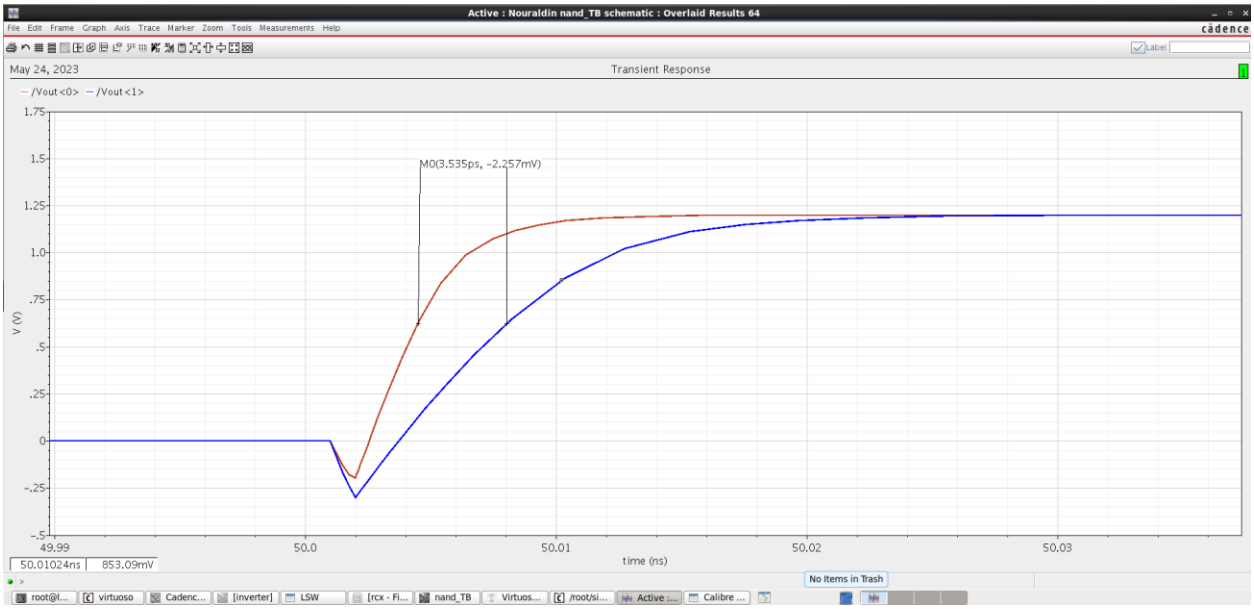


Figure 17: Post Layout Simulation Output

Conclusion:

In this report, we have presented the design process of an NAND gate using the Cadence tool. We have successfully completed the following steps:

- Defined the specifications of the NAND gate
- Created a schematic diagram of the NAND gate
- Tested the functionality and performance of the schematic design
- Designed a layout of the NAND gate
- Tested the layout design for any errors or violations
- Performed a post-layout simulation and verification

We have demonstrated that our design meets the requirements and specifications of an NAND gate. We have also learned how to use the Cadence tool for electronic design automation, and gained valuable experience and skills in digital circuit design. We have encountered some challenges and limitations during the design process, such as choosing the appropriate parameters, optimizing the layout area, and ensuring the reliability and robustness of the design. We have overcome these challenges by applying the relevant concepts, methods, and tools that we have learned in this course. We hope that this report has provided a clear and comprehensive overview of our design process and results.

Reference:

All the references are from the lab manual and from the Lecture by Dr. Ghazal Attia and Eng. Habiba Mohamed