Misr International University
Electronics and Communication Engineering
ECE 542 (VLSI Lab)
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Lab 3:
NOR Gate

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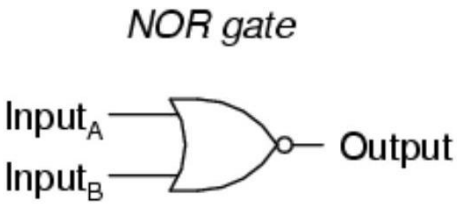
Aim:

The aim of this report is to explain the design process of a NOR gate using the Cadence tool. The design process consists of the following steps:

- Defining the specifications of the NOR gate
- Developing a behavioral model of the NOR gate
- Creating a schematic diagram of the NOR gate
- Testing the functionality and performance of the schematic design
- Designing a layout of the NOR gate
- Testing the layout design for any errors or violations
- Performing a post-layout simulation and verification

Introduction:

A NOR gate is a basic logic gate that produces an output that is 0 if any of its inputs is 1, and 1 otherwise. For example, if the inputs are 0 and 1, the output is 0, and if the inputs are 0 and 0, the output is 1. NOR gates are widely used in digital circuits and systems, such as computers, calculators, and communication devices. In this report, we will describe how we designed a NOR gate using the Cadence tool, which is a software platform for electronic design automation. We will explain the steps we followed to create a schematic diagram, a layout design, and a post-layout simulation of the NOR gate. We will also present the results of our testing and verification of the design and discuss the challenges and limitations we faced during the design process.



A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Figure 2: NOR Truth Table

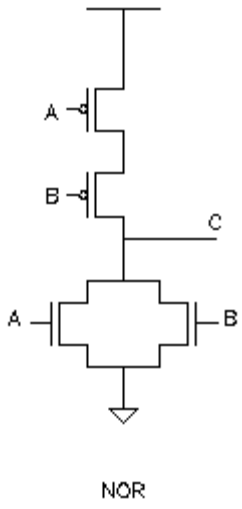


Figure 1: NOR Schematic

NOR Gate Schematic Design

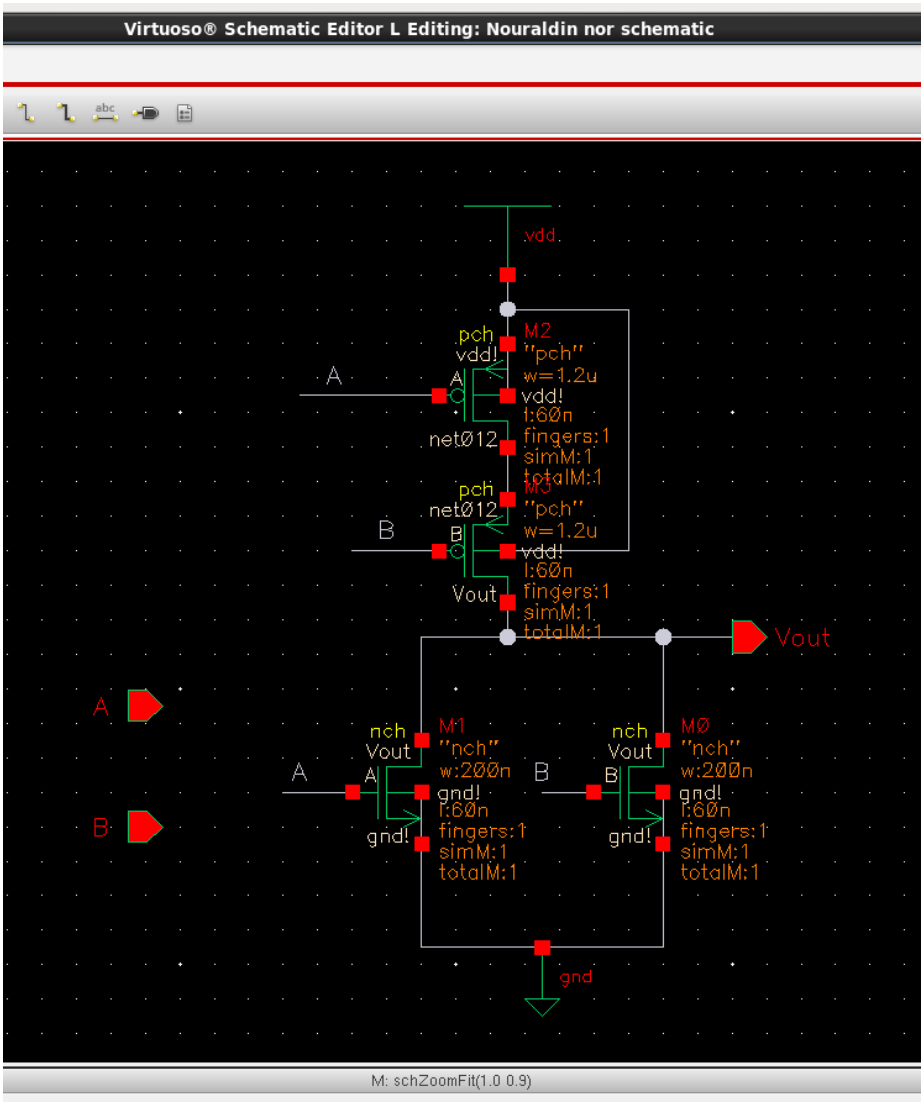


Figure 3: NOR Schematic

- The figure above shows the circuit schematic
- The circuit consists of:
  - Two PMOS transistors with L = 60nm and W = 1.2um
  - Two NMOS transistors with L = 60nm and W = 200nm
- The inputs A and B are connected to:
  - The gate terminals of one PMOS and one NMOS transistor each

NOR Gate Testbench

- We need to create a cell view

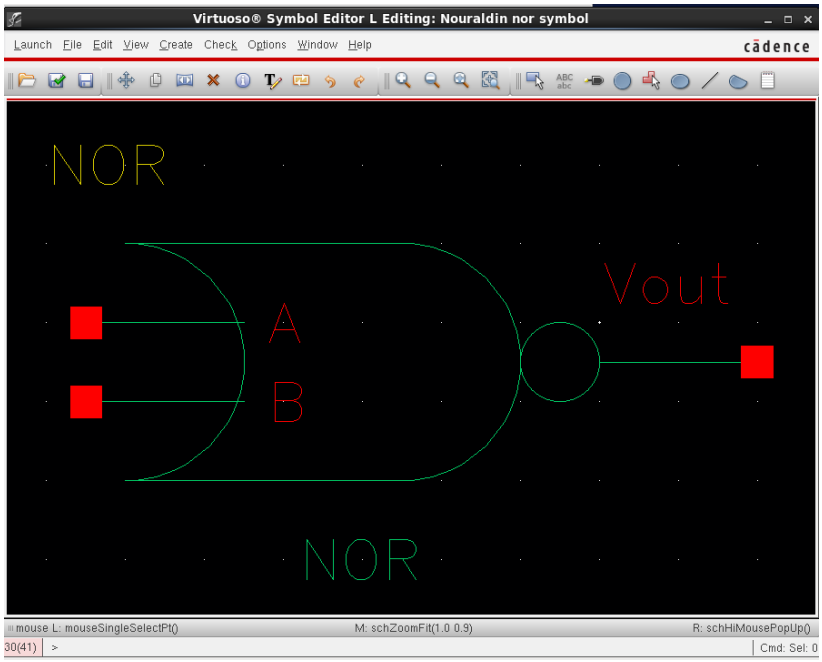


Figure 4: NOR Symbol

- Then we create a new cell called “NOR_TB_DC” for DC analysis and “NOR_TB_trans” for transient analysis.

Figure 5: files of NOR testbench

DC analysis

schematic:

We used a DC voltage source with value = vb as an input.

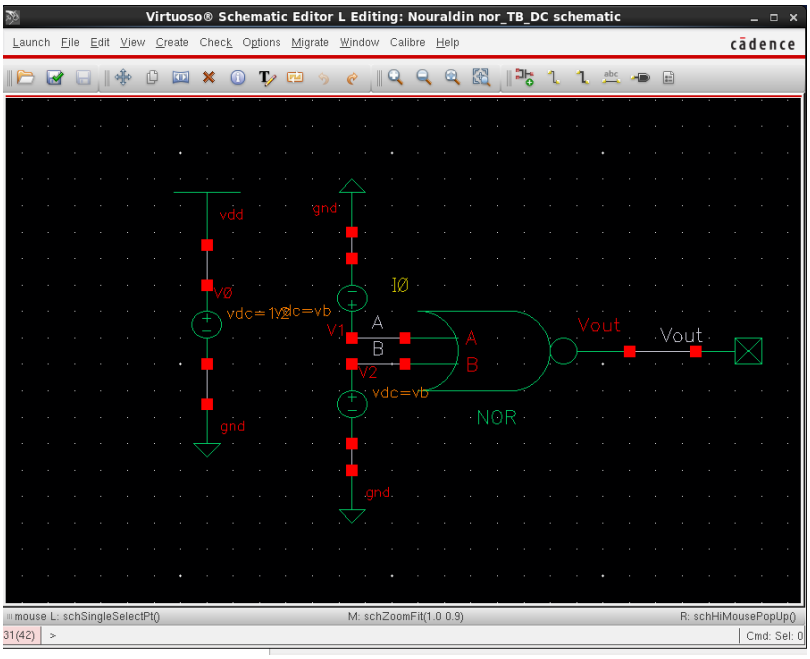


Figure 6: DC analysis Schematic

simulation Output:

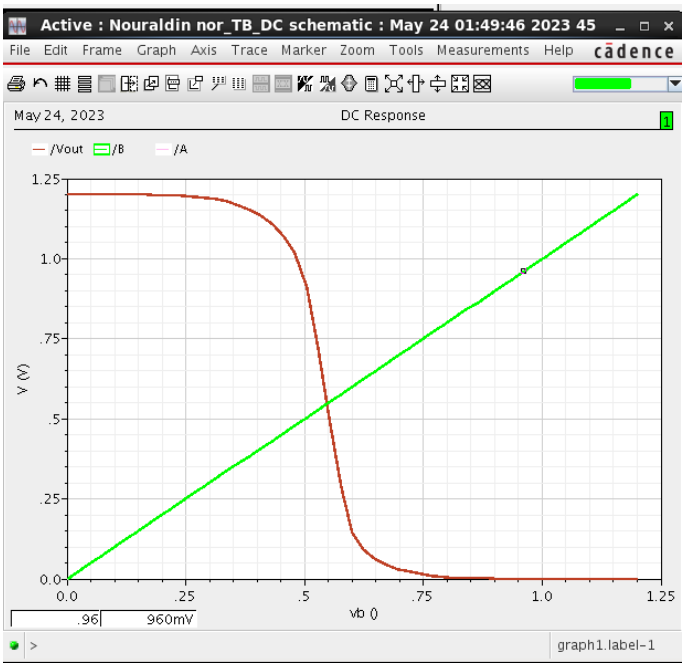


Figure 7: DC analysis Output

Transient Response analysis

schematic:

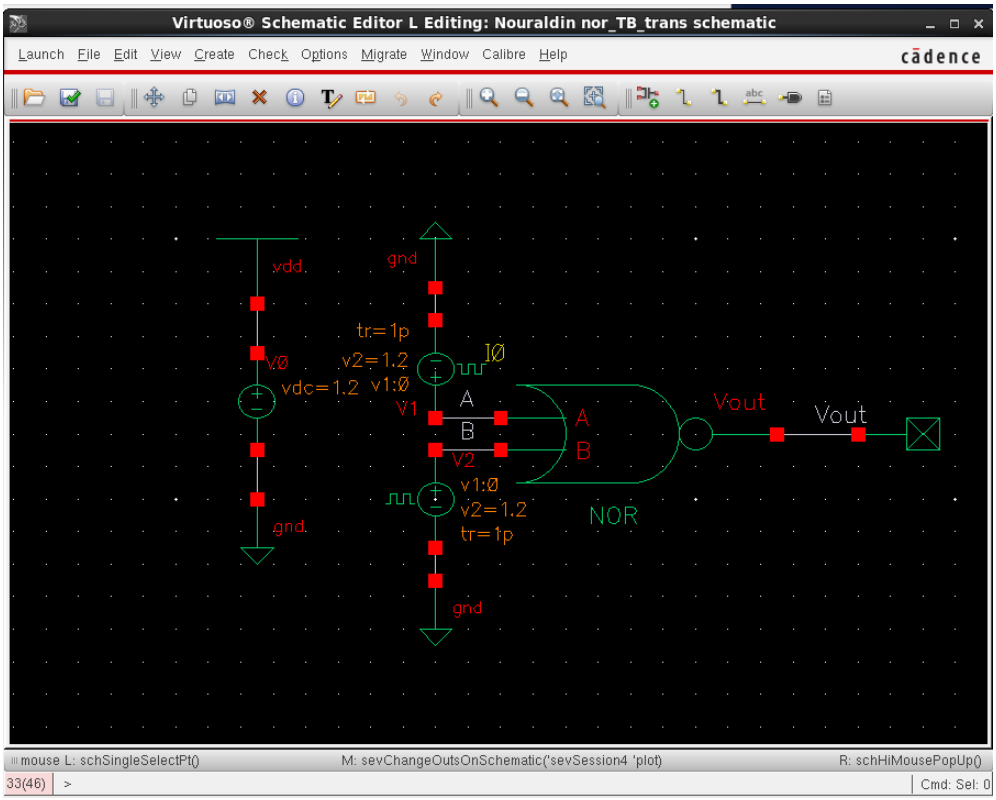


Figure 8: Transient Analysis Schematic

Vpulse voltage source was used to provide the input signal.

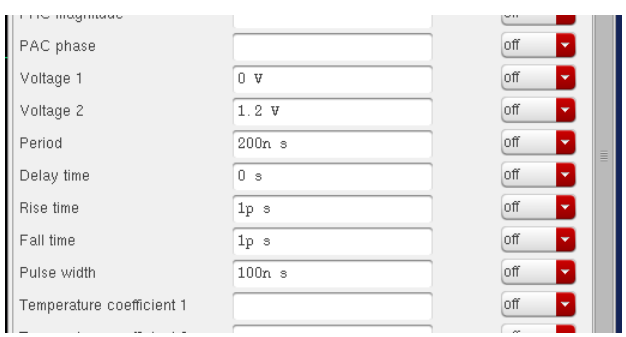


Figure 9: Vpulse 1

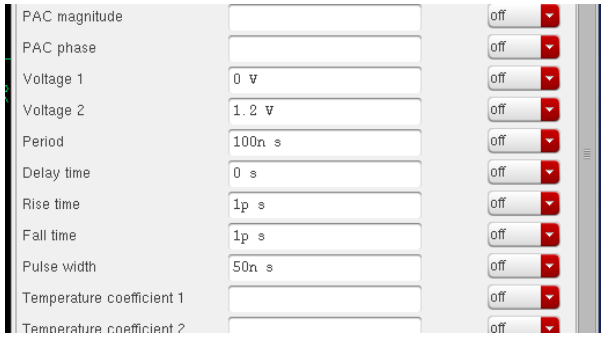


Figure 10: Vpulse 2

simulation Output:

The simulation shows that the output is 1 when Both A and B are 0, which confirms the correct functioning of the NOR.

Figure 11: Transient Analysis Simulation Output

NOR Gate Layout:

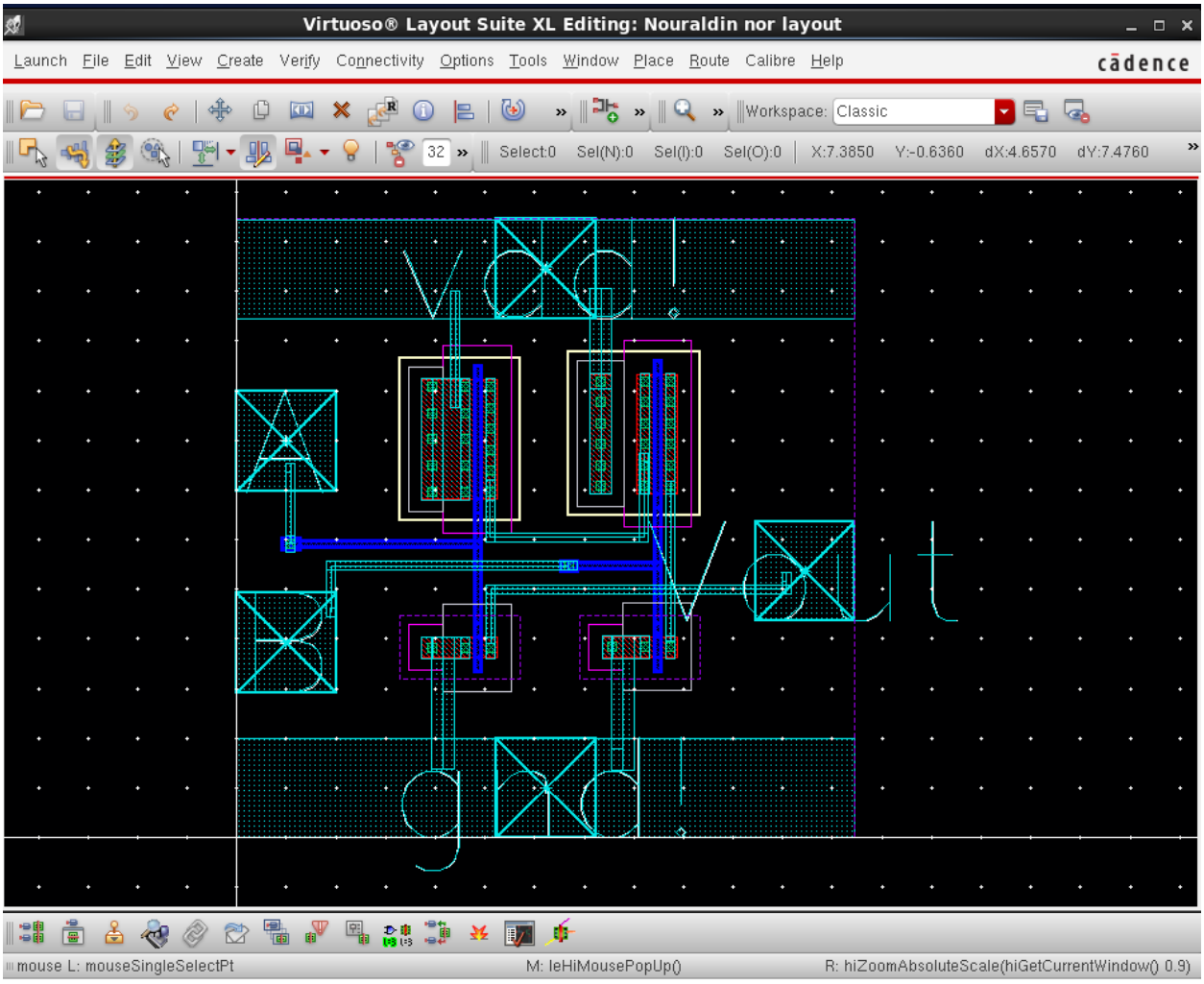


Figure 12: NOR Layout

Testing

Design Rule Check Simulation (DRC):

There is No Mx.S or A or W.

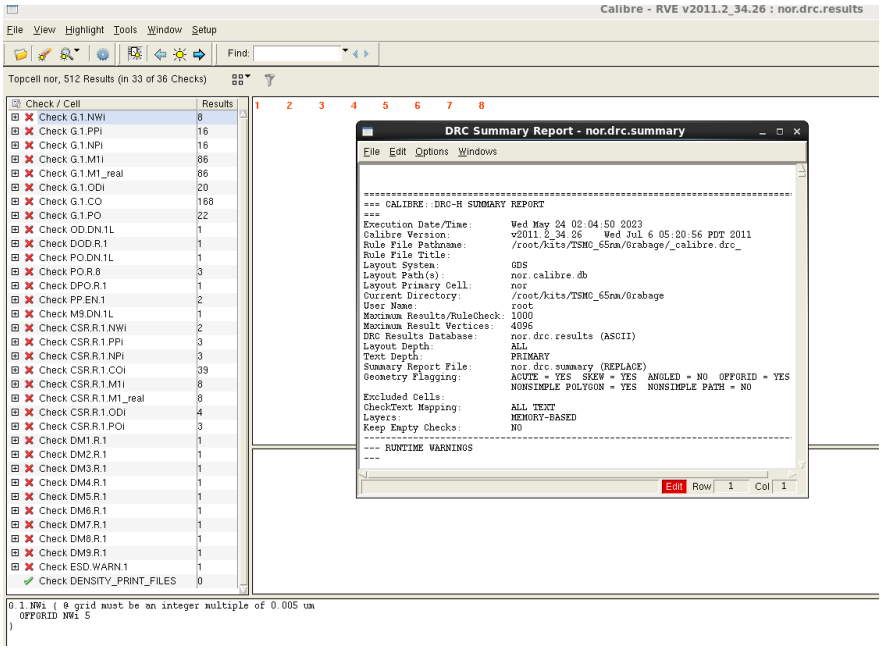


Figure 13: DRC

Layout Versus Schematic (LVS)

We have the smiley face 😊

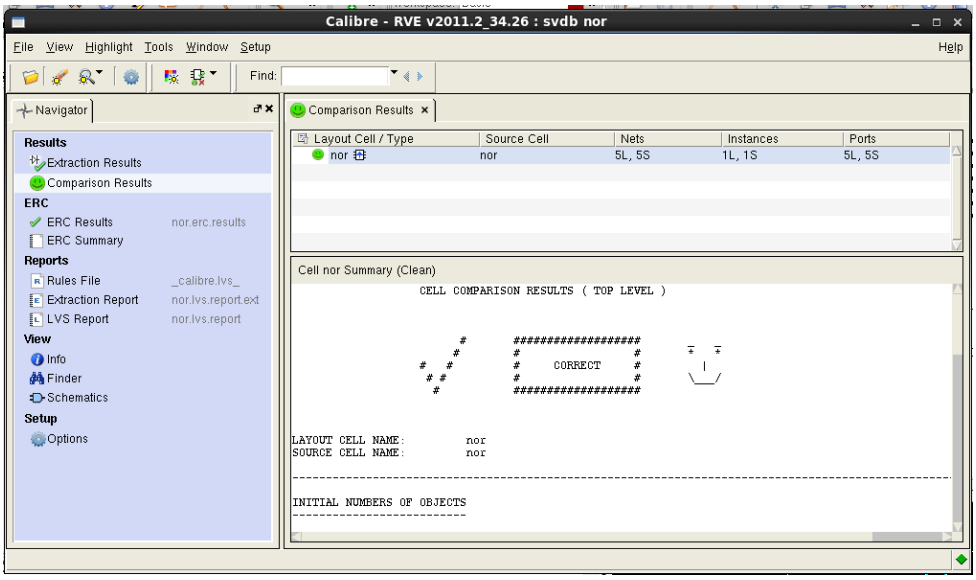


Figure 14: LVS

Parasitic Extraction (PEX)

Parasitic Extraction (PEX) is a process of calculating the unwanted effects of parasitic components, such as resistances, capacitances, and inductances, in an electronic circuit. PEX is used to create an accurate model of the circuit for simulation and verification purposes.

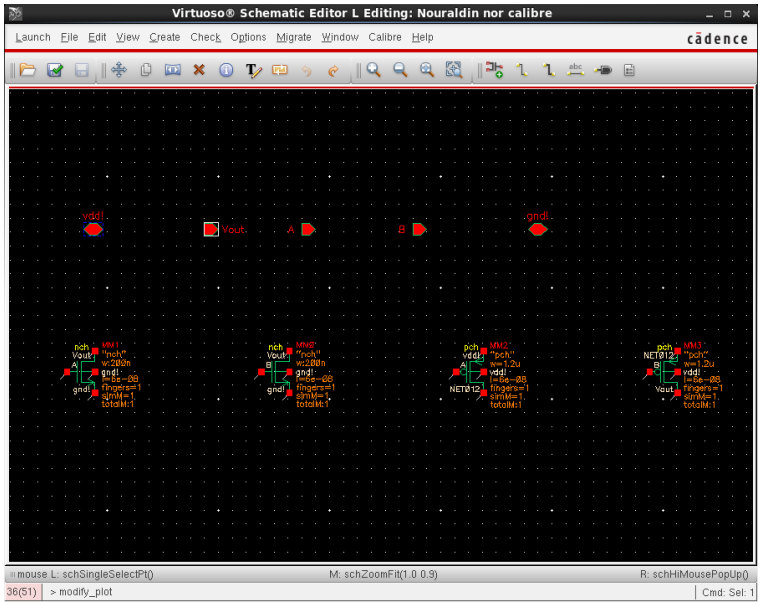


Figure 15

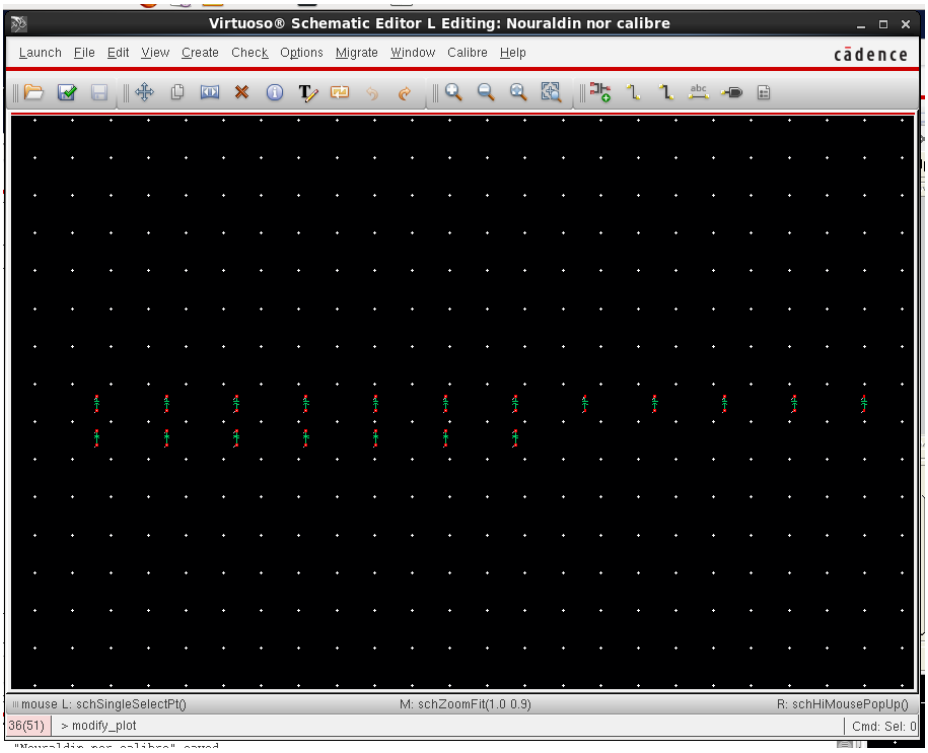


Figure 16: Parasitic Components

Post Layout Simulation

The delay, which is 4.281ps as seen in the following figure, is within the acceptable range.

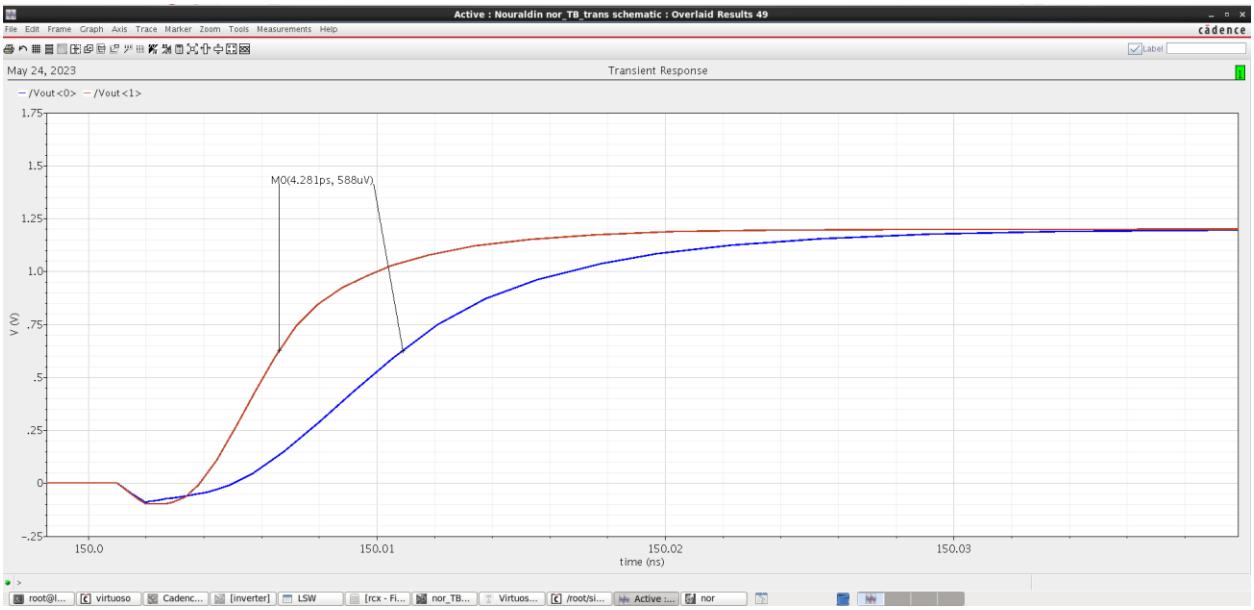


Figure 17: Post Layout Simulation Output

Conclusion:

In this report, we have presented the design process of an NOR gate using the Cadence tool. We have successfully completed the following steps:

- Defined the specifications of the NOR gate
- Created a schematic diagram of the NOR gate
- Tested the functionality and performance of the schematic design
- Designed a layout of the NOR gate
- Tested the layout design for any errors or violations
- Performed a post-layout simulation and verification

We have demonstrated that our design meets the requirements and specifications of an NOR gate. We have also learned how to use the Cadence tool for electronic design automation, and gained valuable experience and skills in digital circuit design. We have encountered some challenges and limitations during the design process, such as choosing the appropriate parameters, optimizing the layout area, and ensuring the reliability and robustness of the design. We have overcome these challenges by applying the relevant concepts, methods, and tools that we have learned in this course. We hope that this report has provided a clear and comprehensive overview of our design process and results.

Reference:

All the references are from the lab manual and from the Lecture by Dr. Ghazal Attia and Eng. Habiba Mohamed