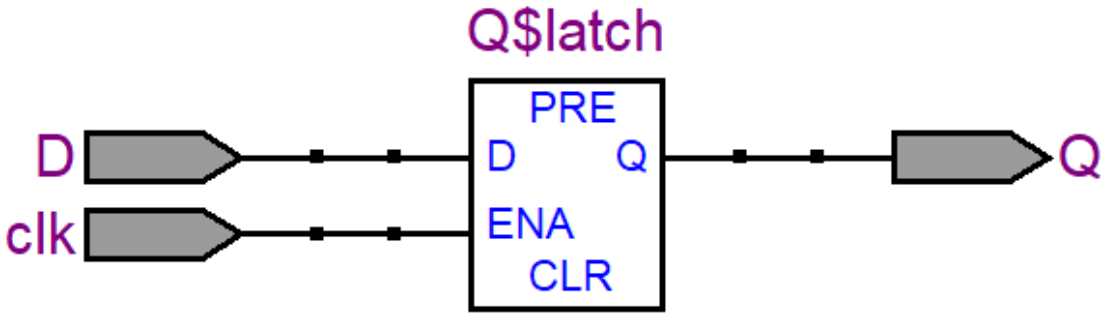
Tutorial 7

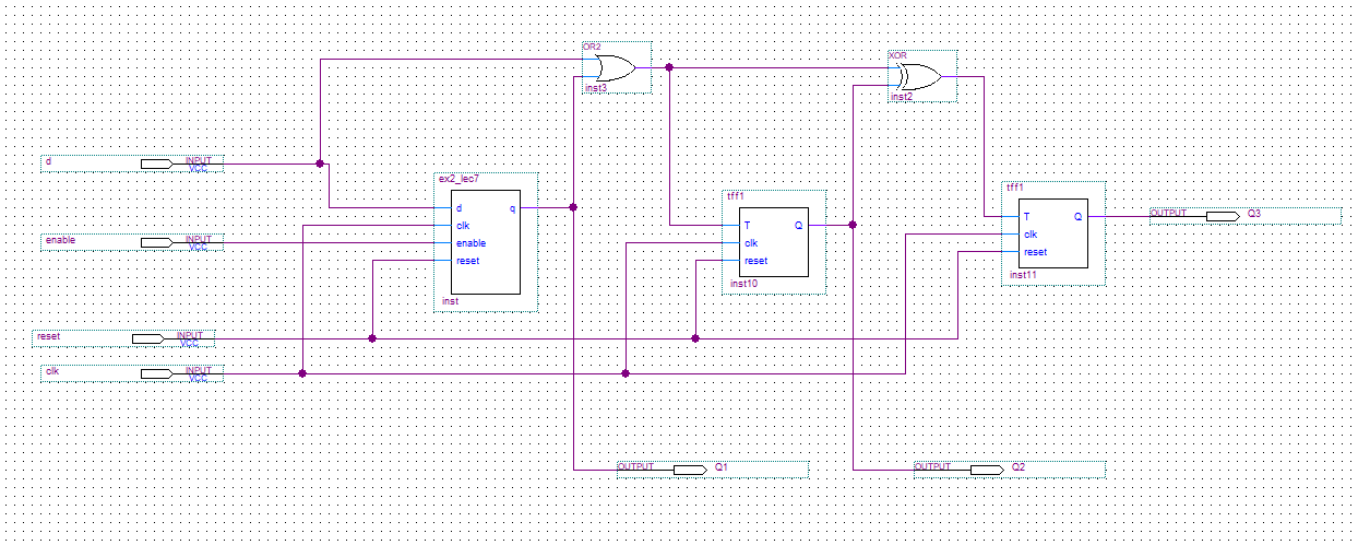
Name: Nour-aldin Ibrahim Ahmed Elbadawy
ID: 2018-13394

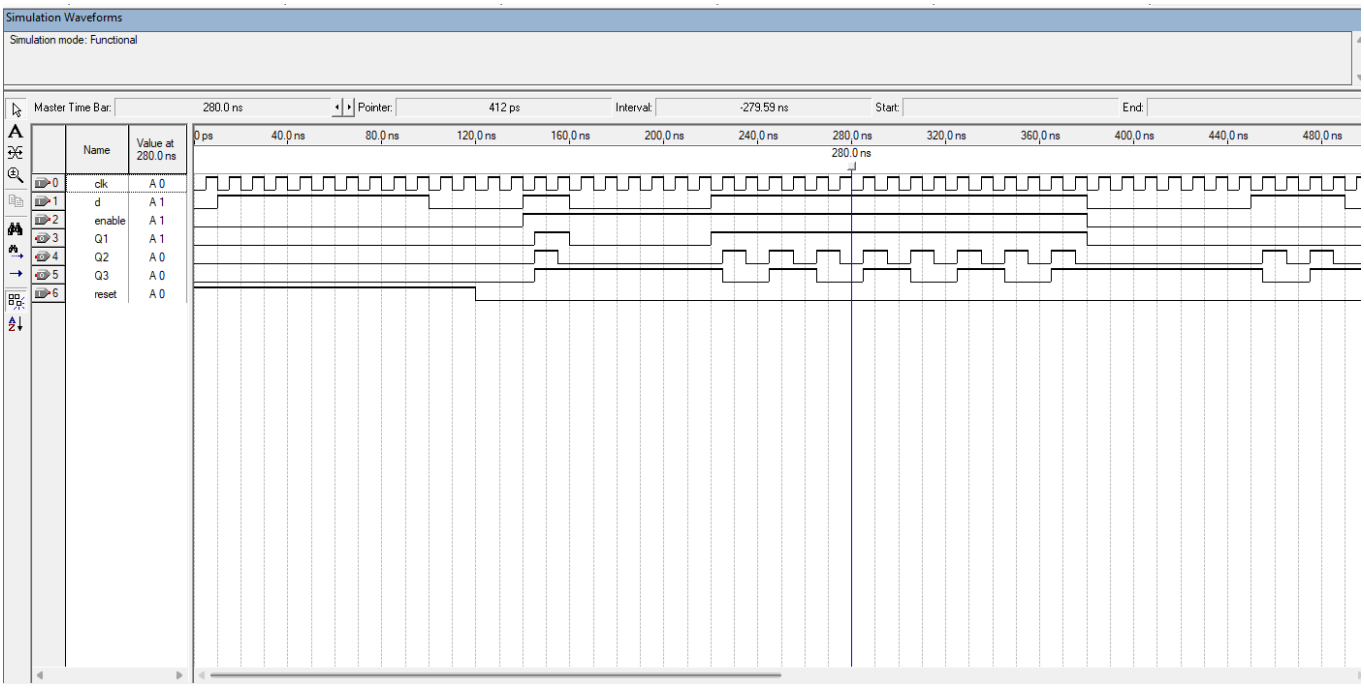
Q4)

```
library ieee;
use ieee.std_logic_1164.all;

entity D_latch is
        port(
                        D,clk :in std_logic;
                        Q: out std_logic
                );
end entity;

architecture behave of D_latch is

begin

        Process(clk, D)
        begin
                if (CLK = '1') then
                        Q <= D ;
                end if;
        end Process;

end behave;
```


Q$latch
PRE
D
Q
ENA
CLR
D
clk
Q

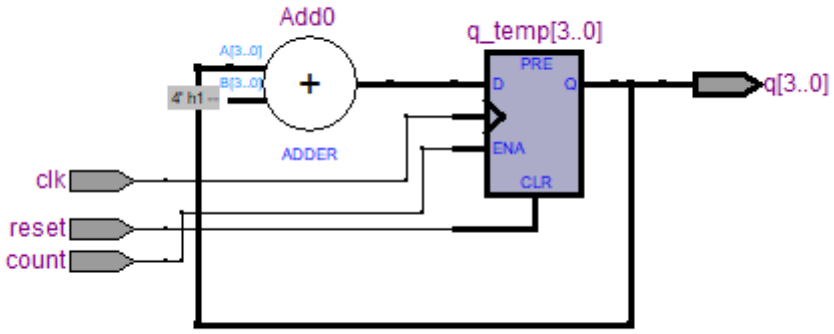
Q5)

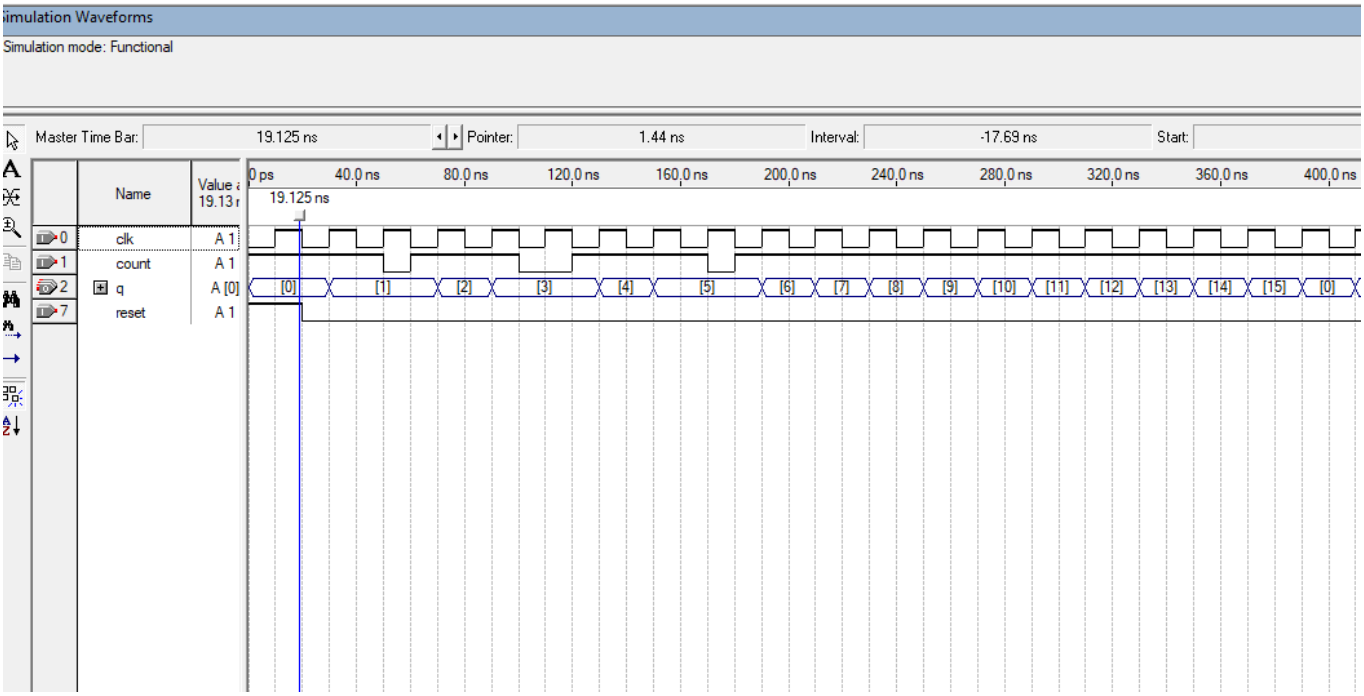

OR2
inst3
XOR
inst2
d
INPUT
enable
INPUT
reset
INPUT
clk
INPUT
ex2_lec7
d
q
clk
enable
reset
inst
tff1
T
Q
clk
reset
inst10
tff1
T
Q
clk
reset
inst11
OUTPUT
Q3
OUTPUT
Q1
OUTPUT
Q2


Simulation Waveforms
Simulation mode: Functional
Master Time Bar:
280.0 ns
Pointer:
412 ps
Interval:
-279.59 ns
Start:
End:
Name
Value at 280.0 ns
0 clk A 0
1 d A 1
2 enable A 1
3 Q1 A 1
4 Q2 A 0
5 Q3 A 0
6 reset A 0
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns
240.0 ns
280.0 ns
320.0 ns
360.0 ns
400.0 ns
440.0 ns
480.0 ns
280.0 ns

Q6)

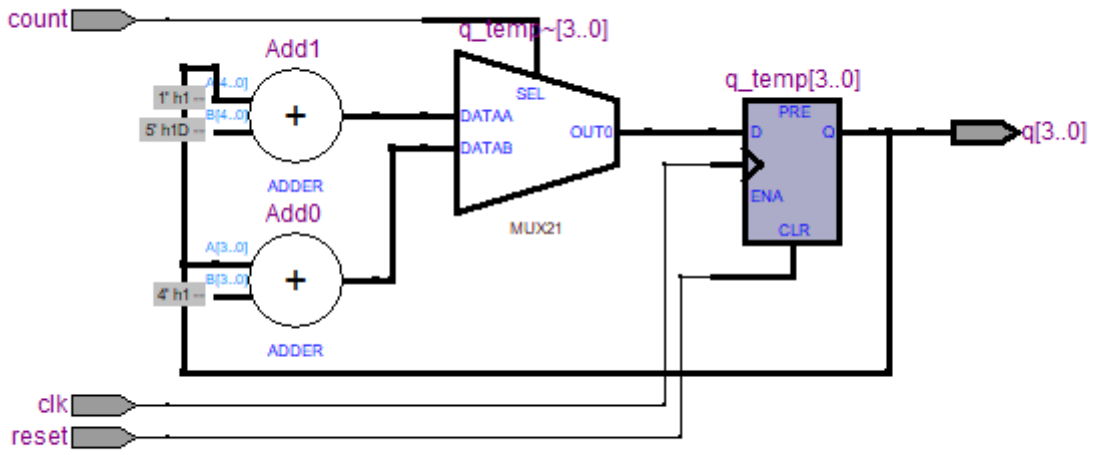
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;


entity mycounter is

        generic( n: natural:=4);

        port
        (
                clk, count, reset: in std_logic;
                q : out std_logic_vector(n-1 downto 0 ) );

end mycounter;

architecture behave of mycounter is
        signal q_temp : std_logic_vector( n-1 downto 0);
begin

        process(clk,count,reset)
        begin
                if(reset='1') then
                        q_temp <= (others => '0');

                elsif (rising_edge(clk)) then
                        if (count='1') then
                                q_temp <= q_temp + 1;
                        end if;
                end if;

        end process;

        q <= q_temp;

end behave;
```

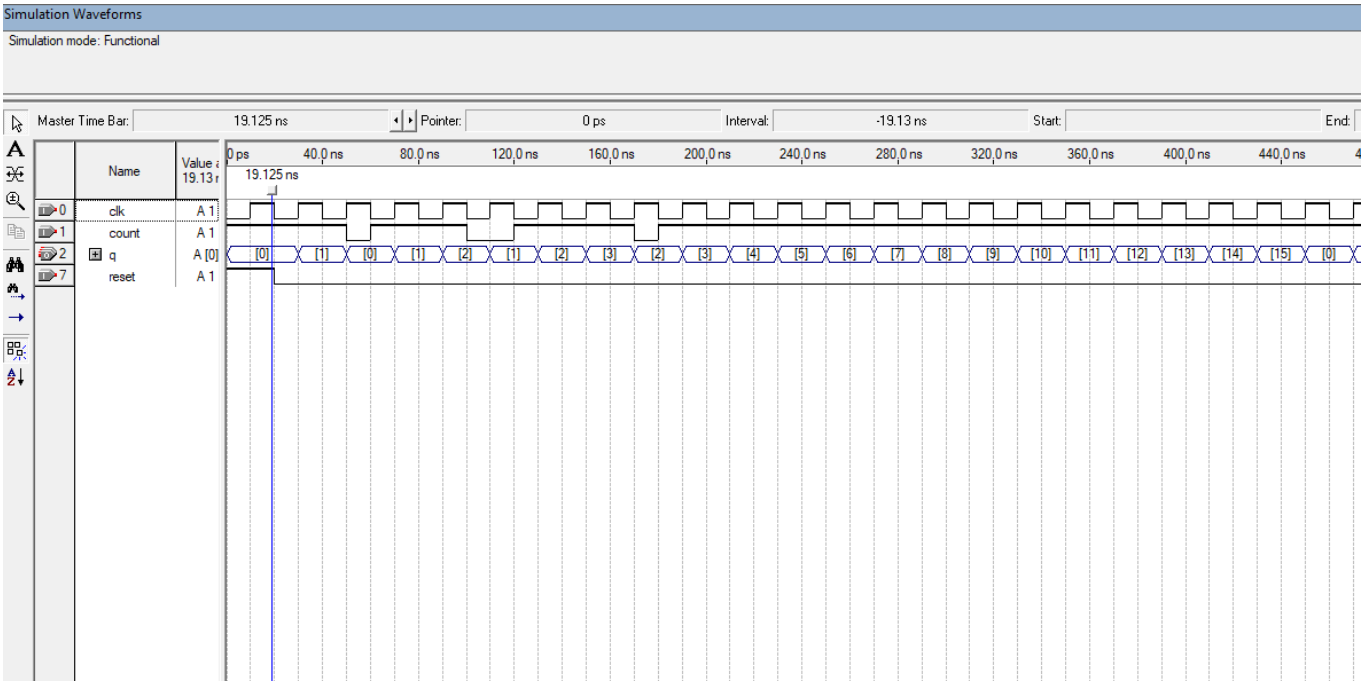

Add0
A[3..0]
B[3..0]
4' h1
ADDER
q_temp[3..0]
PRE
D
Q
ENA
CLR
q[3..0]
clk
reset
count


Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 19.125 ns
Pointer: 1.44 ns
Interval: -17.69 ns
Start:
Name
Value
clk
count
q
reset
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns
240.0 ns
280.0 ns
320.0 ns
360.0 ns
400.0 ns
19.125 ns

Q7)

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;


entity mycounter is

        generic( n: natural:=4);

        port
        (
                clk, count, reset: in std_logic;
                q : out std_logic_vector(n-1 downto 0 ) );

end mycounter;

architecture behave of mycounter is
        signal q_temp : std_logic_vector( n-1 downto 0);
begin

        process(clk,count,reset)
        begin
                if(reset='1') then
                        q_temp <= (others => '0');

                elsif (rising_edge(clk)) then
                        if (count='1') then
                                q_temp <= q_temp + 1;
                        else
                                q_temp <= q_temp - 1;
                        end if;
                end if;

        end process;

        q <= q_temp;

end behave;
```


count
Add1
A[4..0]
1' h1
B[4..0]
5' h1D
ADDER
Add0
A[3..0]
B[3..0]
4' h1
ADDER
q_temp~[3..0]
SEL
DATAA
DATAB
OUT0
MUX21
q_temp[3..0]
PRE
D
Q
ENA
CLR
q[3..0]
clk
reset


Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 19.125 ns
Pointer: 0 ps
Interval: -19.13 ns
Start:
End:
Name
Value at 19.13 ns
0 clk A 1
1 count A 1
2 q A [0]
7 reset A 1
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns
240.0 ns
280.0 ns
320.0 ns
360.0 ns
400.0 ns
440.0 ns
19.125 ns
[0] [1] [0] [1] [2] [1] [2] [3] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [0]