Assignment 3

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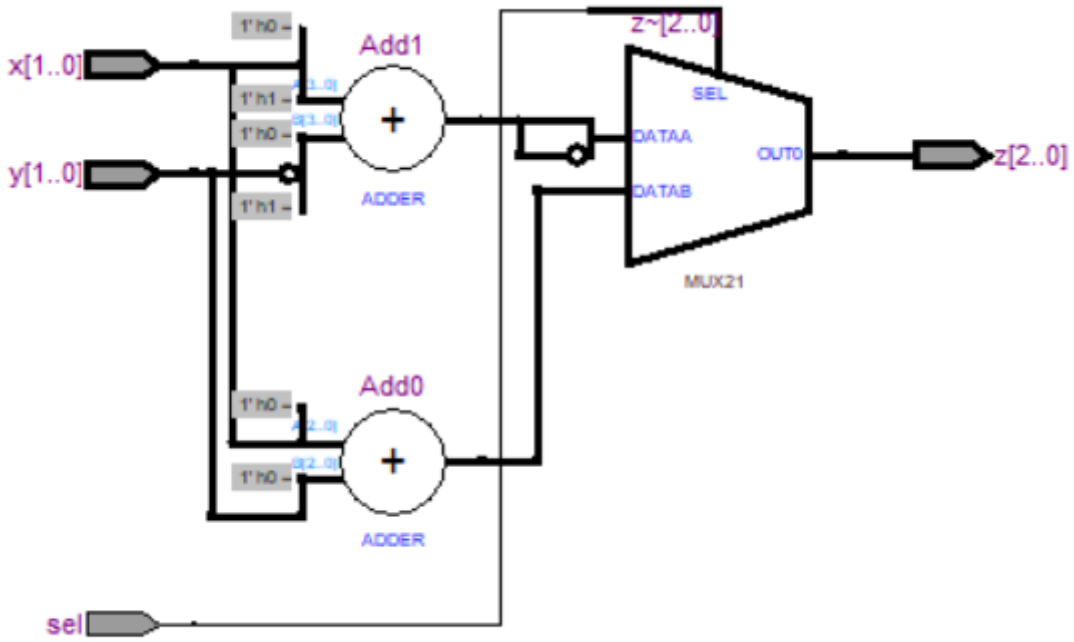
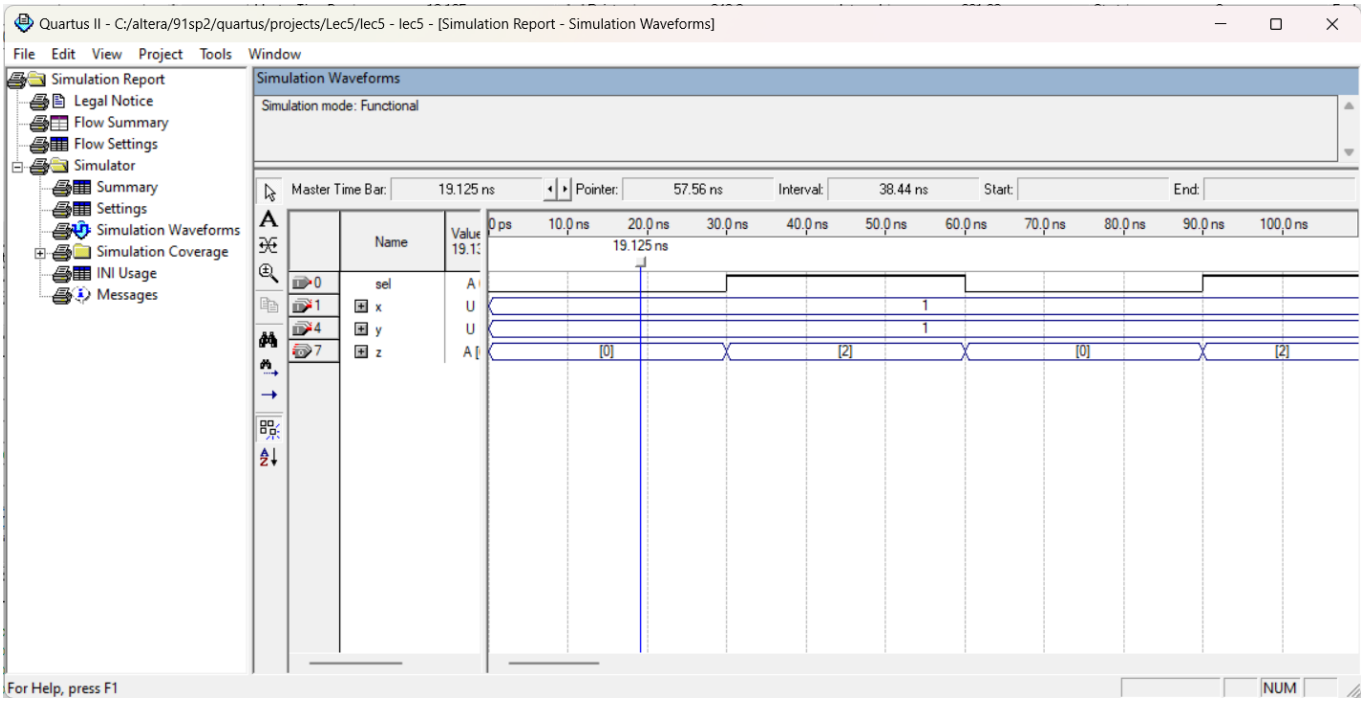
Main Code

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity lec5 is
port(
          x,y : in integer range 0 to 2;

          z : out integer range 0 to 4;
          sel : in std_logic
          );
end lec5;
architecture behave of lec5 is
begin
        process (x,y,sel)
                begin
                        if(sel = '1') then z <= x+y;
                        else z<= x-y;
                        end if;
        end process;
end behave;
```

RTL



Waveform Simulation



Analysis

when the selection line = 0, multiplexer select the subtraction as Output
while in case that selection line = 1, multiplexer select the Addition as Output
and this shown in the waveform simulation above