Sheet 3

Question 1:

Write a VHDL code for a 1 x 4 **Demultiplexer, illustrate graphically how to use it to implement a** 1 x 16 **Demux, then write structural VHDL code to describe the proposed implementation.**

Question 2:

Write a test bench VHDL code for the circuit diagram shown in figure 1 such that the inputs are set as depicted in figure 2. Then draw the corresponding output.

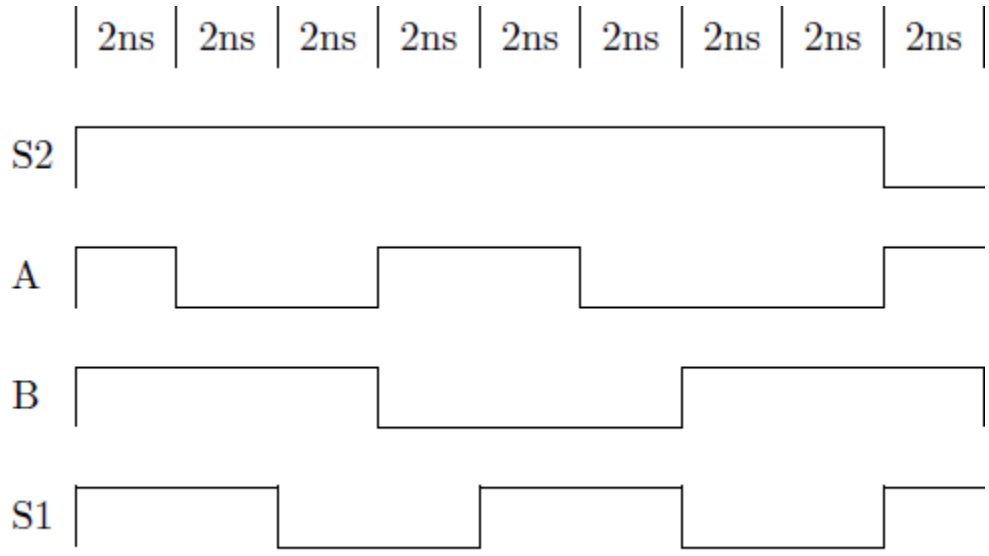
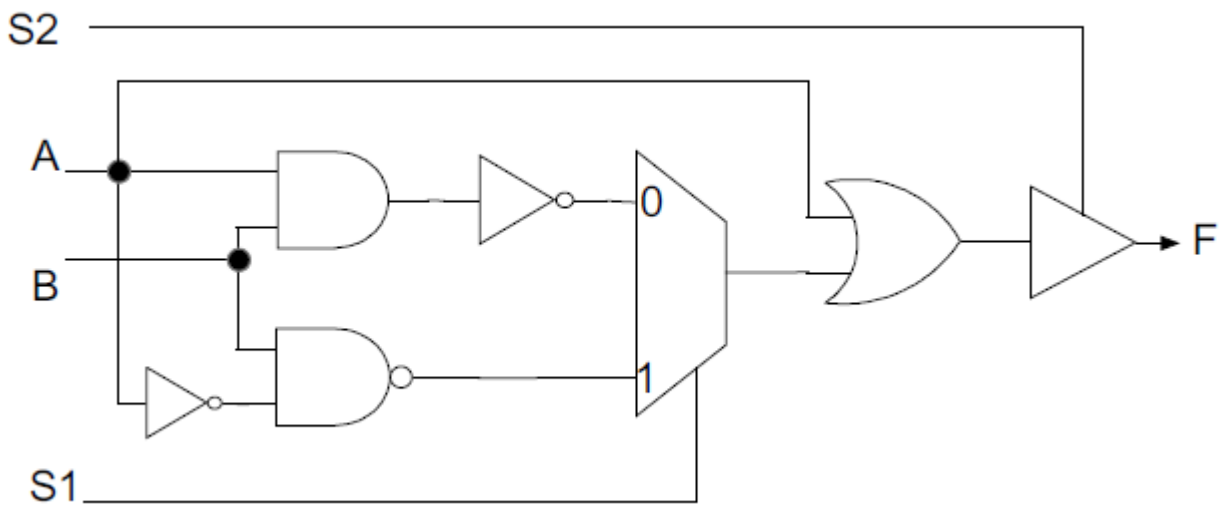
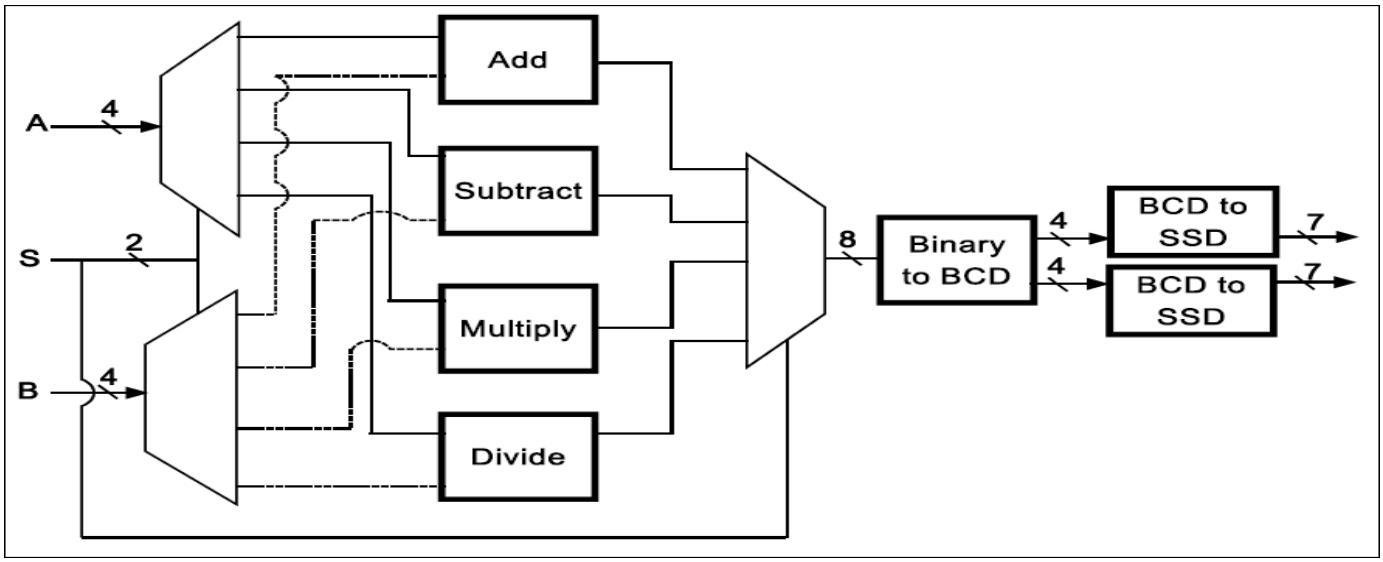


Figure 2: Timing Diagram



Question 3:

Write the Structural VHDL code for the Whole system in figure.

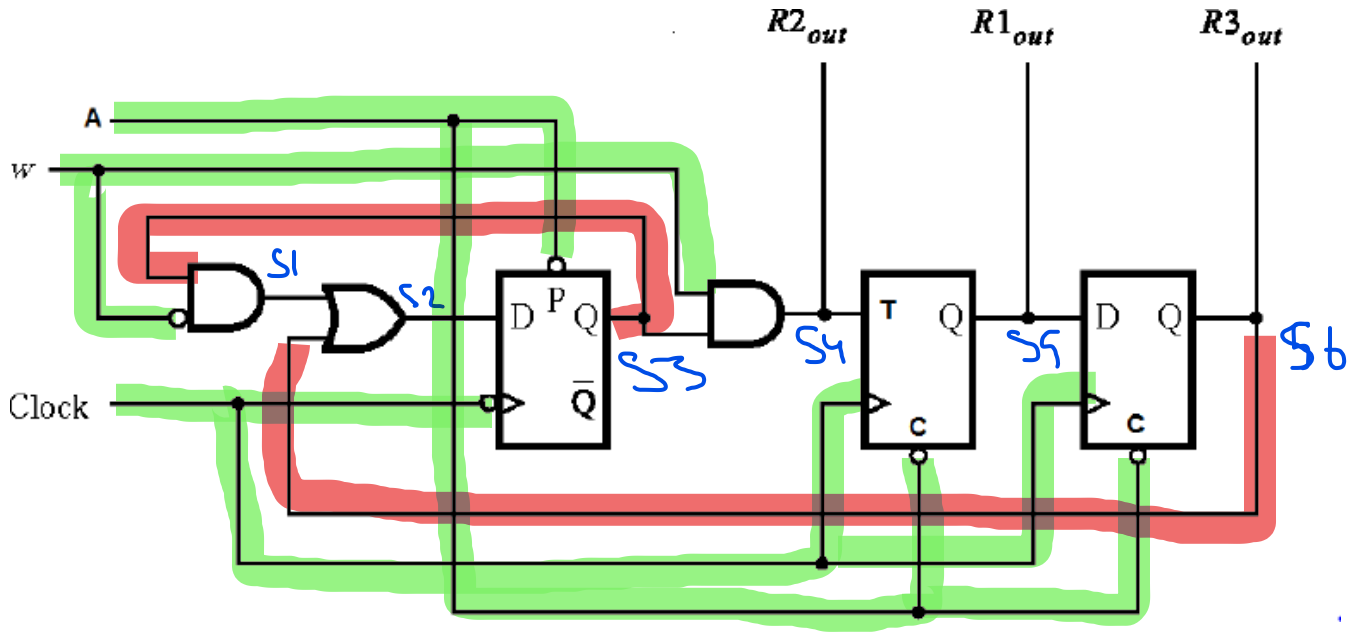


Question 4:

Design a 6-bit Digital addition/subtraction module that accepts two (6 bits) inputs and results in either their sum or difference according to an input selector.

Question 5: (Assignment)

Consider the circuit diagram shown in figure:



1. Write the Behavioral VHDL code for the circuit shown.
2. Rewrite the Structural VHDL code for the same circuit.