Tutorial 5

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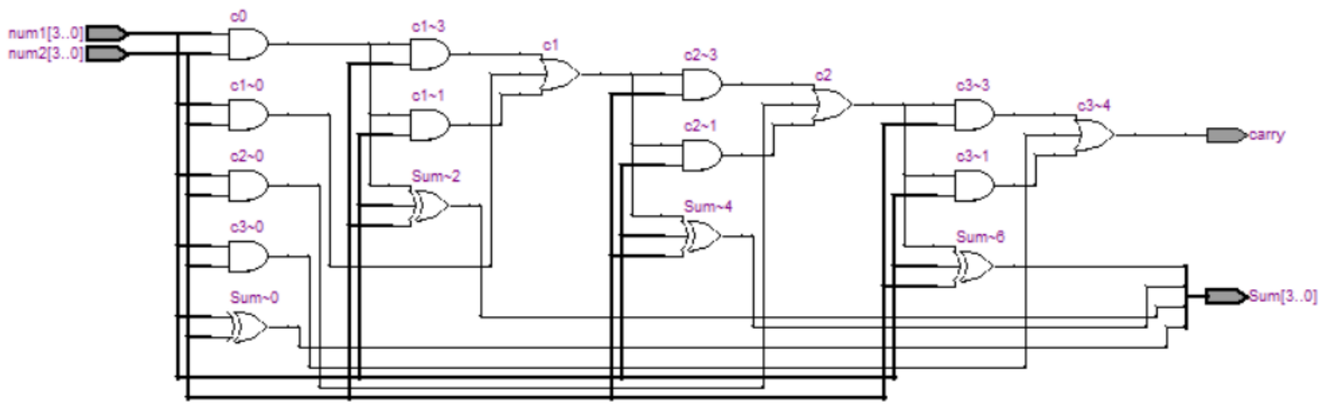
full adder

code

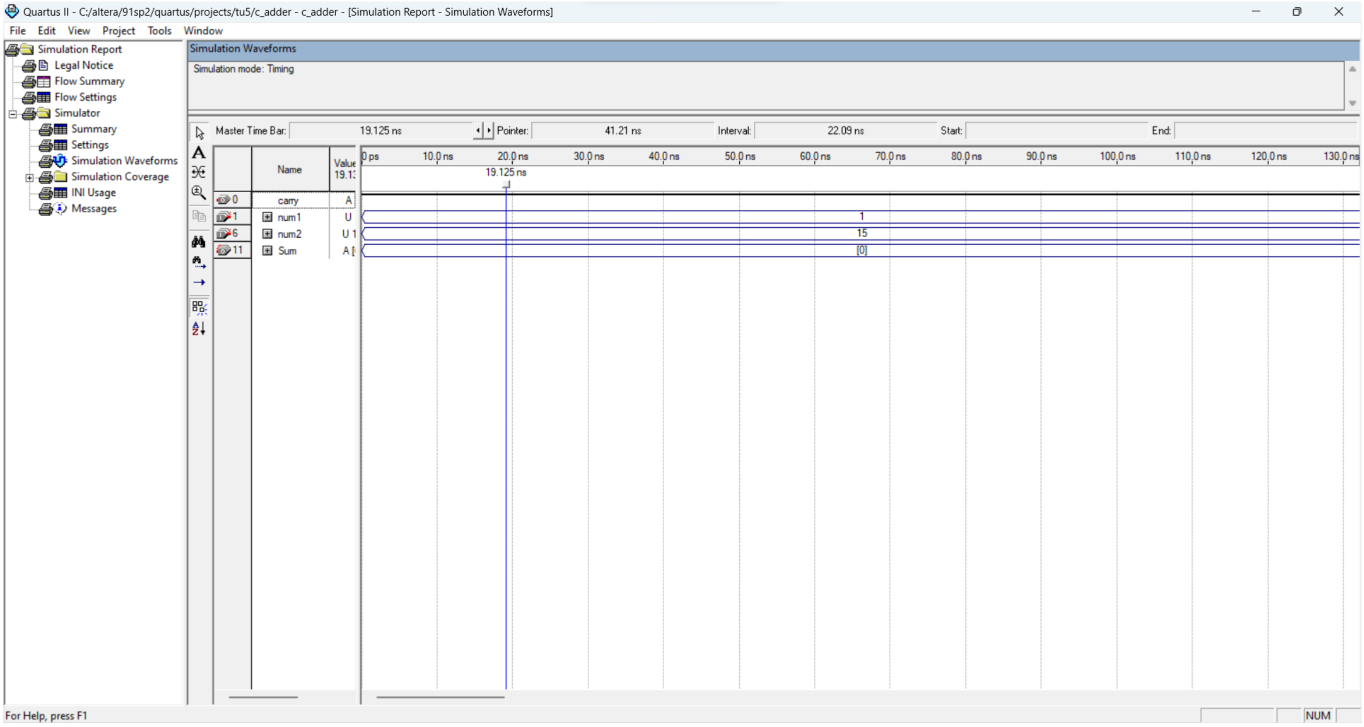
```
-- Full Adder in VHDL
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity c_adder is
    Port ( num1 : in  STD_LOGIC_vector(3 downto 0);
           num2 : in  STD_LOGIC_vector(3 downto 0);
           Sum : out  STD_LOGIC_vector(3 downto 0);
           carry : out  STD_LOGIC);
end c_adder;

architecture Behavioral of c_adder is

signal c0,c1,c2,c3 : std_logic := '0';

begin
    -- first full adder
    Sum(0) <= num1(0) XOR num2(0); --sum calculation
    c0 <= num1(0) and num2(0); --carry calculation

    -- second full adder
    Sum(1) <= num1(1) XOR num2(1) XOR c0; --sum calculation
    c1 <= (num1(1) and num2(1) ) or (num1(1) and c0) or ( num2(1) and c0); --carry calculation

    -- third full adder
    Sum(2) <= num1(2) XOR num2(2) XOR c1; --sum calculation
    c2 <= (num1(2) and num2(2) ) or (num1(2) and c1) or ( num2(2) and c1); --carry calculation

    -- fourth full adder
    Sum(3) <= num1(3) XOR num2(3) XOR c2; --sum calculation
    c3 <= (num1(3) and num2(3) ) or (num1(3) and c2) or ( num2(3) and c2); --carry
```

```
calculation

    -- final carry assignment
    Carry <= c3;

end Behavioral;
```

RTL



Waveform



Simulation Waveforms

Simulation mode: Timing

Master Time Bar: 19.125 ns Pointer: 41.21 ns Interval: 22.09 ns Start: End:

	Name	Value 19.1:	Waveform
0	carry	A	
1	num1	U	1
6	num2	U 1	15
11	Sum	A [	[0]

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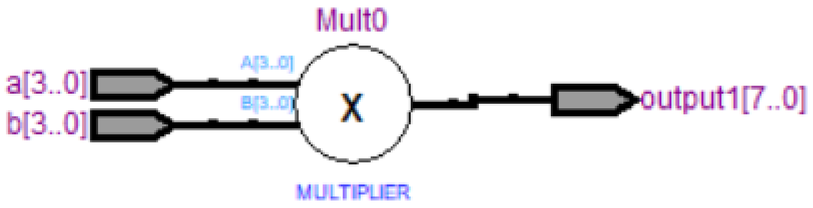
-
-
-
-

Multiplication

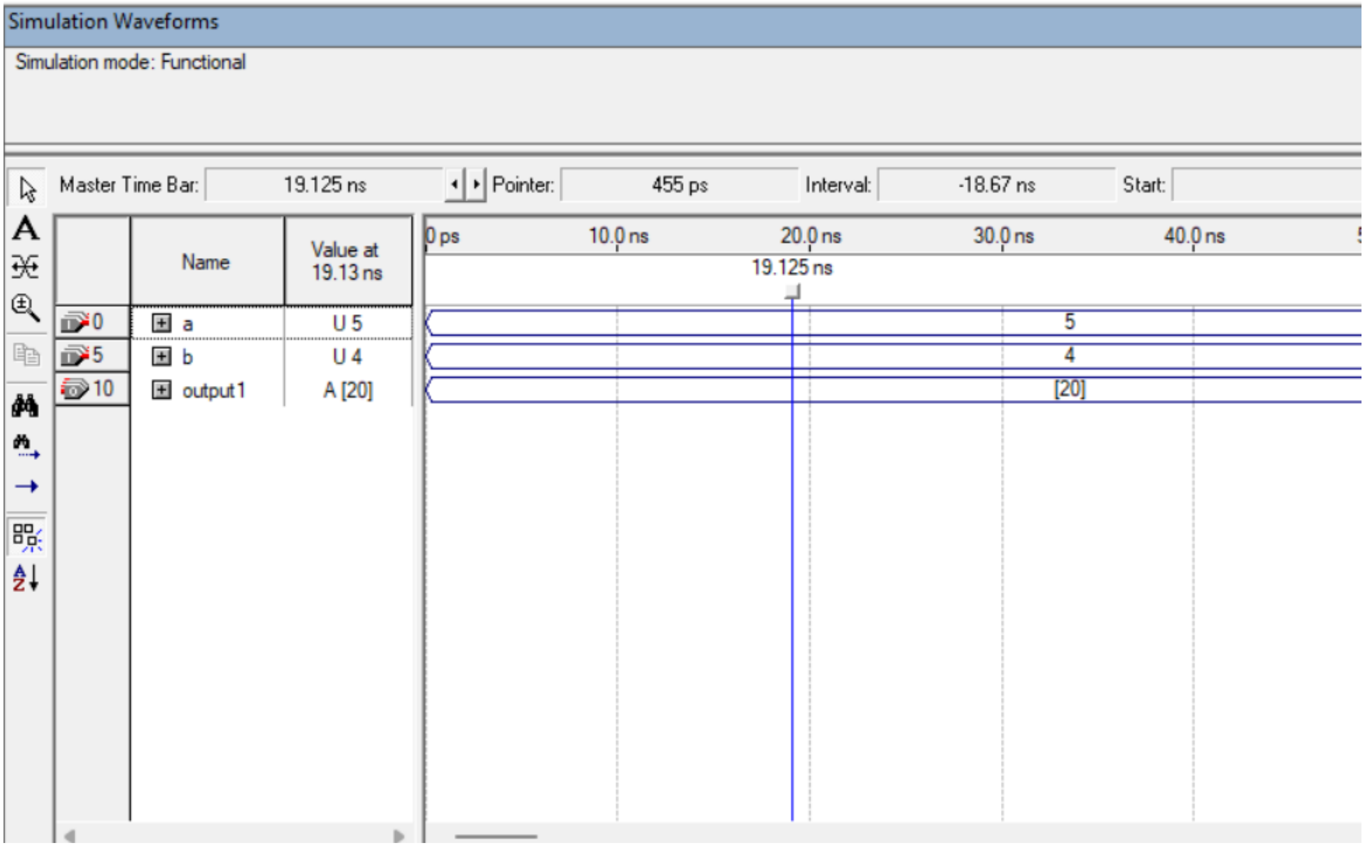
code

```
-- Multipilcation in VHDL

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;


entity multi is
    Port ( a : in  STD_LOGIC_vector(3 downto 0);
           b : in  STD_LOGIC_vector(3 downto 0);
           output1 : out  STD_LOGIC_vector(7 downto 0)
           );
end multi;

architecture Behavioral of multi is

signal ua: unsigned ( 3 downto 0);
signal ub: unsigned ( 3 downto 0);
signal uc: unsigned ( 7 downto 0);

begin

        --unsigned multiplication
    ua <= unsigned(a);
    ub <= unsigned(b);
    uc <= ua * ub;
    output1 <= std_logic_vector(uc);

end Behavioral;
```

RTL



Waveform



Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 19.125 ns Pointer: 455 ps Interval: -18.67 ns Start:

	Name	Value at 19.13 ns
0	a	U 5
5	b	U 4
10	output1	A [20]