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Interrupt Control in the ISP116x

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Application Note
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Note: ISP116x denotes the ISP1161, the ISP1161A, the ISP1161A1 and the ISP1160. The ISP1161, the ISP1161A, and the ISP1161A1 are single-chip Universal Serial Bus Host and Device Controllers, and the ISP1160 is a Universal Serial Bus Host Controller.

Revision History:

Version	Date	Descriptions	Author
1.0	Aug 2002	First draft	Alvin Lim and Chee Yu

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1. Introduction

This application note explains the behavior of the interrupt logic in the Host Controller and the Device Controller of ISP116x.

Note: Section 3 "Interrupt Controller in the Device Controller" does not apply to the ISP1160.

2. Interrupt Control in the Host Controller

2.1. Registers

The following registers are used to control interrupt generation in the ISP116x Host Controller:

- HcInterruptStatus
- HcμPInterrupt
- HcInterruptEnable
- HcInterruptDisable
- HcμPInterruptEnable.

2.1.1. Occurrence Recording Registers

The registers under this category are:

- HcInterruptStatus
- HcμPInterrupt.

These two registers are used to record the occurrence of any interrupt event (such as, SOF and EOT). This function cannot be disabled by any register setting; that is, these two registers will *always* record the occurrence of any interrupt event.

2.1.2. Interrupt Generation Control Registers

The interrupt generation control registers are:

- HcInterruptEnable
- HcInterruptDisable
- HcμPInterruptEnable.

These three registers determine whether logic 1 in the HcInterruptStatus or HcμPInterrupt register will cause the INT1[1] pin to be asserted.

[1] This is the INT pin in the ISP1160.

2.1.3. HcHardwareConfiguration Register

The following three bits in the HcHardwareConfiguration register are used to configure interrupt generation:

- Bit 0 InterruptPinEnable
- Bit 1 InterruptPinTrigger
- Bit 2 InterruptOutputPolarity.

2.2. Logical Connection

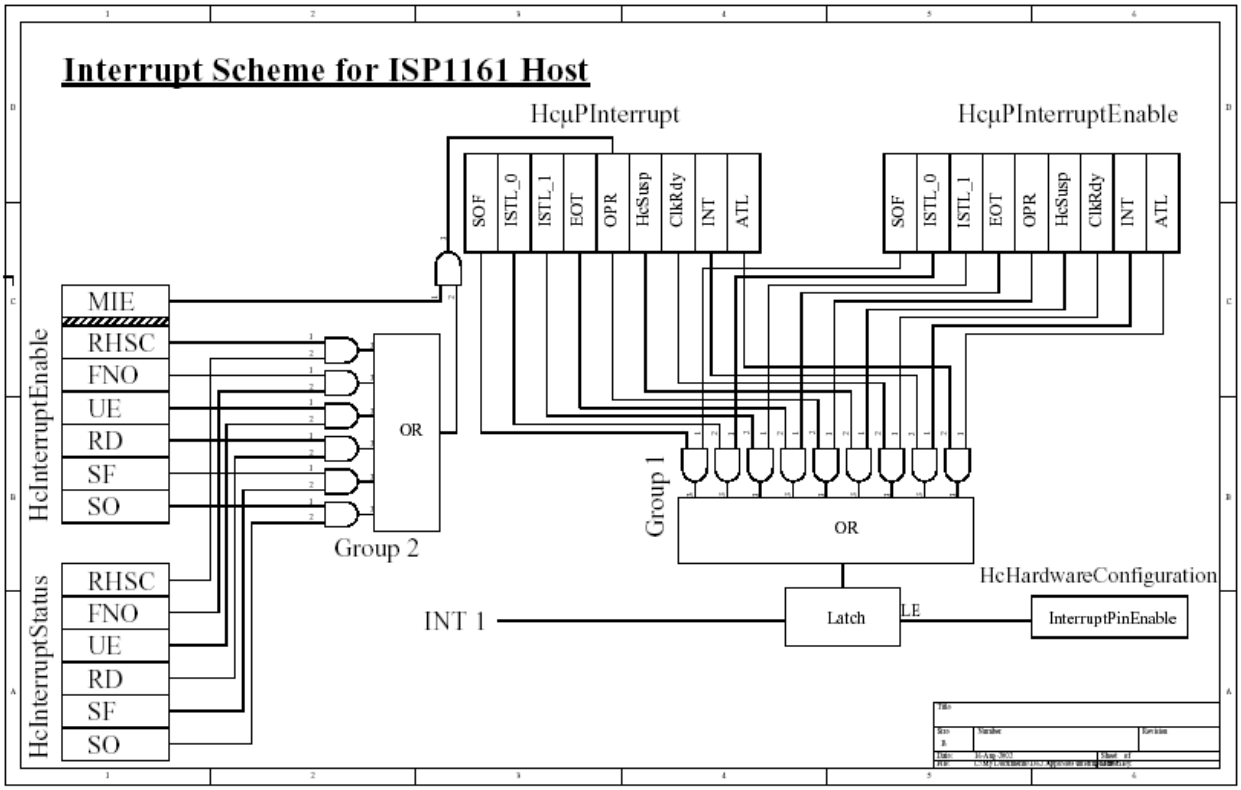

Figure 2-1: Logical Connection of the ISP116x INT1

There are two groups of interrupts, represented as Group 1 and Group 2 in Figure 2-1. A pair of registers controls each group.

Group 2 contains six possible interrupt events (recorded in the HcInterruptStatus register). On occurrence of any of these events, the corresponding bit would be set to logic 1; and if the corresponding bit in the HcInterruptEnable register is also logic 1, the 6-input OR gate would output logic 1. This output is ANDed with the value of MIE (bit 31 of HcInterruptEnable). Logic 1 at the AND gate would cause the OPR bit in the HcμPInterrupt register to be set to logic 1.

Group 1 contains 10 possible interrupt events, one of which is the output of Group 2 interrupt sources. The HcμPInterrupt and HcμPInterruptEnable registers work in the same way as the HcInterruptStatus and HcInterruptEnable registers in the interrupt Group 2. The output from the 10-input OR gate is connected to a latch, which is controlled by InterruptPinEnable (bit 0 of the HcHardwareConfiguration register).

2.3. Disabling and Enabling the Interrupt

To temporarily disable the interrupt output of the ISP116x Host Controller through software:

1. Make sure that the InterruptPinEnable bit in the HcHardwareConfiguration register is set to logic 1.
2. Clear *all* bits in the HcμPInterrupt register.
3. Set the InterruptPinEnable bit to logic 0.

To re-enable the interrupt generation:

1. Set *all* bits in the HcμPInterrupt register.
2. Set the InterruptPinEnable bit to logic 1.

Note: the InterruptPinEnable bit in the HcHardwareConfiguration register latches the interrupt output. When this bit is set to logic 0, the interrupt output will remain unchanged, regardless of any operations on the interrupt control registers.

If INT1 is asserted, and the HCD wishes to temporarily mask off the INT signal without clearing the HcμPInterrupt register, the following procedure should be followed:

1. Make sure that the InterruptPinEnable bit is set to logic 1.
2. Clear all bits in the HcμPInterruptEnable register.
3. Set InterruptPinEnable to logic 0.

To re-enable the interrupt:

1. Set the bits in the HcμPInterruptEnable register according to the HCD requirements.
2. Set InterruptPinEnable to logic 1.

3. Interrupt Control in the Device Controller

(Not applicable to ISP1160)

3.1. Registers

The following registers control interrupt generation in the ISP116x Device Controller:

- DcInterruptEnable register
- DcInterrupt register
- Mode register.

3.1.1. DcInterruptEnable Register

The DcInterruptEnable Register is used to individually enable or disable interrupts from all endpoints, and interrupts caused by events on the USB bus. That is, if an interrupt event occurs while the interrupt is not enabled, nothing will be seen on the interrupt pin. Even if you then enable the interrupt during the interrupt event, there will still be no interrupt seen on the interrupt pin, see Figure 3-1.

The Interrupt Register will not register any interrupt, if it is not already enabled using the Interrupt Enable Register. The Interrupt Enable Register is not an Interrupt Mask Register.

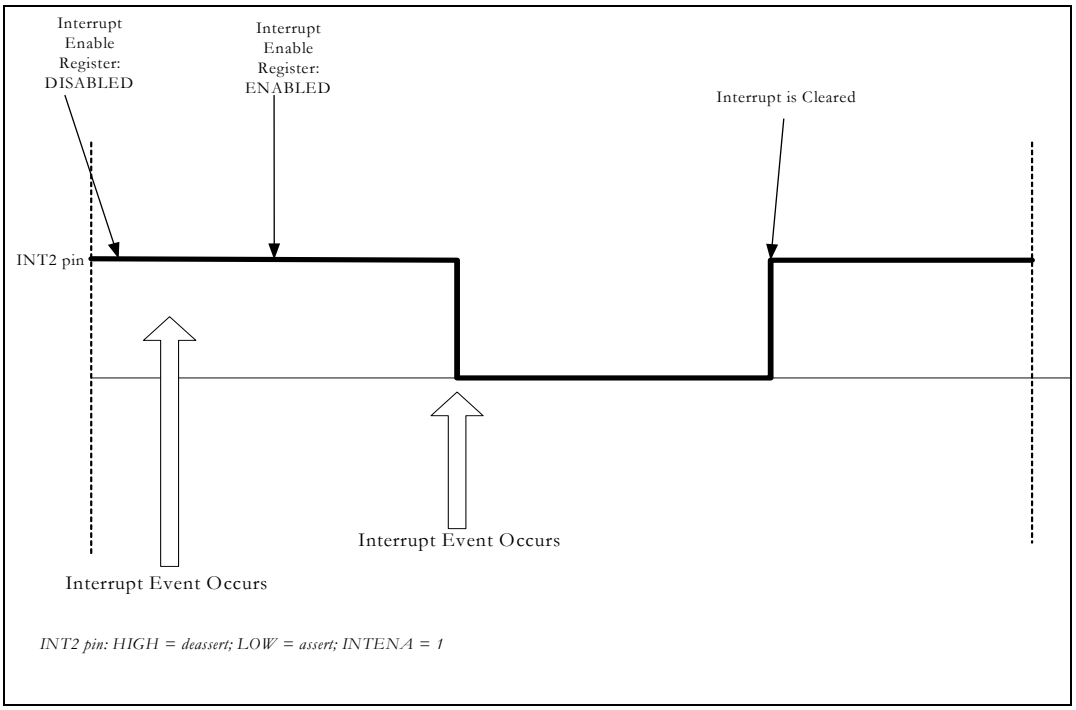

Figure 3-1: Interrupt Pin Waveform

3.1.2. DcInterrupt Register

The Interrupt Register informs the microcontroller or microprocessor about the interrupt events that occur on the various endpoints of the ISP116x, as well as different bus conditions (for example, BUS RESET, SUSPEND and SOF). When an Interrupt Register bit is 1, it indicates an interrupt has occurred because of the corresponding event.

Table 3-1: Interrupt Register

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	EP14	EP13	EP12	EP11	EP10	EP9	EP8	EP7
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	EP6	EP5	EP4	EP3	EP2	EP1	EP0IN	EP0OUT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BUSTATUS	SP_EOT	PSOF	SOF	EOT	SUSPND	RESUME	RESET
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

3.1.3. INTENA Bit

The INTENA bit in the Mode Register is a global interrupt enable or disable bit. The behavior of this bit is given in Figure 3-2.

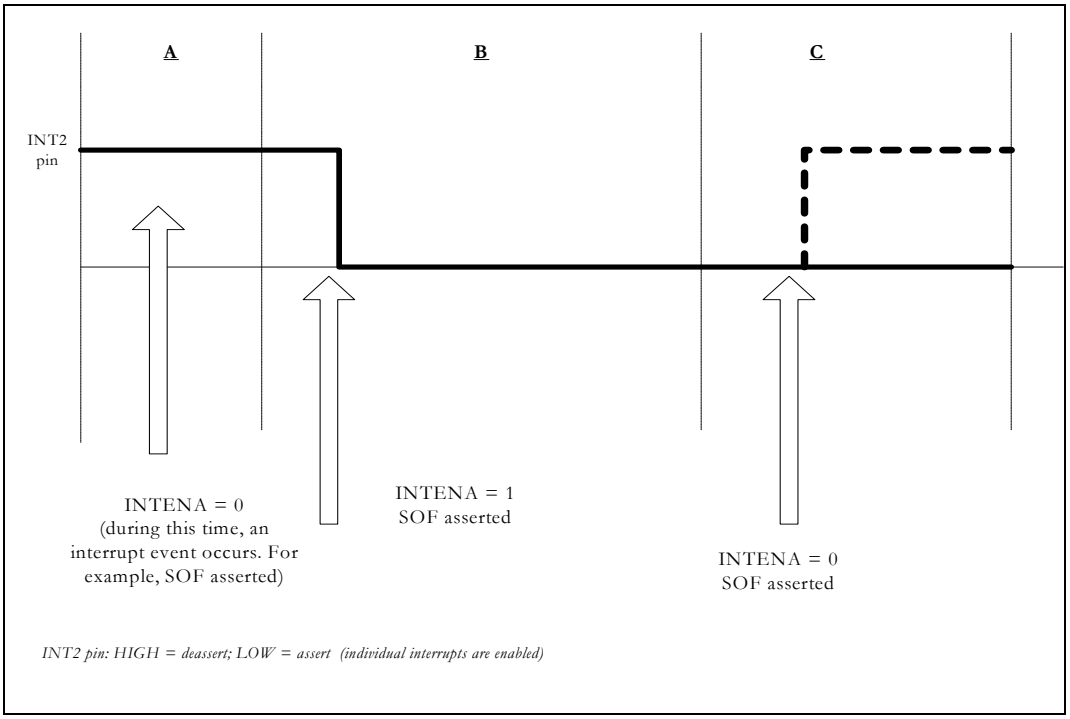

Figure 3-2: Behavior of the INTENA Bit

Event A (see Figure 3-2): When an interrupt event occurs (for example, SOF interrupt) with the INTENA bit set to logic 0, an interrupt will not be generated at the INT pin. However, it will be registered in the corresponding interrupt register bit.

Event B (see Figure 3-2): When the INTENA bit is set to logic 1, the INT pin is asserted because the SOF bit in the Interrupt Register is already asserted.

Event C (see Figure 3-2): If the firmware sets the INTENA bit to logic 0, the INT pin will still be asserted. The bold dashed line shows the desired behavior of the INT pin. Deassertion of the INT pin can be achieved in the following manner. Interrupt Register bits [23:8] are endpoint interrupts. These interrupts are cleared on reading their respective Endpoint Status Register. Interrupt Register bits [7:0] are bus status and EOT interrupts that are cleared on reading the interrupt register. Make sure that the INTENA bit is set to logic 1 when you perform the clear interrupt commands.

4. References

- *Universal Serial Bus Specification Rev. 2.0*
- *ISP116x full-speed Universal Serial Bus single-chip host and device controller* datasheet.