

# **King Saud University**

College of Computer and Information Sciences
Department of Computer Science

## **CSC 220: Computer Organization**

### **Lab Project**

Due Date: Sunday, Jun 4

**Project Description:** The aim of this project is to design an 8-bit Function Unit Combining Arithmetic Logic Unit (ALU) and a Shifter that can perform the operations given in table 1 below.

- 1. Use X and Y as 8 bits input and G as 8 bits output as shown in Figure 1.
- 2. S0, S1, S2 and S3 represent the selection code of the operations.
- 3. Three statue bits V (overflow), C (carry), N (negative) are related to arithmetic operations and statue bit Z (zero) is related to both arithmetic and logic operation.
- 4. Use constant inputs when needed.
- 5. Test your designed Function Unit with necessary tables.

**Marking:** Total marks for the project is five (5).

#### **Groups:**

- 1. Each group should contain 2 students only. The maximum group size is 2 students.
- 2. Members of the group must belong to the same section.
- 3. Only one of the group members is responsible to submit the project.
- 4. Late submissions will NOT be accepted.

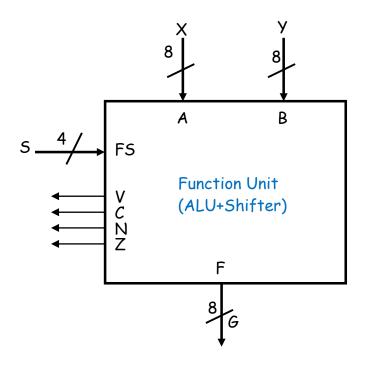


Figure 1: Block diagram of 5-bit Function Unit

Table1: Set of operations

| <b>S3</b> | <b>S2</b> | S1 | S0 | Operation                   |
|-----------|-----------|----|----|-----------------------------|
| 0         | 0         | 0  | 0  | G=X+Y                       |
| 0         | 0         | 0  | 1  | G=X+Y+1                     |
| 0         | 0         | 1  | 0  | G=X+Y'                      |
| 0         | 0         | 1  | 1  | G=X-Y                       |
| 0         | 1         | 0  | 0  | G=2X                        |
| 0         | 1         | 0  | 1  | G=2X+1                      |
| 0         | 1         | 1  | 0  | G=X                         |
| 0         | 1         | 1  | 1  | G=X+1                       |
| 1         | 0         | 0  | 0  | G=X AND Y'                  |
| 1         | 0         | 0  | 1  | G= X OR Y'                  |
| 1         | 0         | 1  | 0  | G=X XOR Y                   |
| 1         | 0         | 1  | 1  | G= X'                       |
| 1         | 1         | 0  | 0  | G=Y                         |
| 1         | 1         | 0  | 1  | G= Switch Tail Right Y      |
| 1         | 1         | 1  | 0  | G= Arithmetic Shift Right Y |
| 1         | 1         | 1  | 1  | G= Logical Shift Left Y     |

## **Submission**: (Upload your project on LMS before **Sunday, Jun 4**- 11:59 PM)

You need to submit the following:

- 1. Your circuit in Logisim file. (.circ).
- 2. A **PDF** file contains: a screenshot of your circuit and test cases for each operation. In each case you need to specify the value of S, X and Y with the corresponding output as following:

| Input          |                |                |                | Operation | Inp       | out       | Expected output |   |   |   |   |
|----------------|----------------|----------------|----------------|-----------|-----------|-----------|-----------------|---|---|---|---|
| S <sub>3</sub> | S <sub>2</sub> | S <sub>1</sub> | S <sub>0</sub> |           | X         | У         | G               | C | ٧ | 2 | Z |
| 0              | 0              | 0              | 0              | G=X+Y     | 0000 0011 | 0000 0010 | 0000 0101       | 0 | 0 | 0 | 0 |

#### Note:

- 1. Use the same values of X and Y as in the table above for all the test cases.
- 2. Use **X** in case you don't care what the value of inputs or status bits.
- 3. One screenshot of your circuit is enough.

### **Submission instructions:**

- 1. Put your files (circuit + PDF) in one folder.
- 2. Name the folder with Your names.
- 3. Compress the folder and upload it on LMS.
- 4. Only one of the group members is responsible to submit the project (one submission per group).