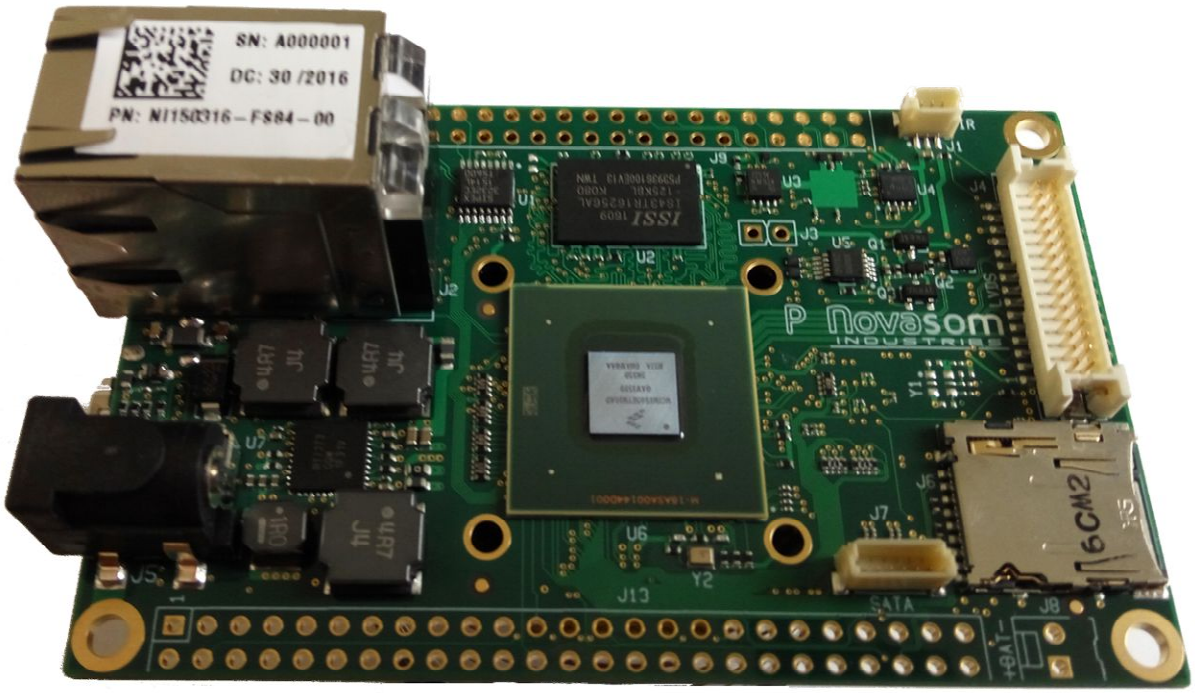
NOVAsomP



Hardware User Manual

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1 : Welcome to the NOVAsom P world

Thank you for choosing this NOVAsom Industries product.
Please carefully read this user guide before using the device for the first time to ensure safe and proper use.
In particular note that :

- Contents and illustrations may differ from your device, depending on the software version, OS version or product improvements that NOVAsom Industries judges important, and are subject to change without prior notice. Always stay updated visiting www.novasomindustries.com .
- Descriptions are based on the device default settings.
- Modifying the device, the device's operating system or installing software from unofficial sources may damage the device itself and lead to data corruption or data loss, or worst, hardware damage. Such actions will violate your NOVAsom Industries license agreement and void your warranty.
- Always use genuine NOVAsom Industries accessories. The supplied items are designed only for this device and may not be compatible with other devices. To have further information on this specific item visit www.novasomindustries.com .
- Default applications on the device are subject to updates, and support for these applications may be withdrawn without prior notice. If you have any questions about an application provided with the device, please contact NOVAsom Industries at www.novasomindustries.com .
- Software, audio, wallpaper, images, and other media supplied with your device or found in the appropriate SDK are licensed for limited use. If you extract and use these materials for commercial or other purposes, you may be infringing copyright laws. As a user, you are fully responsible for the illegal use of media.

The NOVAsom P family is a product line from NOVAsom Industries, targeted toward the low price market (vending, domotics, IoT, etc.) and designed to compete with low cost boards while maintaining NOVAsom Industries high quality level.
NOVAsom P is a very small NOVAsom board, approximately credit card size, but with all the necessary to guarantee an immediate bootstrap, driving a display, connecting via Ethernet and USB.
It's equipped with two 2.54 mm. dual row strips for external expansions and a mPCIe slot ready for use, i.e. with a WiFi , a BlueTooth™, a 3G with full PCM audio support or a GPS card, or what you may need.

3 different standard products (with different configurations) are available:

• NOVAsomP6B: with processor NXP® iMX6 SOLO @1GHz,512MB RAM DDR3

• NOVAsomP7D: with processor NXP® iMX6 Dual Lite@1GHz, 1GB RAM DDR3, RS485/CAN drivers

• NOVAsomP8E: with processor NXP® iMX6 Quad @1GHz,1GB RAM DDR3, eMMC (4GB), RS485/CAN drivers, 3 channel USB on strip, SATA connector, RTC battery connector, remote IR input connector.

This list is only an example and will vary with time, more information about product status and availability can be found visiting www.novasomindustries.com .

2 : Features

From the integrator point of view the board is a full fledged SBC, with video and communications capabilities and requires a single supply from a wall cube or a generic external power supply.
The main characteristics of the NOVAsom P are:

On Board Peripherals:

- Up to 32GBytes bootable eMMC (Option)
- Up to 1GBytes 32 bit wide DDR
- 1 bootable uSD slot up to 32GBytes
- 1 Ethernet port @ 10/100 Mbit/sec.
- 1 Dual Channel LVDS up to 1920x1080 with PWM brightness control and I2C for touch screen
- 1 Full Size HDMI connector with audio and CEC
- 1 mPCIe slot with optional SIM bay (the SIM bay is for 3G mPCIe boards)
- 1 Integrated RTC with optional external battery connector (the RTC draws up to 50 uA)
- 1 USB Host connector
- 1 Remote IR input with optional connector
- 1 Power led and 1 User Driven led, plus one led driven by the mPCIe board if present
- Standard 2.5mm Power Supply Jack for 6.5Vcc to 18Vcc input, central positive

On Expansion Connectors (J9 and J13):

- 1 I2C @ 3.3V
- 4 SPI @ 50 MHz maximum, 3 of them with 2 Slave Select and 1 with 1 slave select
- 8 GPIO @ 3.3V
- 1 Full UART @ 3.3V (TX ; RX ; RTS ; CTS)
- 1 PCM AUDIO @ 3.3V
- 1 SPDIF OUT
- 2 LANE CSI for Camera Sensor (Note 1)
- 2 LANE DSI for External Display (Note 1)
- 1 x OTG port, 2 x HOST port, two of them with power management (Note 1)
- 1 x console @ RS232 (Note 2)

- 1 x RS232 (Note 2)
- 1 x CAN with optional transceiver (Note 2)
- 1 x optional RS485 with transceiver and optional termination(Note 2)
- 1 x uSD/eMMC plus 3 GPIO externally powered @ 3.3/1.8V expansion (Note 3)
- 1 x TX/RX only UART externally powered @ 3.3/1.8V (Note 3)
- 1 x Full UART externally powered @ 3.3/1.8V (TX ; RX ; RTS ; CTS) (Note 3)
- 1 x I2C externally powered @ 3.3/1.8V (Note 3)

Note 1 : these pins have a dedicated function and cannot be used as GPIO
Note 2 : these pins have the appropriate driver
Note 3 : these pins are powered externally from a 1.8V or 3.3V source. The 3.3V source can be from the NOVAsom P shorting the appropriate pin on one of the two expansion connectors (J9) , other supplies must be provided from the expansion board that will utilize them.

All the pins without (Note 1) , (Note 2) or (Note 3) can be programmed as GPIO or programmed accordingly to the functions described in table 6 and table 7 below.

The connectors J9 and J13 are normally not equipped with the pin strip.
The user has so the choice to use a male or female contact type, and to solder the strips on top or bottom of the NOVAsom P, use partially populated connectors or a mix of them.

3 : Description

The NOVAsom P family is equipped with 3 different processors and different combinations of RAM and peripherals:

• iMX6 SOLO @1GHz,512MB DDR3

• iMX6 Dual Lite@1GHz, 1GB DDR3, RS485/CAN drivers

• iMX6 Quad @1GHz,1GB DDR3, eMMC (4GB), RS485/CAN drivers, 3 USB on strip, SATA connector, RTC battery connector, remote IR input connector

Visit www.novasomindustries.com , you can download 3D drawings and detailed mechanical drawing.

4 : Connectors description and Configuration

4.1 Connectors list and function

In Figure 2 you can see the NOVAsom P board connectors top placement, while in Figure 3 you can see the NOVAsom P board connectors bottom placement

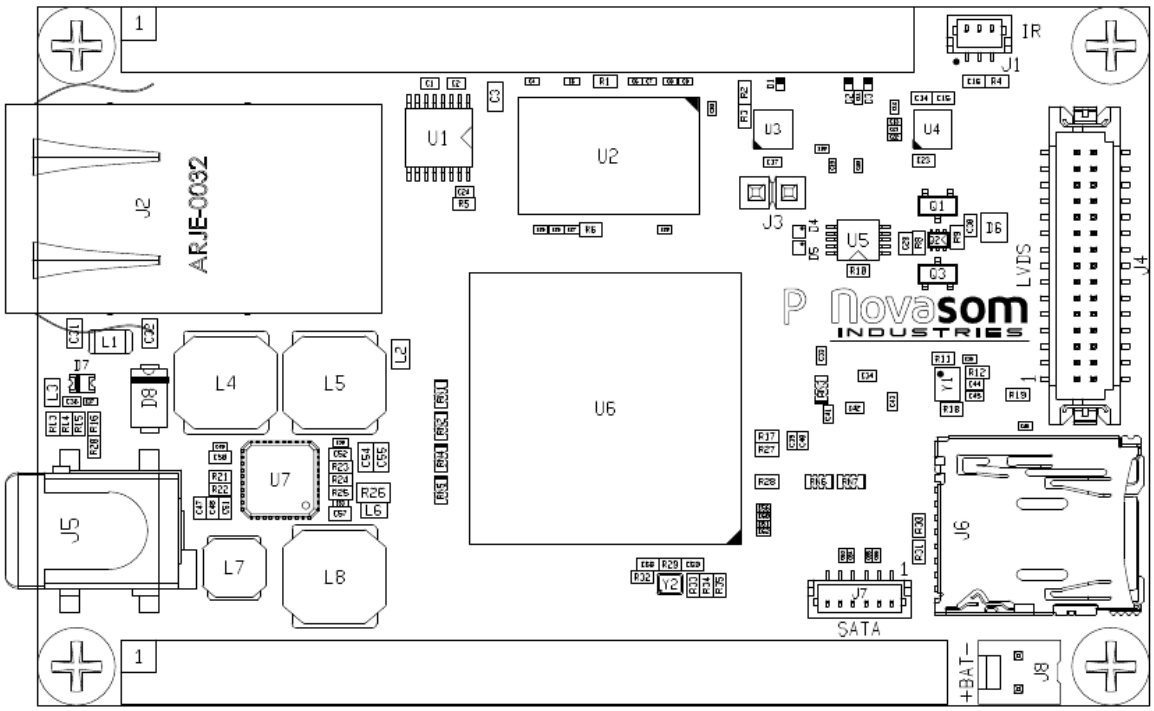

Figure 1 : NOVAsom P top view

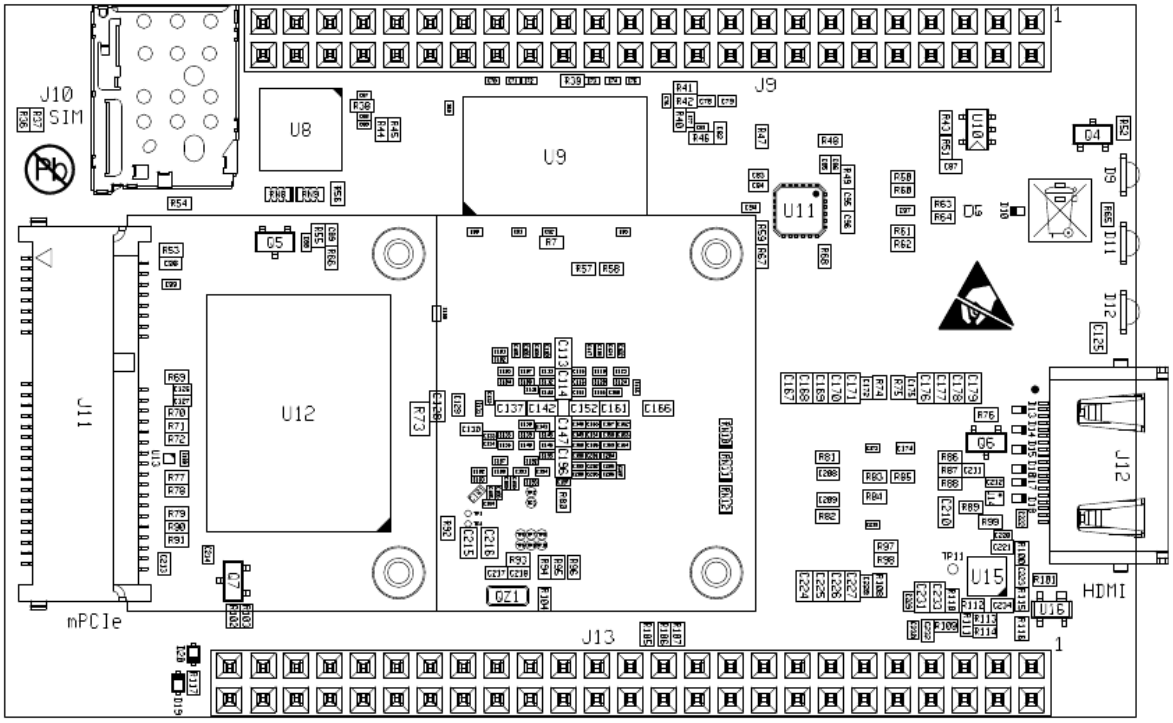

Figure 2 : NOVAsom P bottom view

In Table 1 you can see the NOVAsom P board connectors and the mating connectors.

Connector	Manufacturer	Connector Type	Mating Connector	Function
J1	JST	BM03B-SRSS-TB(LF)(SN)(P)	SHR-03V-S-B	IR Detector
J2	Abracon	ARJE-0032	Std RJ45 + USB	Ethernet+USB
J3	Jumper	-	-	2 pin header
J4	Hirose	DF13A-30DP-1.25V	DF13-30DS-1.25C	LVDS
J5	CUI Inc.	PJ-002AH-SMT-TR	-	POWER
J6	Hirose	uSD card	-	uSD
J7	JST	BM06B-SRSS-TB(LF)(SN)	SHR-06V-S-B	SATA
J8	Molex	22232021	22013027	CMOS Battery
J9	NP	-	-	48 pin header
J10	JAE	SF72S006VBAR2500	-	nanoSIM
J11	JAE	MM60-52B1-E1-R650	-	mPCIe
J12	TE AMP	2-1903015-2	-	HDMI
J13	NP	-	-	50 pin header

Table 1 : Connectors list

4.2 Connectors pinout

In the Table 2 you can see the NOVAsom P board connectors functions and pin assignement.

Connector	Manufacturer	Connector P/N	Function	Pinout	Signal Name		
J1	JST	BM03B-series	IR Detector	4	IR_DETECT		
				3	3.3V		
				2	GND		
				1	IR FEEDBACK		
J2	Abracon	ARJE-0032	Ethernet+USB	See ARJE-0032 datasheet			
J3	Jumper			Closed : LVDS_BL_POWER from VIN Open : LVDS_BL_POWER from 5V			
J4	Hirose	DF13A-30DP-1.25V	LVDS	1	LVDS_BL_POWER	LVDS_BL_POWER	2
				3	LVDS0_TX2_P	LVDS0_TX0_P	4
				5	LVDS0_TX2_N	LVDS0_TX0_N	6
				7	LVDS0_TX3_P	LVDS0_TX1_P	8
				9	LVDS0_TX3_N	LVDS0_TX1_N	10
				11	LVDS1_TX0_N	LVDS0_CLK_P	12
				13	LVDS1_TX0_P	LVDS0_CLK_N	14
				15	LVDS1_TX1_P	LVDS1_CLK_P	16
				17	LVDS1_TX1_N	LVDS1_CLK_N	18
				19	LVDS1_TX2_N	LVDS1_TX3_N	20
				21	LVDS1_TX2_P	LVDS1_TX3_P	22
				23	LVDS_POWER	LVDS_POWER	24
				25	GND	GND	26
				27	BL_PWM	I2C3_SCL	28
				29	TOUCH_IRQ	I2C3_SDA	30
J5	CUI Inc.	PJ-002AH-SMT-TR	POWER	1	VIN		
				2	GND		
J6	Hirose	uSD card	uSD	1	DATA2(*)		
				2	DATA3(*)		
				3	CMD(*)		
				4	VDD(*)		
				5	CLK(*)		
				6	VSS(*)		
				7	DATA0(*)		
				8	DATA1(*)		
J7	JST	BM06B-series	SATA	1	VCC (***)		
				2	RXP		
				3	RXN		
				4	TXN		
				5	TXP		
				6	GND		
J8	Molex	22232021	CMOS Battery	1	VBAT+		
				2	GND		
J9	NP		48 pin header	See below			

J10	JAE	SF72S006VBAR2500	nanoSIM	1	SIM VCC		
				2	SIM RST		
				3	SIM CLK		
				5	GND		
				6	SIM VPP		
				7	SIM I/O		
J11	JAE	MM60-52B1-E1-R650	mPCIe	1	WAKE#	3.3V	2
				3	Reserved	GND	4
				5	Reserved	1.5V(*****)	6
				7	Reserved	SIM VCC (****)	8
				9	GND	SIM I/O(****)	10
				11	REFCLK-	SIM CLK(****)	12
				13	REFCLK+	SIM RST(****)	14
				15	GND	SIM VPP(****)	16
				17	Reserved	GND	18
				19	Reserved	W_DISABLE#	20
				21	GND	PERST#	22
				23	PERn0	+3.3Vaux	24
				25	PERp0	GND	26
				27	GND	+1.5V(*****)	28
				29	GND	SMB_CLK	30
				31	PETn0	SMB_DATA	32
				33	PETp0	GND	34
				35	GND	USB_D-	36
				37	GND	USB_D+	38
				39	3.3V	GND	40
				41	3.3V	LED_WWAN#	42
				43	GND	LED_WLAN#	44
				45	AUD3_TXC (**)	LED_WPAN#	46
				47	AUD3_RXD(**)	+1.5V(*****)	48
				49	AUD3_TXD(**)	GND	50
				51	AUD3_TXFS(**)	+3.3V	52
J12	TE AMP	2-1903015-2	HDMI	1	TMDS Data2+		
				2	GND		
				3	TMDS Data2–		
				4	TMDS Data1+		
				5	GND		
				6	TMDS Data1–		
				7	TMDS Data0+		
				8	GND		
				9	TMDS Data0–		
				10	TMDS Clock+		
				11	GND		
				12	TMDS Clock–		
				13	CEC		
				14	Reserved		
				15	DDC SCL (******)		
				16	DDC SDA (******)		

				17	GND
				18	+5V
				19	HPG
J13	NP		50 pin header	See below	

Table 2 : Connectors pinout

(*) Note : the uSD slot is 3.3V powered and has no provisions to manage the insertion or the removal of the uSD card with power applied, and thus no ESD protections equip the uSD slot.
The insertion or the removal of a uSD card with applied power may result in a permanent damage to the card or, worst, to the NOVAsom P board.
The card MUST be inserted without power applied.
The presence switch that equips the uSD slot of the NOVAsom P board signals to the processor that a card is in the slot, thus allowing the boot process to read the bootloader from the uSD slot.
If the card is not found when the power is applied the boot process will look in eMMC chip for a valid bootloader code but the presence of the eMMC depends on the NOVAsom P board equipment.
The uSD slot is a push-push operated slot.
Removing the uSD card without pushing will result in mechanical failure of the slot itself.

(**) Note : the audio PCM pins AUD3_TXC, AUD3_RXD, AUD3_TXD and AUD3_TXFS on mPCIe connector J12 are powered externally by NVCC_SD3_FROM_EXP (pin 4 of J9), thus allowing the connections of a low voltage interface mPCIe device (e.g. 1.8V).
In order to use this feature the user must connect NVCC_SD3_FROM_EXP to a power source, e.g. 1.8V with enough available current as specified by the device manufacturer. Consult the mPCIe module manufacturer to collect this information.
Note also that all the I/O powered from NVCC_SD3_FROM_EXP, marked with the orange box in the following tables, will be powered by this user provided power, so be careful in order to avoid over voltages at the pin level, as specified in Absolute Maximum Ratings chapter.

(***) On SATA connector J7 the pin 1, indicated as generic VCC, can be powered from the 3.3V or the 5V. The default is 3.3V.
The user must indicate the power before ordering the board.

(****) There are no connections between the SIM card and the processor on the NOVAsom P board, as the SIM is used only when a 3G module is inserted in the mPCIe slot of the NOVAsom P board.
Power and logic signals will be delivered only from the module at the appropriate voltage of the module itself.

(*****) The 1.5V power rail on the mPCIe slot is actually connected to a 1.45V rail because depends on the DDR power supply. In case of LP-DDR (powered at 1.35V) the 1.5V rail on the mPCIe slot will be at 1.35V. This should not be a problem with most of the mPCIe cards like WiFi or LAN, but user should check carefully with the manufacturer of the mPCIe card if this feature is compatible.

(******) DDC_SCL and DDC_SDA, although are a true I2C bus and ESD protected and cannot be connected to anything different from an HDMI connector as they have a translator to the +5V of the HDMI powered interface. In the standard BSP these lines are defined only for DDC functions.

(*******) LVDS_POWER is 3.3V

4.3 J9 Connector pinout

The colors description is at chapter 4.5

Pin	Signal Name	Function	i.MX6 ball	Power	Color
1	VINHIGH	Input Power	-	-	
2	NVCC_3V3	3.3V Power	-	-	
3	GPIO3_IO19	GPIO	G21	3.3V	
4	NVCC_SD3_FROM_EXP	Power	-	-	
5	GPIO4_IO26	GPIO	R25	3.3V	
6	GPIO3_IO20	GPIO	G20	3.3V	
7	GPIO4_IO28	GPIO	R24	3.3V	
8	GPIO4_IO27	GPIO	R23	3.3V	
9	GPIO1_IO00	GPIO	T5	3.3V	
10	GPIO4_IO29	GPIO	R22	3.3V	
11	GPIO6_IO05	GPIO	L6	3.3V/1.8V ext	
12	GPIO4_IO14	GPIO	T6	3.3V	
13	CONSOLE_RS232_TXD	SERIAL	-	-	
14	CONSOLE_RS232_RXD	SERIAL	-	-	
15	GEN_5V	5V Power	-	-	
16	GND	Power	-	-	
17	AUX_RS232_TXD (***)	SERIAL	-	-	
18	AUX_RS232_RXD (***)	SERIAL	-	-	
19	AUD6_TXD	PCM AUDIO	N25	3.3V	
20	AUD6_RXD	PCM AUDIO	P25	3.3V	
21	AUD6_TXFS	PCM AUDIO	N20	3.3V	
22	AUD6_TXC	PCM AUDIO	N21	3.3V	
23	I2C1_SDA	I2C1	N6	3.3V/1.8V ext	
24	I2C1_SCL	I2C1	N5	3.3V/1.8V ext	
25	UART1_TXD	UART	M1	3.3V/1.8V ext	
26	UART1_RXD	UART	M3	3.3V/1.8V ext	
27	SPDIF_OUT	AUDIO	R1	3.3V	
28	UART4_RTS_L	UART	L4	3.3V/1.8V ext	
29	UART4_TXD	UART	M2	3.3V/1.8V ext	
30	UART4_RXD	UART	L1	3.3V/1.8V ext	
31	CANH	CAN	-	-	
32	UART4_CTS_L	UART	L3	3.3V/1.8V ext	
33	CANL	CAN	-	-	
34	RS485_RX+ (****)	RS485	-	-	
35	RS485_TX- (****)	RS485	-	-	
36	RS485_RX- (****)	RS485	-	-	
37	RS485_TX+ (****)	RS485	-	-	
38	USB_OTG_VBUS	USB	-	-	
39	USB_OTG_DP	USB	-	-	
40	USB_OTG_DN	USB	-	-	
41	USB_PWR3(*)	USB	-	-	
42	USB_PWR2(**)	USB	-	-	
43	USBDN_DP2	USB	-	-	
44	USBDN_DM2	USB	-	-	

45	USBDN_DP3	USB	-	-	
46	USBDN_DM3	USB	-	-	
47	GND	Power	-	-	
48	GND	Power	-	-	

Table 3 : J9 Connectors pinout

(*) The USB_PWR3 is minded to power a user provided USB connector for channel 3 (USBDN_DP3, USBDN_DM3). The switch in the board protects from overload and disconnect the load when power draw exceeds 500 mA. No ESD protections are provided on the NOVAsom P board.

(**) The USB_PWR2 is minded to power a user provided USB connector for channel 2(USBDN_DP2, USBDN_DM2). The switch in the board protects from overload and disconnect the load when power draw exceeds 500 mA. No ESD protections are provided on the NOVAsom P board.

(***) Connected to *ttymxc1*. No ESD protections are provided on the NOVAsom P board.

(****) Connected to *ttymxc4*. ESD protections and default pullups / pulldowns are provided on the NOVAsom P board, no termination resistor provided.

4.4 J13 Connector pinout

The colors description is at chapter 4.5

Pin	Signal Name	Function	i.MX6 Ball	Power	
1	VINHIGH	Input Power	-	-	
2	NVCC_3V3	3.3V Power	-	-	
3	EXT_RESET	System Reset	-	3.3V	
4	ONOFF_IMX6	Power On Signal	-	3.3V	
5	ECSPI1_MISO	SPI1 MISO	V24	3.3V	
6	ECSPI1_MOSI	SPI1 MOSI	T20	3.3V	
7	ECSPI1_SS0	SPI1 SS0	W24	3.3V	
8	ECSPI1_SCK	SPI1 CLOCK	U22	3.3V	
9	ECSPI2_SS0	SPI2 SS0	V25	3.3V	
10	ECSPI2_SS1	SPI2 SS1	T22	3.3V	
11	ECSPI2_MISO	SPI2 MISO	U24	3.3V	
12	ECSPI2_MOSI	SPI2 MOSI	T21	3.3V	
13	ECSPI2_SCK	SPI2 CLOCK	U23	3.3V	
14	ECSPI3_SCK	SPI3 CLOCK	P24	3.3V	
15	ECSPI3_MISO	SPI3 MISO	P23	3.3V	
16	ECSPI3_MOSI	SPI3 MOSI	P22	3.3V	
17	ECSPI3_SS0	SPI3 SS0	P21	3.3V	
18	ECSPI3_SS1	SPI3 SS1	P20	3.3V	
19	ECSPI4_MISO	SPI4 MISO	E23	3.3V	
20	ECSPI4_MOSI	SPI4 MOSI	G23	3.3V	
21	ECSPI4_SS0	SPI4 SS0	J19	3.3V	
22	ECSPI4_SCK	SPI4 CLOCK	H20	3.3V	

23	I2C3_SCL	I2C3 SCL	F21	3.3V	
24	I2C3_SDA	I2C3 SDA	D24	3.3V	
25	SD3_CMD	uSD 3 CMD	B13	3.3V/1.8V ext	
26	32KHZ_CLK_OUT	32KHz Ref Out	R5	3.3V	
27	SD3_CLK	uSD 3 CLK	D14	3.3V/1.8V ext	
28	GND	Power	-	-	
29	SD3_DATA0	uSD3 DATA 0	E14	3.3V/1.8V ext	
30	SD3_DATA1	uSD3 DATA 1	F14	3.3V/1.8V ext	
31	SD3_DATA2	uSD3 DATA 2	A15	3.3V/1.8V ext	
32	SD3_DATA3	uSD3 DATA 3	B15	3.3V/1.8V ext	
33	SD3_DATA4	uSD3 DATA 4	D13	3.3V/1.8V ext	
34	SD3_DATA5	uSD3 DATA 5	C13	3.3V/1.8V ext	
35	SD3_DATA6	uSD3 DATA 6	E13	3.3V/1.8V ext	
36	SD3_DATA7	uSD3 DATA 7	F13	3.3V/1.8V ext	
37	CSI_D1M	CSI D1 Negative	-	-	
38	CSI_D1P	CSI D1 Positive	-	-	
39	CSI_D0M	CSI D0 Negative	-	-	
40	CSI_D0P	CSI D0 Positive	-	-	
41	CSI_CLK0M	CSI CLK Negative	-	-	
42	DSI_CLK0P	DSI CLK Positive	-	-	
43	DSI_D1M	DSI D1 Negative	-	-	
44	DSI_D1P	DSI D1 Positive	-	-	
45	DSI_D0M	DSI D0 Negative	-	-	
46	DSI_D0P	DSI D0 Positive	-	-	
47	DSI_CLK0M	DSI CLK Negative	-	-	
48	DSI_CLK0P	DSI CLK Positive	-	-	
49	NVCC_3V3	Power	-	-	
50	GND	Power	-	-	

Table 4 :J13 Connector pinout

4.5 Connectors table color code

	VINHIGH	Input Power, from 6.5V to 18V
	NVCC_3V3	3.3V Power generated from the board, maximum 400 mA
	Dedicated pin	Dedicated level logic, can be RS232, RS485, CAN or other
	5V Power	5V Power generated from the board, maximum 400 mA
	GND	GND
	NVCC_SD3_FROM_EXP	These pins are powered from the pin called NVCC_SD3_FROM_EXP. The possible values are 1.8V 2.5V or 3.3V. If no power is provided the pins will be constantly low.
	3.3V	These pins are 3.3V logic compliant

Table 5: Connectors table color codes

4.6 J9 Signal Association and Alternate Functions

Each i.MX6 pin has several function, and some are compiled by default in the BSP.

The user can modify the BSP in order to support different function on a particular pin.

In the following table the functions with colored background are the default settings on the NOVAsom P BSP.

The power domain NVCC_EIM0 , NVCC_GPIO , NVCC_LCD are powered from the NVCC_3V3 from the NOVAsom P.

The power domain NVCC_CSI , NVCC_SD3 are powered from the NVCC_SD3_FROM_EXP from the pin 4 of J9 on the NOVAsom P.

The NOVAsom P drives the pin 4 of J9 only if the user shorts it with the pin 2 of J9, thus using NVCC_3V3 from the NOVAsom P power, otherwise the power for these two domains must be provided externally.

The colors description is at chapter 4.5.

	Signal Name	Power Domain	BGA Pin	ALT 0	ALT 1	ALT 2	ALT 3	ALT 4	ALT 5	ALT 6
1	VINHIGH			Input Power						
2	NVCC_3V3			1.8V or 3.3V Power Input						
3	GPIO3_IO19	NVCC_EIM0	G21	EIM_DATA19	ECSPI1_SS1	IPU1_DI0_PIN08	IPU1_CSI1_DATA16	UART1_CTS_B	**GPIO3_IO19**	EPIT1_OUT
4	NVCC_SD3_FROM_EXP			Power						
5	GPIO4_IO26	NVCC_LCD	R25	IPU1_DISP0_DATA05	LCD_DATA05	ECSPI3_SS2	AUD6_RXFS		**GPIO4_IO26**	
6	GPIO3_IO20	NVCC_EIM0	G20	EIM_DATA20	ECSPI4_SS0	IPU1_DI0_PIN16	IPU1_CSI1_DATA15	UART1_RTS_B	**GPIO3_IO20**	EPIT2_OUT
7	GPIO4_IO28	NVCC_LCD	R24	IPU1_DISP0_DATA07	LCD_DATA07	ECSPI3_RDY			**GPIO4_IO28**	
8	GPIO4_IO27	NVCC_LCD	R23	IPU1_DISP0_DATA06	LCD_DATA06	ECSPI3_SS3	AUD6_RXC		**GPIO4_IO27**	
9	GPIO1_IO00	NVCC_GPIO	T05	CCM_CLKO1		KEY_COL5	aASRC_EXT_CLK	EPIT1_OUT	**GPIO1_IO00**	USB_H1_PWR
10	GPIO4_IO29	NVCC_LCD	R22	IPU1_DISP0_DATA08	LCD_DATA08	PWM1_OUT	WDOG1_B		**GPIO4_IO29**	
11	GPIO6_IO05	NVCC_CSI	L06	IPU1_CSI0_DATA19	EIM_DATA15		UART5_CTS_B		**GPIO6_IO05**	
12	GPIO4_IO14	NVCC_GPIO	T06	FLEXCAN2_TX	IPU1_SISG4	USB_OTG_OC	KEY_COL4	UART5_RTS_B	**GPIO4_IO14**	
13	CONSOLE_RS232_TXD									
14	CONSOLE_RS232_RXD									
15	GEN_5V			5V Power						
16	GND			Power						
17	AUX_RS232_TXD									
18	AUX_RS232_RXD									
19	AUD6_TXD	NVCC_LCD	N25	IPU1_DI0_PIN02	LCD_HSYNC	**AUD6_TXD**			GPIO4_IO18	
20	AUD6_RXD	NVCC_LCD	P25	IPU1_DI0_PIN04	LCD_BUSY	**AUD6_RXD**	SD1_WP		GPIO4_IO20	
21	AUD6_TXFS	NVCC_LCD	N20	IPU1_DI0_PIN03	LCD_VSYNC	**AUD6_TXFS**			GPIO4_IO19	
22	AUD6_TXC	NVCC_LCD	N21	IPU1_DI0_PIN15	LCD_ENABLE	**AUD6_TXC**			GPIO4_IO17	
23	I2C1_SDA	NVCC_CSI	N06	IPU1_CSI0_DATA08	EIM_DATA06	ECSPI2_SCLK	KEY_COL7	**I2C1_SDA**	GPIO5_IO26	
24	I2C1_SCL	NVCC_CSI	N05	IPU1_CSI0_DATA09	EIM_DATA07	ECSPI2_MOSI	KEY_ROW7	**I2C1_SCL**	GPIO5_IO27	
25	UART1_TXD	NVCC_CSI	M01	IPU1_CSI0_DATA10	AUD3_RXC	ECSPI2_MISO	**UART1_TX_DATA**		GPIO5_IO28	

26	UART1_RXD	NVCC_CSI	M03	IPU1_CSI0_DATA11	AUD3_RXFS	ECSPI2_SS0	**UART1_RX_DATA**		GPIO5_IO29		
27	SPDIF_OUT	NVCC_GPIO	R01	ESAI_TX0	ENET_1588_EVENT3_IN	CCM_PMIC_READY	SDMA_EXT_EVENT0	**SPDIF_OUT**	GPIO7_IO12		
28	UART4_RTS_L	NVCC_CSI	L04	IPU1_CSI0_DATA16	EIM_DATA12		**UART4_RTS_B**		GPIO6_IO02		
29	UART4_TXD	NVCC_CSI	M02	IPU1_CSI0_DATA12	EIM_DATA08		**UART4_TX_DATA**		GPIO5_IO30		
30	UART4_RXD	NVCC_CSI	L01	IPU1_CSI0_DATA13	EIM_DATA09		**UART4_RX_DATA**		GPIO5_IO31		
31	CANH										
32	UART4_CTS_L	NVCC_CSI	L03	IPU1_CSI0_DATA17	EIM_DATA13		**UART4_CTS_B**		GPIO6_IO03		
33	CANL										
34	RS485_RX+										
35	RS485_TX-										
36	RS485_RX-										
37	RS485_TX+										
38	USB_OTG_VBUS										
39	USB_OTG_DP										
40	USB_OTG_DN										
41	USB_PWR3										
42	USB_PWR2										
43	USBDN_DP2										
44	USBDN_DM2										
45	USBDN_DP3										
46	USBDN_DM3										
47	GND			Power							
48	GND			Power							

Table 6 : J9 Signal Association and Alternate Functions

4.7 J13 Signal Association and Alternate Functions

Each i.MX6 pin has several function, and some are compiled by default in the BSP.

The user can modify the BSP in order to support different function on a particular pin.

In the following table the functions with colored background are the default settings on the NOVAsom P BSP.

The power domain NVCC_EIM0 , NVCC_GPIO , NVCC_LCD are powered from the NVCC_3V3 from the NOVAsom P.

The power domain NVCC_CSI , NVCC_SD3 are powered from the NVCC_SD3_FROM_EXP from the pin 4 of J9 on the NOVAsom P.

The NOVAsom P drives the pin 4 of J9 only if the user shorts it with the pin 2 of J9, thus using NVCC_3V3 from the NOVAsom P power, otherwise the power for these two domains must be provided externally.

The colors description is at chapter 4.5.

	Signal Name	Power Domain	BGA Pin	ALT 0	ALT 1	ALT 2	ALT 3	ALT 4	ALT 5	ALT 6	
1	VINHIGH			Input Power							
2	NVCC_3V3			3.3V Power							
3	EXT_RESET			System Reset(3.3V)							
4	ONOFF_IMX6			Power On Signal(3.3V)							
5	ECSPI1_MISO	NVCC_LCD	V24	IPU1_DISP0_DATA22	LCD_DATA22	**ECSPI1_MISO**	AUD4_TXFS		GPIO5_IO16		
6	ECSPI1_MOSI	NVCC_LCD	T20	IPU1_DISP0_DATA21	LCD_DATA21	**ECSPI1_MOSI**	AUD4_TXD		GPIO5_IO15		
7	ECSPI1_SS0	NVCC_LCD	W24	IPU1_DISP0_DATA23	LCD_DATA23	**ECSPI1_SS0**	AUD4_RXD		GPIO5_IO17		
8	ECSPI1_SCK	NVCC_LCD	U22	IPU1_DISP0_DATA20	LCD_DATA20	**ECSPI1_SCLK**	AUD4_TXC		GPIO5_IO14		
9	ECSPI2_SS0	NVCC_LCD	V25	IPU1_DISP0_DATA18	LCD_DATA18	**ECSPI2_SS0**	AUD5_TXFS	AUD4_RXFS	GPIO5_IO12		
10	ECSPI2_SS1	NVCC_LCD	T22	IPU1_DISP0_DATA15	LCD_DATA15	ECSPI1_SS1	**ECSPI2_SS1**		GPIO5_IO09		
11	ECSPI2_MISO	NVCC_LCD	U24	IPU1_DISP0_DATA17	LCD_DATA17	**ECSPI2_MISO**	AUD5_TXD	SDMA_EXT_EVENT1	GPIO5_IO11		
12	ECSPI2_MOSI	NVCC_LCD	T21	IPU1_DISP0_DATA16	LCD_DATA16	**ECSPI2_MOSI**	AUD5_TXC	SDMA_EXT_EVENT0	GPIO5_IO10		
13	ECSPI2_SCK	NVCC_LCD	U23	IPU1_DISP0_DATA19	LCD_DATA19	**ECSPI2_SCLK**	AUD5_RXD	AUD4_RXC	GPIO5_IO13		
14	ECSPI3_SCK	NVCC_LCD	P24	IPU1_DISP0_DATA00	LCD_DATA00	**ECSPI3_SCLK**			GPIO4_IO21		
15	ECSPI3_MISO	NVCC_LCD	P23	IPU1_DISP0_DATA02	LCD_DATA02	**ECSPI3_MISO**			GPIO4_IO23		
16	ECSPI3_MOSI	NVCC_LCD	P22	IPU1_DISP0_DATA01	LCD_DATA01	**ECSPI3_MOSI**			GPIO4_IO22		
17	ECSPI3_SS0	NVCC_LCD	P21	IPU1_DISP0_DATA03	LCD_DATA03	**ECSPI3_SS0**			GPIO4_IO24		
18	ECSPI3_SS1	NVCC_LCD	P20	IPU1_DISP0_DATA04	LCD_DATA04	**ECSPI3_SS1**			GPIO4_IO25		

19	ECSPI4_MISO	NVCC_EIM0	E23	EIM_DATA22	**ECSPI4_MISO**	IPU1_DI0_PIN01	IPU1_CSI1_DATA10	USB_OTG_PWR	GPIO3_IO22	SPDIF_OUT	
20	ECSPI4_MOSI	NVCC_EIM0	G23	EIM_DATA28	I2C1_SDA	**ECSPI4_MOSI**	IPU1_CSI1_DATA12	UART2_CTS_B	GPIO3_IO28	IPU1_EXT_TRIG	
21	ECSPI4_SS0	NVCC_EIM0	J19	EIM_DATA29	IPU1_DI1_PIN15	**ECSPI4_SS0**		UART2_RTS_B	GPIO3_IO29	IPU1_CSI1_VSYNC	
22	ECSPI4_SCK	NVCC_EIM0	H20	EIM_DATA21	**ECSPI4_SCLK**	IPU1_DI0_PIN17	IPU1_CSI1_DATA11	USB_OTG_OC	GPIO3_IO21	I2C1_SCL	
23	I2C3_SCL	NVCC_EIM0	F21	EIM_DATA17	ECSPI1_MISO	IPU1_DI0_PIN06	IPU1_CSI1_PIXCLK	DCIC1_OUT	GPIO3_IO17	**I2C3_SCL**	
24	I2C3_SDA	NVCC_EIM0	D24	EIM_DATA18	ECSPI1_MOSI	IPU1_DI0_PIN07	IPU1_CSI1_DATA17	IPU1_DI1_D0_CS	GPIO3_IO18	**I2C3_SDA**	
25	SD3_CMD	NVCC_SD3	B13	**SD3_CMD**	UART2_CTS_B	FLEXCAN1_TX			GPIO7_IO02		
26	32KHZ_CLK_OUT	NVCC_GPIO	R05	ESAI_TX5_RX0	**XTALOSC_REF_CLK_32K**	EPIT2_OUT	FLEXCAN1_RX	UART2_RX_DATA	GPIO1_IO08	SPDIF_SR_CLK	
27	SD3_CLK	NVCC_SD3	D14	**SD3_CLK**	UART2_RTS_B	FLEXCAN1_RX			GPIO7_IO03		
28	GND			Power							
29	SD3_DATA0	NVCC_SD3	E14	**SD3_DATA0**	UART1_CTS_B	FLEXCAN2_TX			GPIO7_IO04		
30	SD3_DATA1	NVCC_SD3	F14	**SD3_DATA1**	UART1_RTS_B	FLEXCAN2_RX			GPIO7_IO05		
31	SD3_DATA2	NVCC_SD3	A15	**SD3_DATA2**					GPIO7_IO06		
32	SD3_DATA3	NVCC_SD3	B15	**SD3_DATA3**	UART3_CTS_B				GPIO7_IO07		
33	SD3_DATA4	NVCC_SD3	D13	**SD3_DATA4**	UART2_RX_DATA				GPIO7_IO01		
34	SD3_DATA5	NVCC_SD3	C13	**SD3_DATA5**	UART2_TX_DATA				GPIO7_IO00		
35	SD3_DATA6	NVCC_SD3	E13	**SD3_DATA6**	UART1_RX_DATA				GPIO6_IO18		
36	SD3_DATA7	NVCC_SD3	F13	**SD3_DATA7**	UART1_TX_DATA				GPIO6_IO17		
37	CSI_D1M			CSI D1 Negative							
38	CSI_D1P			CSI D1 Positive							
39	CSI_D0M			CSI D0 Negative							
40	CSI_D0P			CSI D0 Positive							
41	CSI_CLK0M			CSI CLK Negative							
42	CSI_CLK0P			CSI CLK Positive							
43	CSI_D1M			CSI D1 Negative							
44	CSI_D1P			CSI D1 Positive							
45	CSI_D0M			CSI D0 Negative							
46	CSI_D0P			CSI D0 Positive							
47	CSI_CLK0M			CSI CLK Negative							
48	CSI_CLK0P			CSI CLK Positive							
49	GND			Power							
50	GND			Power							

Table 7 : J13 Signal Association and Alternate Functions

5 : Electrical characteristic

5.1 Absolute maximum ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

VINHIGH	5.5V to 21Vcc
3.3V pin input voltage (2)	-0.3V to 3.6V
Battery Voltage Input	-0.3V to 3.6V
3.3V pin output voltage (2)	-0.3V to 3.6V
Input clamp current for 3.3V pin (2)	±10mA
NVCC_SD3_FROM_EXP voltage (2)	-0.3V to 3.6V
NVCC_SD3_FROM_EXP powered pin input voltage (2)	-0.3V to NVCC_SD3_FROM_EXP +0.3V
NVCC_SD3_FROM_EXP powered pin output voltage (2)	-0.3V to NVCC_SD3_FROM_EXP +0.3V
Input clamp current for NVCC_SD3_FROM_EXP powered pin (2)	±10mA
Dedicated pin : RS232	±15V
Dedicated pin : CAN	±40V (CANH / CANL vs. GND)
Dedicated pin : RS485	-8V to +13V on I/O, short circuit protected
Dedicated pin : CSI and DSI	-0.3V to 2.7V
Power drawn from NVCC_3V3	600mA
Power drawn from GEN_5V	800mA
Power drawn from LVDS power	600mA
Power drawn from LVDS backlight (J3 closed)	800 mA

Table 8 : Absolute maximum ratings

(1) Stresses beyond those listed under “Absolute maximum ratings” may cause permanent damage to the board. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect board reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended operating conditions

VINHIGH	6.5V to 18Vcc
3.3V pin input voltage (2)	0V to 3.3V
Battery Voltage Input	0V to 3V
3.3V pin output voltage (2)	0V to 3.3V
Input clamp current for 3.3V pin (2)	±2mA
NVCC_SD3_FROM_EXP voltage (2)	0V to 3.3V
NVCC_SD3_FROM_EXP powered pin input voltage (2)	0V to NVCC_SD3_FROM_EXP
NVCC_SD3_FROM_EXP powered pin output voltage (2)	0V to NVCC_SD3_FROM_EXP
Input clamp current for NVCC_SD3_FROM_EXP powered pin (2)	±2mA
Dedicated pin : RS232	±12V
Dedicated pin : CAN	±12V (CANH / CANL vs. GND)
Dedicated pin : RS485	0 to 5V on I/O
Dedicated pin : CSI and DSI	0V to 2.5V
Power drawn from NVCC_3V3	400mA
Power drawn from GEN_5V	400mA
Power drawn from LVDS power	300mA
Power drawn from LVDS backlight (J3 closed)	400 mA

Table 9 : Recommended operating conditions

5.3 Power consumption and power dissipation

All measurements are done with an input voltage of 12V on a SOLO board with a Base file system and a 1920x1080 HDMI monitor.

- Boot phase : 230 mA ,(2.76W)
- Running : 280 mA during write, 210 mA during display (3.36W , 2.52W)
- Suspend to memory : 110 mA (1.32W)
- Standby to memory : 110 mA (1.32W)
- Freeze to memory : 140 mA (1.68W)

For the details of the low power modes consult the NXP i.MX 6Solo/6DualLite Applications Processor Reference Manual

5.4 LVDS relevant standards

- ANSI EIA-644-A. Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits.
- SPWG Notebook Panel Specification (V3.8 from 03/2007) .
- PSWG standards (Panel Standardization Working Group) - set of standards for panels using LVDS. All are available from http://www.vesa.org.
- Standard JEIDA-59-1999

5.5 HDMI relevant standards

- High-Definition Multimedia Interface Specification, Version 1.4a
- Digital Visual Interface, Revision 1.0
- HDMI Compliance Test Specification, Version 1.4a

5.6 USB relevant standards

- Universal Serial Bus Specification, Rev. 2.0 (Compaq, Hewlett-Packard, Intel,Lucent, Microsoft, NEC, Philips; 2000)
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification (Hewlett-Packard Company, Intel Corporation, LSI Corporation, Microsoft Corporation, Renesas Electronics Corporation,ST-Ericsson; 2012).

5.7 PCI express relevant standards

- PCI Express Base Specification, Revision 2.0 (including legacy 2.5-Gbps support)
- 5.0 Gbps data rate
- PCI Express Base Specification, Revision 1.1
- 2.5 Gbps data rate

5.8 SATA relevant standards (QUAD only)

- Serial ATA 3.0
- AHCI Revision 1.3
- AMBA 2.0 from ARM
- SATA 1.5 Gb/s and SATA 3.0 Gb/s speed
- eSATA (external analog logic also needs to support eSATA)

6 : Operational characteristics

6.1 : Development system requirements

From the NOVAsom Industries web site www.novasomindustries.com the user can download the NOVAsom SDK to ease the development process for all the NOVAsom Industries boards.
The NOVAsom P board is currently supported in all flavours (SOLO , DualLight and QUAD) at the boot level, and there is the standard BSP support in form of device tree blob, or DTB.
The NOVAsom SDK is a virtual machine tool, running on a Fedora 20 core and based on VirtualBox.
The Virtual Machine is thus compatible with hosts based on Windows™ , MacOS™ or Linux machines.
More detailed information aboaut the installation process of the NOVAsom SDK can be found visiting the NOVAsom Industries web site at www.novasomindustries.com .
Normally, for a relatively relaxed development, an I5 host with 60 GBytes of free hard disk space and 8GBytes of RAM is enough.
For very heavy developments (as a complex 3D supported Qt file system or a Chromium X based application) “the bigger is better”, so more RAM you can dedicate to the Virtual Machine the faster the Virtual Machine will run.
A more than good situation is an I7 host with 16GB of RAM and 128GB of free disk space.
For connecting to the NOVAsom P console you need a serial port, and considering that on modern desktop the serial port is not present a USB to Serial adapter is probably the only choice you have.
Finally, you need a uSD written with a basic file system, and a way to physically write the uSD itself.
You can download a uSD image from the www.novasomindustries.com page in the NOVAsom P dedicated section, where you can find all the information about how to write a uSD from the NOVAsom P image you just downloaded using your preferred host system.

6.2 : The NOVAsom P console

In order to use the serial console available on the NOVAsom P board you need a serial terminal.
GtkTerm is a good choice for Linux users, Teraterm is a nice choice for Windows™ users, it's up to MacOS™ users to understand which kind of terminal application they need.
The NOVAsom P port is a standard RS232 serial port with a bit rate of 115200 with no flow control and 1 stop bit.
The pins from where to connect the serial port are pin 13 of J9 (TXD from NOVAsom P board), pin 14 of J9 (RXD to NOVAsom P board) and pin 16 of J9 (the GND connection), respectively connected to the pins 2 ,3 and 5 of a 9 pins DB connector, normally found on USB to Serial adapters.
Just plug both the power supply and the serial port and you will see the boot process of your new NOVAsom P board.

6.3 : The first boot

The steps in order to boot your NOVAsom P board are :

- Create the uSD with a standard file system as described in chapter 6.1 above
- Insert the just written uSD in the J6 slot (note this is a push-push connector, avoid to extract the uSD forcing it or you can break the J6 uSD slot)
- Connect the serial port to your NOVAsom P
- Insert an appropriate power source chord in the J5 connector and power it on.

After just some half a second you should see on your terminal application something similar to what you see in Figure 2 below, and this means you have your NOVAsom P powered up and running.

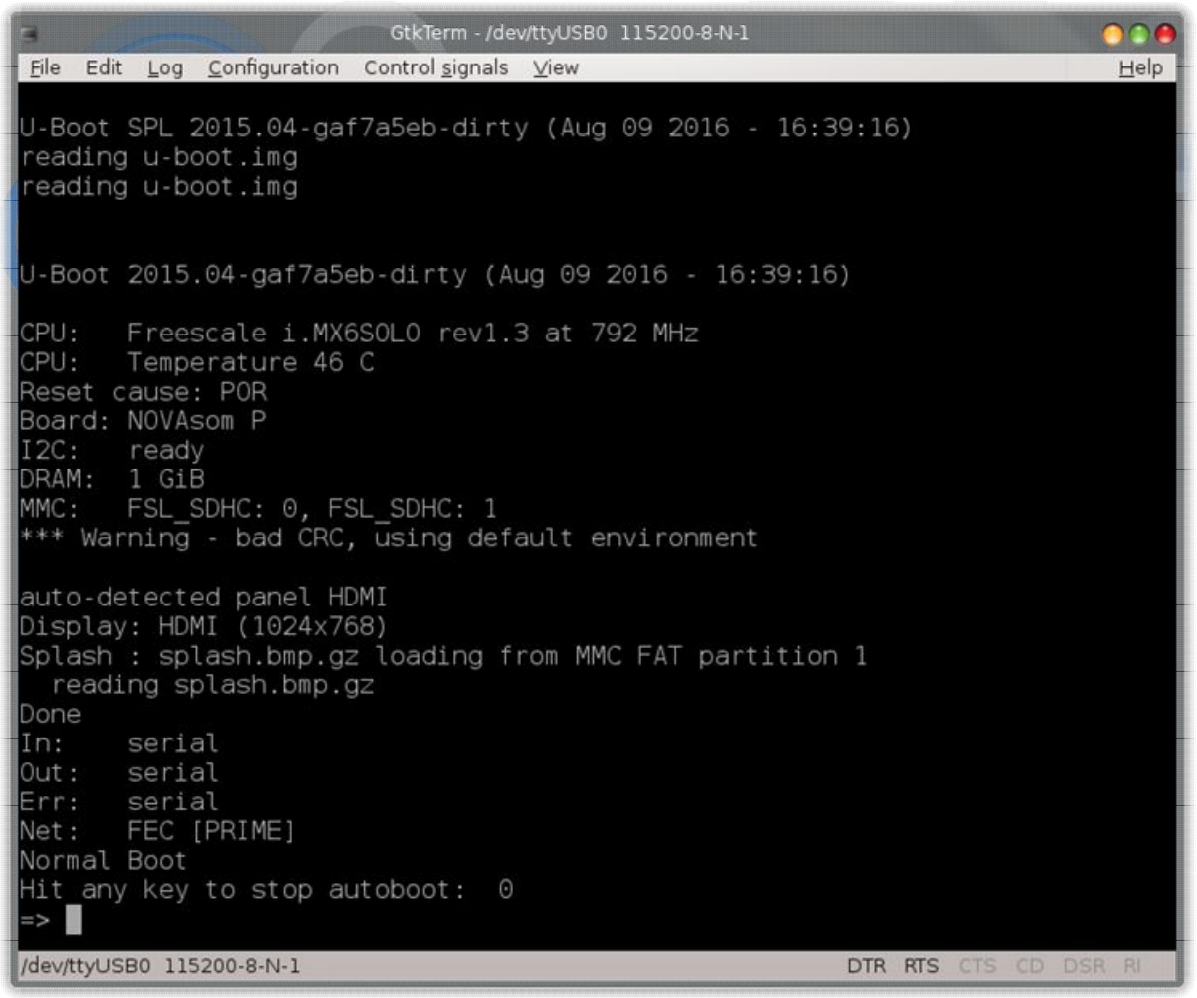

Figure 3 : The NOVAsomP first boot

A special note about the uSD slot : the uSD slot has not been designed to insert or remove the uSD card with power applied, so inserting or removing a uSD card with applied power may result in a permanent damage to the card or, worst, to the NOVAsom P board.
The card MUST be inserted without power applied.
The presence switch that equips the uSD slot of the NOVAsom P board signals to the processor that a card is in the slot, thus allowing the boot process to read the bootloader from the uSD slot.
If the card is not found when the power is applied the boot process will look in eMMC chip for a valid bootloader code but remember that the presence of the eMMC depends on the NOVAsom P board equipment.
In case of a NOVAsom P board with eMMC there are all the information and all the scripts to download the image on the eMMC, thus allowing the boot without a uSD inserted.

6.4 : Connections to J9 and J13

J9 and J13 sports a lot of signals, and most of them are connected at the processor level without buffering or protection.
Although the processor is quite protected on over and under voltages, care should be taken in order to avoid to stress the processor outside the recommended operating conditions, or permanent damages will result on the processor itself.
It's quite common to overtake a ringing digital signal that stresses the processor outside the recommended operating conditions, so if you are in doubt use dump series resistors in the order of 1 KΩ for input signals.
If you intend to use the standard 3.3V on all the ports marked with the orange box in tables 4.3 and 4.4 you can simply short the pin 2 and pin 4 of J9, thus effectively powering all these pins with the NOVAsom P board 3.3V power supply.
In the tables 4.3 and 4.4 the signals are named as the standard DTB factory functions, and the colored functions are the functions provided by the standard DTB factory functions.
You can find all the information on how to change a pin function visiting the www.novasomindustries.com page in the NOVAsom P dedicated section, where you can find a lot of application notes and already developed tools and examples.
All the J9 and J13 signals marked with yellow boxes are "special" signals, this means they are at different voltage levels from the standard 3.3V.
As an example, the RS232 signals (AUX_RS232_TXD and AUX_RS232_RXD) are at RS232 level, so suitable to be connected with a standard serial port.
The same is for all the signals characterized by a yellow box such as RS485, CAN, CSI/DSI and USB that are at their own voltage level.
A special note on the OTG signals : they are minded to be connected directly to a µUSB connector, so the ESD protection are provided at the NOVAsom P board level.
Finally, on J9 and J13 there are two signals that behaves differently from the standard or "special" I/O signals.

This signals are :

- ONOFF_IMX6 : behind request, and only when a battery is connected to J8, a NOVAsom P board can be equipped with this functionality to power up / power down the board itself. Normally this function is an option. This pin has an internal pullup of 10KΩ to some 3V, and the external signal MUST BE an open collector / open drain signal. Overdriving this pin can result in a permanent damage to the processor.
- EXT_RESET : bringing this pin to a logic low level will reset the board. This signal is level sensitive, so as long as this signal is low the board will remain in the reset state. This pin has an internal pullup of 10KΩ to some 3V, and the external signal MUST BE an open collector / open drain signal. Overdriving this pin can result in a permanent damage to the processor.

6.5 : Connecting an external battery to the NOVAsom P board

The connector J8 is minded to connect a 3V external battery.
The external battery will be used on systems that need to maintain the date and time information when the power is removed or if you have a system that must be powered off as described in the previous chapter and makes use of the ONOFF_IMX6 signal.
The battery is connected directly to SNVS powered RTC of the i.MX6 processor, so the power drawn from the battery is quite a bit high, some 50 µA in the worst temperature/load case.
Compared with a standard RTC chip is some 50 times higher, so you need to choose an adequate battery for your application.
On the other hand, the battery can be of a rechargeable type (LiIon or Lithium coin cell) and will be charged through a 470Ω resistor from the 3.3V supply.
Care should be taken to connect the correct battery (a 3V battery is requested, higher voltages will immediately destroy the processor on your NOVAsom P board) and connect the battery in the correct way, where the pin 1 of J8 is the positive and the pin 2 is the negative. A power inversion can permanently damage the battery or, worst, damage the processor of your NOVAsom P board.
In Table 1 you can find the mating connector for the J8 connector.

6.6 : Developing a NOVAsom P extension board

The i.MX 6SOLO/DualLight/6QUAD contains a limited number of pins, most of which have multiple signal options. These signal to pin and pin to signal options are selected by the input/output multiplexer called IOMUX.
The IOMUX is also used to configure other pin characteristics, such as voltage level, drive strength, and hysteresis.

Due to this, all the I/O pins on J9 and J13 behave as input at power up, and until the bootloader or the kernel are up and running, they are substantially configured as input.
All the inputs have an internal 100kΩ pull up to the VCC rail, whichever the VCC is.
Keeping this in mind, all the pins that are configured to be an output needs a pull down resistor in the range of 15kΩ in order to keep the particular signal at the low level, if needed.
This is true for all the I/O pins marked with the green or orange box in Table 3 for J19 and Table 4 for J13.
Conversely, all the pins marked with the yellow box in Table 3 and Table 4 doesn't need external pull up or pull down, but require correct impedance matching depending of the line characteristics of the function the pin is associated to, so you should observe the basic recommendation in Table 10.

If you plan to power the NOVAsom P board through the VINHIGH pin (pin 1 of both J9 and J13) consider the insertion of an appropriate choke for EMI filtering. Pay attention on VINHIGH polarity and limits, as the VINHIGH is after the inversion protection diode D8 on the NOVAsom P board. A wrong VINHIGH connection will immediately destroy the NOVAsom P board. In Figure 4 you can see the input power schematic part of the NOVAsom P board.

The following Table 10 indicates the recommendations of the special function pin.

Signal Group	Recommendations
USB: USB_OTG_DP, USB_OTG_DN, USBDN_DP2, USBDN_DM2, USBDN_DP3, USBDN_DM3 : 90 Ω impedance	• Route the high speed clocks and the DP and DM differential pair first. • Route DP and DM signals on the top or bottom layer of the board • The trace width and spacing of the DP and DM signals should be such that the differential impedance is 90 Ω. • Route traces over continuous planes (power and ground). — They should not pass over any power/GND plane slots or anti-etch. — When placing connectors, make sure the ground plane clearouts around each pin have ground continuity between all pins. • Maintain the parallelism (skew matched) between DP and DM; these traces should be the same overall length. • Do not route DP and DM traces under oscillators or parallel to clock traces and/or data buses. • Minimize the lengths of high speed signals that run parallel to the DP and DM pair. • Keep DP and DM traces as short as possible. • Route DP and DM signals with a minimum amount of corners. Use 45-degree turns instead of 90-degree turns. • Avoid layer changes (vias) on DP and DM signals. • Do not create stubs or branches. • Ferrite beads should NOT be placed on the USB D+/D– signal lines as this can cause USB signal integrity problems. For radiated emissions problems due to USB, a common mode choke may be placed on the D+/D– signal lines. However, in most cases, it should not be required if the PCB layout is satisfactory. Ideally, the common mode choke should be approved for high speed USB use or tested thoroughly to verify there are no signal integrity issues created.
MIPI CSI: CSI_D0M, CSI_D0P, CSI_D1M, CSI_D1P, CSI_CLK0M, CSI_CLK0P : 100 Ω impedance	• Route CSI_DxM / CSI_DxP and CSI_CLK0M / CSI_CLK0P signals on the top or bottom layer of the board • The trace width and spacing of the CSI_DxM / CSI_DxP

	and CSI_CLK0M / CSI_CLK0P signals should be such that the differential impedance is 100 Ω. • Route traces over continuous planes (power and ground). They should not pass over any power/GND plane slots or anti-etch. When placing connectors, make sure the ground plane clear outs around each pin have ground continuity between all pins. • Maintain the parallelism (skew matched) between CSI_DxM / CSI_DxP and CSI_CLK0M / CSI_CLK0P signals; these traces should be the same overall length. • Do not route CSI_DxM / CSI_DxP and CSI_CLK0M / CSI_CLK0P traces under oscillators or parallel to clock traces and/or data buses. • Minimize the lengths of high speed signals that run parallel to the CSI_DxM / CSI_DxP and CSI_CLK0M / CSI_CLK0P pair. • Keep CSI_DxM / CSI_DxP and CSI_CLK0M / CSI_CLK0P traces as short as possible. • Route CSI_DxM / CSI_DxP and CSI_CLK0M / CSI_CLK0P signals with a minimum amount of corners. Use 45-degree turns instead of 90-degree turns. • Avoid layer changes (vias) on CSI_DxM / CSI_DxP and CSI_CLK0M / CSI_CLK0P signals. • Do not create stubs or branches.
MIPI DSI: DSI_D0M, DSI_D0P, DSI_D1M, DSI_D1P, DSI_CLK0M, DSI_CLK0P : 100 Ω impedance	• Route DSI_DxM / DSI_DxP and DSI_CLK0M / DSI_CLK0P signals on the top or bottom layer of the board • The trace width and spacing of the DSI_DxM / DSI_DxP and DSI_CLK0M / DSI_CLK0P signals should be such that the differential impedance is 100 Ω. • Route traces over continuous planes (power and ground). They should not pass over any power/GND plane slots or anti-etch. When placing connectors, make sure the ground plane clear outs around each pin have ground continuity between all pins. • Maintain the parallelism (skew matched) between DSI_DxM / DSI_DxP and DSI_CLK0M / DSI_CLK0P signals; these traces should be the same overall length.

	• Do not route DSI_DxM / DSI_DxP and DSI_CLK0M / DSI_CLK0P traces under oscillators or parallel to clock traces and/or data buses. • Minimize the lengths of high speed signals that run parallel to the CSI_DxM, CSI_DxP and the CSI_CLK0M and CSI_CLK0P pair. • Keep DSI_DxM / DSI_DxP and DSI_CLK0M / DSI_CLK0P traces as short as possible. • Route DSI_DxM / DSI_DxP and DSI_CLK0M / DSI_CLK0P signals with a minimum amount of corners. Use 45-degree turns instead of 90-degree turns. • Avoid layer changes (vias) on DSI_DxM / DSI_DxP and DSI_CLK0M / DSI_CLK0P signals. • Do not create stubs or branches.
Driver based logic : CONSOLE_RS232_TXD, CONSOLE_RS232_RXD, AUX_RS232_TXD, AUX_RS232_RXD, CANH, CANL, RS485_TX-,RS485_TX+,RS485_RX-,RS485_RX+,USB_OTG_VBUS	No particular attention
I2C buses : I2C1_SCL, I2C1_SDA, I2C3_SCL, I2C3_SDA	No particular attention. The pull up resistor are on board, so they are not needed. Keep in mind that I2C1_SCL and I2C1_SDA are powered from the NVCC_SD3_FROM_EXP pin, so in the absence of NVCC_SD3_FROM_EXP the I2C1 bus will not function properly.

Table 10 : Groups recommendations

Also, keep in mind that the track length on the MIPI_CSI and MIPI_DSI group must have equal lengths, to avoid differences in data lines and clocks.

Here there are some basic rules for the correct interfacing to J9 and J13 :

- Don't overdrive an input pin : e.g., if the pin is powered from external NVCC_SD3_FROM_EXP that is powered by 1.8V don't drive the pin with a 3.3V logic. Avoid to drive a normally powered 3.3V pin with values that exceeds those defined in Table 9 : Recommended operating conditions.
- Pay attention to overshoot or undershoot, and if present use a damp resistor in the range of 100 Ω to 1K Ω in series. The internal protection of the i.MX6 will do the rest.
- Understand the idle logic level (e.g. during reset) and use the appropriate pull up or pull down if needed, in the range of 15kΩ. The i.MX6 processor has an internal pull up of 100 kΩ at power up on all I/O pins, so during the reset phase and for all the boot phases the I/O pins of the i.MX6 will float high. For example, if you drive an external load activated with a low level, you will get a logic one on the I/O pin until the kernel has not defined this is an output pin (some 5 to 12 seconds after power is applied, depending on file system size), so you will have your load activated during all the

boot phases.

- Avoid short circuits between pins or between pins and power, even for limited time. Although the i.MX6 is quite well protected, this rises power dissipation, may lead to pin breaks or worst and in any case is not a good practice.
- Check thoroughly the impedance matching and trace lengths on the “special” signals listed in Table 10.
- Select the right output strength in the DTB file of your BSP and avoid using excessive strength for signals that don’t need this. Also, consider carefully the FAST output mode, as this leads to EMI problems and ring on not well matched traces.
- Never drive EXT_RESET or ONOFF_IMX6 with totem pole output. Drive this pins with an open drain driver (a 2N7002 mosfet is more than enough).
- Pay attention on VINHIGH polarity and limits, as the VINHIGH is after the inversion protection diode D8 on the NOVAsom P board. A wrong VINHIGH connection will immediately destroy the NOVAsom P board. In Figure 4 you can see the input power schematic part of the NOVAsom P board.

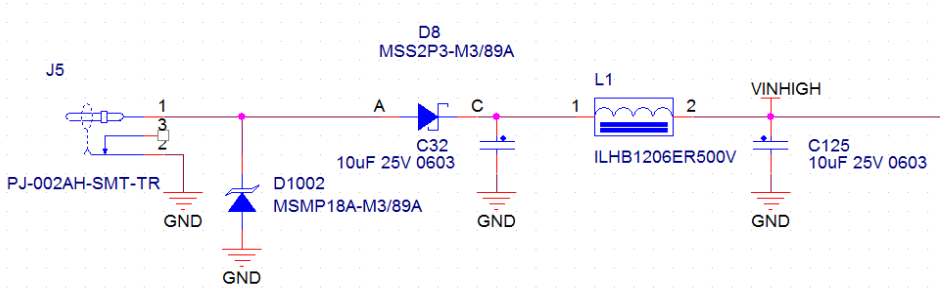

Figure 4 : Power input section

- If you don’t need the NVCC_SD3_FROM_EXP powered I/O you can leave the pin NVCC_SD3_FROM_EXP unconnected, or connected to ground.
- The I2C lines (I2C1_SCL, I2C1_SDA, I2C3_SCL, I2C3_SDA) has a 3.3KΩ pull ups on the NOVAsom P board to their own power. I2C1 bus is referenced to NVCC_SD3_FROM_EXP, so it will not function properly when NVCC_SD3_FROM_EXP is absent or tied to ground. Avoid to place additional pull ups on the I2C lines, as this may lead to malfunctioning due to excessive load.
- The USB HOST channels on J9 (USBDN_DP2, USBDN_DM2, USBDN_DP3, USBDN_DM3) has already the power protections and management on the the NOVAsom P board , and can be driven using a schematic like the one in the following Figure 5 (USBDN_DP2, USBDN_DM2 is shown, but the same can be used for USBDN_DP3, USBDN_DM3 with the USB_PWR3 signal).

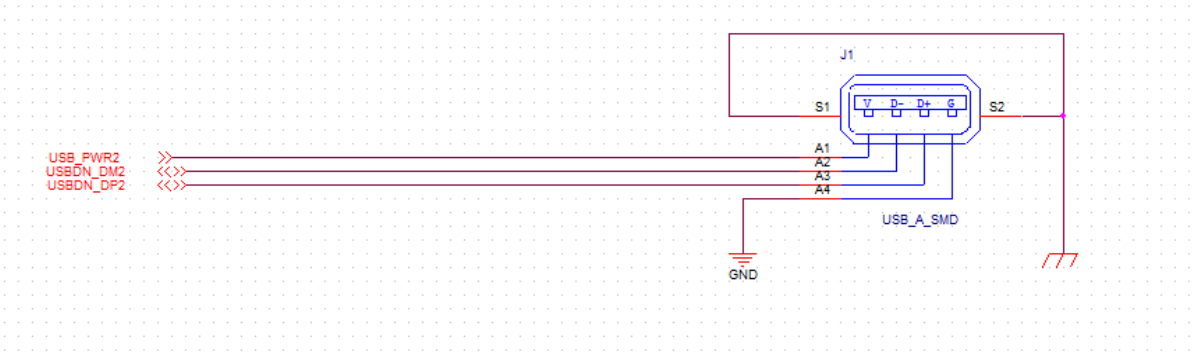

Figure 5: USB Host example

- The USB OTG channel on J9 (USB_OTG_DN, USB_OTG_DP) has no power protections. There is no connections with the OTG ID signal, so it can be left floating on the connector side. The OTG can be driven using a schematic like the one in the following Figure 6 (Note : U1 is optional, the power on the V+ pin of the connector is powered from a 5V with a series 33Ω) :

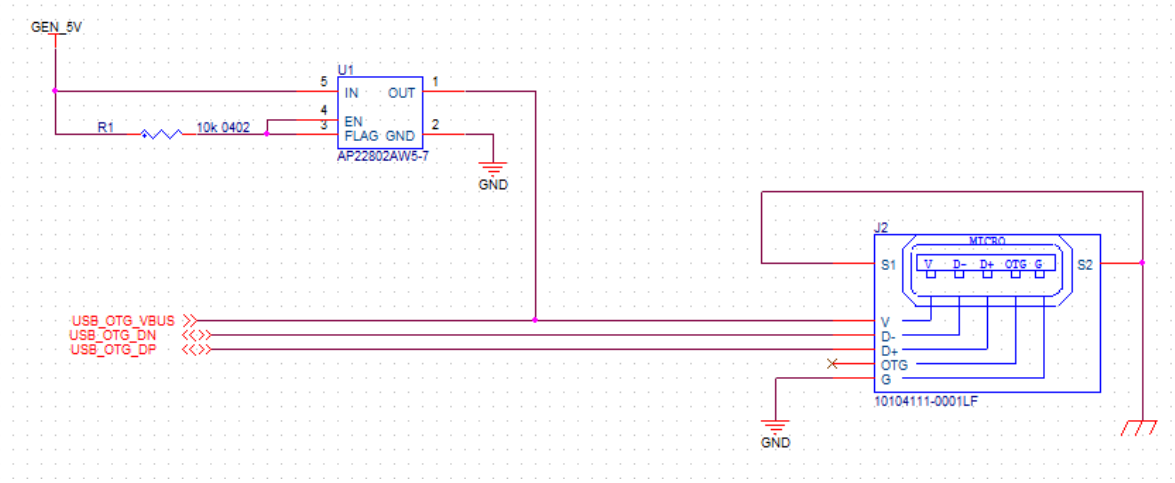

Figure 6 : USB OTG example

With these simple hints you will successfully design your own Extension board.

7 : Board outline and mechanical dimensions

Detailed drawings, 3D drawings, full mechanical specifications and additional information can be found visiting the www.novasomindustries.com page in the NOVAsom P dedicated section or contacting the appropriate sales person or distributors.

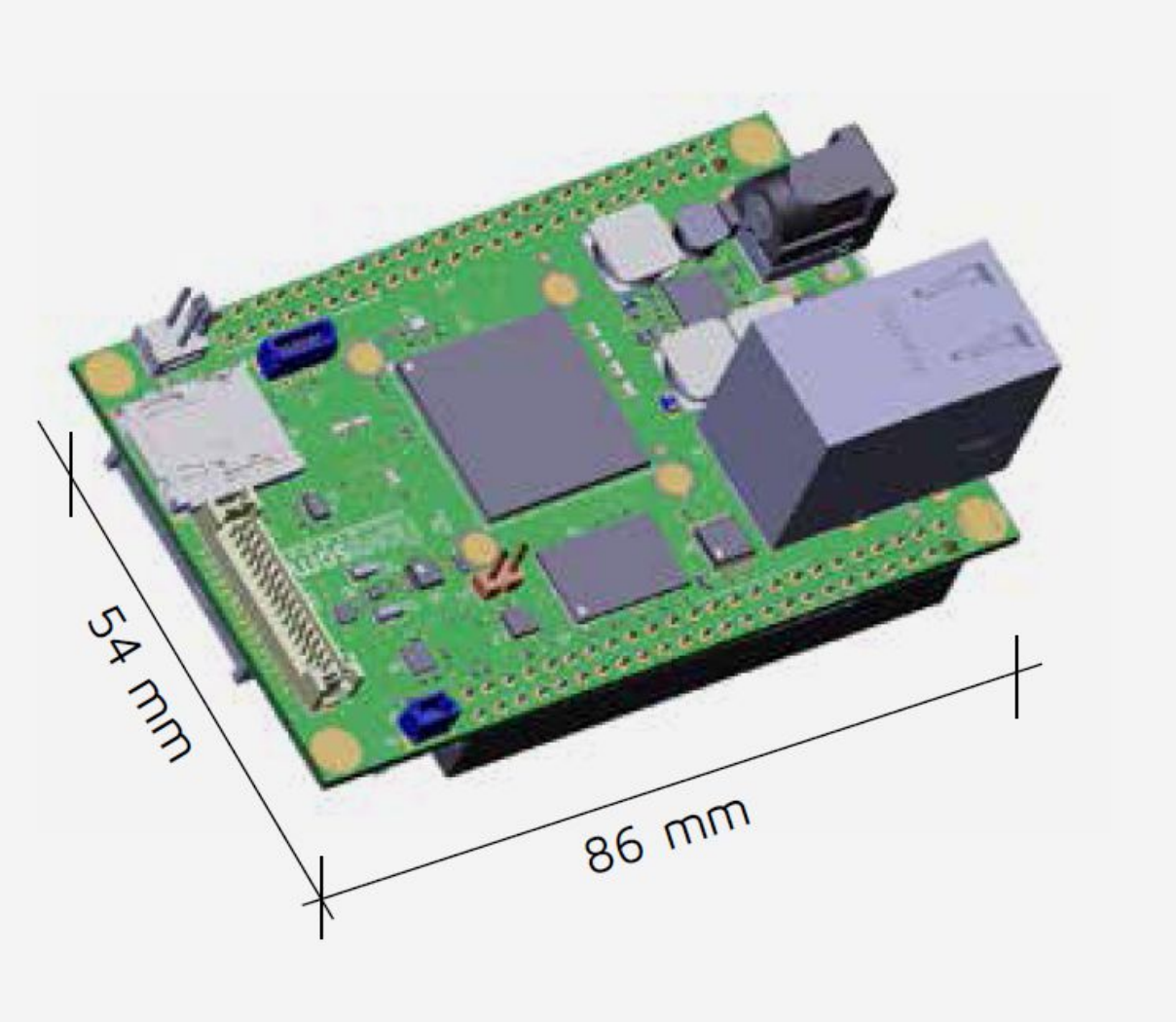

Figure 7 :The NOVAsom P in 3D

8 : Trobleshooting

Here you can find a very basic list of things that can happen at the unexperienced user at the very first boot.
In case of hardware failure contact us at www.novasomindustries.com for additional support and follow carefully the instructions.

Power is applied but I can't see anything on the terminal output.	• Check your uSD has been correctly inserted in J6 slot and power is applied. • Check your uSD has been correctly written. The uSD has an initial FAT partition, so you can check if it's correctly written on a Windows™ , MacOS™ or Linux machine. If you can't read the uSD this means it is broken or badly written, try to rewrite it or substitute it with a new one. • Check if the green led D11 (power) is on. If it's not on check your power supply voltage, current and wire orientation. Protections on the NOVAsom P board permit you to connect an inverted power, but not on overvoltage, so be careful. An undervoltage situation will not damage the NOVAsom P board, an overvoltage will damage your NOVAsom P board for sure. • Check if the green led D9 (heartbeat) blinks. If the steps above are checked this should indicate an hardware failure. • Check the connection with your serial port or the application you use as a terminal are correct. If still you don't find anything wrong this should indicate an hardware failure.
I see the terminal but I have no connection with the network	Check your cables and your connectivity, maybe you need to ask your network administrator. The NOVAsom P base image has a dhcp client active, so you need an accessible dhcp server to effectively use the network interface. If still you don't find anything wrong this should indicate an hardware failure.

I can't see any video on the HDMI monitor	Check your log (on the terminal the command is *dmesg | grep HDMI)*. If the result doesn't contain *Detected HDMI controller* check your cable and your monitor settings (note that some HDMI to VGA adapter exhibits this behavior if not externally powered). If still you don't find anything wrong this should indicate an hardware failure.
I can't see any video on the LVDS monitor	• Check the voltage levels for the LCD power supply and the backlight power supply. • Check your DTB has a correct description of the LCD panel and the timings. • Check your DTB defines correctly the PWM output. • If still you don't find anything wrong and you are sure your panel is not broken this should indicate an hardware failure.
I can't detect my mPCIe board	• Check that your board is not broken. • Check that your board can be run with 1.45V on the 1.5V power rail. Note that this power rail can be powered at 1.35V in case of LP-DDR, so check the board complies to this too. Most of the mPCIe cards like WiFi or LAN doesn't make use of this power rail, but check with the manufacturer of the mPCIe card to understand if this feature is compatible. • Check your log (on the terminal the command is *dmesg | grep pcie)*. If the result doesn't contain a lot of messages related to the PCI windows normally allocated for a mPCIe and doesn't contain *link down* the root cause can be a kernel without the PCIe enabled or an hardware failure.

Table 11 : Troubleshooting

9 : Contacts

Web page : www.novasomindustries.com

10 : Document revisions, references and notes

10.1 Document revisions

NI150316-HUM-P-V1.0	11/04/2017 Updates

10.2 External references

For the NOVAsom Industries products and NOVAsom P in detail : www.novasomindustries.com

For the i.MX processors : NXP i.MX 6Dual/6Quad Applications Processor Reference Manual

NXP i.MX 6Solo/6DualLite Applications Processor Reference Manual

NXP i.MX BSP Porting Guide

10.3 Notes

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates.
It is your responsibility to ensure that your application meets with your specifications.
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