EE 230: Analog Circuits Lab
Lab No. 10 - 11
Differential Operational Amplifier

Anupam Rawat, 22b3982

March 28, 2024

1 Differential Amplifier with Resistive Load

1.1 Aim of the experiment

The aim of this experiment is to design and analyze a basic differential amplifier with a resistive load.

1.2 Design

1.2.1 Required Specifications of the Device:

- Gain 12 dB
- $V_{in,cm(min)} = 3.5$V
- 5V $< V_{out,cm} <$ 7V

1.2.2 Device Specifications:

NMOS:

- $K_n{}' = 106\mu A/V^2$
- $\frac{W}{L} = 5$
- $K_n = 0.53mA/V^2$
- $V_{th,n} = 0.45$V

PMOS:

- $K_p{}' = 80\mu A/V^2$
- $\frac{W}{L} = 5$
- $K_p = 0.16mA/V^2$
- $V_{th,p} =$ -0.5V

1.2.3 Circuit Design:

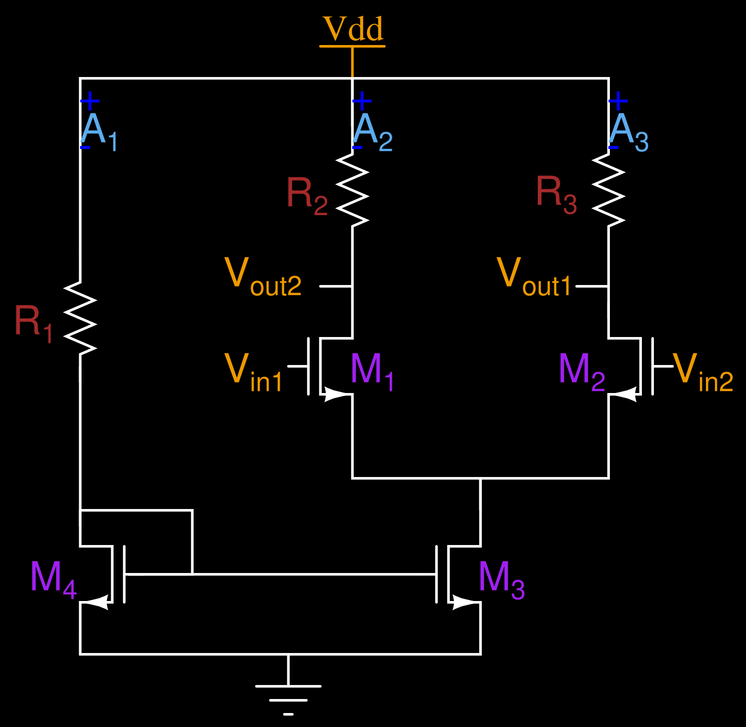


Figure 1: Differential Amplifier with Resistive Load

1.2.4 Equations:

$$V_{in,cm(min)} = V_{GS1} + V_{dsat3} \tag{1}$$

$$V_{in,cm(min)} = V_{TH1} + \sqrt{\frac{I_{tail}}{K_{n1}}} + \sqrt{2 \cdot \frac{I_{tail}}{K_{n3}}} \tag{2}$$

$$A_v = gm1 \cdot R_2 \tag{3}$$

$$A_v = \sqrt{I_{tail} \cdot K_{n1}} \cdot R_2 \tag{4}$$

$$V_{out,cm} = V_{DD} - \frac{I_{trail} \cdot R_2}{2} \tag{5}$$

1.3 Simulation Results:

Using , Equation(1) we get, $I_{tail} = 0.845$ mA.

Using, $V_{in1} = V_{in2} = 4.5$V and $V_{dd} = 10$V.
Let $A_v = 15\text{dB} = 20 \cdot \log_{10}(\frac{V_{o,d}}{V_{in,d}})$

We get, $I_{tail} = 0.85$mA. Let $I_{ref} = 1$mA.
It can be seen from figure 1 that current through $M_4 = 1$mA,
$V_{G4} = V_{D4} = 1.94 + V_{th,n} \approx 2.40V$.
Thus, $R_1 = \frac{V_{DD} - V_{D4}}{I_{ref}} = \frac{10V - 2.4V}{1mA} = 7.61l\Omega$

For current mirror circuit, $I_{tail} = I_{ref} = 1$mA.
And in common mode, $I_{d1} = I_{d2} = 0.5$mA. Thus, $V_{S1} = V_{D3} = 2.68$V

For M_4, V_{DS3} - $V_{(GST)3} = 0.93$V. Hence M_4 is in saturation.

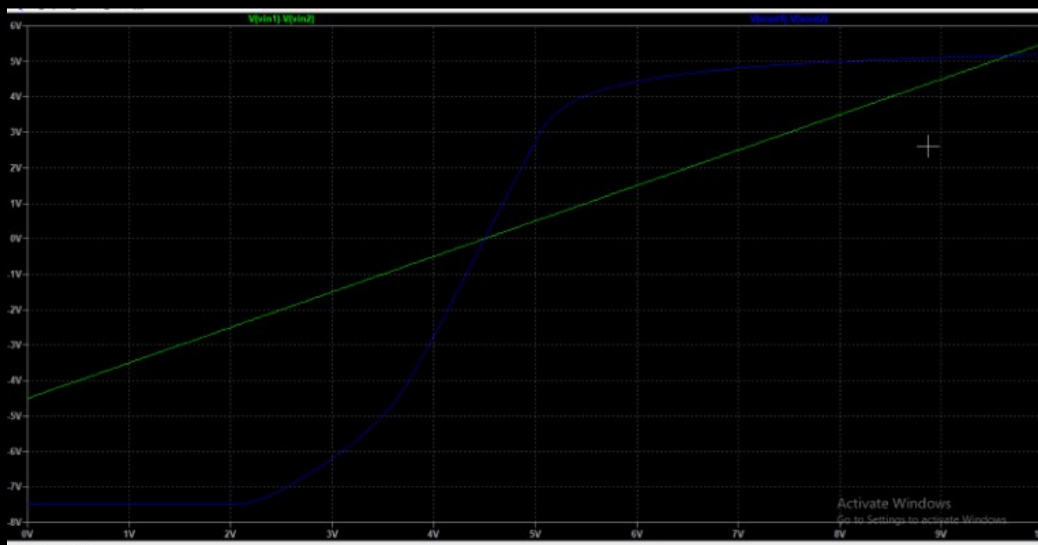
From equation(3) and equation(4), we obtain, $R_2 = 7.72\ k\Omega$

From equation(5), $V_{D1} = V_{D2} = 6.14$V, satisfying, $5V < V_{out} < 7V$.

1.3.1 Values Calculated From this Simulation Section:

$R_1 = 7.61\text{k}\Omega$ and $R_2 = R_3 = 7.72k\Omega$ $V_{out,cm} = V_{d1} = V_{d2} = 6.14$V.
$I_{tail} = I_{ref} = 1$mA $V_{D3} = V_{S1}/2 = 2.68$V
M_1, M_2, M_3, M_4, all are operating in saturation region.

1.3.2 Simulation Results (Images):



1.4 Experiment Results

	Calculated Value	Simulation Result	Experimental Result
I_{tail}	1mA	1.0031mA	0.97mA
I_{ref}	1mA	1.0013mA	1.01mA
$V_{out,cm}$	6.14V	6.13V	6.08V
V_{D3}	2.68V	2.683V	2.21V
$I_{d1} = I_{d2}$	0.5mA	0.5mA	0.51mA
$V_{G4} = V_{G3}$	2.40V	2.38V	2.3V

As it can be seen from the tabulated values, that the (hand) calculated values, values calculated by simulation and the values calculated from experimentation are all very close.

Also, $V_{out,AC} = 56\text{mV}$ and $V_{in,AC} = 10\text{mV}$; $A_v = \frac{V_{out,AC}}{V_{in,AC}} = 5.6$

1.5 Experiment completion status

This experiment was completed within the lab itself in its entirety.

2 Differential Amplifier with Active Load

2.1 Aim of the experiment

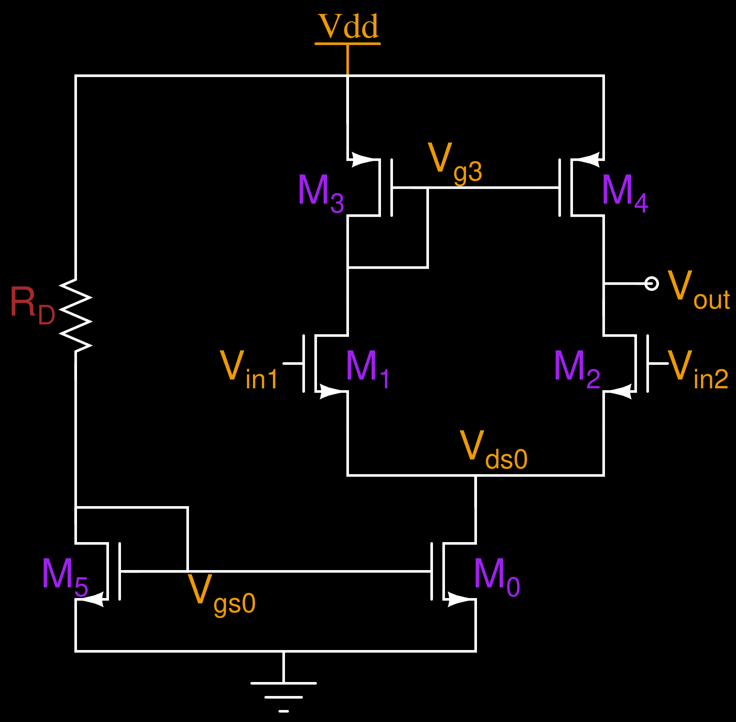
The aim of this experiment is to design, simulate, and implement a differential amplifier with an active load (Five Transistor OTA).

2.2 Design

2.2.1 Required Specification:

- $V_{out,DC} = 6$V
- $V_{dd} = 10$V.

2.2.2 Circuit Design:



2.2.3 Equations:

$$gain = -gm1(r_{o2}||r_{o4}) \tag{6}$$

$$V_{out} = V_{g3} \quad V_{g3} = V_{DD} - V_{sg3} \quad V_{sg3} = \sqrt{\frac{I_o}{K_{n3}}} + V_{th3} \tag{7}$$

$$V_{g3} = V_{DD} - \sqrt{\frac{I_o}{K_{n3}}} - V_{th3} \tag{8}$$

$$V_{in,cm(min)} = \sqrt{2 \cdot \frac{I_o}{K_{n3}}} + \sqrt{\frac{I_o}{K_{n1}}} + V_{th1} \tag{9}$$

$$V_{in,cm(max)} = V_{out,dc} + V_{th1} \tag{10}$$

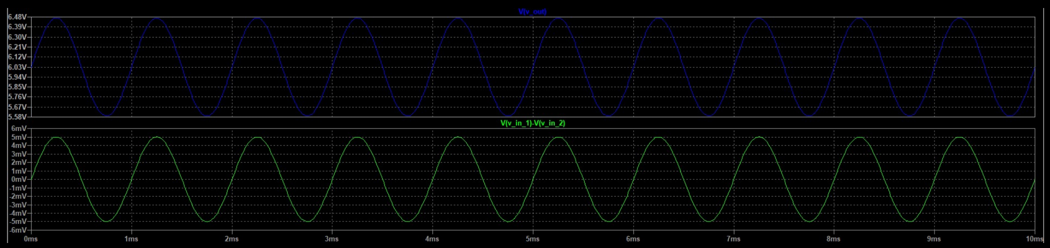
2.3 Simulation Results:

2.3.1 Calculated Values:

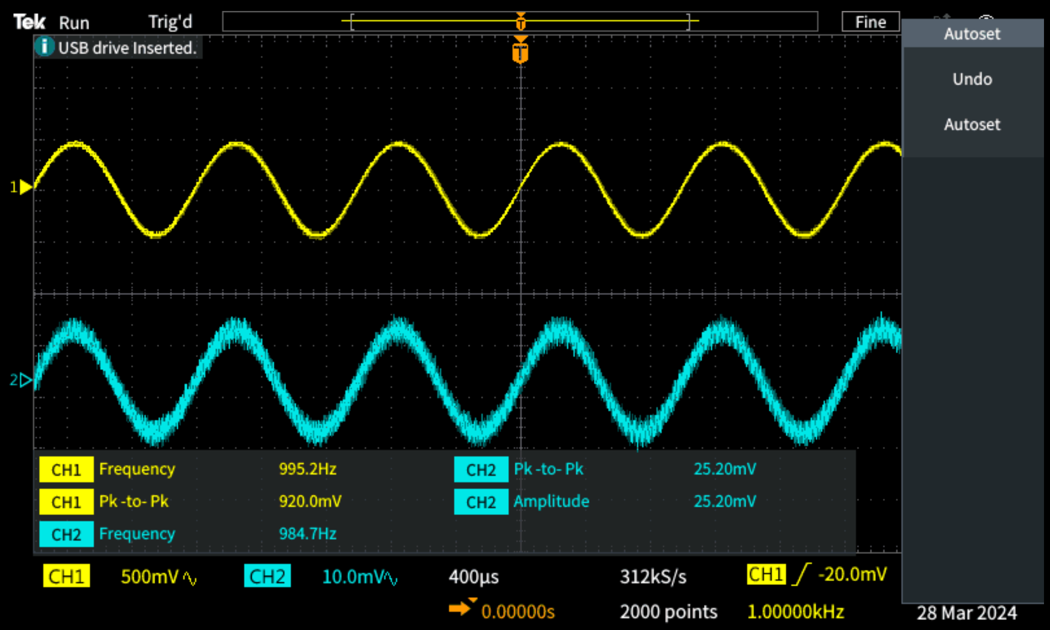
Using the equations, we obtained the following values:

- $I_o = 1.96$mA • $V_{in,cm(min)} = 5.09$V • $V_{in,cm(max)} = 6.45$V
- Let $V_{in,cm} = 6$V and also $I_{ref} = I_o = 1.96$mA
- $V_{(GST)5} = 2.719$ V • $V_{(GS)5} = V_{(DS)5} = 3.17$V.
- $r_{o2} = 170.07k\Omega$ $r_{o4} = 170.07k\Omega$
- $R_D = 3.48\ k\Omega$ R_D = -86.67 = 38.76 dB

LTSpice Simulation Results:



Results from DSO (Circuit Simulation):



2.4 Experiment Results

	Calculated Value	Simulation Result	Experimental Result
$V_{in,cm}$	6V	6V	6.09V
$V_{out,cm}$	6V	6.03V	6.26V
I_{ref}	1.96mA	1.966mA	2mA
I_{copy}	1.96mA	1.9716mA	1.98mA
$I_{d1} = I_{d2}$	0.98mA	0.985mA	1mA
V_{ds0}	3.63V	3.6351V	3.08V
V_{g3}	6V	6.030V	6.47V
V_{out2}	6V	6.030V	6.26V

Also, $A_v = \frac{V_{out,AC}}{(V_{in1}-V_{in2})_{AC}} = \frac{0.865V}{10mV} = 86.5$
DSO Measurements : • $V_{in1} = 24\text{m}V_{pp}$ $V_{out} = 920\text{m}V_{pp}$
Phase Shift between V_{in1} and $V_{out} = 180°$
Differential Gain $= \frac{920}{40} = 23$

2.5 Experiment completion status

This experiment was completed entirely in the lab.

3 Some Application design around Five Transistor OTA

3.a Unity Gain Amplifier:

3.a.1 Aim of the experiment

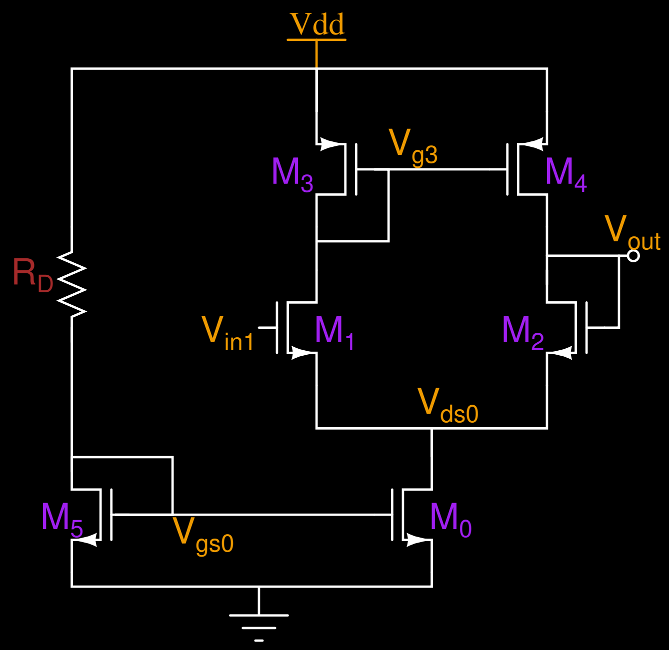
The experiment aims to build and analyze a unity gain buffer circuit using the Five Transistor OTA.

3.a.2 Design:

3.a.2.A Circuit Input Conditions:

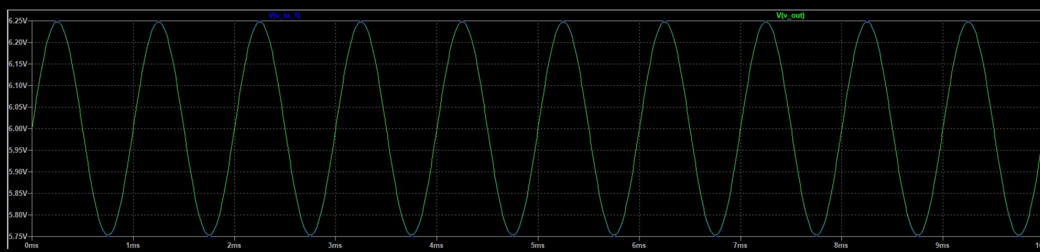
- V_{in1} = 500mV_{pp} with 1kHZ.
- $V_{in,cm}$ = +6V.

3.a.2.B Circuit Design:

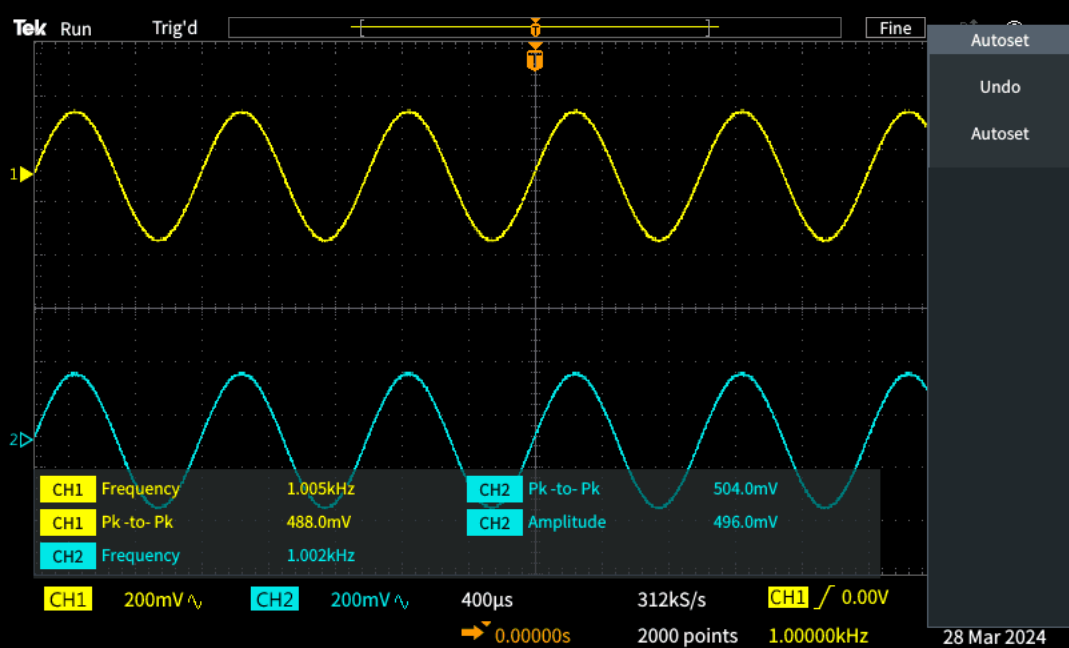


3.a.3 Simulation Results:

LTSpice Simulation Results:



Results from DSO (Circuit Simulation):



3.a.4 Experimental Results:

We conclude that, V_{out} and V_{in1} are completely same even in terms of amplification and phase shift.

3.a.5 Conclusion and Inferences:

Since, we obtain the V_{out} and V_{in1} to be completely in sync in all terms, we can conclude that this is a unity gain amplifier.

3.a.6 Experiment Completion Status:

This experiment was completed within the lab itself in its entirety.

3.b Inverting Amplifier:

3.b.1 Aim of the experiment

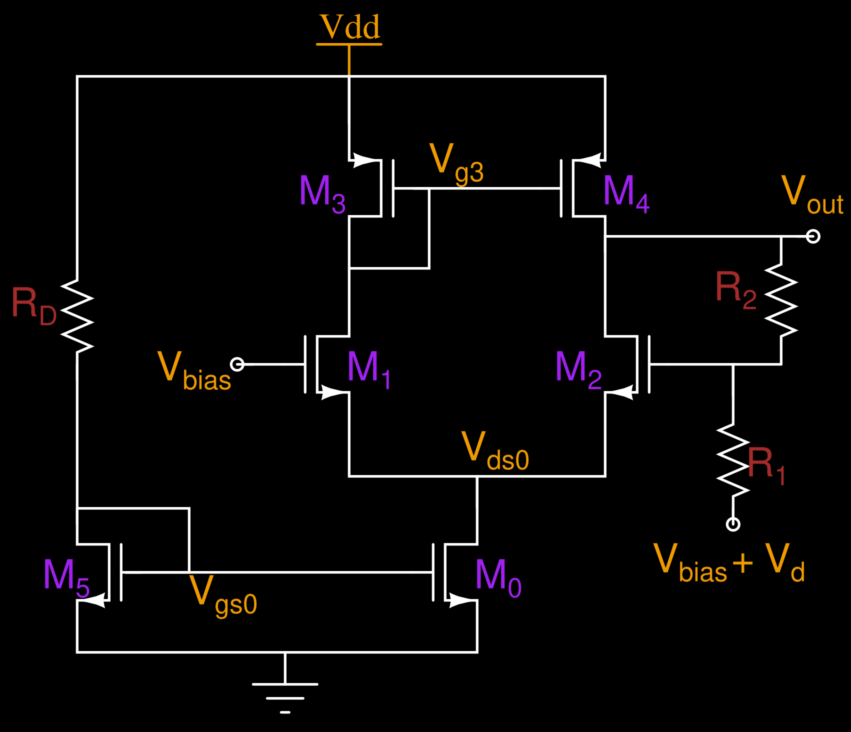
The experiment aims to design and analyze inverting amplifier using the Five Transistor OTA.

3.b.2 Design:

3.b.2.A Circuit Input Conditions:

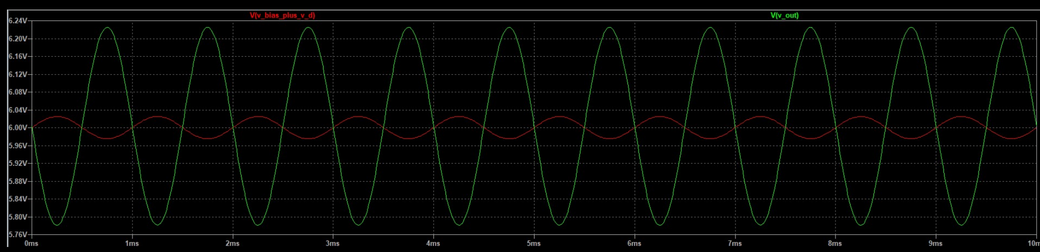
- $V_{bias} = V_{in,cm} = 6$V.
- $R_2 = 10M\Omega, R_1 = 1M\Omega$
- $A_v = -\frac{R_2}{R_1} =$ -10

3.b.2.B Circuit Design:



3.b.3 Simulation Results:

LTSpice Simulation Results:



Results from DSO (Circuit Simulation):

3.b.4 Experimental Results:

<u>Need for high resistance (≈ in $M\Omega$):</u>

- Having a high input impedance calls for a minimized loading effect and
- Having less current flowing reduces the risk of current sinking.

Tabulate theoretical and measured value of amplifier gain and phase shift:

- $V_d = 25\text{m}V_{pp}$, 1kHz

	Theoretical value	Simulation Result	Measured Result
Gain ($\frac{V_{out}}{V_d}$)	-10	-8.883	-7.2 (= 360mV/50mV)
Phase Shift	180°	180°	180°

3.b.5 Conclusion and Inferences:

The V_{out} is 10 times in magnitude as compared to the V_d and is also phase shifted by 180°, thus we can conclude that this a inverting amplifier with a gain of 10(in theory).

3.b.6 Experiment Completion Status:

This experiment was completed within the lab itself in its entirety.

3.c Differentiator Circuit (BONUS):

3.c.1 Aim of the experiment

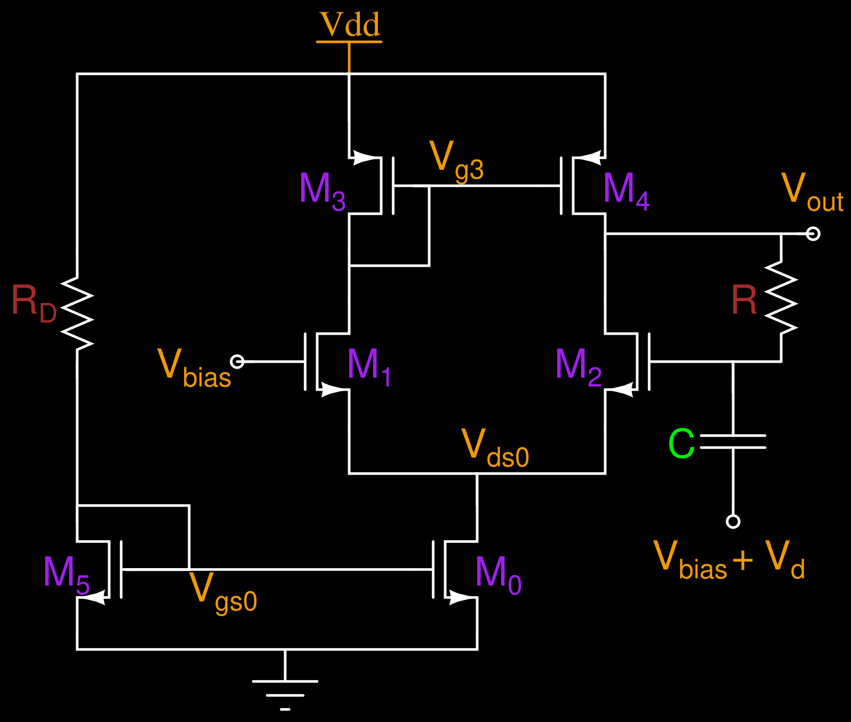
The experiment aims to design a differentiator circuit using the Five Transistor OTA

3.c.2 Design:

3.c.2.A Circuit Input Conditions:

- Let R = $1M\Omega$
- Let C = 100pF
- $R_2 = 10M\Omega, R_1 = 1M\Omega$
- $A_v = -\frac{R_2}{R_1}$ = -10
- V_{in} = 100mV_{pp}, 1kHz triangular wave => Time Period = 1ms

3.c.2.B Circuit Design:



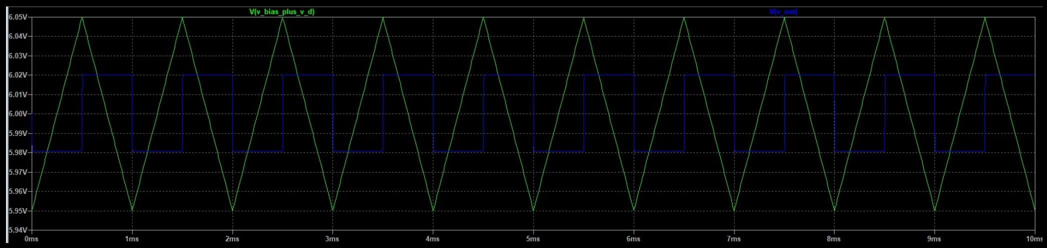
3.c.2.C Equations:

$$I = C \cdot \frac{\mathrm{d}v_{in}}{\mathrm{d}t} \tag{11}$$

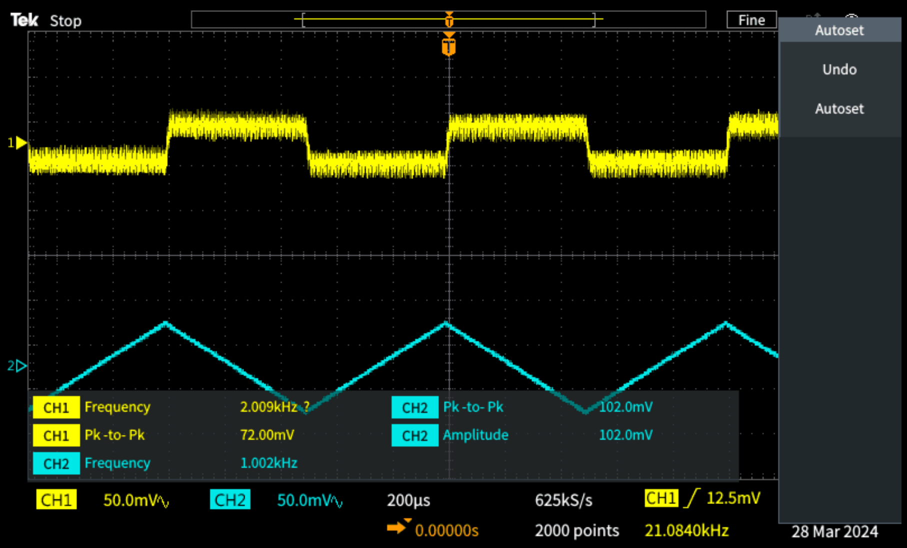
$$V_{out} = -R \cdot C \cdot \frac{\mathrm{d}v_{in}}{\mathrm{d}t} \tag{12}$$

3.c.3 Simulation Results:

LTSpice Simulation Results:



Results from DSO (Circuit Simulation):



3.c.4 Experimental Results:

As per the DSO output, it can be seen that for the input being a triangular wave, we obtain a square wave with same frequency as per the triangular wave.

3.c.5 Conclusion and Inferences:

The input is a triangular wave and the output is a square wave. The differentiation of a triangular wave leads to square wave, hence it can be concluded that this is a differentiator circuit.

3.c.6 Experiment Completion Status:

This experiment was completed within the lab itself in its entirety.