EE 230 - Analog Lab
Wadhwani Electronics Laboratory
Electrical Engineering IIT Bombay

Lab: 8 Date: March 7th, 2024

Instructions:

- Write down all your observations in notebook.
- Verify your calculations with your respective TA.

Objectives:

- To extract mosfet parameters.
- To design CS amplifier for given specifications.
- To understand the working and design of basic current mirror.
- Using Simulations to support analytical analysis.

---

1. **MOSFET Characterization**
   In this section, an Excel File is provided which contains experimental Id values for corresponding Vgs values (0 to 5 V) for a constant Vds of 5 V and Vbs of 0 V.

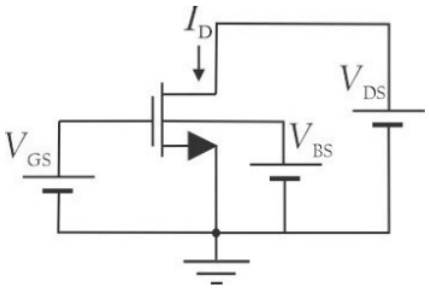

Figure 1: Testbench to extract Mosfet Parameters

The expression for Id is given by

$$Id = \frac{kn}{2}(Vgs - Vth)^2$$

where kn is the transistor transconductance (in $\mu A/V^2$) and Vth is the threshold voltage (in Volts). Using the data,

(a) Plot Id v/s Vgs from the given data

(b) Extract Kn and Vth referring to the Video and tabulate them. **[2 Marks]**

(c) Include these parameters (kn and Vth) into the model file and then simulate (DC Sweep on Vgs from 0 to 5 V, Vds = 5 V, Vbs = 0 V) the schematic in Ltspice as shown in Fig[1] and plot Id v/s Vgs. **[2 Marks]**

(d) Extract the simulation data (Id and Vgs values) from LtSpice and plot in Excel with the experimental data provided on the same plot. These plots should coincide with each other. **[1 Mark]**

In the subsequent sections, You will use these parameters to design a Common Source Amplifier and Current Mirror using Ltspice. Assume Vth and Kp to be 0.5 V and 200 (in $\mu A/V^2$) respectively for PMOS.

2. **Common Source (CS) Amplifier with Resistive Load**

(a) **Theory**

i. **Introduction:**
MOSFET-based Common Source (CS) Amplifier with resistive load is as shown in the figure [2]. M_1 is an NMOS with R_D resistor as load. Input, V_{in} is applied at the gate of M_1. V_{in} consists of DC bias voltage of V_{bias} and ac signal v_{in} (i.e. $V_{in} = V_{bias} + v_{in}$). V_{bias} is responsible for biasing M_1 in proper operating region. Output is observed at the drain of M_1. This circuit is called a common source amplifier with a resistive load.

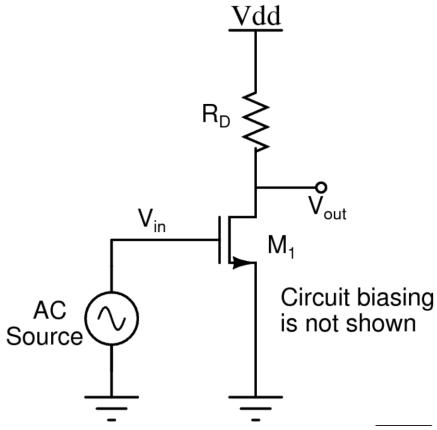

Figure 2: CS amplifier with Resistive Load

ii. **Small signal gain (A_v):**
Fig[3] is a small signal model of CS amplifier with resistive load. v_{in} is small signal applied between gate and source where source is grounded. This v_{in} causes change in current flowing from drain to source. This change is given by $g_m v_{in}$ where gm is transconductance of M_1 mosfet. $g_m v_{in}$ flows from parallel combination of R_D and r_o (i.e. $R_D||r_o$) generating voltage change at drain (v_{out}) of $-g_m(R_D||r_o)v_{in}$. Thus, change of v_{in} voltage at gate causes $-g_m(R_D||r_o)v_{in}$ change in drain voltage. Gain (A_v) of CS amplifier is defined as v_{out}/v_{in}. Thus, $A_v = -g_m(R_D||r_o)$. For simplicity r_o is assumed infinite (Practically it is a high value). Thus small signal gain is simplified to $A_v = -g_m R_D$.

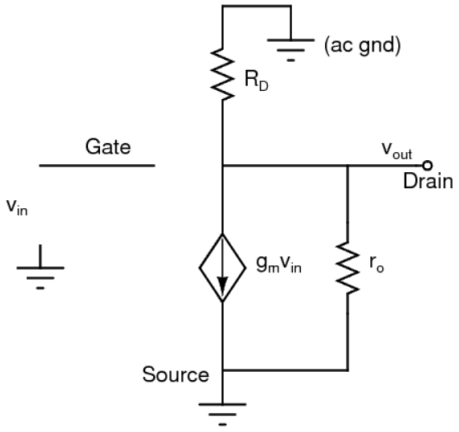

Figure 3: Small signal model of CS amplifier with resistive load

iii. **Biasing M_1 in saturation region**
M_1 should be biased in saturation region for amplifier to work. For this, $V_{ds1} > V_{gs1} - V_{th1}$. As a safety margin let us consider V_{ds1} is V_m voltage higher than $V_{gs1} - V_{th1}$. In our case $V_{ds1} = V_{out}$ and $V_{gs1} = V_{in} - V_{th}$. Let I_D be the current flowing through M_1. Thus, V_{out} can be expressed as $V_{dd} - I_D R_D$. Thus the constraint to keep M_1 in saturation is $V_{dd} - I_D R_D = V_{in} - V_{th} + V_m$. I_D in saturation region is given as $\frac{K_n}{2}(V_{in} - V_{th})^2$ and transconducatnce, $g_m = K_n(V_{in} - V_{th})$. Thus

$I_D R_D$ can be expressed as $\frac{A_v(V_{in}-V_{th})}{2}$. Substituting this in above inequality and rearranging terms to get V_{in} we get $V_{in} = \frac{V_{dd}-V_m}{1+\frac{A_v}{2}} + V_{th}$. This V_{in} is the DC bias voltage (V_{bias}).

(b) **Simulation**

Design a CS amplifier with resistive load for a small signal gain $A_v > 18$ dB.

i. Perform hand calculations to meet gain specifications. Use the extracted parameter values for K_n and V_{th} and tabulate DC bias Voltage (V_{bias}), Drain resistance (R_D) and DC output voltage ($V_{out_{dc}}$). **[3 Marks]**

ii. Draw Schematic in LtSpice and use the same model file (containing parameters you extracted from the data provided). Select the standard value of R_D, available in the lab, as shown in Fig.[8] and is close to the value calculated previously. Run Transient Simulation by applying V_{in} of 10 mV_{pp}, 1 KHz sinusoidal signal with DC voltage offset of V_{bias} and $V_{dd} = 5V$. Plot V_{out} and V_{in}. **[1 Mark]**

iii. Determine the gain A_v. If gain specification is not meet then make appropriate changes in the circuit parameters to meet the specs. Tabulate the final values of all parameters. **[1 Mark]**

iv. Tabulate the DC Operating point(Vgs,Vds,Id and gm) and region of operation of transistor. **[2 Marks]**

---

3. **Common Source (CS) Amplifier with Diode Connected Load**

(a) **Theory**

i. **Introduction**

MOSFET-based Common Source (CS) Amplifier with diode connected load is as shown in the figure [4]. M_1 is a NMOS with M_2 as a diode load. Input, V_{in} is applied at the gate of M_1. V_{in} consists of dc bias voltage of V_{bias} and ac signal v_{in} ($V_{in} = V_{bias} + v_{in}$). V_{bias} is responsible for biasing M_1 in proper operating region. Output is observed at the drain of M_1. Thus this circuit is called as a common source amplifier with diode connected load.

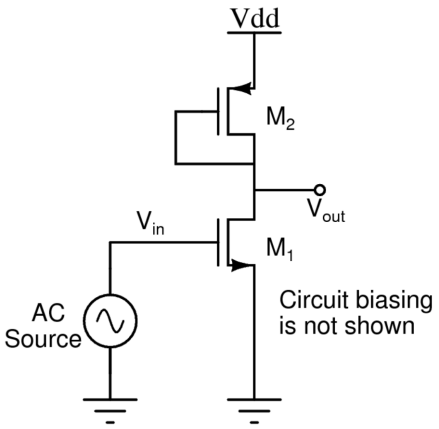

Figure 4: CS amplifier with diode connected load

ii. **Small signal gain (A_v)**

Small signal model of CS amplifier with diode connected load is shown in Fig.[5]. For simplicity let us consider r_{o1} and r_{o2} be infinite (In practical cases both this resistances are very high but not infinite). Thus there is no current flowing through these resistances. Writing KCL at node v_{out} we get $g_{m2}v_{sg2} = g_{m1}v_{gs1}$. Where $v_{gs1} = v_{in}$ and $v_{sg2} = -v_{out}$. g_{m1} can be expressed as $\sqrt{2I_{d1}K_{n1}}$ similarly g_{m2} can be expressed as $\sqrt{2I_{d2}K_{p2}}$. Thus $A_v = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{m2}} = -\sqrt{\frac{K_{n1}}{K_{p1}}}$

iii. **Biasing M_1, M_2 in saturation region**

Drain and Gate of M_2 are connected to each other. Thus M_2 if on then will always be biased in saturation region.(prove why?). M_1 will remain in saturation as long as $V_{out} > V_{in} - V_{th1}$. Thus, $V_{out} = V_{in} - V_{th1} + V_m$. Current from M_2 and M_1 are same. Thus, $K_{n1}(V_{in} - V_{th1})^2 = K_{p2}(V_{dd} - V_{out} - V_{th2})^2$. Input voltage can be expressed as $V_{in} = \sqrt{\frac{K_{p2}}{K_{n1}}}(V_{dd} - V_{out} - V_{th2}) + V_{th1}$. Let V_m be the margin voltage by which V_{out} is greater than $V_{in} - V_{th1}$. Substituting this in V_{in} equation we can solve for V_{in}. This value will be the bias voltage (V_{bias}) of M_1.

(b) **Simulation**

Design a CS amplifier with diode load

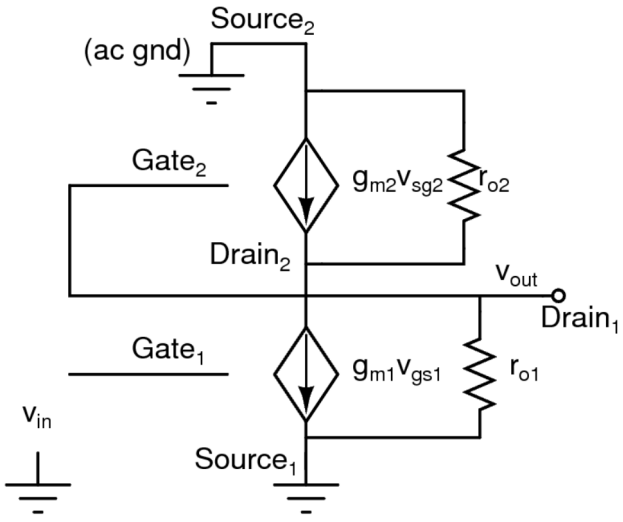

Figure 5: Small signal model of CS amplifier with diode connected load

i. Perform hand calculations. Use the extracted parameter values for K_n and V_{th} (assume K_p and V_{th} for PMOS as given in question 1). Tabulate DC bias Voltage (V_{bias}), DC output voltage ($V_{out_{dc}}$) and small signal gain (A_v). **[3 Marks]**

ii. Draw Schematic in LtSpice. Use the same model file as earlier.
Run transient simulation by applying V_{in} of 10 mV_{pp}, 1 KHz sinusoidal signal with DC voltage offset of V_{bias} and $V_{dd} = 5V$. Plot V_{out} and V_{in}. **[1 Marks]**

iii. Determine the gain A_v. Compare with the hand-calculated gain value. **[1 Marks]**

iv. Tabulate the DC Operating point and region of operation for both the transistors. **[4 Marks]**

4. **Current Mirror (CM) Design**

(a) **Introduction**

Current mirror is an analog circuit which senses the reference current and mirrors it to the load. It is widely used in modern ICs. Most common applications are amplifiers, D/A converters, Delay elements, Bias circuits etc.

(b) **Basic Design Concepts**

Basic idea is to the generate a reference voltage (V_{GS1}) by pushing current (I_{REF}) into the the diode connected MOSFET (M_1) as shown in Fig.[6]and use this voltage to bias another MOSFET (M2) such that the another MOSFET acts as a current source providing same current (I_{copy}) as reference current (I_{REF}). Let's derive the equation for I_{COPY} in terms of I_{REF} and device parameters.

The current equation of a MOSFET, ignoring channel length modulation and biased in saturation region is

$$I_{DS} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{1}$$

Above equation can be rearranged to get

$$V_{GS} = \sqrt{\frac{2I_{ds}}{\mu C_{OX}\frac{W}{L}}} + V_{TH} \tag{2}$$

Referring to Fig.[**??**] and Eqn.[2] we can write V_{GS1} as

$$V_{GS1} - V_{TH1} = \sqrt{\frac{2I_{REF}}{\mu C_{OX}\frac{W_1}{L_1}}} \tag{3}$$

Since $V_{GS1} = V_{GS2}$ and assuming $V_{TH1} = V_{TH2}$ we can write I_{COPY} as

$$I_{COPY} = \frac{1}{2}\mu C_{OX}\frac{W_2}{L_2}(V_{GS1} - V_{TH1})^2 \tag{4}$$

$$I_{COPY} = \frac{W_2}{L_2}\frac{I_{REF}}{\frac{W_1}{L_1}} \tag{5}$$

generally written as

$$\frac{I_{COPY}}{\frac{W_2}{L_2}} = \frac{I_{REF}}{\frac{W_1}{L_1}} \tag{6}$$

In many applications we may require to copy more current from reference. This is simply achieved by connecting current source MOSFETs in parallel and with appropriate sizing.
Note that all the above equations are derived by ignoring channel length modulation effect thus if this effect is considered there may be error in copying current, usually length of devices are chosen high to minimize the error and V_{DS1}, V_{DS2} are made equal. Both the MOSFETS (M1 and M2) are in saturation region. Since, M1 is in diode connected it will always be in saturation region given enough overdrive is provided but there is a possibility of M2 going in triode region due to inadequate drain to source voltage across it. Thus, if M2 is biased in triode then current mirroring will not happen. The derived equation is valid for older technology models where MOSFET obeys the square law behaviour. In small scale devices this is not true but however it will still be able to mirror the current but will follow different equation as opposed to Eqn.[6]

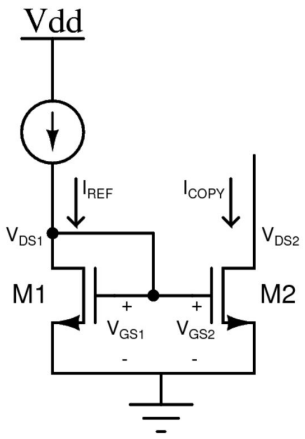

Figure 6: Basic NMOS current mirror circuit

(c) **Simulation**
Fig.[6] is an equivalent model of Fig. 7 simplified for simulation purposes.

i. Perform hand calculations to calculate value of R_1 such that $I_{REF} = 2$ mA. What is the value of V_{GS1}? Use Vdd =8 V. **[2 Marks]**

ii. Draw LtSpice Schematic for Fig.[7] circuit. Set the value of R_1 and perform DC simulation to find I_{REF}. Tweak value of R_1 (if required) until I_{REF} is 2 mA. **[1 Marks]**

iii. Sweep V_{DS2} from 0 V to 8 V. Plot I_{COPY} *vs* V_{DS2}. Determine value of V_{DS2} at which $I_{COPY} = I_{REF}$. What is the relationship between this V_{DS2} and V_{DS1}. **[3 Marks]**

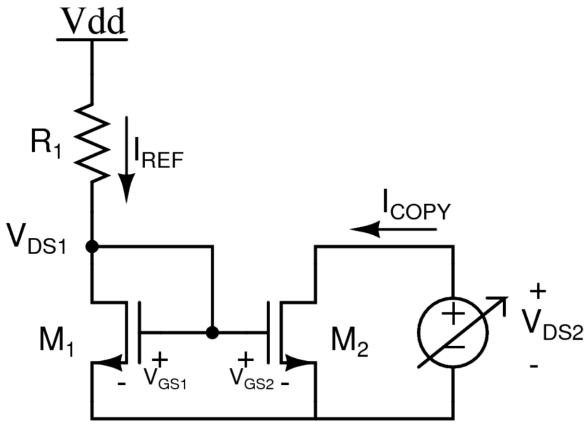

Figure 7: NMOS current mirror circuit setup for simulation

Value	Value	Value	Value	Value	Value	Value
1 Ω	10 Ω	100 Ω	1 kΩ	10 kΩ	100 kΩ	1 MΩ
1.2 Ω	12 Ω	120 Ω	1.2 kΩ	12 kΩ	120 kΩ	1.2 MΩ
1.5 Ω	15 Ω	150 Ω	1.5 kΩ	15 kΩ	150 kΩ	1.5 MΩ
1.8 Ω	18 Ω	180 Ω	1.8 kΩ	18 kΩ	180 kΩ	1.8 MΩ
2.2 Ω	22 Ω	220 Ω	2.2 kΩ	22 kΩ	220 kΩ	2.2 MΩ
2.7 Ω	27 Ω	270 Ω	2.7 kΩ	27 kΩ	270 kΩ	2.7 MΩ
3.3 Ω	33 Ω	330 Ω	3.3 kΩ	33 kΩ	330 kΩ	3.3 MΩ
3.9 Ω	39 Ω	390 Ω	3.9 kΩ	39 kΩ	390 kΩ	3.9 MΩ
4.7 Ω	47 Ω	470 Ω	4.7 kΩ	47 kΩ	470 kΩ	4.7 MΩ
5.6 Ω	56 Ω	560 Ω	5.6 kΩ	56 kΩ	560 kΩ	5.6 MΩ
6.8 Ω	68 Ω	680 Ω	6.8 kΩ	68 kΩ	680 kΩ	6.8 MΩ
8.2 Ω	82 Ω	820 Ω	8.2 kΩ	82 kΩ	820 kΩ	8.2 MΩ

Figure 8: Standard Resistors values with a tolerance of ±10%