# EE230: Analog Circuits Lab
# Square Root Amplifier Implementation
# Lab No. 5

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## 1 Aim of the experiment

Construct a square root amplifier and fine tune it to utmost precision

## 2 Design

The current through the diode in forward bias is given by the following equation

$$I_D = I_S * (e^{V_D/nV_T} - 1) \tag{1}$$

Rearranging the terms we get

$$V_D = n \cdot V_T * (ln(I_D) - ln(I_S)) \tag{2}$$

The output of Block-1 is given by $V_{out1}$:

$$V_{out1} = -V_D = n \cdot V_T * (ln(I_S R) - ln(V_{in})) \tag{3}$$

The output of Block-2 is given by $V_{out2}$:

$$V_{out2} = -n \cdot V_T \cdot ln(I_S R) + (ln(V_{in}))V_T \cdot n + 2V_{b1} \tag{4}$$

We can remove the offset terms which don't include $V_{in}$ by choosing:

$$V_{b1} = \frac{n \cdot V_T \cdot ln(I_S \cdot R)}{2} \tag{5}$$

$$V_{out2} = n \cdot V_T \cdot ln(V_{in}) \tag{6}$$

The output of Block-3 can be given by:

$$V_{out3} = -\frac{R_{22}}{R_{21}} \cdot V_{out2} = -\frac{R_{22}}{R_{21}} \cdot V_T \cdot ln(V_{in}) = ln(V_{in}^{-\frac{R_{22}}{R_{21}} nVT}) \tag{7}$$

For Block-4, $V_x = V_{b2}$ (virtual ground) and:

$$V_{out} = R_3 \cdot I_{D2} + V_{b2} = R_3 \cdot T_{S2} \cdot e^{\frac{V_{b2}}{n_2 \cdot V_T}} V_{in}^{\frac{n_1}{n_2}\frac{R_{22}}{R_{21}}} + V_{b2} \tag{8}$$

We can simplify the circuit as:

$$V_{R3} = V_{out} - V_x = \beta_1 \cdot V_{in}^{\beta 2} \tag{9}$$

For square root amplifier, we can choose $\beta_1 = 1$ and $\beta_2 = \frac{1}{2}$

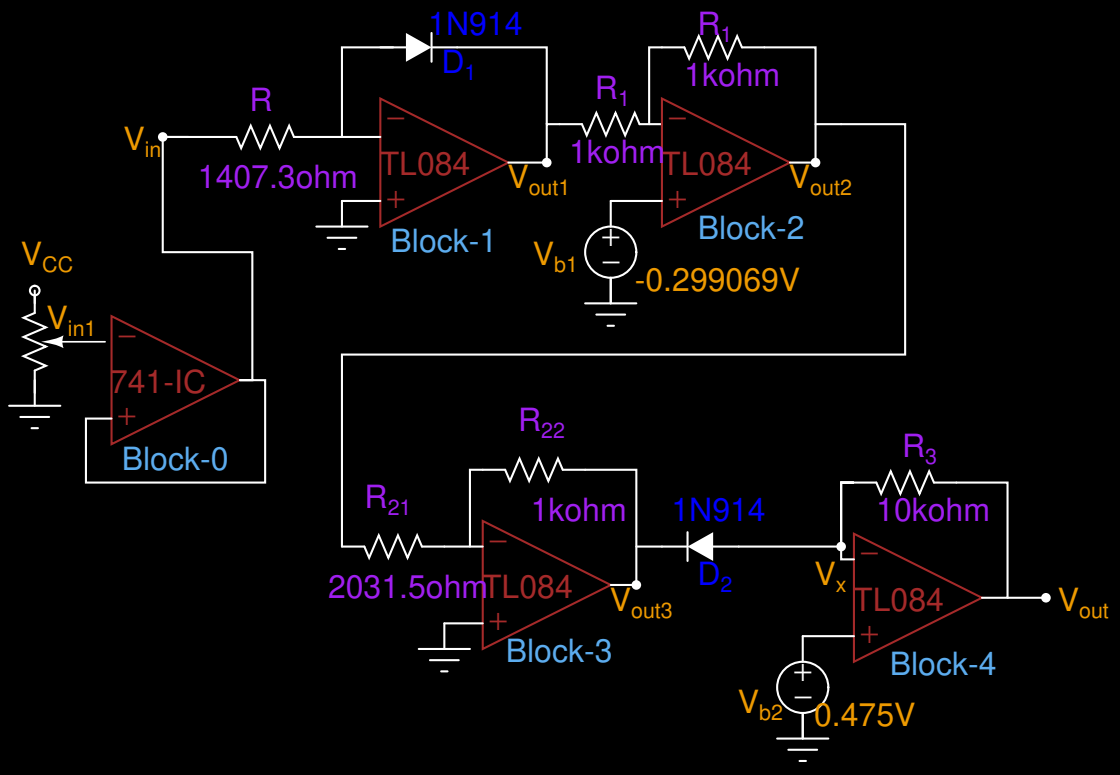


Figure 1: Circuit Diagram

# 3 Experimental results

***What is the purpose of Block - 0*:**

Block 0 is a voltage buffer. It provides very high input impendance and about zero output impendance.

***What if $V_{in}$ is directly connected to $V_{in1}$*:**

If $V_{in}$ is directly connected to $V_{in1}$; loading effect will be caused and current flowing through the potentiometer in block 0 could cause unneccessary losses in current.

***Derive both $V_{b1}$ and $V_{b2}$ DC voltages using multi turn potentiometer*:**

at $V_{in}$ = 1V, $V_{out2}$ = 0V.
Adjusting $V_{b1}$ to get 0V output, we get $V_{b1}$ = -0.24V and on fine tuning we get $V_{b2}$ = 0.44V.

***Why $V_{b2}$ potentiometer is coarse measurement whereas $R3$ is a fine one*:**

As it can be seen from the **equation (9)** that $V_{R3}$ is directly proportional to $exp(\frac{V_{b2}}{n_2 \cdot V_T})$. Now since, 1 / ($n_2$ ·$V_T$) >> 1, a slight change in the value fo $V_{b2}$ leads to a huge change in the value of $V_{R3}$. And it can also be seen from the **equation (9)** that $V_{R3}$ is directly proportional to $R_3$. And since we know that after the input value crosses the 1 mark, the exponential value increases very rapidly as compared to the linear dependence. Hence, the $V_{b2}$ is a coarse adjustment while $R_3$ is a fine adjustment.

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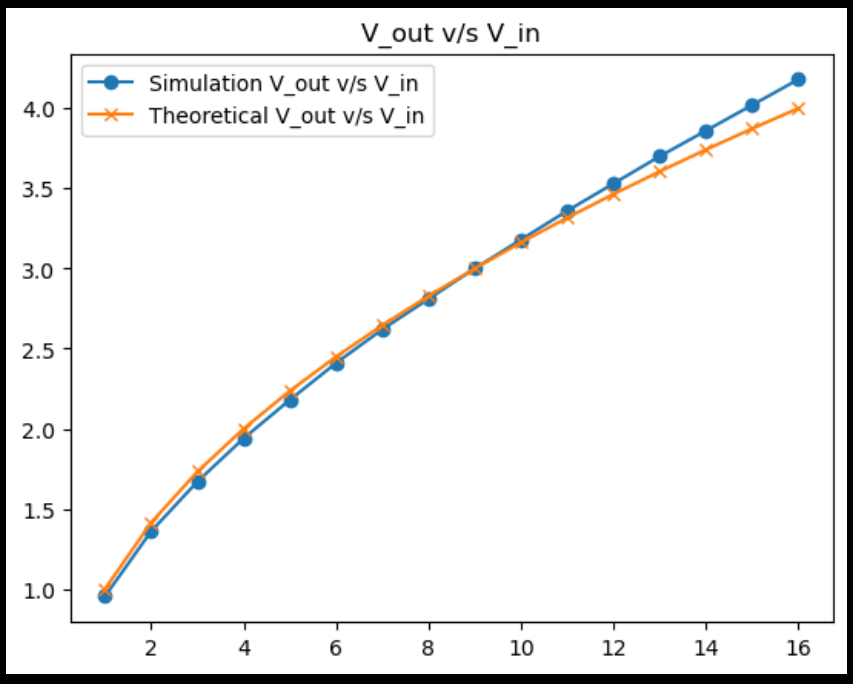
***Sweep $V_{in}$ from 1V to 15V in uniform steps of 1V. Tabulate your readings*:**

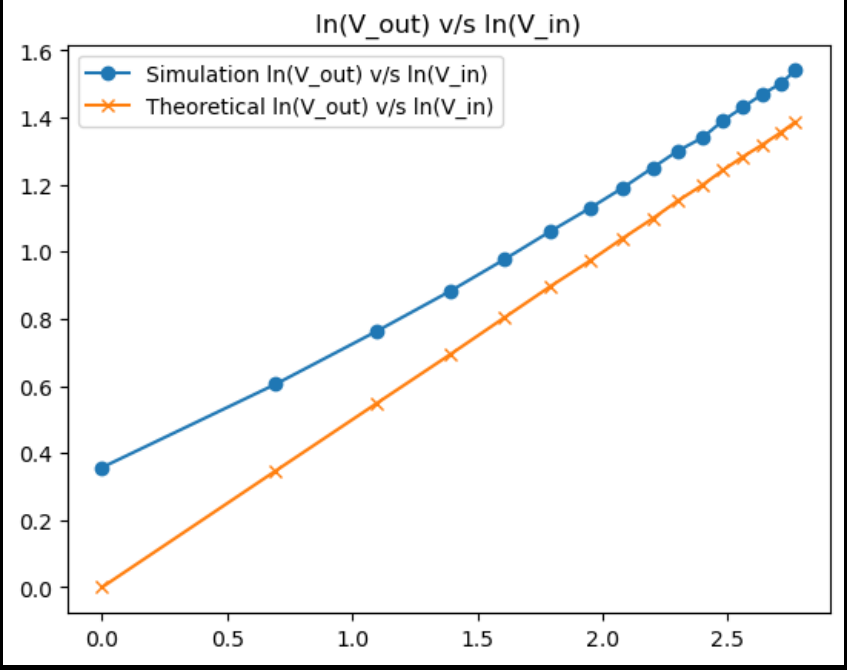
These are simulation results.

| $V_{in}$ (in Volts) | $V_{R3}$ (in Volts) | $V_{in}$ (in Volts) | $V_{R3}$ (in Volts) |
|---|---|---|---|
| 1 | 0.95388 | 2 | 1.357 |
| 3 | 1.68 | 4 | 1.95 |
| 5 | 2.184 | 6 | 2.407 |
| 7 | 2.60 | 8 | 2.813 |
| 9 | 3.0003 | 10 | 3.184 |
| 11 | 3.360 | 12 | 3.532 |
| 13 | 3.698 | 14 | 3.862 |
| 15 | 4.021 | 16 | 4.179 |

***Plot $V_{out}$ v/s $V_{in}$*:**



***Plot ln($V_{out}$) v/s ln($V_{in}$):***




***What should be the expected slope of the above plot:***

The expected slope of the above plot which is ln($V_{out}$) v/s ln($V_{in}$) should be 0.5

***What happens if the polarity of the diode $D_2$ is reversed:***

Reversing D2's polarity may lead to non-linear behavior, impacting amplifier effectiveness. Maintaining correct diode orientation is crucial

# 4 Experiment completion status

The observation values could not be taken during the experiment. The circuit connections was completely correct and was also verified by two TAs and an RA.

We faced saturation after block-1. The output of block-1 was 13.47V which ideally should have been around -0.589V and hence the output of block-2 was 14.57V which ideally should have been 0V.
The TAs and RAs also couldn't help much with this. We changed the IC, diodes several times. We also explored the possibility of having a faulty LM741 but that was also not the case. We also didn't keep the circuit in ON state for too long and were also repeatedly checking for any blown up potentiometers, but that was also not the case. We verified other values before block-1, which were totally correct. We concluded that we were facing some issues after block-1. And this problem was faced by a lot of groups in the lab.

We along with TAs, RAs tried debugging for 1.5 hours, but it didn't help much and in the end, we couldn't take any observations.