

## Instructions:

- Write down all your observations in notebook.
- Verify your calculations with your respective TA.

### 1. Common Source (CS) Amplifier with Resistive Load

#### (a) Theory

##### i. Introduction:

MOSFET-based Common Source (CS) Amplifier with resistive load is as shown in the figure [ 1].  $M_1$  is an NMOS with  $R_D$  resistor as load. Input,  $V_{in}$  is applied at the gate of  $M_1$ .  $V_{in}$  consists of DC bias voltage of  $V_{bias}$  and ac signal  $v_{in}$  (i.e.  $V_{in} = V_{bias} + v_{in}$ ).  $V_{bias}$  is responsible for biasing  $M_1$  in proper operating region. Output is observed at the drain of  $M_1$ . This circuit is called a common source amplifier with a resistive load.

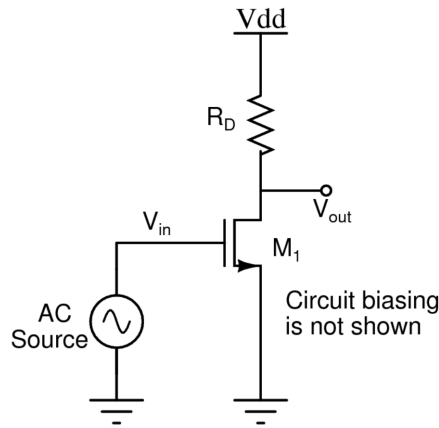


Figure 1: CS amplifier with Resistive Load

##### ii. Small signal gain ( $A_v$ ):

Fig[ 2] is a small signal model of CS amplifier with resistive load.  $v_{in}$  is small signal applied between gate and source where source is grounded. This  $v_{in}$  causes change in current flowing from drain to source. This change is given by  $g_m v_{in}$  where  $g_m$  is transconductance of  $M_1$  mosfet.  $g_m v_{in}$  flows from parallel combination of  $R_D$  and  $r_o$  (i.e.  $R_D || r_o$ ) generating voltage change at drain ( $v_{out}$ ) of  $-g_m(R_D || r_o)v_{in}$ . Thus, change of  $v_{in}$  voltage at gate causes  $-g_m(R_D || r_o)v_{in}$  change in drain voltage. Gain ( $A_v$ ) of CS amplifier is defined as  $v_{out}/v_{in}$ . Thus,  $A_v = -g_m(R_D || r_o)$ . For simplicity  $r_o$  is assumed infinite (Practically it is a high value). Thus small signal gain is simplified to  $A_v = -g_m R_D$ .

##### iii. Biasing $M_1$ in saturation region

$M_1$  should be biased in saturation region for amplifier to work. For this,  $V_{ds1} > V_{gs1} - V_{th1}$ . As a safety margin let us consider  $V_{ds1}$  is  $V_m$  voltage higher than  $V_{gs1} - V_{th1}$ . In our case  $V_{ds1} = V_{out}$  and  $V_{gs1} = V_{in} - V_{th}$ . Let  $I_D$  be the current flowing through  $M_1$ . Thus,  $V_{out}$  can be expressed as  $V_{dd} - I_D R_D$ . Thus the constraint to keep  $M_1$  in saturation is  $V_{dd} - I_D R_D = V_{in} - V_{th} + V_m$ .  $I_D$  in saturation region is given as  $\frac{K_n}{2}(V_{in} - V_{th})^2$  and transconductance,  $g_m = K_n(V_{in} - V_{th})$ . Thus  $I_D R_D$  can be expressed as  $\frac{A_v(V_{in} - V_{th})}{2}$ . Substituting this in above inequality and rearranging terms to get  $V_{in}$  we get  $V_{in} = \frac{V_{dd} - V_m}{1 + \frac{A_v}{2}} + V_{th}$ . This  $V_{in}$  is the DC bias voltage ( $V_{bias}$ ).

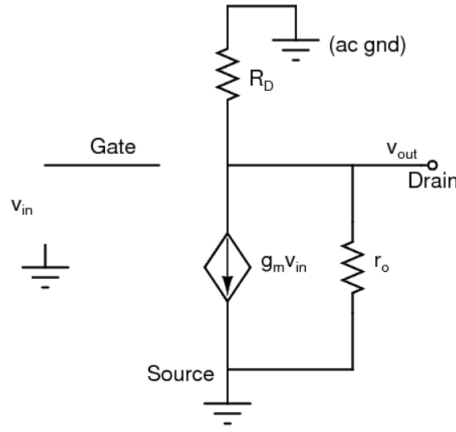


Figure 2: Small signal model of CS amplifier with resistive load

(b) **Experiment**

- i. Assemble CS amplifier on the breadboard. Apply  $V_{dd} = 5V$ .  $V_{in} = 20mV_{pp}$ , 1 KHz sinusoidal with  $V_{bias}$  DC offset. Use the value of  $V_{bias}$  and  $R_D$  as finalized after simulation.
- ii. Tabulate the value of  $V_{out_{dc}}$ . Ensure  $M_1$  is in the saturation region. If not then make the necessary changes. [1 Marks]
- iii. Plot  $V_{out}$  and  $V_{in}$  on DSO. Set probe on AC mode. [2 Marks]
- iv. Calculate small signal gain,  $A_v$ . If gain specifications are not met then make appropriate changes. [1 Marks]

## 2. Common Source (CS) Amplifier with Diode Connected Load

(a) **Theory**

i. **Introduction**

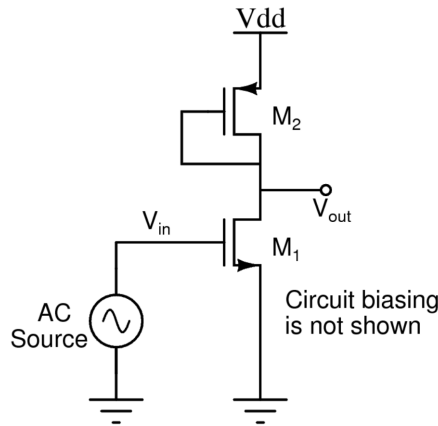


Figure 3: CS amplifier with diode connected load

ii. **Small signal gain ( $A_v$ )**

Small signal model of CS amplifier with diode connected load is shown in Fig.[ 4]. For simplicity let us consider  $r_{o1}$  and  $r_{o2}$  be infinite (In practical cases both these resistances are very high but not infinite). Thus there is no current flowing through these resistances. Writing KCL at node  $v_{out}$  we get  $g_{m2}v_{sg2} = g_{m1}v_{gs1}$ . Where  $v_{gs1} = v_{in}$  and  $v_{sg2} = -v_{out}$ .  $g_{m1}$  can be expressed as  $\sqrt{2I_{d1}K_{n1}}$  similarly  $g_{m2}$  can be expressed as  $\sqrt{2I_{d2}K_{p2}}$ . Thus  $A_v = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{m2}} = -\sqrt{\frac{K_{n1}}{K_{p1}}}$

iii. **Biasing  $M_1$ ,  $M_2$  in saturation region**

Drain and Gate of  $M_2$  are connected to each other. Thus  $M_2$  if on then will always be biased in saturation region.  $M_1$  will remain in saturation as long as  $V_{out} > V_{in} - V_{th1}$ . Thus,  $V_{out} = V_{in} -$

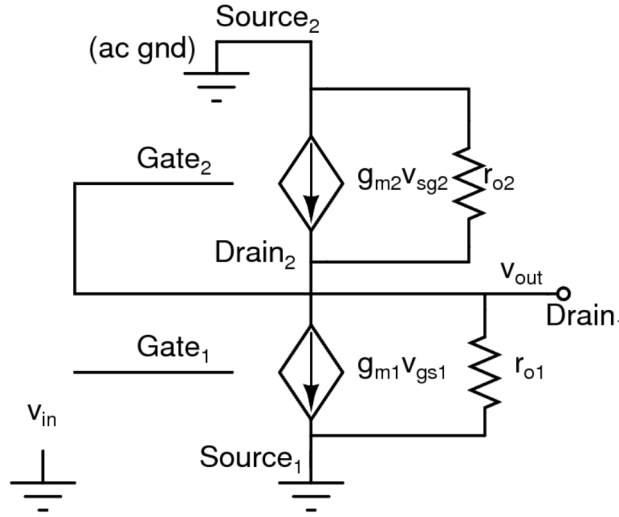


Figure 4: Small signal model of CS amplifier with diode connected load

$V_{th1} + V_m$ . Current from  $M_2$  and  $M_1$  are same. Thus,  $K_{n1}(V_{in} - V_{th1})^2 = K_{p2}(V_{dd} - V_{out} - V_{th2})^2$ . Input voltage can be expressed as  $V_{in} = \sqrt{\frac{K_{p2}}{K_{n1}}}(V_{dd} - V_{out} - V_{th2}) + V_{th1}$ . Let  $V_m$  be the margin voltage by which  $V_{out}$  is greater than  $V_{in} - V_{th1}$ . Substituting this in  $V_{in}$  equation we can solve for  $V_{in}$ . This value will be the bias voltage ( $V_{bias}$ ) of  $M_1$ .

(b) **Experiment**

- Assemble CS amplifier with diode connected load on the breadboard. Apply  $V_{dd} = 5V$ .  $V_{in} = 20mV_{pp}$ , 1 KHz sinusoidal with  $V_{bias}$  DC offset. Use the value of  $V_{bias}$  as finalized after simulation. [1 Marks]
- Tabulate the value of  $V_{out_{dc}}$ . Ensure  $M_1$  is in the saturation region. If not then make the necessary changes. [1 Marks]
- Plot  $V_{out}$  and  $V_{in}$  on DSO. Set the probe on AC mode. [2 Marks]
- Calculate small signal gain,  $A_v$ . Compare results with the hand-calculated and simulated results. [1 Marks]

### 3. Current Mirror (CM) Design

(a) **Introduction**

Current mirror is an analog circuit which senses the reference current and mirrors it to the load. It is widely used in modern ICs. Most common applications are amplifiers, D/A converters, Delay elements, Bias circuits etc.

(b) **Basic Design Concepts**

Basic idea is to generate a reference voltage ( $V_{GS1}$ ) by pushing current ( $I_{REF}$ ) into the diode connected MOSFET ( $M_1$ ) as shown in Fig.[ 5] and use this voltage to bias another MOSFET ( $M_2$ ) such that the another MOSFET acts as a current source providing same current ( $I_{copy}$ ) as reference current ( $I_{REF}$ ). Let's derive the equation for  $I_{COPY}$  in terms of  $I_{REF}$  and device parameters.

The current equation of a MOSFET, ignoring channel length modulation and biased in saturation region is

$$I_{DS} = \frac{1}{2} \mu C_{OX} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (1)$$

Above equation can be rearranged to get

$$V_{GS} = \sqrt{\frac{2I_{ds}}{\mu C_{OX} \frac{W}{L}}} + V_{TH} \quad (2)$$

Referring to Fig.[ 5] and Eqn.[ 2] we can write  $V_{GS1}$  as

$$V_{GS1} - V_{TH1} = \sqrt{\frac{2I_{REF}}{\mu C_{OX} \frac{W_1}{L_1}}} \quad (3)$$

Since  $V_{GS1} = V_{GS2}$  and assuming  $V_{TH1} = V_{TH2}$  we can write  $I_{COPY}$  as

$$I_{COPY} = \frac{1}{2} \mu C_{OX} \frac{W_2}{L_2} (V_{GS1} - V_{TH1})^2 \quad (4)$$

$$I_{COPY} = \frac{W_2}{L_2} \frac{I_{REF}}{\frac{W_1}{L_1}} \quad (5)$$

generally written as

$$\frac{I_{COPY}}{\frac{W_2}{L_2}} = \frac{I_{REF}}{\frac{W_1}{L_1}} \quad (6)$$

In many applications we may require to copy more current from reference. This is simply achieved by connecting current source MOSFETs in parallel and with appropriate sizing.

Note that all the above equations are derived by ignoring channel length modulation effect thus if this effect is considered there may be error in copying current, usually length of devices are chosen high to minimize the error and  $V_{DS1}$ ,  $V_{DS2}$  are made equal. Both the MOSFETs (M1 and M2) are in saturation region. Since, M1 is in diode connected it will always be in saturation region given enough overdrive is provided but there is a possibility of M2 going in triode region due to inadequate drain to source voltage across it. Thus, if M2 is biased in triode then current mirroring will not happen. The derived equation is valid for older technology models where MOSFET obeys the square law behaviour. In small scale devices this is not true but however it will still be able to mirror the current but will follow different equation as opposed to Eqn.[ 6]

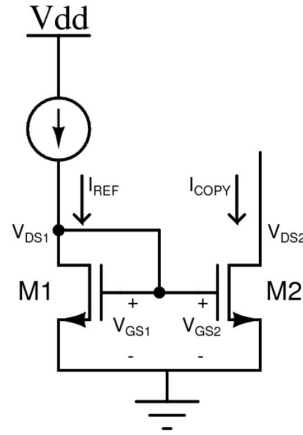


Figure 5: Basic NMOS current mirror circuit

### (c) Experiment

- i. Fig.[ 6] shows a basic current mirror to be implemented on the breadboard. R1 is a fixed resistor, designed to achieve desired  $I_{REF} = 2mA$ . A1 and A2 are Ammeters used to measure current  $I_{REF}$  and  $I_{COPY}$  respectively. R2 is a potentiometer used to vary the load of  $M_2$ .
- ii. Draw a PMOS equivalent basic current mirror. [2 Marks]
- iii. Use the value of R1 as derived from the simulation. VDD = 8 V. Measure  $I_{REF}$ . Compare with the simulation result. [2 Marks]
- iv. Now sweep  $V_{DS2}$  from 0 V to 8 V in 500 mV step size (include the value of  $V_{DS1}$ ). This can be achieved by sweeping the potentiometer R2 appropriately. Measure the readings of  $I_{REF}$ ,  $I_{COPY}$ ,  $V_{DS1}$  and  $V_{DS2}$ . [2 Marks]
- v. When is the error between  $I_{COPY}$  and  $I_{REF}$  minimum? [1 Marks]
- vi. What changes are required to design the current mirror for  $I_{COPY} = N \cdot I_{REF}$ . Where N is a positive integer. [1 Marks]
- vii. Design Current mirror on hardware for  $N = 2$ . [2 Marks]

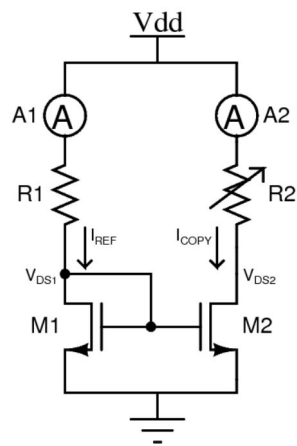


Figure 6: Basic NMOS current mirror circuit