Indian Institute of Technology Bombay
Department of Electrical Engineering
Digital Circuits Lab (EE-214)
Mid Sem Exam, Date: Sep 19, 2021

Timing: 9:30 AM to 1:00 PM | Autumn 2021 | Max mark: 25

1 Instructions

1. Use **Structural style of modelling** only.
2. Image of the first handwritten design to be uploaded by all students on Moodle, and the deadline is 11:00 AM sharp.
3. Handwritten design should comprise of **truth-tables, K-maps, Boolean equations, justifications for the boolean equations by inspection (as the case may be)** to explain your approach and the decomposed components in a **single zip file(RollNumber.zip)**.
4. You are allowed to use only the components in Gates.vhdl and your own VHDL descriptions in the experiments/homework problems so far and div.vhd(provided).
5. Demonstrate your RTL and gate level simulation to your TA using the given tracefile for overall design. You are encouraged to break down your design conveniently.
6. The final Design(VHDL Design files, qpf file) should be uploaded in Moodle(2nd link) by 12:45 PM(Sharp)

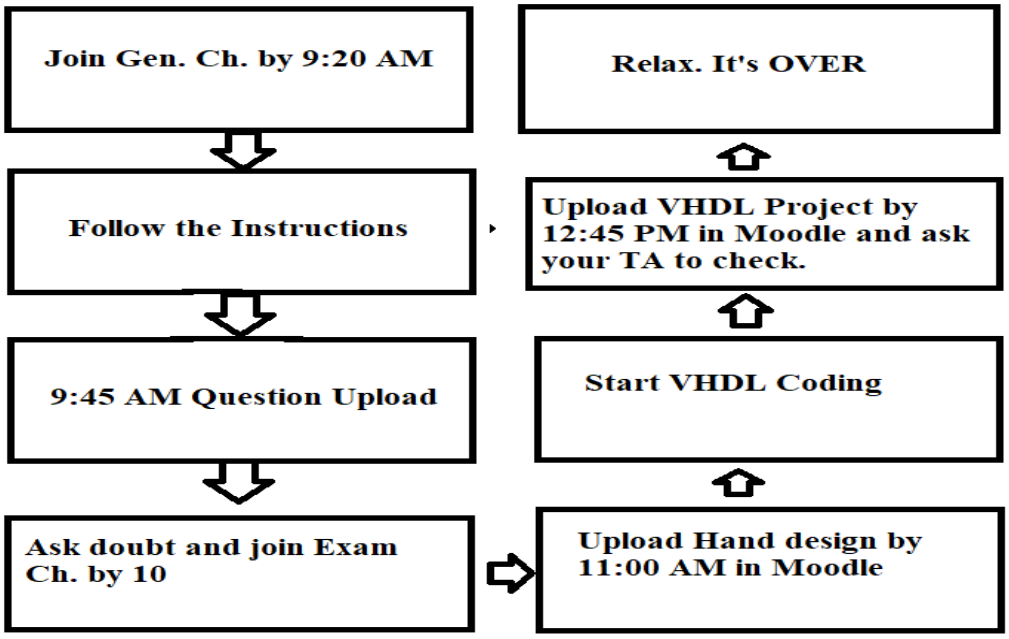

Figure 1: Exam Flowchart

2 Problem Statement

1. (a) Suppose you are designing an ATM machine. Where only following denomination notes and coin(Re.1(one rupee coin)) will be available. Rs.100, Rs.50, Re.1(one rupee coin). And these are available in **unlimited** numbers.

   (b) Suppose a user wants to withdraw some amount between Rs.1 to Rs.255 (No fraction is available). Assume 8 bit binary input (in decimal 0 - 255) will be fed to your designed system.

   (c) You have to design the system that will calculate internally how many denomination notes are required for the entered amount by the user, and tell the user which of the highest denomination notes(Rs. 100/- or Rs. 50/- or Re. 1/-) he/she will get.
   NOTE: Highest denomination will be given priority i.e. it will give minimum number of notes, e.g. User gives the input of Rs. 155. You design should output: One hundred rupees note plus one fifty rupees note and five numbers of one rupee coins i.e. 100+50+5). No other combinations are allowed e.g. three fifty rupees notes and five numbers of one rupee coins. Hints and specifications are given in the next page.

3 Specifications

Strictly follow the following input output format.

1. priority (2bits) = p(1)p(0)
   - "11" if at-least one Hundred rupees note is there in the notes provided by the ATM(fifty rupees note and one rupee coins can also be there).
   - "10" if no hundred rupees note but at-least one fifty rupees note is there(one rupee coins can also be there).
   - "01" if no hundred and fifty rupees note but only one rupee coin, else "00" if user has mistakenly input Rs.0.
2. number of Rs. 100 notes(2 bits) = a
3. number of Rs. 50 notes (1 bit) = b
4. number of Re. 1(one rupee coin) coins (6 bits) = c
5. **TRACEFILE format:**
   input(8 bit)< *space* >***p(1)p(0)abc(11 bit)***< *space* >***11111111111***
6. Number of input bit is 8 and number of output bit is 11
7. Marks division:
   - Correct pen and paper design with neat block diagram and brief explanation : 10
   - Correct design of counting correct number of notes : 10
   - Correct final design that is including the correct design of determining of note of highest denomination will fetch full marks : 5

4 Hints

1. A divider circuit has been provided. Which has the input format as dividend(Numerator of 8 bit), divisor(denominator of 8 bit), remainder and quotient in a single vector(16 bit with higher 8 bit as remainder and lower 8 bit as quotient). You may use it if you need it.
2. Don't go through the code now(Divider). But have a look into it after your exam.(For your own learning :))
3. You may use your own component and from Gates.vhdl as well as previous Lab work components of yours.

Best wishes