Lab 5 Report / 08th September, 2023

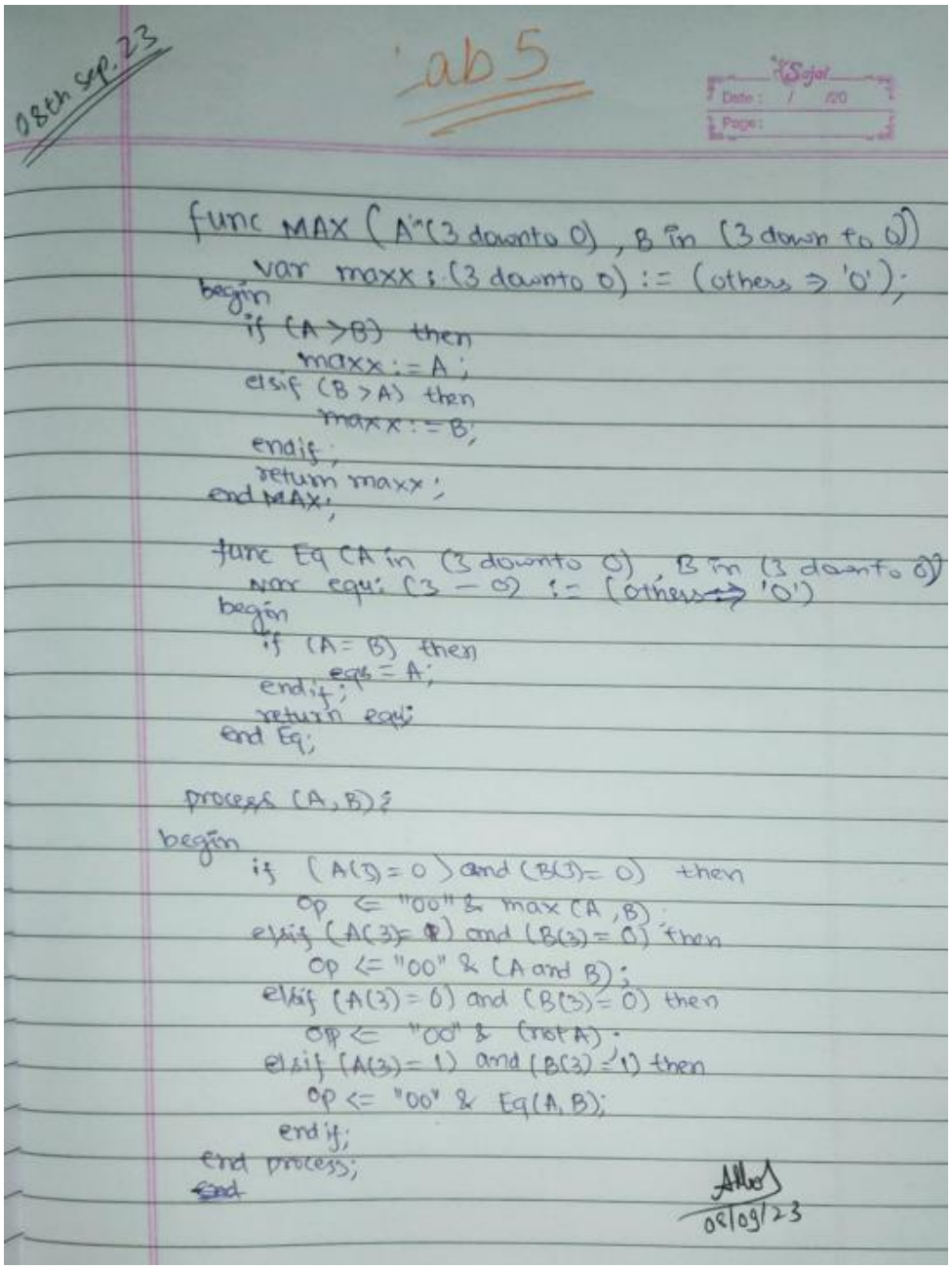
Anupam Rawat

22B3982

WEL – 2 || FR - 2 / T – 2

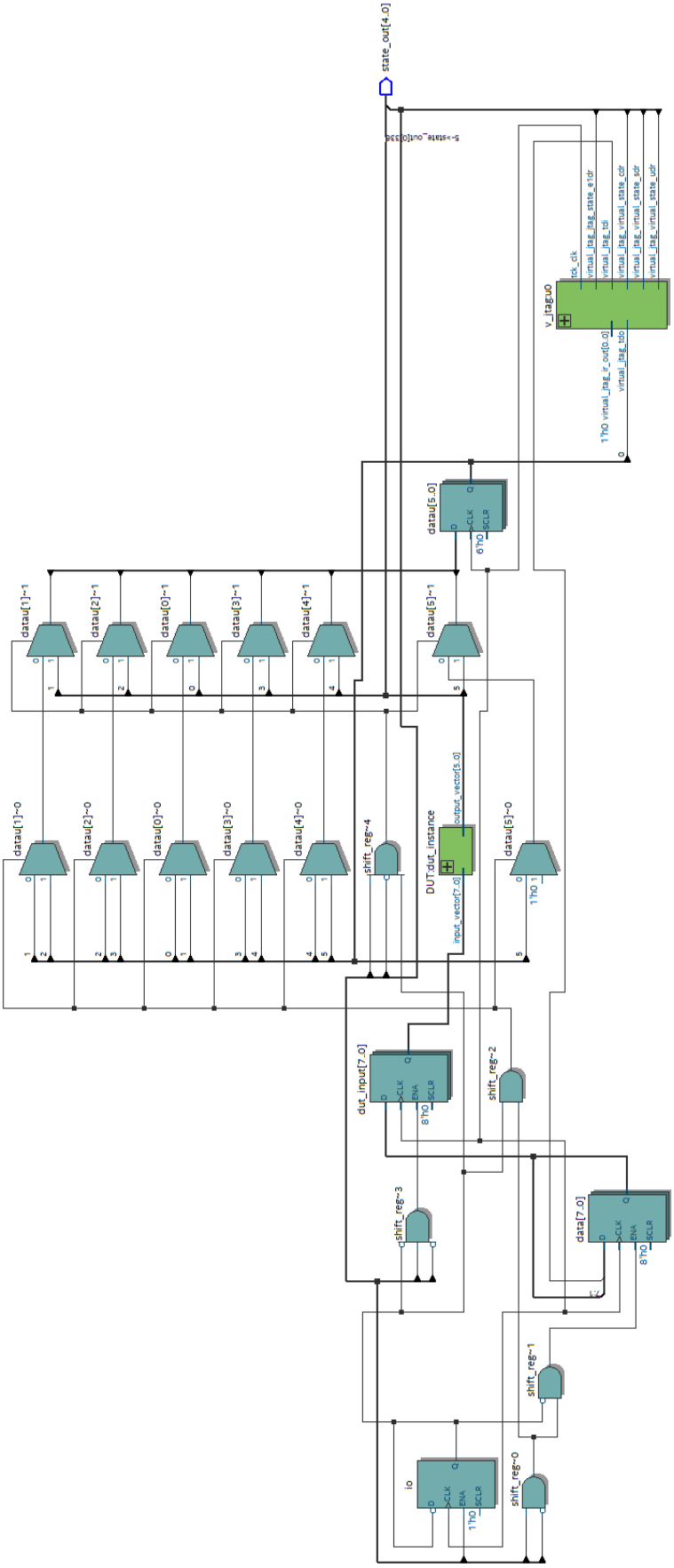
ALU

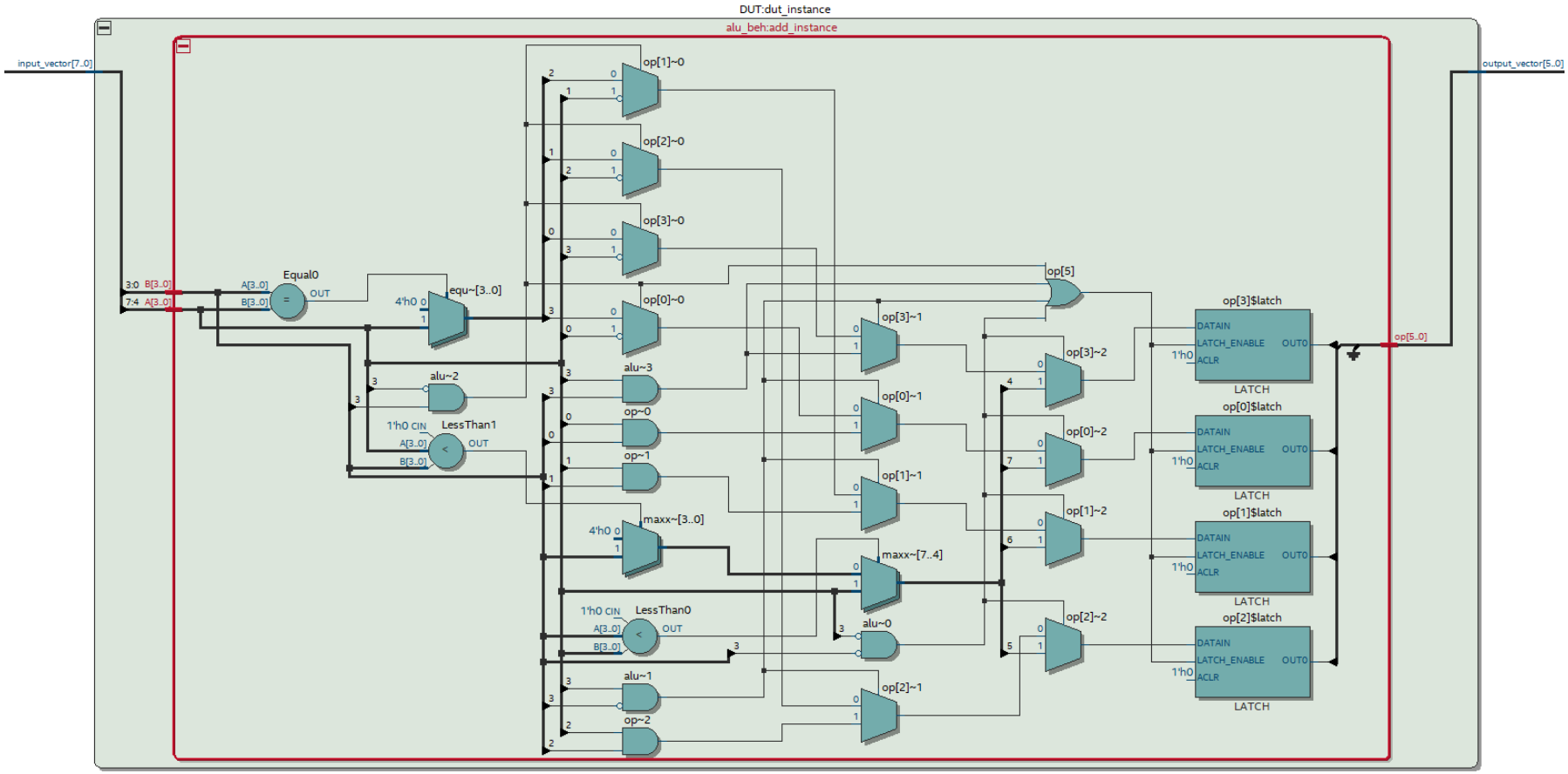
Lab Notebook:



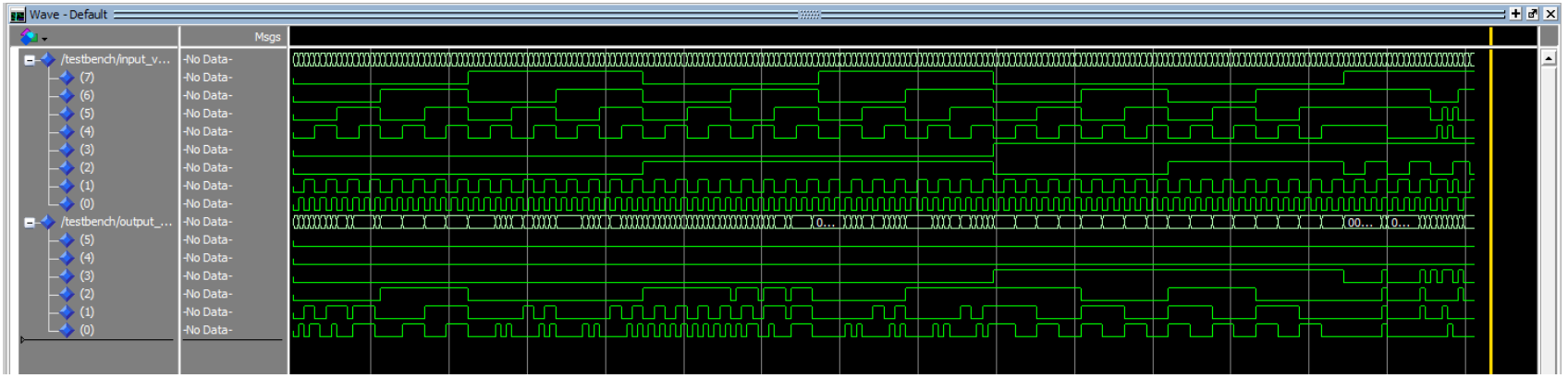
From this page onwards rotate the document.

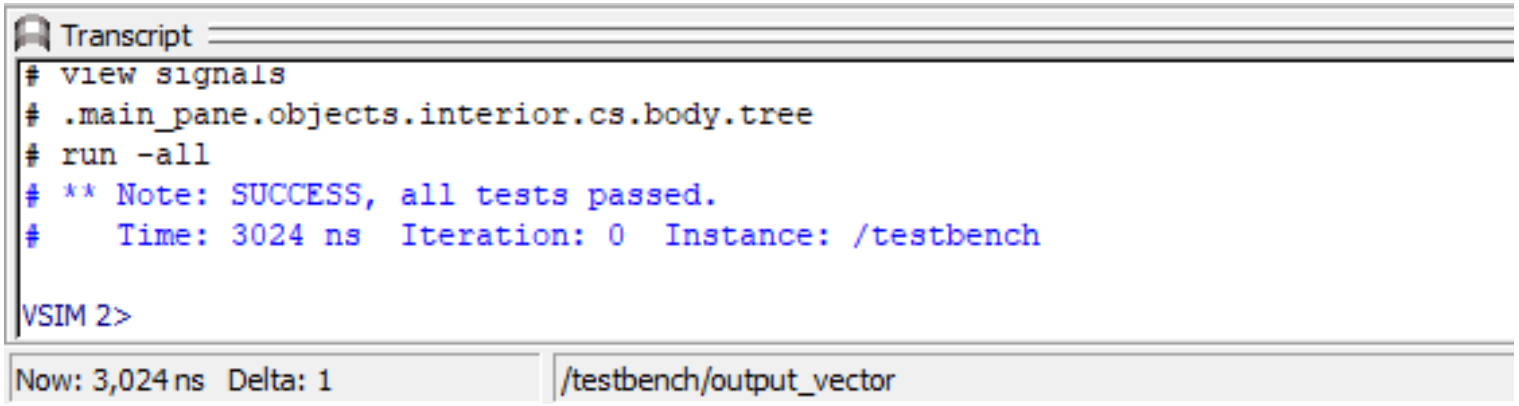
RTL Viewer:

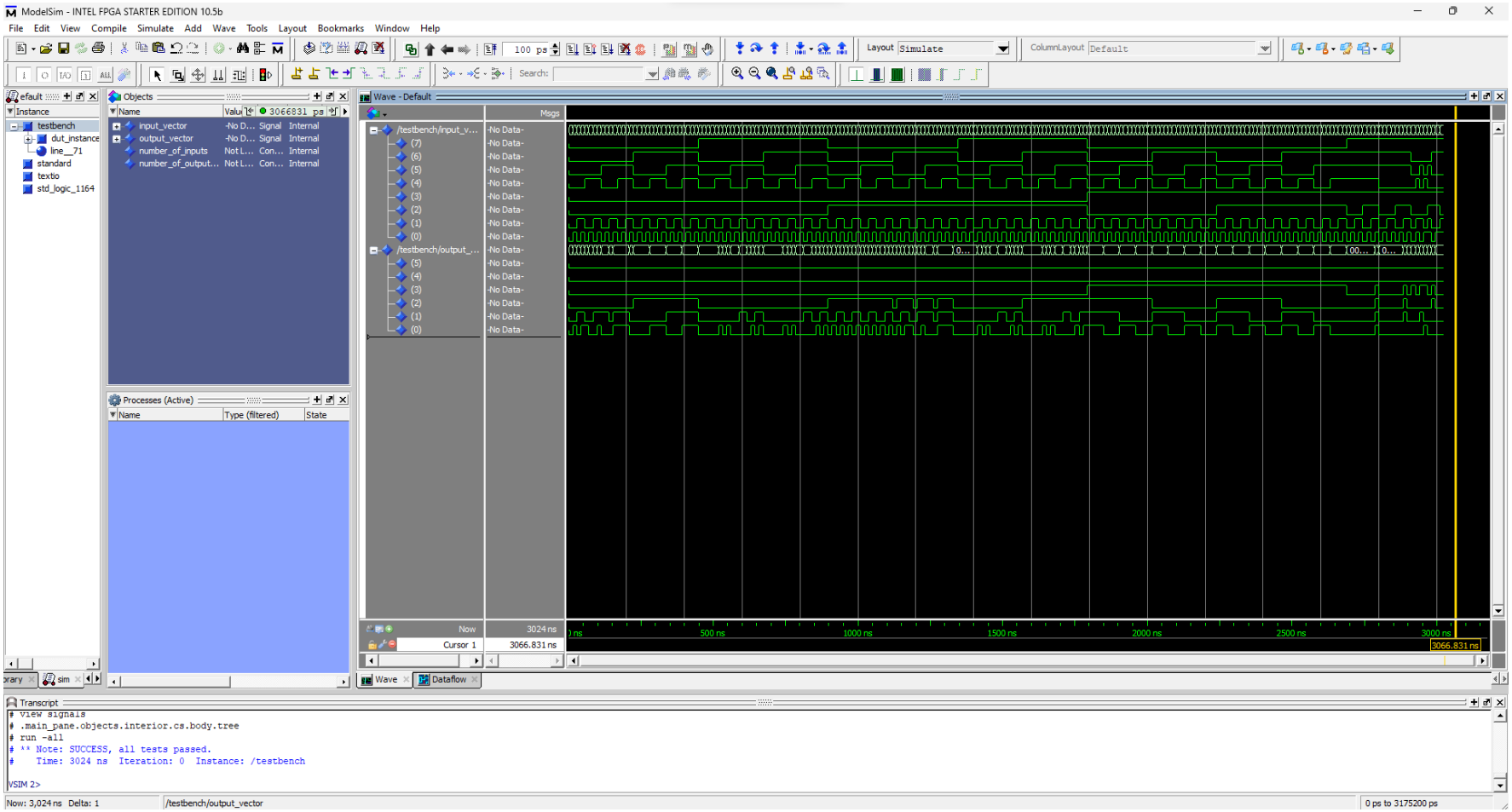

state_out[4..0]
v_itag:u0
tck_clk
virtual_jtag_tdi
virtual_jtag_virtual_state_cdr
virtual_jtag_virtual_state_sdr
virtual_jtag_virtual_state_udr
virtual_jtag_tdo
1'h0
data[5..0]
datau[1]~1
datau[2]~1
datau[0]~1
datau[3]~1
datau[4]~1
datau[5]~1
datau[1]~0
datau[2]~0
datau[0]~0
datau[3]~0
datau[4]~0
datau[5]~0
shift_reg~4
DUT:dut_instance
output_vector[5..0]
input_vector[7..0]
dut_input[7..0]
shift_reg~2
shift_reg~3
data[7..0]
shift_reg~1
io
shift_reg~0


DUT:dut_instance
alu_beh:add_instance
input_vector[7..0]
output_vector[5..0]
op[5..0]
Equal0
LessThan1
LessThan0
equ~[3..0]
maxx~[3..0]
maxx~[7..4]
alu~0
alu~1
alu~2
alu~3
op~0
op~1
op~2
op[1]~0
op[2]~0
op[3]~0
op[0]~0
op[3]~1
op[0]~1
op[1]~1
op[2]~1
op[5]
op[3]~2
op[0]~2
op[1]~2
op[2]~2
op[3]$latch
op[0]$latch
op[1]$latch
op[2]$latch
LATCH
DATAIN
LATCH_ENABLE
ACLR
OUT0

RTL Simulation :






ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Objects
Name
input_vector
output_vector
number_of_inputs
number_of_output...
Processes (Active)
Type (filtered)
State
Wave - Default
Msgs
/testbench/input_v...
/testbench/output_...
Now
Cursor 1
3024 ns
3066.831 ns
500 ns
1000 ns
1500 ns
2000 ns
2500 ns
3000 ns
Wave
Dataflow
Transcript
view signals
.main_pane.objects.interior.cs.body.tree
run -all
** Note: SUCCESS, all tests passed.
Time: 3024 ns Iteration: 0 Instance: /testbench
VSIM 2>
Now: 3,024 ns Delta: 1
/testbench/output_vector
0 ps to 3175200 ps