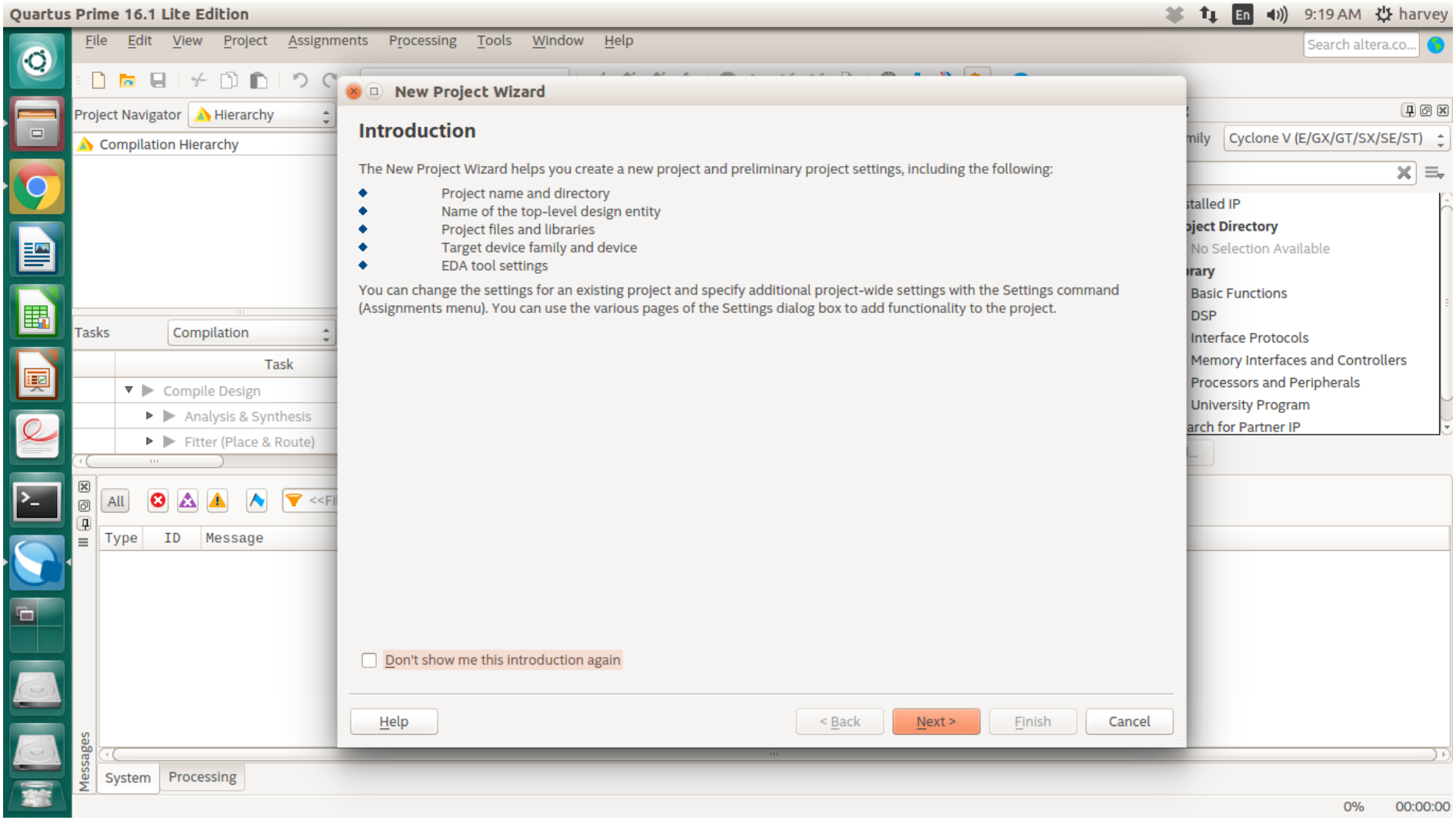
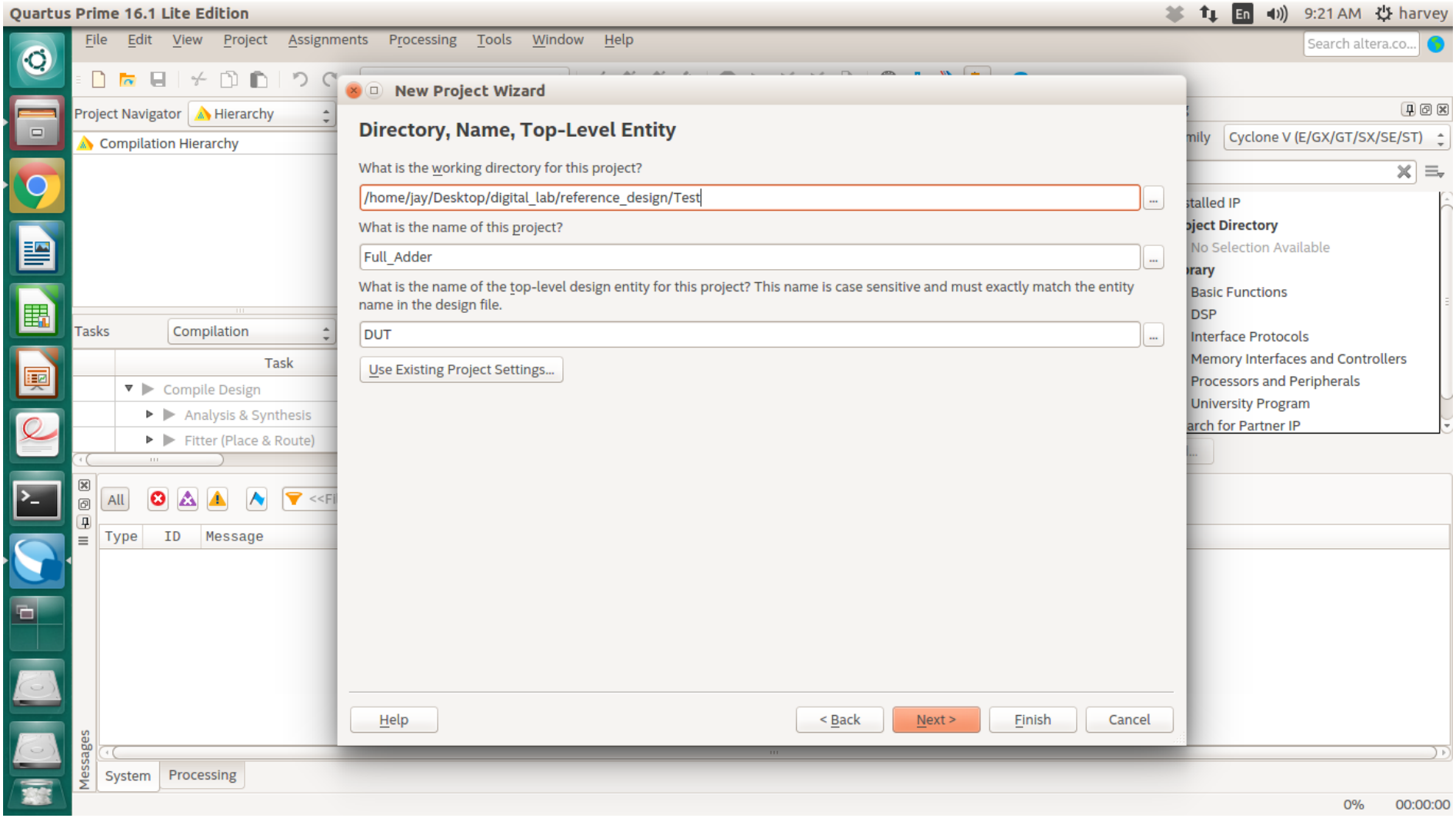
# Using Quartus II - New Project

In the introductory page, click Next.



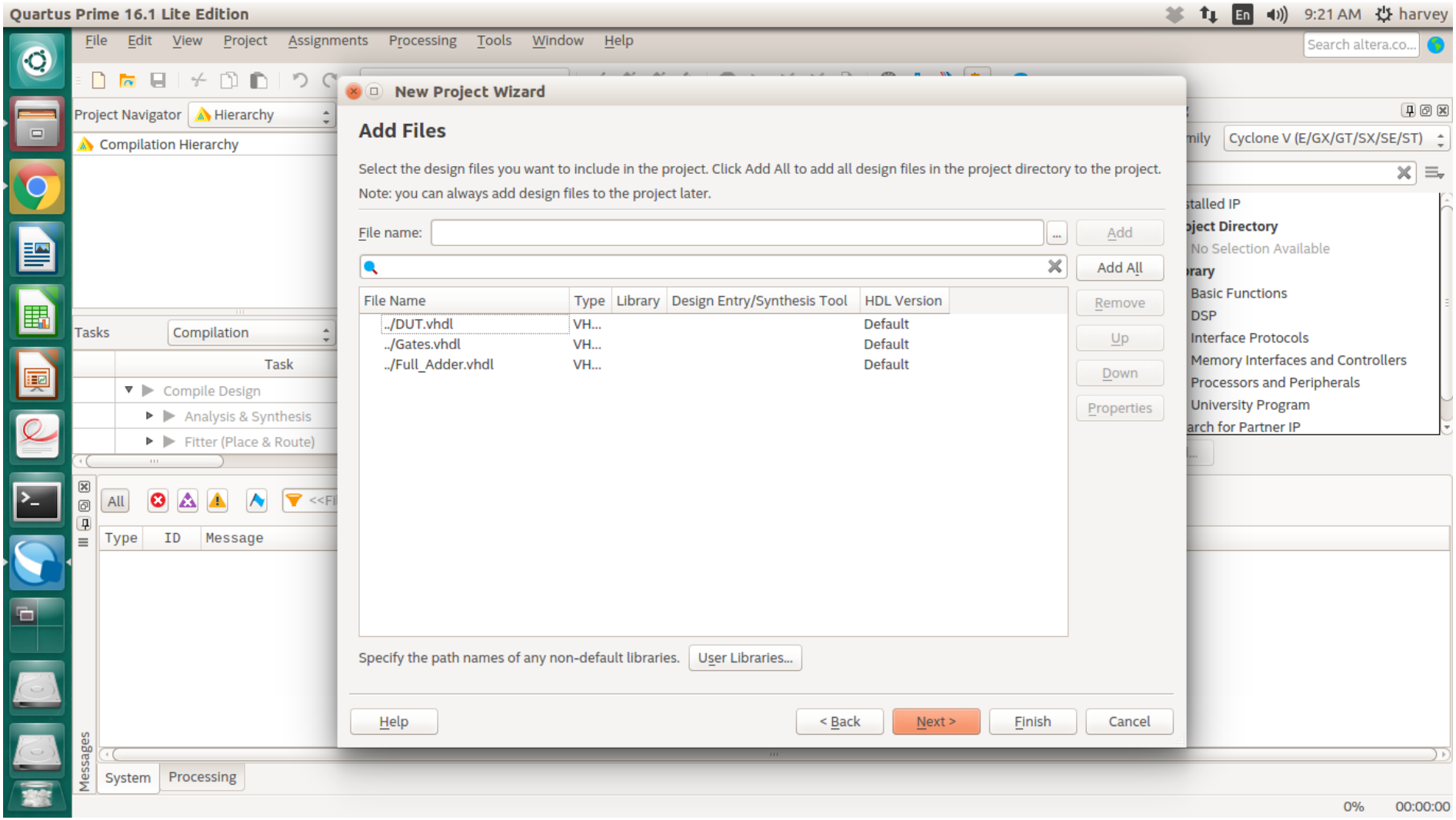
# Using Quartus II- Project Directory and Top-level Module

In this page, specify a working directory for your project. It is a good practice to open a new folder for every new project.



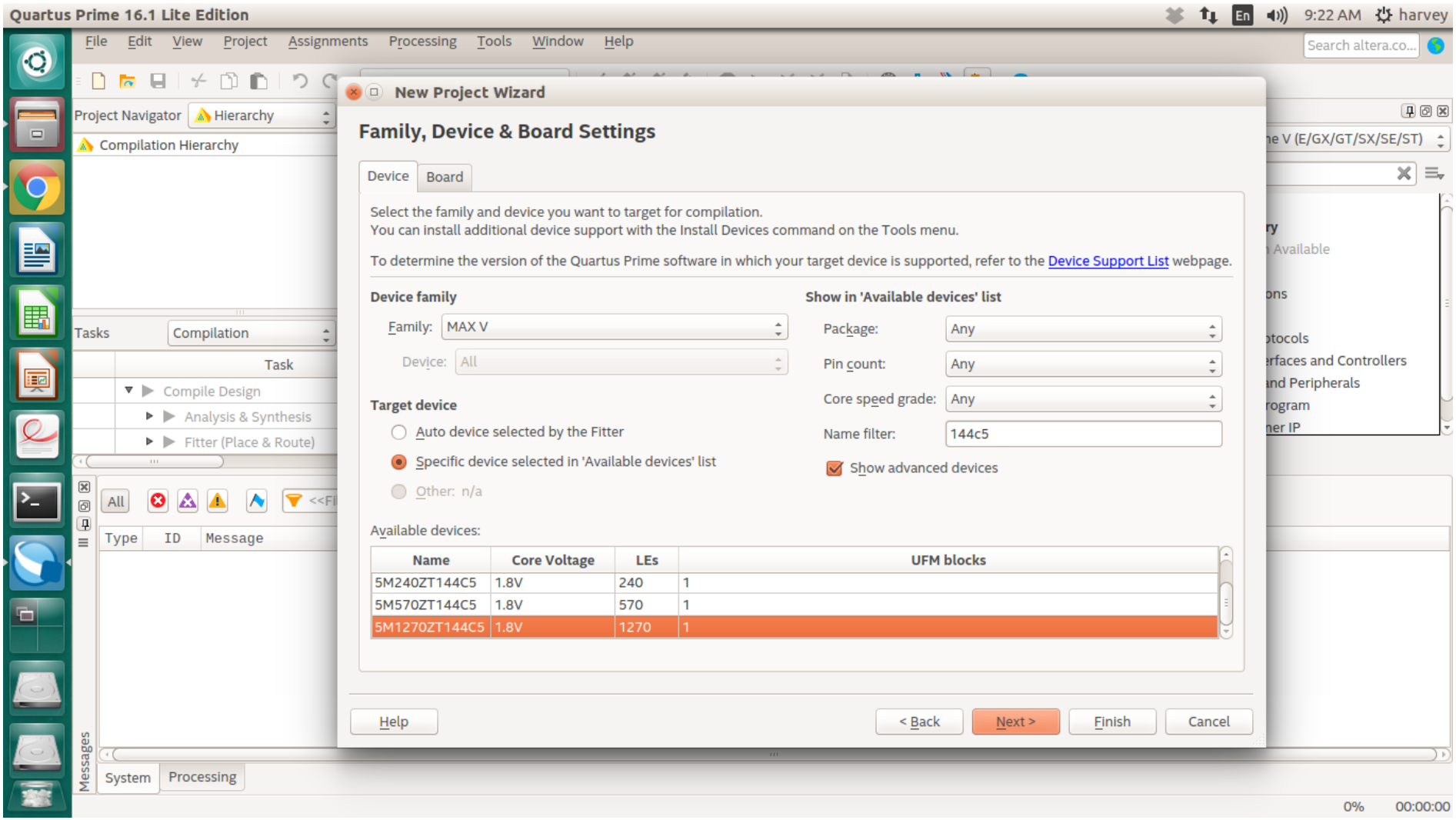
# Using Quartus II- Adding Files to Project

Next page may be skipped, In this page add all relevant files to your project.



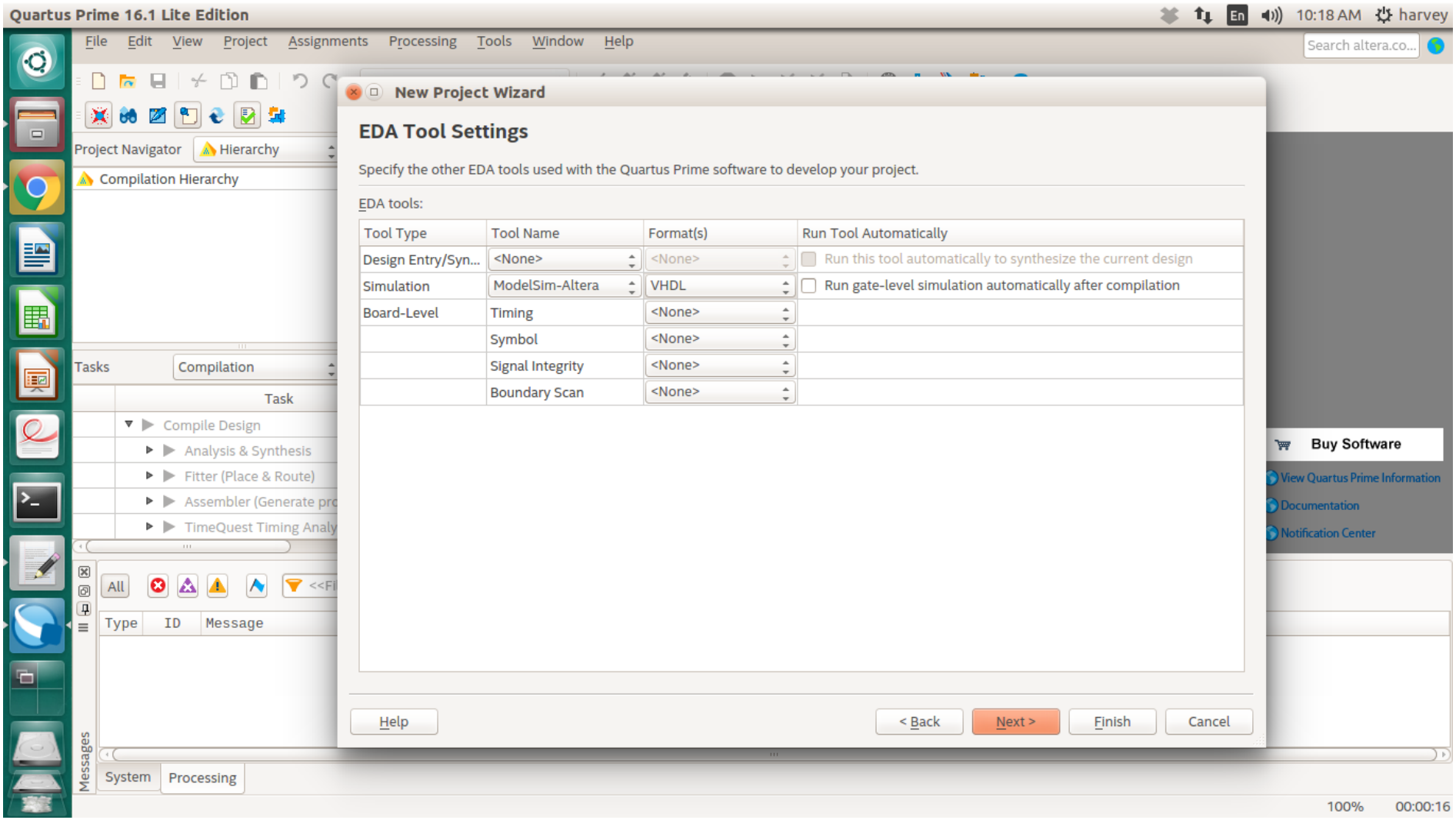
# Using Quartus II- Device Selection

In this page, select the target CPLD. Select Max V from Device family. Then type 144c5 in Name fitter and select last one.



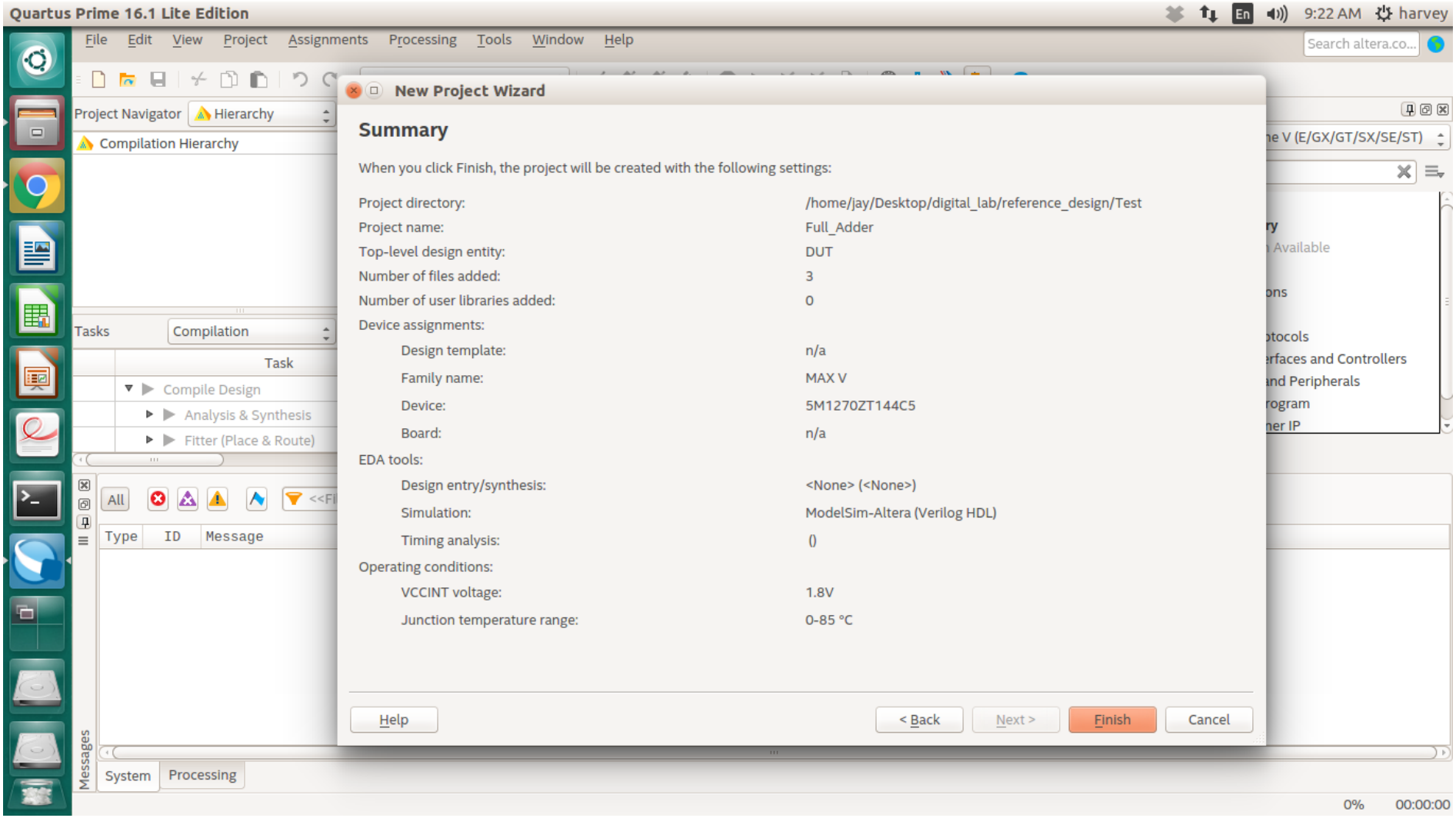
# Using Quartus II- Simulation tool and HDL Selection

In this page, select the target simulation tool as Modelsim-Altera and language as VHDL.



# Using Quartus II- Summary

This page shows you a project summary- the project name, top level module, selected device etc. If there are mistakes, you can go back and change them.

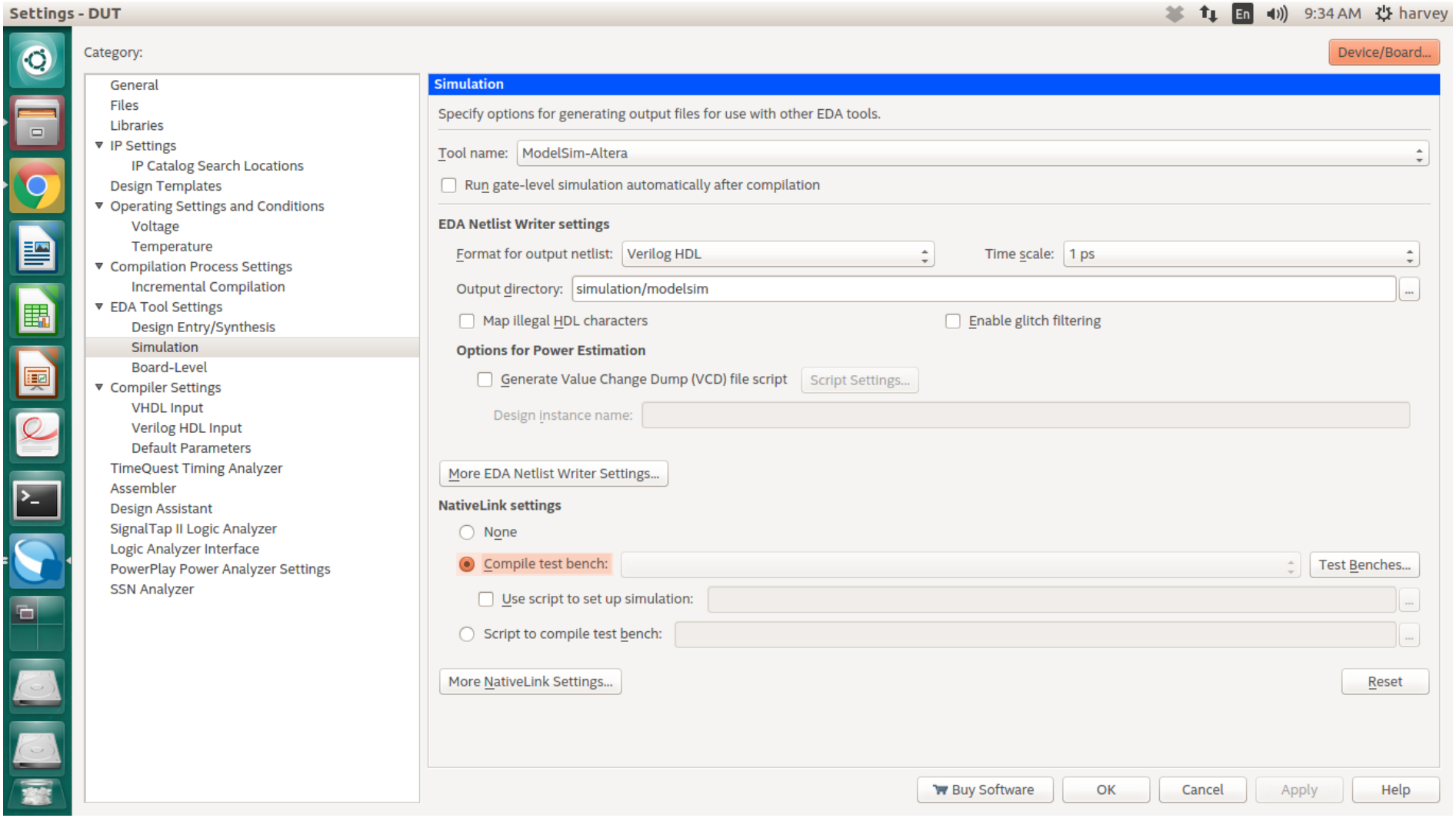


# Using Quartus II- Analysis and Synthesis

- Once you have created project and added files start compilation.
- **Make sure that you have selected proper Top-Level entity and did the full compilation.**
- If you are getting any errors resolve them. Warning can be ignored as of now.
- Now the next step is Gate Level Simulation.

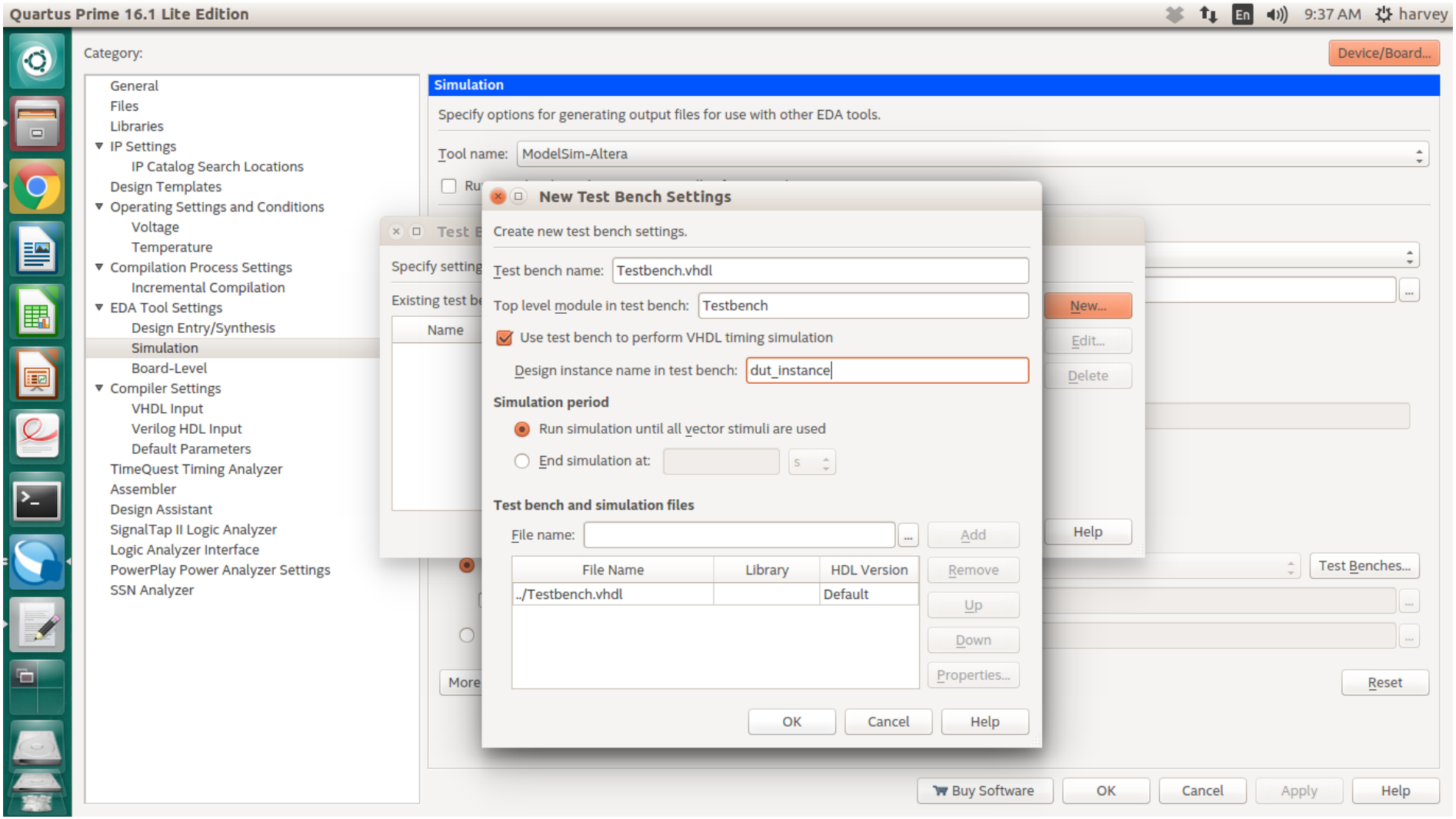
# Using Quartus II- Compiling Test Bench

Add the given Test bench in Compile the Test bench Section. (i.e. Assignmenets > Settings > Simulation). Then select Test Benches and Select New.



# Using Quartus II- Compiling Test Bench

Add the Test bench file and specify Top level module in the test bench file. Tick the Use tench bench to perform timing simulation and select the instance of design file mentioned in test file. *Add Tracefile as well.



# Using Quartus II- Gate Level Simulation

Once you are done with setting up the test bench file run gate level simulation. (Tools > Run Simulation Tool > Gate Level Simulation)