EE214 Digital Circuits Laboratory

Wadhwani Electronics Laboratory
Electrical Engineering IIT Bombay

Total Marks : 40 | MID-SEMESTER EXAM- Part B (36 Marks) | Date: September 27, 2023

Instructions:

1. Use structural modelling i.e., instantiate components, and use port mapping to connect them.
2. Draw the pen-paper design of the circuit.
3. There are 3 TRACEFILEs, one for each simulation. Show the Simulation results to your invigilator as soon as you get the results.
4. Make sure that each TRACEFILE file name is "TRACEFILE" (without the quotes, spaces or any extra character); any change in the TRACEFILE name would throw an error in simulation
5. Perform RTL simulation and Implementation on Board using the given Testbench and Tracefile.

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1. **Objective**
   Design an unsigned **BCD Adder-Subtractor circuit** using X-code.

2. **Design Description**

   The circuit should have the following inputs and outputs -

   - **Inputs: A, B, and M**
     A and B are the first and second 4-bit inputs respectively. M is of 1 bit indicating the operation to be performed. If M = '0', the circuit should perform BCD addition of A and B. If M = '1', the circuit should perform BCD subtraction of B from A.
   - **Outputs: S, Z, P, and Y**
     Y is a 5-bit Output of BCD Adder-Subtractor. S is a 1-bit sign flag which indicates if the answer is positive or negative. S = '0' if the answer is positive. Z is a 1-bit zero flag which is set to '1' if the answer is zero. P is a 1-bit even parity flag, where P = '1' if there are even number of 1's in the output Y $< Y_4Y_3Y_2Y_1Y_0 >$.

   Part - 1

   - Design a circuit to convert BCD code to X-code using **K-Map**.

   Part - 2

   - Design a circuit to perform BCD addition and subtraction using X-code. This circuit takes two inputs in X-code format.

   Part - 3

   - Design a circuit that takes the final output of the BCD adder-subtractor and determines the sign, zero, and parity flags.

3. **Pen-paper design** **[4 + 7 + 3 = 14 MARKS]**
   Draw circuit diagrams in answer sheet for the following circuits:

   (a) BCD to X-code converter using K-Map.
   (b) BCD Adder-Subtractor using X code circuit.
   (c) Circuit to determine the Sign, Zero, and Even Parity flag.
   (d) Toplevel circuit, where all circuits are integrated to realize the final circuit.

4. **RTL Simulation** **[2 + 8 + 2 = 12 MARKS]**
Write VHDL description for the following circuits and simulate each circuit using the TRACEFILEs provided:

Note: Create three distinct entities for the three parts given below.

- **BCD to X-code converter.** (You are allowed to use dataflow modelling just for this part)
(TRACEFILE for BCD to X-Code Conversion inside "TRACEFILE_For_BCD_to_X" folder).
Tracefile Format: (<A3 A2 A1 A0> <Y3 Y2 Y1 Y0> 1111)
- **BCD Adder-Subtractor using X code circuit.**
(TRACEFILE for BCD_Adder_Substractor using "TRACEFILE_BCD_Add_Subtract" folder. This TRACEFILE is for **Part1 and Part2 combined**).
Tracefile format: (<A3 A2 A1 A0 B3 B2 B1 B0 M> <Y4 Y3 Y2 Y1 Y0> 11111)
- **Circuit to determine the sign, zero, and even parity flag.**
(TRACEFILE for Flags & _BCD_Add_Subtract using "TRACEFILE_Flags & _BCD_Add_Subtract" folder. This TRACEFILE is for **Part1, Part2 and Part3 combined**).
Tracefile format: (<A3 A2 A1 A0 B3 B2 B1 B0 M> <S Z P Y4 Y3 Y2 Y1 Y0> 11111111)

Note: Make sure that you use the correct TRACEFILE for each case.

5. **Implemetation on Board** **[10 marks]**
Pin map <S1 to S4> switches to <A3 to A0>, <S5 to S8> switches to <B3 to B0>, input M to push button <PB1> [M = '1' when PB1 is pressed] and output <S Z P Y4 Y3 Y2 Y1 Y0> to Leds <LED1 to LED8>.