



**Department of Electrical Engineering
Indian Institute of Technology, Bombay**

Wadhvani Electronics Lab

**Digital System Lab
EE214**

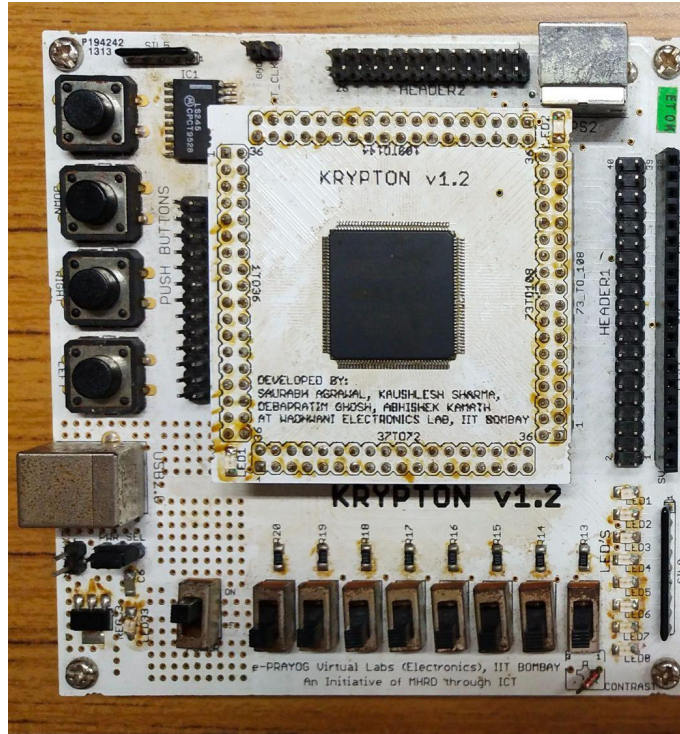
Xen 10 FPGA Board kit Demo

-Ritu Sharma

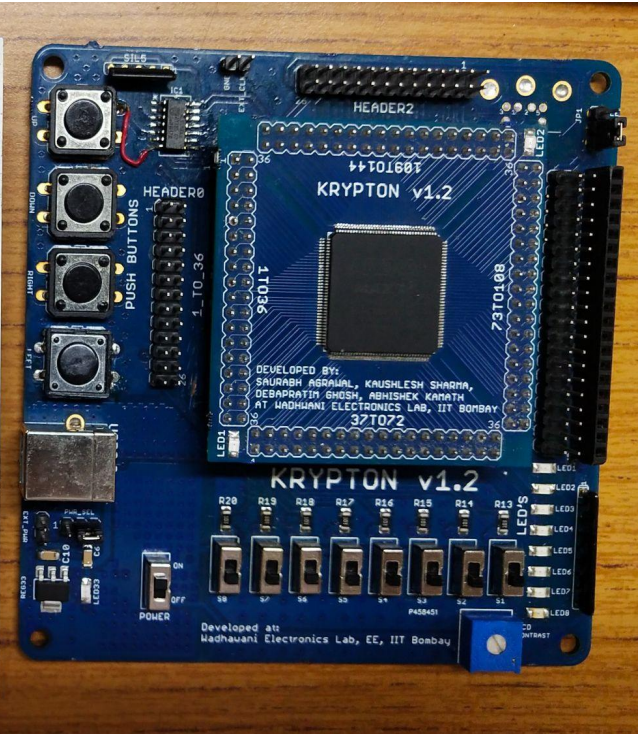
Agenda

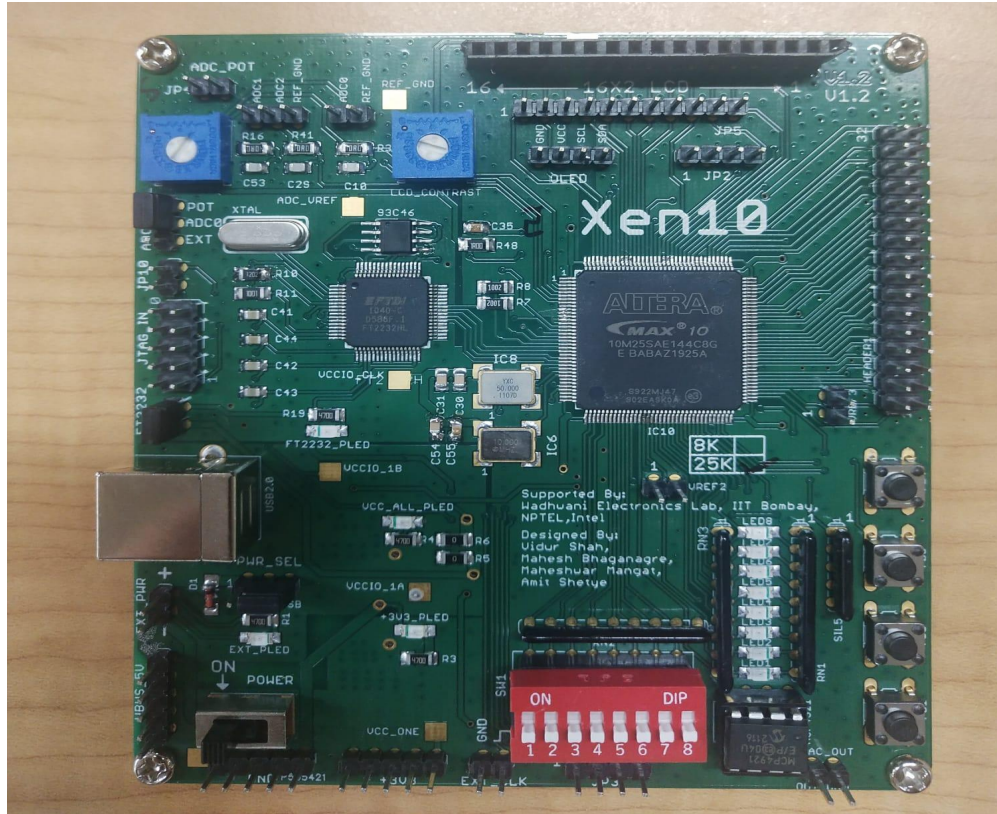
- Introduction to Xen 10 FPGA board
- Pin Planning
- Generate .svf file. svf stands for Serial Vector Format
- UrJTAG Installation and commands used
- Possible Error
- load .svf file into the FPGA using UrJTAG
- Test your Board, in order to confirm its working
- verify your full adder design by loading your fulladder.svf file and testing using the switches and LEDs

White Board



Blue Board





Designed By:
Mahesh Bhaganagre
Maheshwar Mangat
Amit Shetye
Vidur Shah

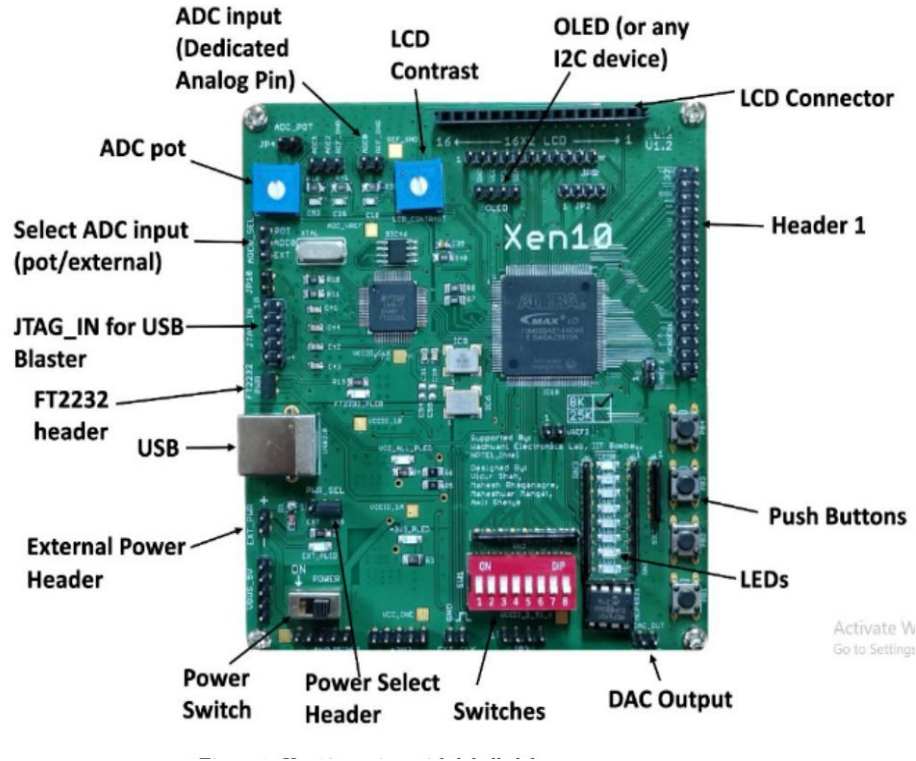


Fig: Top View of Xen 10 Board

- FPGA of Altera's MAX 10 family (**MAX 10 - 10M25SAE144C8G / 10M08SAE144C8G**)
- USB connector.
- 8 on-board switches.
- 8 on-board LEDs.
- 4 push-buttons.
- HEADER to connect to external devices.
- HEADER-1 : pin-31 is tied to VDD and 32 is tied to VSS. Never short and connect other signals to these pins.
- 16-pin connector for LCD panel and OLED or any other device with I2c interface.
- On-board 12-bit single channel MCP4921 DAC.
- On-board clock of 1Hz ,10MHz,50MHz and provision for external clock source connection through EXT CLK header.

In Pin Planning is pairing of signals with pins.

Go to Assignments -> Pin Planner. Following window will open and will be able to see all the signals of DUT .

Pin Planner - C:/Users/Lenovo/Desktop/Demo_Full_Adder_2022/Full_Adder - Full_Adder

File Edit View Processing Tools Window Help

Report not available

Groups Report

Tasks

- Early Pin Planning
 - Early Pin Planning
 - Run I/O Assignment
 - Export Pin Assignment
- Pin Finder...
- Highlight Pins
 - I/O Banks
 - VREF Groups

Top View Wire Bond

MAX 10

10M25SAE144C8G

Pin Legend

- Symbol Pin Type
- User I/O
- User assi...
- Fitter assi...
- Unbonde...
- Reserved ...
- Other co...
- DEV_OE
- DEV_CLR
- DIFF_n
- DIFF_p
- DQSB
- CLK_n
- CLK_p
- Other PLL
- Other du...
- TDI
- TCK
- TMS
- TDO
- VREF
- VCCP/VC...
- VCCA

Filter: Pins: all

Node Name	Direction	Location	I/O Bank	/REF Group	ter Locatc	'O Standar	Reserved	rent Stren	Slew Rate	fferential P	st Preserva
input...tor[2]	Input	PIN_38	3	B3_NO	PIN_38	2.5 V		12mA...ult			
input...tor[1]	Input	PIN_39	3	B3_NO	PIN_39	2.5 V		12mA...ult			
input...tor[0]	Input	PIN_41	3	B3_NO	PIN_41	2.5 V		12mA...ult			
output...tor[1]	Output	PIN_50	3	B3_NO	PIN_50	2.5 V		12mA...ult	2 (default)		
output...tor[0]	Output	PIN_60	3	B3_NO	PIN_60	2.5 V		12mA...ult	2 (default)		

<<new node>>

- Write Pin no in location column for assigning Input and output pins to the signals .
- Go to Processing -> Start I/O Assignment analysis.
- Once done close the window and compile your design again.

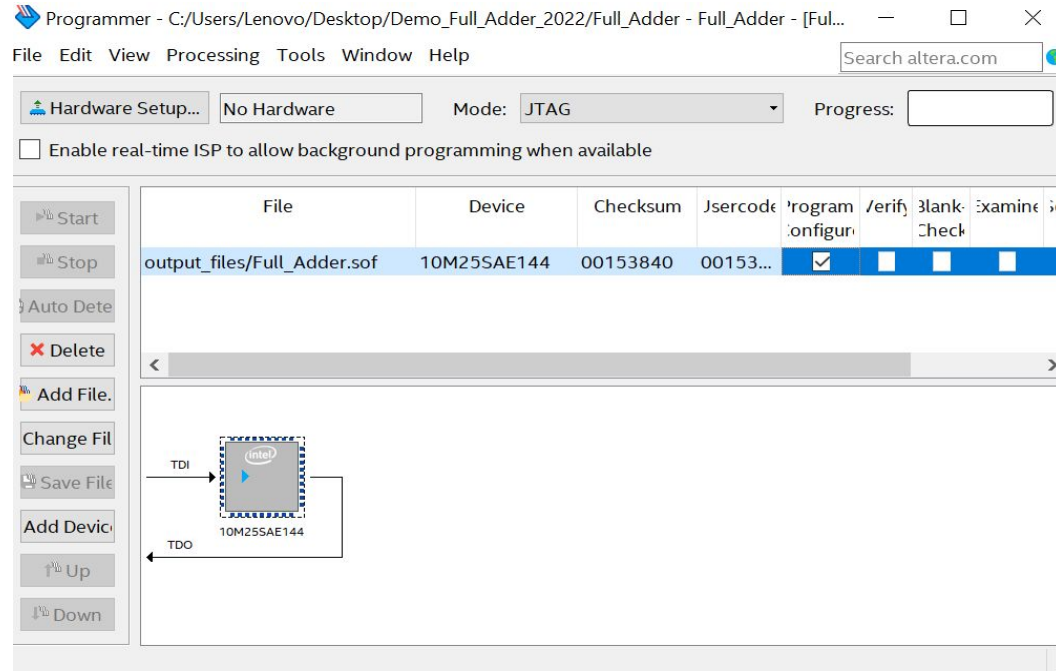
Named: *	▼	⚡	Edit: X	✓	PIN_60
Node Name	Direction	Location	I/O Bank		
in input_vector[2]	Input	PIN_38	3		
in input_vector[1]	Input	PIN_39	3		
in input_vector[0]	Input	PIN_41	3		
out output_vector[1]	Output	PIN_50	3		
out output_vector[0]	Output	PIN_60	3		
<<new node>>					

Assignment of Input /Output Pins

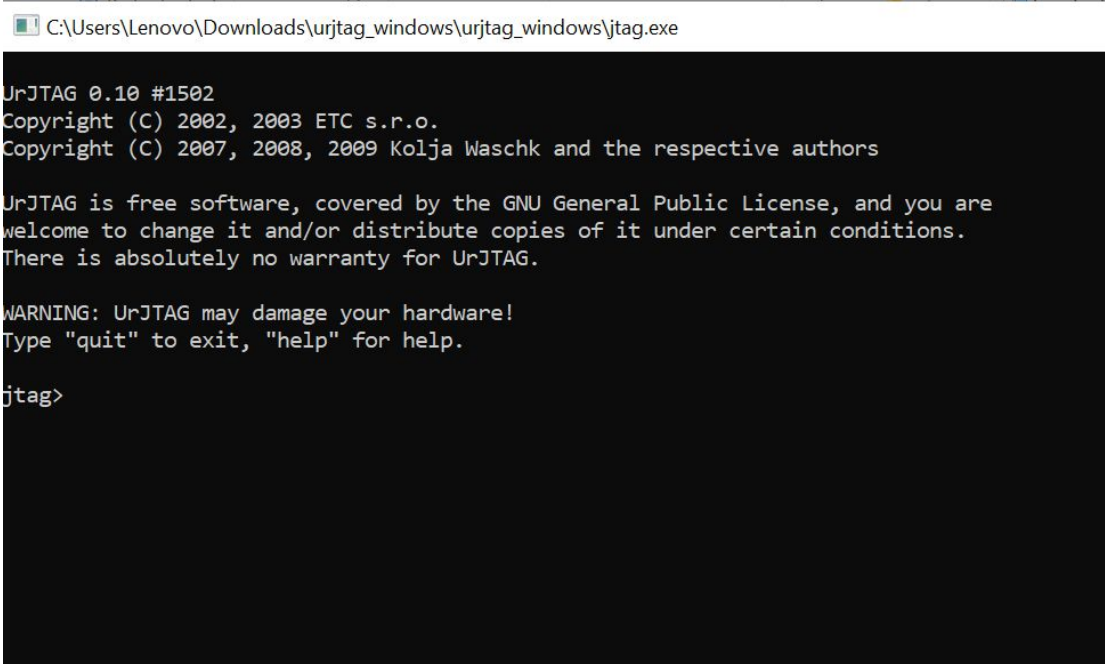
Switch	FPGA Pin no.	LED	FPGA Pin no.
SW 8	47	LED 8	60
SW 7	46	LED 7	59
SW 6	45	LED 6	58
SW 5	44	LED 5	57
SW 4	43	LED 4	56
SW 3	41	LED 3	54
SW 2	39	LED 2	52
SW 1	38	LED 1	50

Pin Mapping for On-board switches and leds

- Go to Tools -> Programmer (Following Window will appear)
- Go to File -> Click on Create JAM,JBC,SVF or ISC file
- Change the File format to .svf then Click OK(Can change the file name also)
- .svf file will be generated in your folder.



- JTAG : Joint Test action Group
- Download the UrJTAG_Max10 Zip folder [Link for UrJTAG](#) and extract it.
- Inside UrJTAG open jtag.exe file , below jtag window will open.
- Connect your Xen10 Board to your device.



```
C:\Users\Lenovo\Downloads\urjtag_windows\urjtag_windows\jtag.exe

UrJTAG 0.10 #1502
Copyright (C) 2002, 2003 ETC s.r.o.
Copyright (C) 2007, 2008, 2009 Kolja Waschk and the respective authors

UrJTAG is free software, covered by the GNU General Public License, and you are
welcome to change it and/or distribute copies of it under certain conditions.
There is absolutely no warranty for UrJTAG.

WARNING: UrJTAG may damage your hardware!
Type "quit" to exit, "help" for help.

jtag>
```

- In terminal type: **jtag**
Now you will be presented with a command console. (Only for Ubuntu)
- Type: **cable ft2232 vid=0x0403 pid=0x6010**
An indication should now appear that the driver is connected. You can use lsusb command after connecting the board to know pid and vid.
- Now type: **detect**
which displays the detected CPLD device (Details like IRChain length, Manufacturer, Device ID, Stepping etc.)
- Load the svf file into the CPLD device by typing
svf <path> /<Name_of_File.svf> progress
Either drag the file to the jtag window for path or Copy the .svf file to UrJTAG folder.

LINK FOR DEMO OF FULL ADDER ON XEN 10 BOARD

[Link For Xen10 Demo video](#)

- ❖ Hardware Detect, TDI/TDO stuck at 0/1.
 - Reconnect the board
 - Use different USB port
 - Restart your computer/Laptop.
- ❖ Part not found/ Unknown Manufacturer.
 - Reinstall using the script for Ubuntu.
- ❖ Segmentation Fault.
 - Reinstall using the script for Ubuntu.
- ❖ Strange error : SIR Instruction Length Inconsistent.
 - Create new project.

Test File will be provided just need to load and test the board with proper connections .

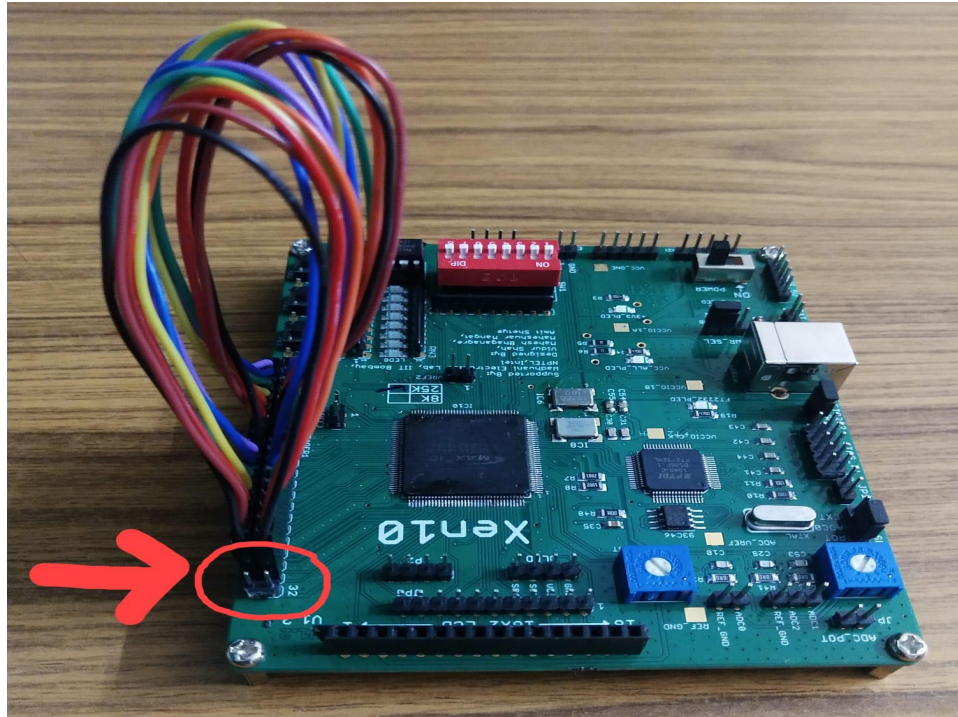
[Link for Xen10 Board Testing files 10M25SAE144C8G](#)

[Link for Xen10 Board Testing Files 10M08SAE144C8G](#)

Required Connection:

- Connect LCD to LCD header , ensuring pin-1 of LCD is connected to the corresponding pin-1 of the 16x2 LCD header.
- Connect pins of Header-1 using strip cables. Pin-1 should be connected to pin-2, similarly pin-3 to pin -4 and so on until pin-29 to pin-30 .
Make sure that pin-31 (i.e. VDD) should not be connected to pin-32(i.e. GND) of the header .





Header 1 Connection : Pin 31 is not connected to Pin 32.

Svf file to be loaded according to your device , initially all switches are to be kept off.

- ❖ Make SW8 on to reset the system and make it off after resetting. On successful reset LCD will display “**Welcome: Xen10 Design by WEL**” this implies SW8 is working properly.
- ❖ After that LCD will displayed “**Push PB1 for starting**”. Press PB1 to start Xen 10 board testing.
- ❖ Testing will start with Clock frequencies testing : **50 MHz, 10 MHz and 1 Hz** clock generators are tested sequentially. Clock pulses are counted and displayed on LED's in binary encoded format, once a threshold count is reached, LCD will display “**Done**” message.

- ❖ “**Test SW and LED**” will appear on LCD .
Turn on SW1. Notice one led will blink at a time and shift through all the LEDs. Similarly when SW2 is turned on keeping the SW1 on, two LEDs will blink and shift and so on until SW7 is turned on where seven LEDs will blink and shift. Once all switches till SW7 are on, LCD will display “**Done**”.
- ❖ **Push Button Testing:** After completing switch and LED test, LCD will display “**Test: Push Button**”. Press each push button at least once to pass the test.
- ❖ **Bidirectional Pin Header Testing:** Switch on SW4 and press PB2 after the LCD displays “**SW on SW4, Press PB2: test Header**”. Result of Header-1 testing will be displayed on LCD within few seconds.

Can we use this (Pin Planning) method to verify any design ?

Thank you