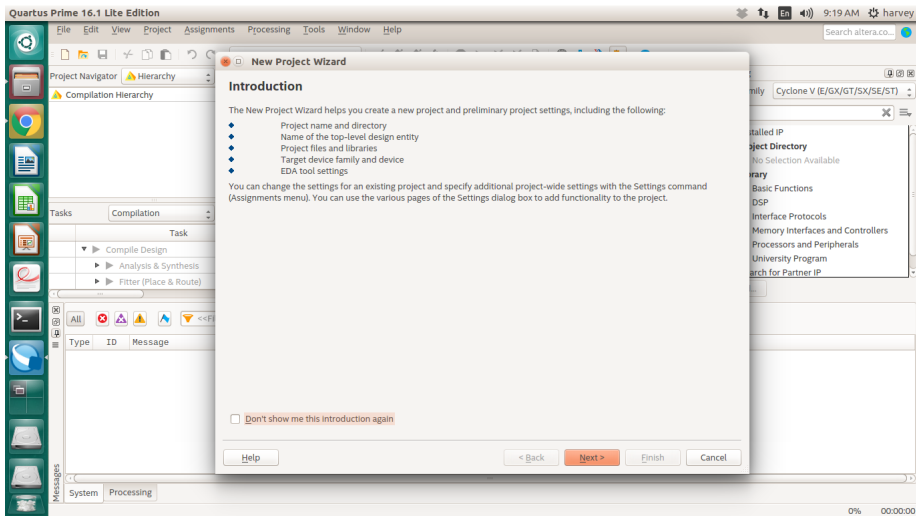


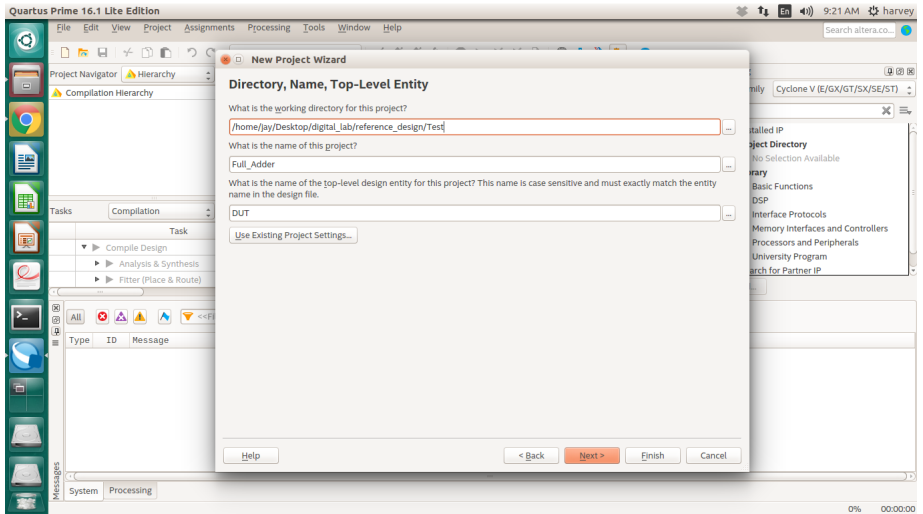
Using Quartus II - New Project

In the introductory page, click Next.



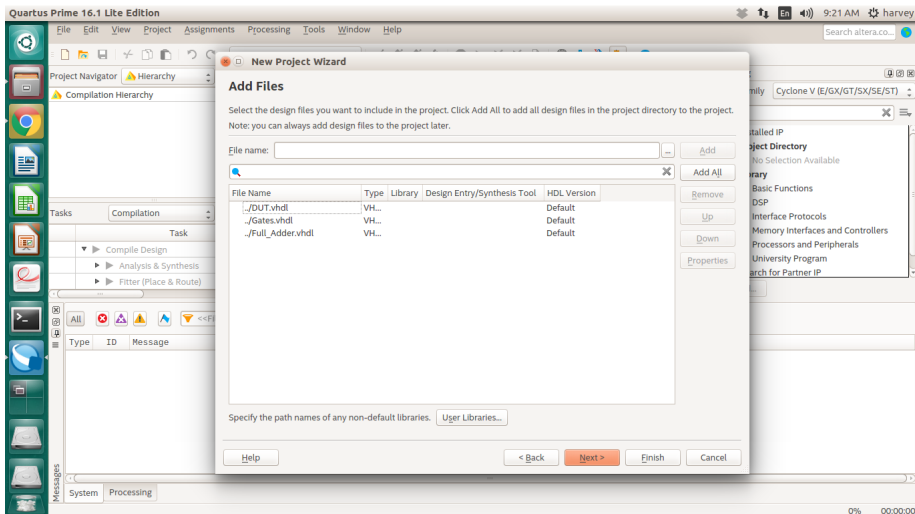
Using Quartus II- Project Directory and Top-level Module

In this page, specify a working directory for your project. It is a good practice to open a new folder for every new project.



Using Quartus II- Adding Files to Project

Next page may be skipped, In this page add all relevant files to your project.



Using Quartus II- Device Selection

In this page, select the target CPLD. Select Max V from Device family. Then type 144c5 in Name filter and select last one.

Quartus Prime 16.1 Lite Edition

File Edit View Project Assignments Processing Tools Window Help

Search altera.co...

Project Navigator Hierarchy

Compilation Hierarchy

Tasks Compilation

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

All

Type ID Message

Messages

System Processing

New Project Wizard

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: MAX V

Device: All

Show in 'Available devices' list

Package: Any

Pin count: Any

Core speed grade: Any

Name filter: 144c5

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

☒ Show advanced devices

Available devices:

Name	Core Voltage	LEs	UFM blocks
5M240ZT144C5	1.8V	240	1
5M570ZT144C5	1.8V	570	1
5M1270ZT144C5	1.8V	1270	1

Help < Back Next > Finish Cancel

0% 00:00:00

Using Quartus II- Simulation tool and HDL Selection

In this page, select the target simulation tool as Modelsim-Altera and language as VHDL.

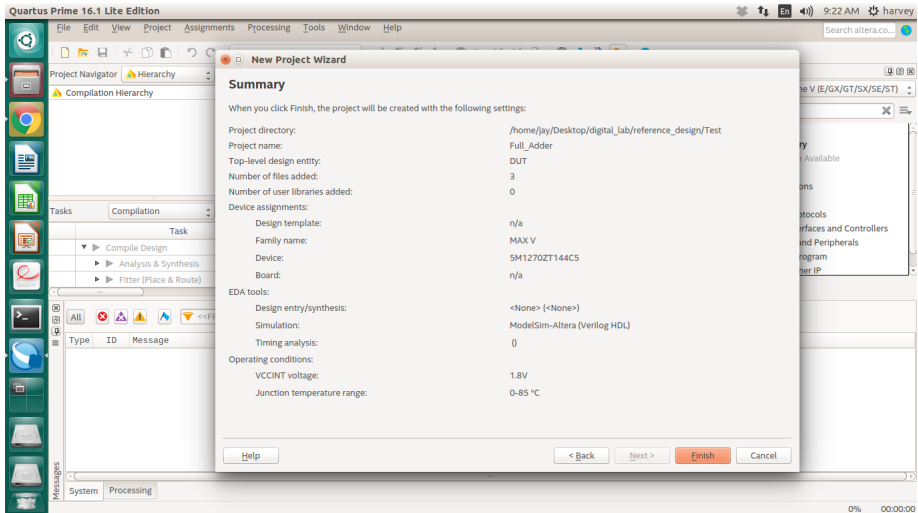
The screenshot shows the Quartus Prime 16.1 Lite Edition interface. The 'New Project Wizard' dialog box is open, displaying the 'EDA Tool Settings' tab. The dialog box prompts the user to specify other EDA tools used with the Quartus Prime software. The 'EDA tools' section contains a table with the following data:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Syn...	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	VHDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

Below the table, there are buttons for 'Help', '< Back', 'Next >', 'Finish', and 'Cancel'. The 'Next >' button is highlighted in orange. The background shows the Quartus Prime interface with the 'Project Navigator' and 'Tasks' panels visible.

Using Quartus II- Summary

This page shows you a project summary- the project name, top level module, selected device etc. If there are mistakes, you can go back and change them.

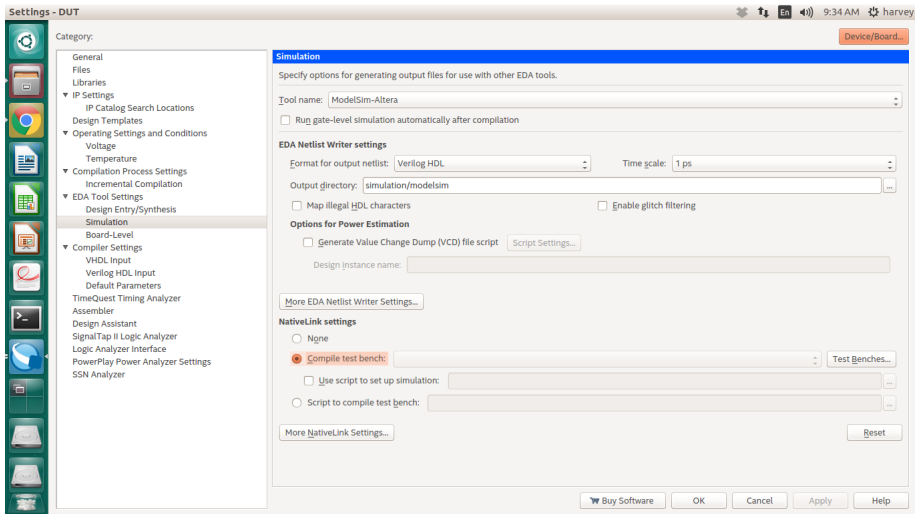


Using Quartus II- Analysis and Synthesis

- Once you have created project and added files start compilation.
- **Make sure that you have selected proper Top-Level entity and did the full compilation.**
- If you are getting any errors resolve them. Warning can be ignored as of now.
- Now the next step is Gate Level Simulation.

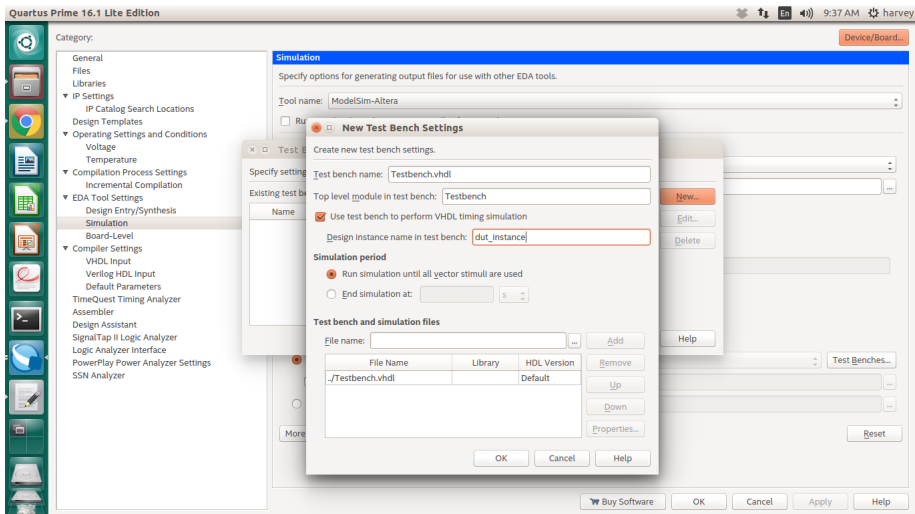
Using Quartus II- Compiling Test Bench

Add the given Test bench in Compile the Test bench Section. (i.e. Assignments > Settings > Simulation). Then select Test Benches and Select New.



Using Quartus II- Compiling Test Bench

Add the Test bench file and specify Top level module in the test bench file. Tick the Use tench bench to perform timing simulation and select the instance of design file mentioned in test file. ***Add Tracefile as well.**



Using Quartus II- Gate Level Simulation

Once you are done with setting up the test bench file run gate level simulation.
(Tools > Run Simulation Tool > Gate Level Simulation)

The screenshot displays the Quartus Prime 16.1 Lite Edition interface. The Project Navigator on the left shows files: ./DUT.vhdl, ./Gates.vhdl, and ./Full_Adder.vhdl. The Tasks window shows 'Compile Design' (00:00:22) and 'Analysis & Synthesis' (00:00:11). The Messages window shows two messages: 'Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning' and '293000 Quartus Prime Full Compilation was successful. 0 errors, 13 warnings'. The EDA Gate Level Simulation dialog box is open, showing 'Timing model: "Slow Model"' and a 'Run' button. The Flow Summary window on the right provides details about the compilation process.

EDA Gate Level Simulation

Timing model: "Slow Model" [Run]

Flow Summary

Flow Status: Successful - Mon Jan 28 09:38:02 2019

Quartus Prime Version: 16.1.0 Build 196 10/24/2016 SJ Lite Edition

Entity Name: DUT

Entity Name: DUT

MAX V

5M12702T144C5

Timing Models: Final

Total logic elements: 2 / 1,270 (< 1 %)

Total pins: 5 / 114 (4 %)

Total virtual pins: 0

UFM blocks: 0 / 1 (0 %)

System: Processing (104)

100% 00:00:22