



Designing Circuits using Universal Gate NAND

Instructions:

1. NAND is a universal gate.
2. For writing VHDL description, use the NAND gate provided in Gates.vhdl (which has been provided in [Resource Files](#)).
3. Do pen paper design, use proper labeling for each wire and use the same labels in the VHDL code.
4. Perform RTL simulation using the provided testbench and tracefile.

Problem Statement:

1. Design and describe AND gate, XOR gate, OR Gate using NAND gate in VHDL using Structural modeling.
2. Design Half Adder and Full Adder using NAND gates (pen-paper design).
3. Describe Half Adder and Full Adder using NAND gates in VHDL using Structural modeling (use the XOR gate that you have designed using NAND gates).
4. Verify the working of your design by performing RTL simulation using the given tracefile and testbench.

NOTE:

- TRACEFILE for AND gate: [AND_Tracefile](#)
Format: InputX1 X0 OutputY0 MASK1
- TRACEFILE for OR gate: [OR_Tracefile](#)
Format: InputX1 X0 OutputY0 MASK1
- TRACEFILE for XOR gate: [XOR_Tracefile](#)
Format: InputX1 X0 OutputY0 MASK1
- TRACEFILE for HalfAdder: [HalfAdder_Tracefile](#)
Format: Input{X1 X0} Output{Sum Carry} MASK{1 1}
- TRACEFILE for FullAdder : [FullAdder_Tracefile](#)
Format: Input{X2 X1 X0} Output{Sum Carry} MASK{1 1}