Practice Problems

General Instruction

- Create your own testbench for all the problem given to you.

Level I

1. Create a D-latch using behavioral modelling.
2. Create a JK-Flipflop using behavioral modelling. (Make sure to have Enable signal, preset and reset signal while creating the flipflop other than clock and J,K input signals)
3. Create a D-FlipFlop using JK-Flipflop created above. Use structural modelling. Use JK-Flipflop as an component. (Make sure to have Enable signal, preset and reset signal while creating the flipflop.other than clock and D input signal)

Level II

1. Create an 4-bit asynchronous up counter using the JK-Flipflop created in the above question. Use the structural modelling.
2. Create an 4-bit synchronous down counter using the D-Flipflop created in the above question.

Level III

1. Create a 16-bit up-down synchrounous counter. Use structural modelling. Take a input "M". If M = '0', it will work as up counter and if M = '1' it will work as down counter. (Take the help of entities created by you in above problems)
   HINT: There is a pattern involved when finding the equation for input to each stage Flipflop. This will ease your coding length.
2. Solve the FSM problem of "STUDENTS" (given as homework at beginning of FSM experiment) using only Structural modelling. (Take the help of entities created by you in above problems)