Functions in VHDL

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2022

Functions

- Functions are part of a group of structures in VHDL called subprograms.
- Functions are small sections of code that perform an operation that is reused throughout your code.
- Functions are used to describe frequently used sequential algorithms that return a single value.
- Functions always use a return statement. They are generally good for doing a small amount of logic or math and returning a result.
- **Note: "wait" statements can not be used in a function.**

Function Syntax

```
function <function_name> (<parameter1_name> : <parameter1_type> := <default_value>;
                          <parameter2_name> : <parameter2_type> := <default_value>;
                          .
                          .
                          <parameterN_name> : <parameterN_type> := <default_value>)
                          return <return_type> is

<constant_or_variable_declaration>

begin

    <code_performed_by_the_function>
    return <value>

end function;
```

Example

```
function add(A: in std_logic_vector(3 downto 0);
             B: in std_logic_vector(3 downto 0))
return std_logic_vector is
    variable sum   : std_logic_vector(3 downto 0);
    variable carry : std_logic_vector(3 downto 0);

begin
    L1: for i in 0 to (operand_width-1) loop
            if i = 0 then
                sum(i)   := A(i) Aor B(i) Aor '0';
                carry(i) := A(i) and B(i);
            else
                sum(i)   := A(i) Aor B(i) Aor carry(i-1);
                carry(i) := (A(i) and B(i)) or (carry(i-1) and (A(i) or B(i)));
            end if;
        end loop L1;
    return carry(3) & sum;
end add;
```