Implementation of Parallel Dictionary LZW (PDLZW) Data Compression Algorithm on FPGA

Digital Circuits Lab

EE-214

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1 Abstract:

Lempel-Ziv-Welch (LZW) technique is a lossless data compression algorithm. Parallel dictionary LZW (PDLZW) is a modified version of LZW, which is compatible with the VLSI design implementation Data Compression method. It also speeds up the LZW encoding by using multiple dictionaries. It encodes rules that allow a substantial reduction in the total number of bits to store or transmit a file. LZW is commonly used in GIF files, optionally in PDF and TIFF.

2 Introduction:

You are supposed to implement a research paper published on the parallel dictionary LZW algorithm (mentioned in reference). You will require a thorough understanding of the Finite State Machine. You will learn how to design a circuit using a datapath and controller

3 Weekly Milestones to be followed by Students

1. **Week 1:**
   Design the circuit and FSM controller (Datapath-Controller style) to realize the algorithm on pen and paper. Write a VHDL description for each entity required in datapath and FSM controller. You can use structural, behavioral, or dataflow modeling as per your ease to define these entities. However, the top-level entity where all components are integrated should be in structural modeling. (This will give you a better understanding of digital circuits). You are expected to complete till RTL simulation.

2. **Week 2:**
   Implement this on the MAX-10 FPGA Board. Design interfacing between the host and FPGA board to send text/GIF data from the host to FPGA and get it compressed back to the host. (You can use scan chain for this).

   At the end you are expected to show the uncompressed and compressed files.

4 References:

[1.] M. -b. Lin, J. -f. Lee and G. E. Jan, "A Lossless Data Compression and Decompression Algorithm and Its Hardware Architecture," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 14, no. 9, pp. 925-936, Sept. 2006, doi: 10.1109/TVLSI.2006.884045.

[2.] Ming-Bo Lin, "A Parallel VLSI Architecture For The LZW Data Compression Algorithm," Proceedings of Technical Papers. International Symposium on VLSI Technology, Systems, and Applications, Taipei, Taiwan, 1997, pp. 98-101, doi: 10.1109/VTSA.1997.614737.