

EECS 318
Electronics Lab
Laboratory #7
Binary Adders

Objective:

The objective for this lab is to understand the design of a half adder and a full adder using logic gates.

Equipment:

- 1 - Digital Probe Kit (You should check out)
- 1 - Breadboard (You should check out)
- 1 - DC Power Supply

Components:

- 1 - 74HC08 (AND)
- 1 - 74HC32 (OR)
- 1 - 74HC86 (XOR)
- 2 - 240Ω Resistors
- 2 - LED
- 3 - 1kΩ Resistors
- 1 - DIP Switch

Background:

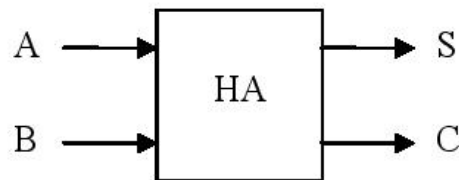
The adder is a major component of an Arithmetic Logic Unit (ALU) of a CPU. A half adder adds two bits and produces a sum bit and a carry bit. A full adder is constructed using two half adders, and it adds three input bits to produce a sum bit and a carry bit. An N-bit binary adder can be created by cascading full adders. Full adders are cascaded by connecting the carry output of one adder to the carry input of the next. A brief description of a half adder and a full adder is given below.

A *half adder* is a logical circuit that performs an addition operation on two binary digits. The half adder produces a sum and a carry value which are both binary digits. The Boolean logic for a half adder is as follows.

$$S = A \text{ XOR } B$$

$$C = A \text{ AND } B$$

The block diagram of a half adder is shown below.



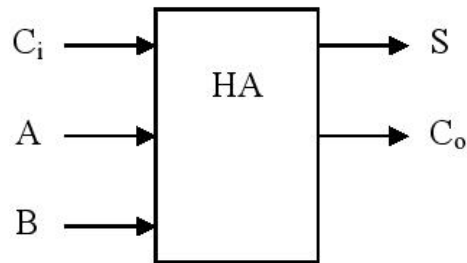
Block Diagram #1 – Half Adder

A *full adder* is a logical circuit that performs an addition operation on three binary digits. The full adder produces a sum and a carry value, which are both binary digits. The Boolean logic for a full adder is as follows.

$$S = (A \text{ xor } B) \text{ xor } C_i$$

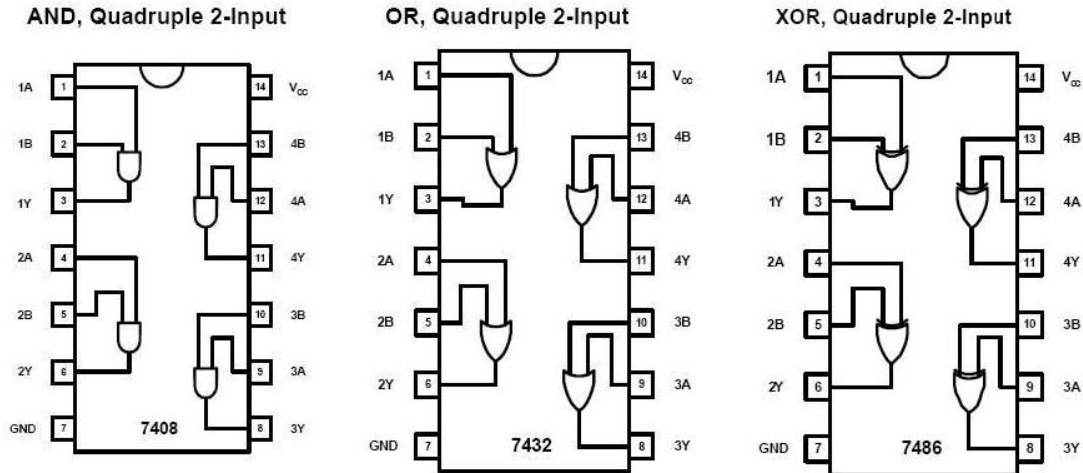
$$C_o = (A \text{ and } B) \text{ or } (C_i \text{ and } (A \text{ xor } B)) = (A \text{ and } B) \text{ or } (B \text{ and } C_i) \text{ or } (C_i \text{ and } A)$$

The block diagram of a full adder is shown below.



Block Diagram #2 - Full Adder

In this experiment, you will construct and verify a Half Adder and a Full Adder circuit. The internal connections for each of the integrated circuits are shown below. The power connections for each of the integrated circuits are also shown below.



Integrated Circuit Connections

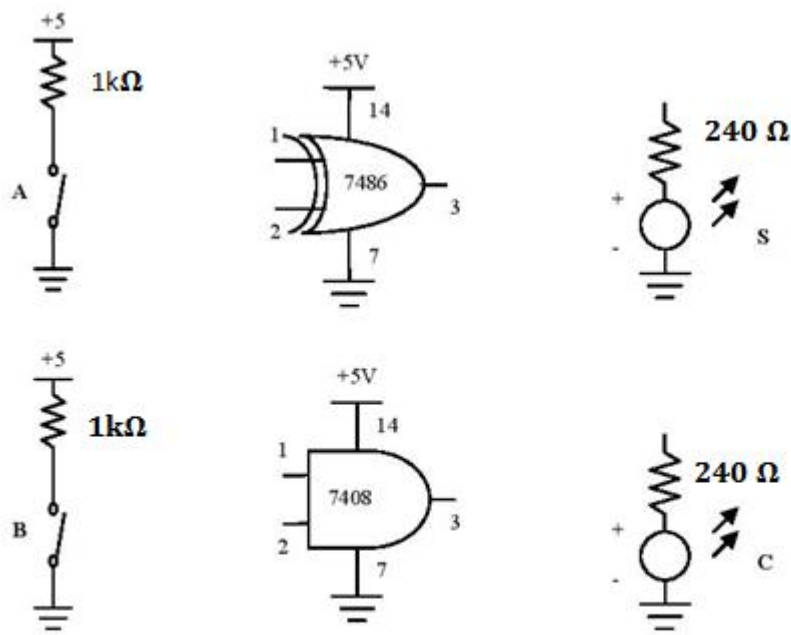
Procedure:

1. Place the integrated circuits with AND, OR, and XOR gates on a breadboard properly. Also place the DIP switch. All of these components should be placed across the gap in the center of the breadboard.

2. Complete the truth table for the half adder.

Half Adder			
A	B	$S = A \text{ XOR } B$	$C = AB$
0	0		
0	1		
1	0		
1	1		

3. Finish designing and sketching the circuit schematic for the half adder. Remember, multiple outputs cannot be connected to the same input, but an output can be connected to multiple inputs.



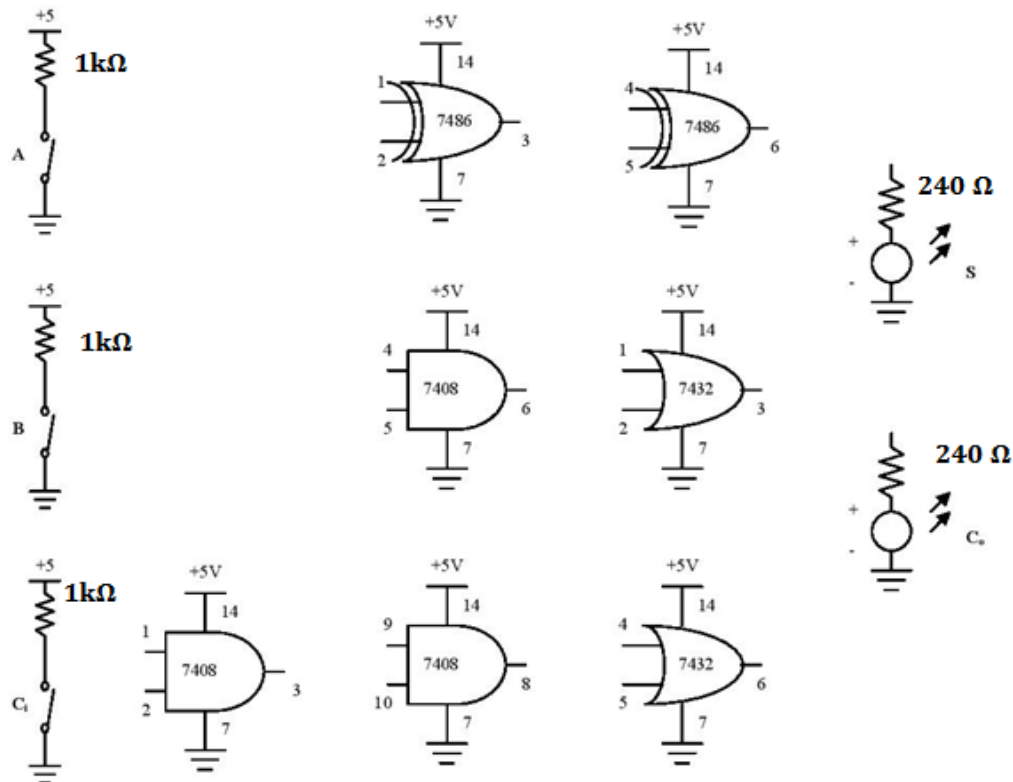
4. Construct the circuit on a breadboard with switches and 2 LEDs. Experimentally verify the truth table. A and B are switches.
The output for each logic gate will be on an LED.
Verify output with the instructor.

Half Adder			
A	B	S	C
0	0		
0	1		
1	0		
1	1		

5. Complete the truth table for the full adder.

Full Adder								
A	B	C_i	$A \text{ XOR } B$	$S = (A \text{ XOR } B) \text{ XOR } C_i$	AB	BC_i	AC_i	$C_o = AB + AC_i + BC_i$
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

6. Finish designing and sketching the circuit schematic for the full adder.
Remember, multiple outputs cannot be connected to the same input, but an output can be connected to multiple inputs.



7. Construct the circuit on a breadboard with switches and 2 LEDs. Experimentally verify the truth table. A and B are switches.
The output for each logic gate will be on an LED.

Verify output with the instructor.

Full Adder				
A	B	C _i	S	C_o
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		