BUBT

Bangladesh University of Business & Technology

Assignment On

MUX and comparator

Course Code: CSE 205

Course Title: Digital Logic Design (DLD)

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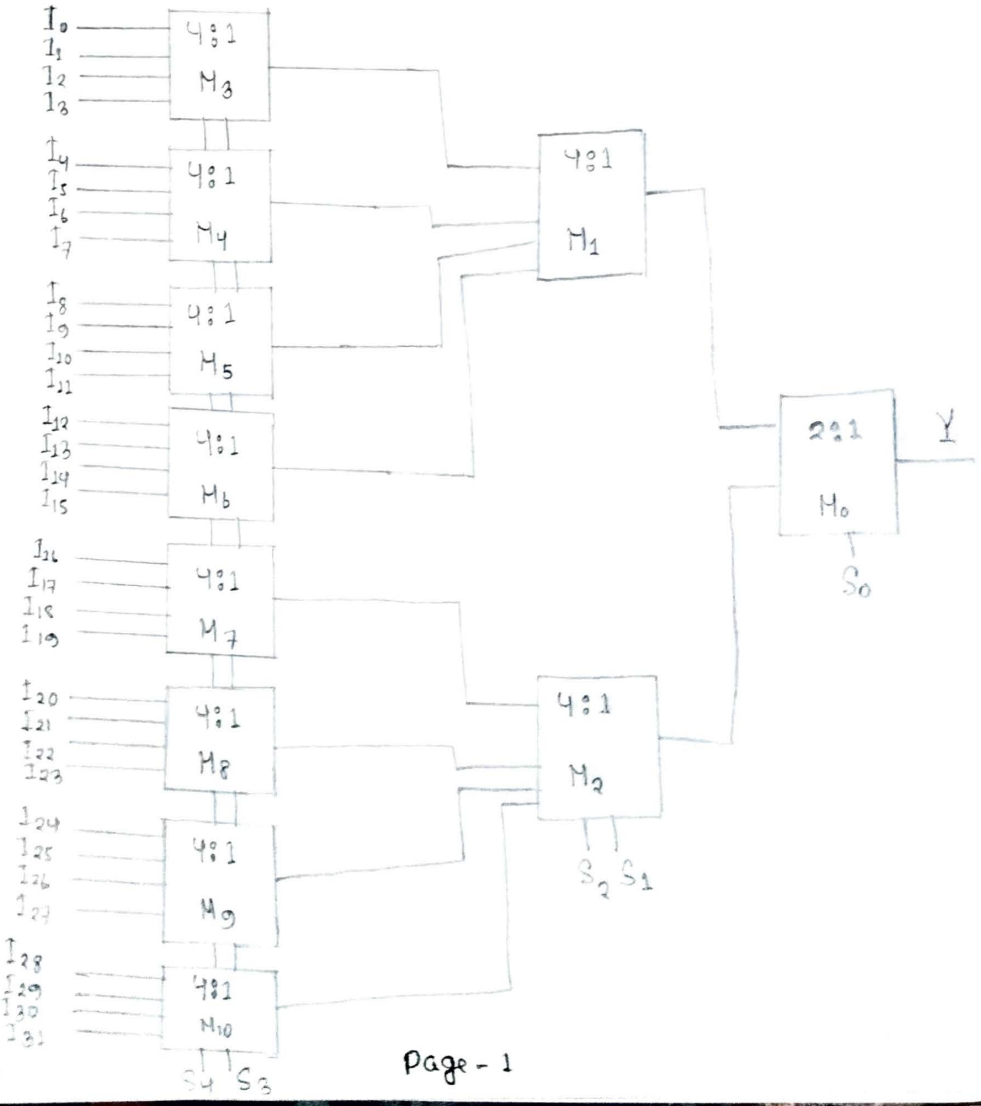
Question 1: Design 32X1 MUX using 4X1 MUX.

Soln: A multiplexer (or MUX), also known as a data selector, is a device that selects between several analog or digital input signals and forwards it to a single output line. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth.

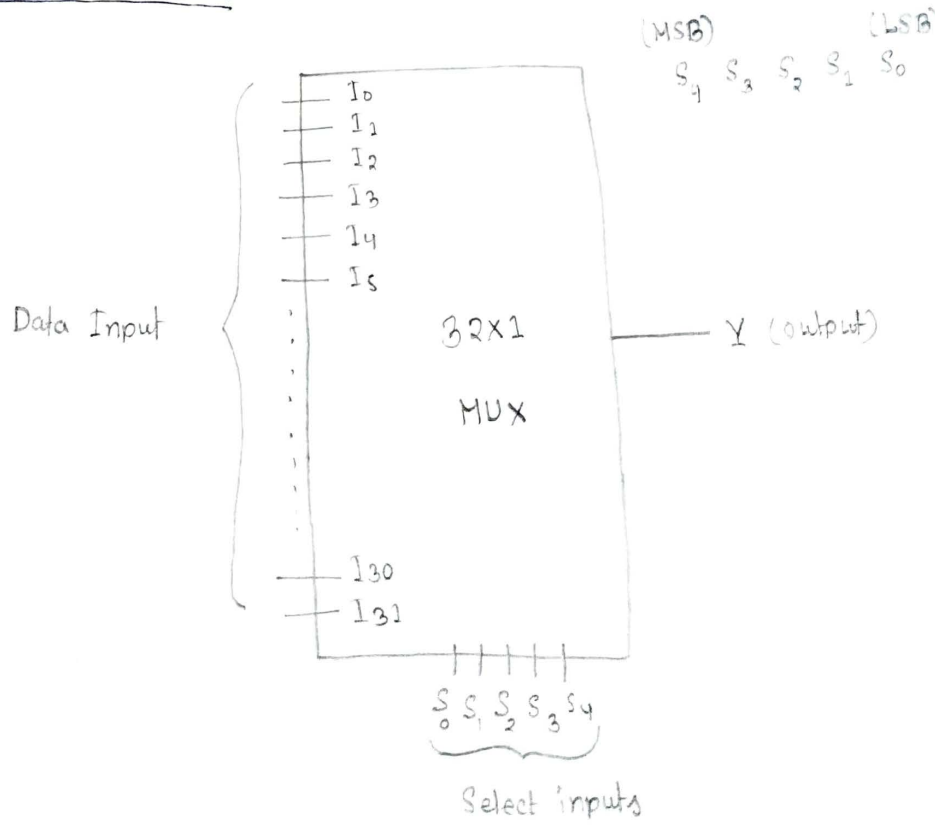
Now, designing 32X1 MUX using 4X1 MUX:



Truth table:

S_4	S_3	S_2	S_1	S_0	Inputs (Y)	MUX
0	0	0	X	X	$I_0 - I_3$	M_3
0	0	1	X	X	$I_4 - I_7$	⋮
0	1	0	X	X	⋮	⋮
0	1	1	⋮	⋮	⋮	⋮
1	0	0	⋮	⋮	⋮	⋮
⋮			⋮	⋮	⋮	⋮
1	1	1	X	X	$I_{28} - I_{31}$	M_{10}

Block Diagnam :



Question: 02 Design 4-bit comparator.

Soln: A comparator is a combinational circuit that compare two numbers, A and B, and determine their relative magnitudes. The outcome of the comparison is specified by three binary variables that indicate whether $A > B$, $A = B$, or $A < B$.

Now, Designing 4-bit comparator (magnitude):

Input:
$A = A_3A_2A_1A_0$
$B = B_3B_2B_1B_0$

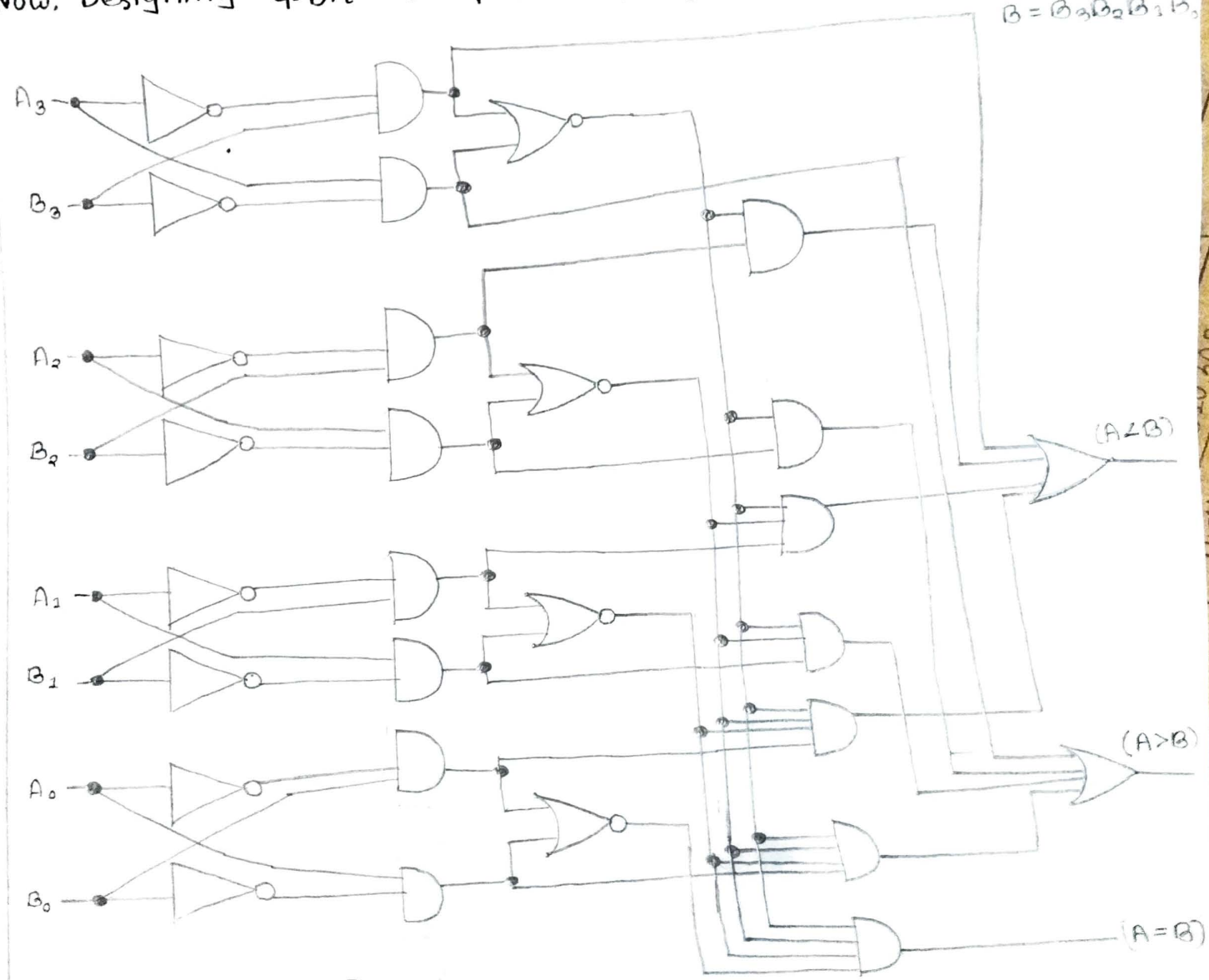


Figure: 4-bit magnitude comparator design

(1) $A=B : A_3=B_3,\ A_2=B_2,\ A_1=B_1,\ A_0=B_0$

$x_i = A_iB_i + A_i'B_i'$

X-OR Invert $= (A_iB_i' + A_i'B_i)'$

$= (A_i' + B_i)(A_i + B_i')$

$= A_i'A_i + A_iB_i' + A_iB_i + B_iB_i'$

$= A_iB_i + A_i'B_i'$

Output: $X_3 \cdot X_2 \cdot X_1 \cdot X_0$

(2) $(A>B)$

Output: $A_3B_3' + X_3A_2B_2' + X_3X_2A_1B_1' + X_3X_2X_1A_0B_0'$

(3) $(A<B)$

Output: $A_3'B_3 + X_3A_2'B_2 + X_3X_2A_1'B_1 + X_3X_2X_1A_0'B_0$

Truth table:

COMPARING INPUTS				OUTPUT		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$A>B$	$A<B$	$A=B$
$A_3>B_3$	X	X	X	H	L	L
$A_3<B_3$	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H

H = High Voltage, L = Low Voltage, Level, X = Don't care