

“DIRECT MEMORY ACCESS (DMA) IS A FEATURE OF COMPUTERIZED SYSTEMS THAT ALLOWS CERTAIN HARDWARE SUBSYSTEMS TO ACCESS MAIN SYSTEM MEMORY INDEPENDENTLY OF THE CENTRAL PROCESSING UNIT (CPU).”

– WIKIPEDIA

“Direct memory access (DMA) is a means of having a peripheral device control a processor's memory bus directly.”

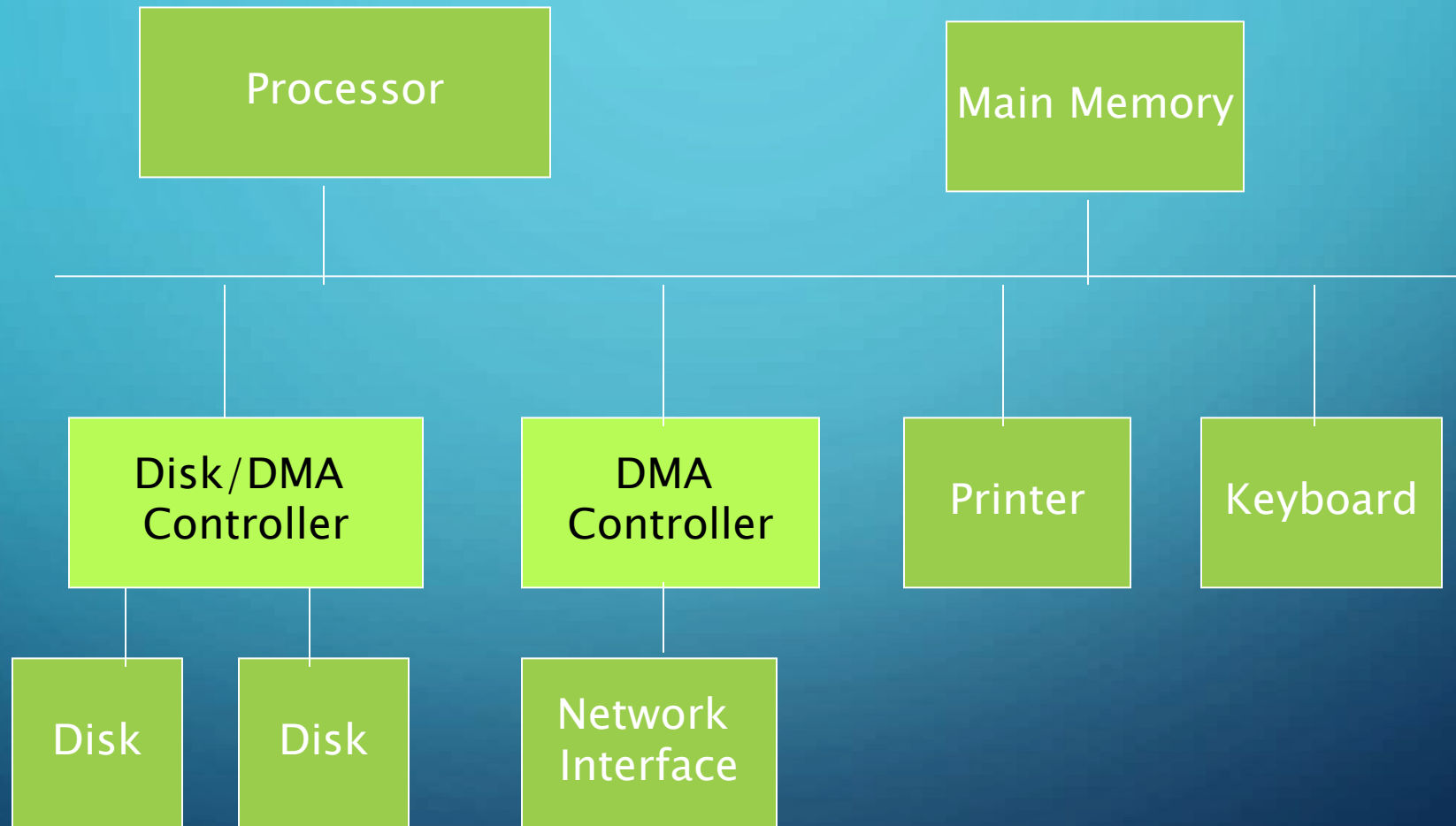
What is DMA?

- The direct memory access (DMA) I/O technique provides direct access to the memory while the microprocessor is temporarily disabled.
- I/O devices are connected to system bus via a special interference circuit known as “DMA Controller”.
- In DMA, both CPU and DMA controller have access to main memory via a shared system bus having data, address and control lines.
- It is sometimes referred to as a channel. In an alternate configuration, the DMA controller may be incorporated directly into the I/O device.

What is DMA?

- A DMA controller temporarily borrows the address bus, data bus, and control bus from the microprocessor and transfers the data bytes directly between an I/O port and a series of memory locations.
- The DMA transfer is also used to do high-speed memory-to-memory transfers.
- DMA transfer can be done in tow ways. A) DMA Transfer Blocks. B) Cycle Stealing

USE OF DMA CONTROLLERS IN A COMPUTER SYSTEM



Why DMA?

- An important aspect of governing the Computer System performance is the transfer of data between memory and I/O devices.
- The operation involves loading programs or data files from disk into memory, saving file on disk, and accessing virtual memory pages on any secondary storage medium.
- The process would be much quicker if we could bypass the CPU & transfer data directly from the I/O device to memory. Direct Memory Access does exactly that.
- During DMA transfer, the CPU is idle and no control of the memory buses.

DMA VS. NO DMA

| Without DMA | With DMA |
|--|--|
| When the CPU is using programmed input/output, it is typically fully occupied for the entire duration of the read or write operation, and is thus unavailable to perform other work. | The CPU initiates the transfer, does other operations while the transfer is in progress, and receives an interrupt from the DMA controller when the operation is done. |

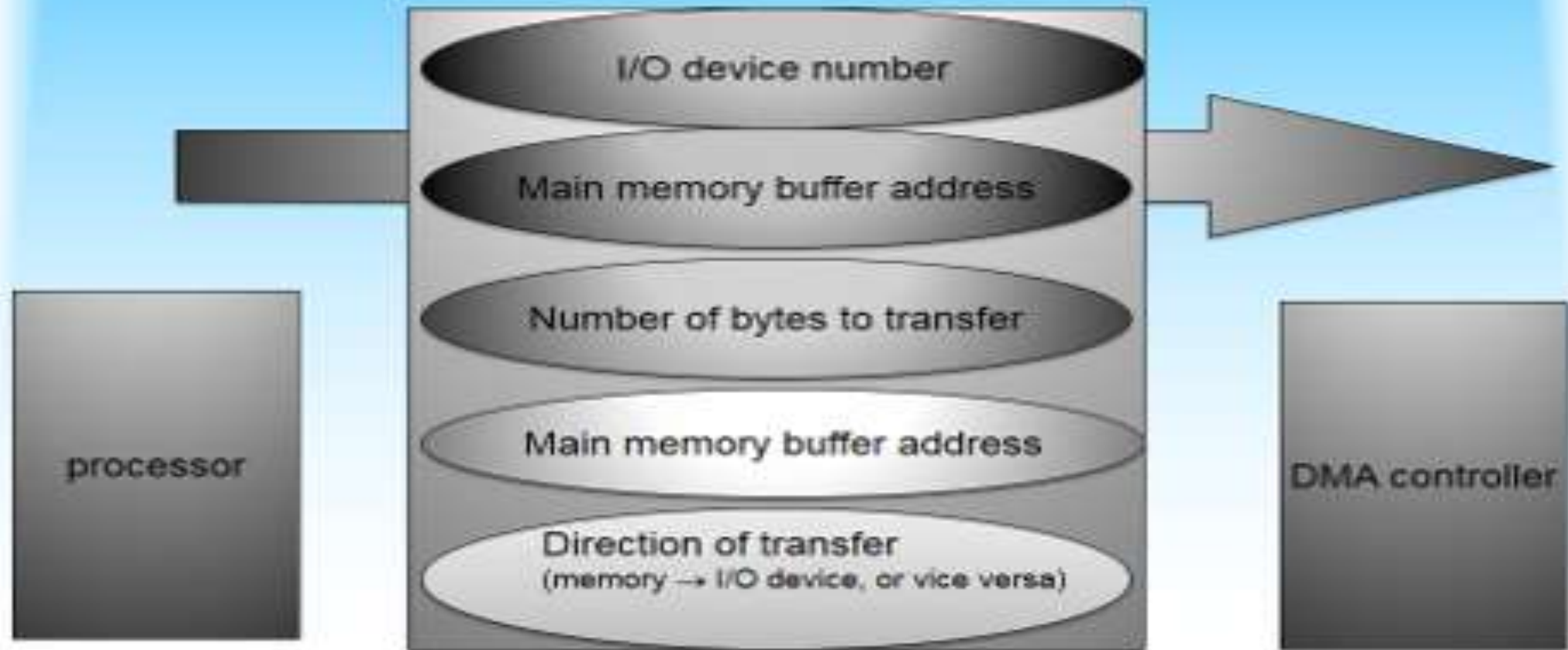
This feature is useful any time the CPU cannot keep up with the rate of data transfer, or where the CPU needs to perform useful work while waiting for a relatively slow I/O data transfer.

DMA INITIALIZATION

DMA controllers require initialization by software. Typical setup parameters include the base address of the source area, the base address of the destination area, the length of the block, and whether the DMA controller should generate a processor interrupt once the block transfer is complete.

Example: Reading from an I/O device

Processor gives details to the DMA controller



TYPES OF DMA TRANSFER:

1. DMA TRANSFER BLOCK

- In this DMA mode , DMA controller is master of memory bus.
- This mode is needed by the secondary memory like disk drives, that have data transmission and are not to be stopped or slowed without any loss of data transfer of blocks.
- Block DMA transfer supports faster I/O data transfer rates but the CPU remains inactive for relatively long period by tying up the system bus.

2.CYCLE STEALING

- In this method, system allows DMA controller to use system bus to transfer one word, after which it should return back control of bus to CPU.
- This method reduces maximum I/O transfer rates
- It also reduces interference of DMA controller in CPU memory access
- It is completely eliminated by designing DMA interface so that system bus cycles are stolen only when CPU is not actually using system bus.
- This is also called as Transparent DMA

DMA DATA TRANSFER: BLOCK DIAGRAM

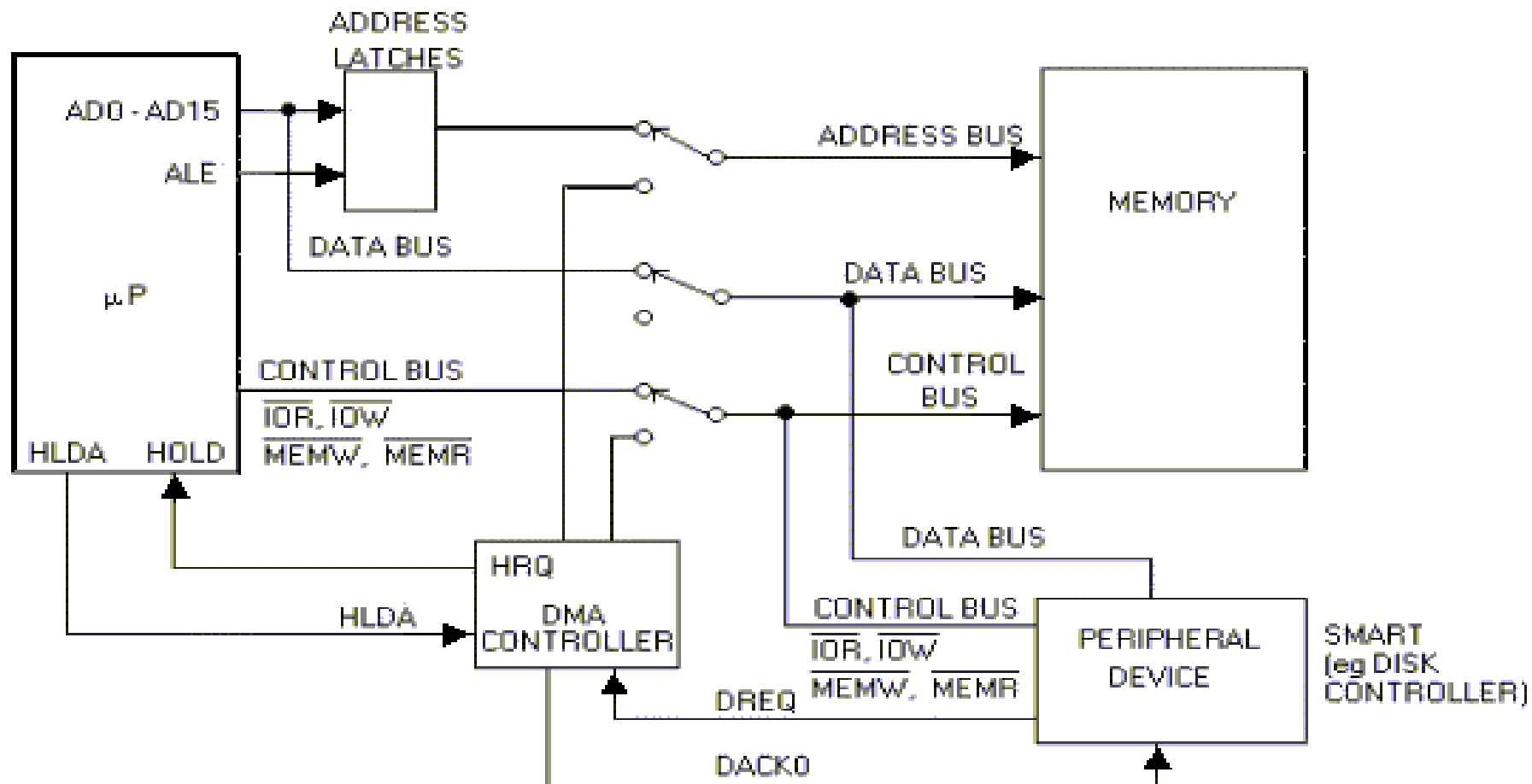


Figure 2: Block diagram showing how a DMA controller operates in a microcomputer system

DATA TRANSFER: BLOCK COMPONENTS

- Two control signals are used to request and acknowledge a DMA transfer .
- The HOLD signal is a bus request (BR) signal which asks the microprocessor to release control of the buses after the current bus cycle.
- The HLDA signal is a bus grant (BG) signal which indicates that the microprocessor has indeed released control of its buses by placing the buses at their high-impedance states.
- DREQi (DMA request): Used to request a DMA transfer for a particular DMA channel.
- DACKi (DMA channel acknowledge): Acknowledges a channel DMA

INTERNAL CONFIGURATION OF DMA CONTROLLER

The DMA controller includes several internal registers :-

- The DMA Address Register contains the memory address to be used in the data transfer. The CPU treats this signal as one or more output ports.
- The DMA Count Register, also called Word Count Register, contains the number of bytes of data to be transferred. Like the DMA address register, it too is treated as an O/P port (with a different address) by the CPU.
- The DMA Control Register accepts commands from the CPU. It is also treated as an O/P port by the CPU.
- The DMA Data Register are used to store intermediate data values

DMA DATA TRANSFER

Data transfer technique directly between memory and I/O device

Steps:

1. I/O device asserts DREQ signal.
2. DMA controller sends HOLD signal to CPU
3. CPU sends HLDA back to DMA controller
4. DMA controller give DMA acknowledgment back to I/O.

DMA DATA TRANSFER

5. DMA controller places memory address on address bus
6. DMA controller updates memory address register and word counter register
7. When DC register becomes zero ,DMA controller sets HOLD=0
8. Data transfer process terminates and processor regain control of system bus.

OS INVOLVED

- I/O operations are always performed by the OS in response to a request from an application program.
- OS is also responsible for suspending the execution of one program and starting another.
 - ❖ OS puts the program that requested the transfer in the Blocked state, initiates the DMA operation,
 - ❖ starts execution of another program.
- When the transfer is complete, the DMA controller informs the processor by sending an interrupt request.
 - ❖ OS puts suspended program in the Runnable state so that it can be selected by the scheduler to continue execution.

ADVANTAGES OF DMA

- DMA allows a peripheral device to read from/write to memory without going through the CPU
- DMA allows for faster processing since the processor can be working on something else while the peripheral can be populating memory.

DISADVANTAGES OF DMA

- DMA transfer requires a DMA controller to carry out the operation, hence cost of the system increases.
- Cache Coherence problems.

CACHE COHERENCE PROBLEM



Cache coherency refers to the inconsistency of data stored in local caches of a shared resource and data stored in memory.