

Q: Are all of these enough to get full marks in the exam?

A: NO. This is a practice sheet. Meaning, you can practice all you want using the questions from this sheet. However, doing well in exams depends upon your ability to understand a question, formulate an answer, and express it correctly. You see, these are humane skills which cannot be guaranteed by completing a practice sheet only. But yeah, Best of luck anyway.

Chapter 4 (The Processor)

Question - 1:

PC = 0x0040ABCD123045B1

Instruction Memory:

Address	Content
0x0040ABCD123045B1	0000 0001
0x0040ABCD123045B2	1001 0101
0x0040ABCD123045B3	0000 0101
0x0040ABCD123045B4	0011 0011

Data Memory:

Address	Content
0x0040ABCD123045B1	1111 1111
0x0040ABCD123045B2	1001 0101
0x0040ABCD123045B3	0000 0101
0x0040ABCD123045B4	1101 1010

Fetch the instruction from memory then **decode** and find the risc-v assembly code.

Question - 2:

Draw the Block diagram of the **register file**. Describe how it performs the read and write operation.

Mention all the input and output pins.

Question - 3:

Draw the Block diagram of the **ALU**. Describe how it performs different operations. What is the significance of the Zero pin?

Mention all the input and output pins.

Question - 4:

Draw the Block diagram of the **Data Memory**. Describe how it performs the read and write operation.

Mention all the input and output pins.

Question - 5:

Draw the Block diagram of the **Immediate generation Unit**. Briefly explain what it does?

Question - 6:

Draw the Block diagram of the **Instruction Memory**. Briefly explain what it does?

Question - 7:

Which resources or blocks or components are required to build the datapath of the following instructions:

i.	ADD X_{21}, X_{22}, X_{23}
ii.	AND X_{21}, X_{22}, X_{23}
iii.	OR X_{21}, X_{22}, X_{23}
iv.	ADDi X_{21}, X_{22}, X_{23}
v.	LD $X_{21}, 22(X_{21})$
vi.	SD $X_{21}, 22(X_{21})$
vii.	BEQ $X_{21}, X_{22}, \text{End}$

Question - 8:

Draw a simplified datapath with control unit that can process ADD X_{21}, X_{22}, X_{23}

Question - 9:

Draw a simplified datapath with control unit that can process ADDI $X_{21}, X_{22}, 5$

Question - 10:

Draw a simplified datapath with control unit that can process LD X21, 14(X22)

Question - 11:

Draw a simplified datapath with control unit that can process the following codes:

ADD X21, X22, X23

LD X21, 14(X22)

SD X22, 16(X21)

Question - 11:

Draw a simplified datapath with control unit that can process the following codes:

ADDI X21, X22, 5

LD X21, 14(X22)

Question - 12:

Draw a simplified datapath with control unit that can process the following codes:

ADDI X21, X22, 5

LD X21, 14(X22)

Question - 13:

Instruction	Time (PS)
Add X21, X22, X23	10
Sub X21, X23, X24	20
Mul X22, X23, X26	15
LD X22, 0(X21)	25

The above instructions are being run in a single cycle datapath. Now determine what is the clock period of this system?

Question - 13:

Stage	Time (PS)
IF	10
ID	20
EX	20
MEM	20
WB	10

The below instructions are being run in a pipelined datapath. Calculate the time required to execute each instruction.

Instruction	Time (PS)
Add X21, X22, X23	
Sub X21, X23, X24	
Mul X22, X23, X26	
LD X22, 0(X21)	

Determine what is the clock period of this system?

Question - 14:

The below instructions are being run in a pipelined datapath. How many clock cycles are required for the above code sequence in case of an ideal pipeline? (no hazard)

Add X21, X22, X23

Sub X21, X23, X24

Mul X22, X23, X26

LD X22, 0(X21)

Question - 14:

Add X21, X22, X23

Sub X23, X22, X24

Mul X22, X22, X26

LD X22, 0(X21)

- a. The below instructions are being run in a pipelined datapath. How many clock cycles are required for the above code sequence in case of an ideal pipeline? (no hazard)
- b. How many data hazards are there in the given code sequence?
- c. Apply only stall + forwarding to overcome the data hazards.

Question - 15:

sd x29, 12(x16)

ld x29, 8(x16)

sub x17, x15, x14

beq x17, x18, label

add x15, x11, x14

sub x15, x30, x14

Suppose we modify the pipeline so that it has only one memory (that handles both instructions and data). In this case, there will be a structural hazard every time a program needs to fetch an instruction during the same cycle in which another instruction accesses data.

- a. How many structural hazards are there in the given code sequence?

Question - 16:

Modify the BEQ datapath so that it works for BNE.