

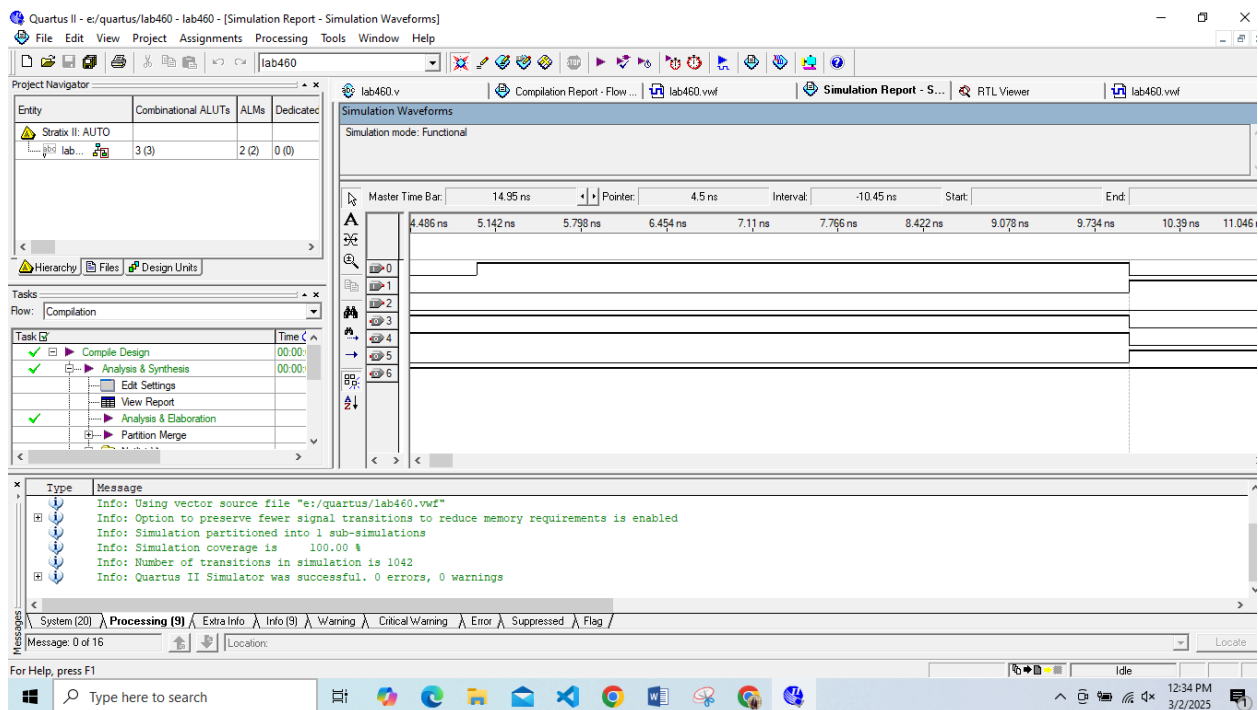
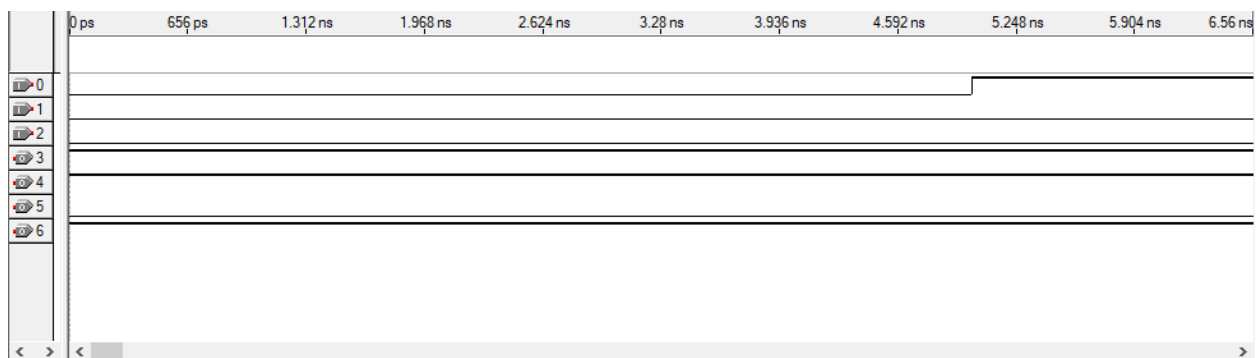
```

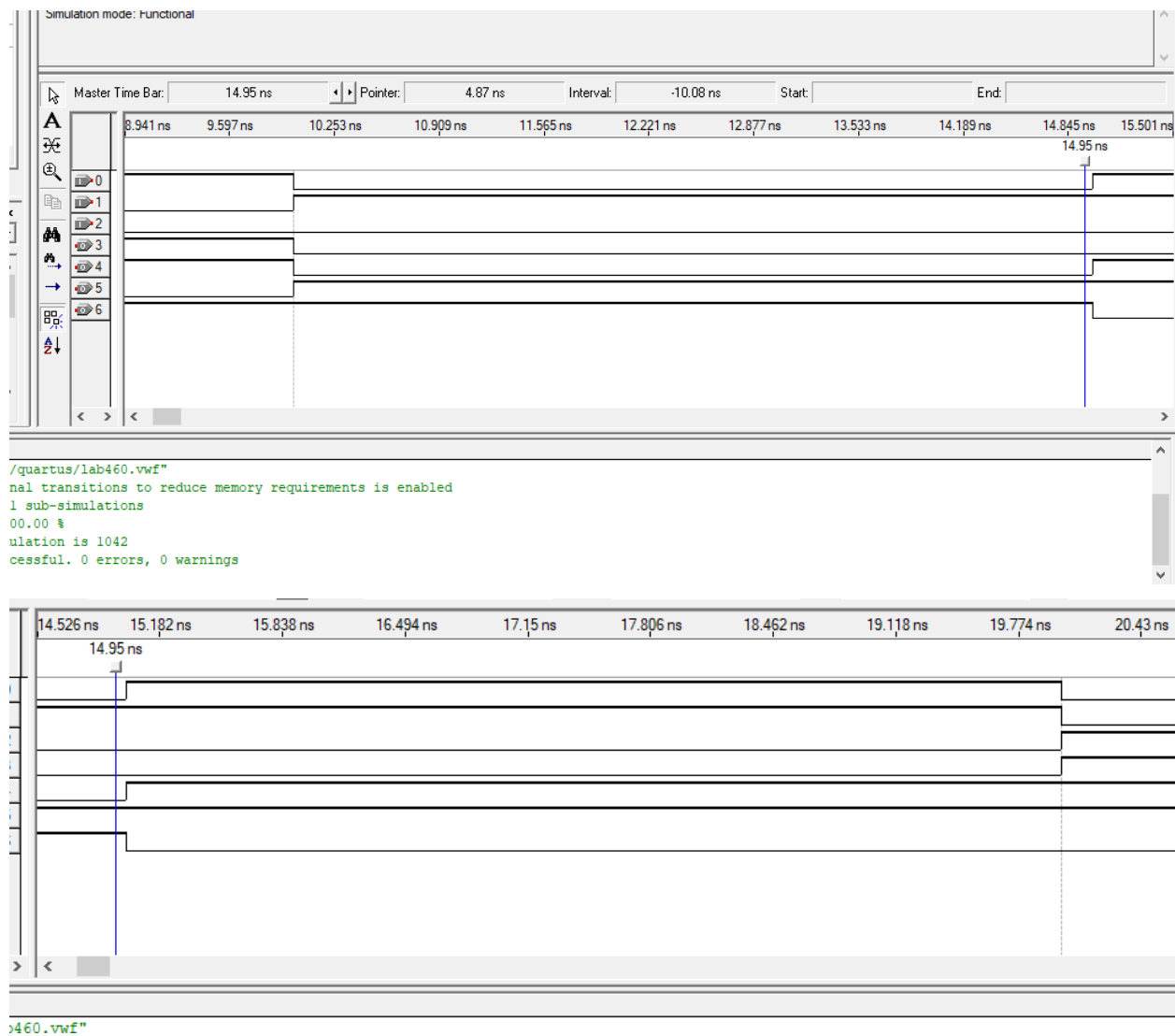
module lab460(a,b,c,f1,f2,f3,f4);
  input a,b,c;
  output f1,f2,f3,f4;
  assign f1=~(b);
  assign f2= (a|f1);
  assign f3= (b^c);
  assign f4=~(f2&f3);

endmodule

```

Input 10,20,40





Input 5,10,15

