```
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Sec:06
CSE460
Lab:03
5>2>0>1>4>3
module exam( w,y);
 input[5:0]w;
output reg [2:0]y;
 always @(w)
 casex (w)
  6'b1xxxxx: y=5;
  6'b0xx1xx: y=2;
  6'b0xx0x1: y=0;
  6'b0xx010: y=1;
  6'b01x000: y=4;
  6'b001000: y=3;
  default : y=3'b000;
 endcase
endmodule
```

