Laboratory Exercise #6.2

Behavioral Modeling of Sequential Circuits

Name: _____ **Group:** _____

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Intended Learning Outcomes:

- Create design entry of a sequential circuit using behavioral modeling in Verilog HDL code
- Synthesize the Verilog HDL design entry
- Simulate the designed circuit using a testbench file
- Fit a synthesized circuit into an Intel FPGA
- Programming and configuring the FPGA chip on Intel DE-series board (DE10-Lite)

Supplement:

This exercise requires a basic understanding of the Intel Quartus Prime design flow with ModelSim functional verification, as detailed in Units 1-2 and Laboratory Exercises #1-2. It is also expected that Laboratory Exercise #6 has already been completed before performing this exercise.

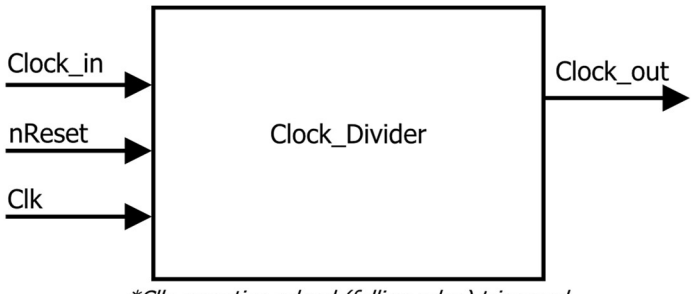
Instructions:

Perform this hands-on laboratory exercise after attending/watching the onsite/online lecture for Unit 6. This activity is intended to be done individually.

[ADDENDUM]: The section hereafter is a continuation of Laboratory Exercise #6.

Exercise 6C: Clock Divider

Create a **Verilog description** of a ***Clock Divider***, as required by Laboratory Exercise #6 (A and B) for FPGA implementation. The description may be **behavioral** and/or **behavioral with dataflow modeling**. Refer to the entity diagram below for reference.



**Clk: negative-edged (falling-edge) triggered*
nReset: asynchronous reset (active low)

Figure 1. Entity Diagram of Clock Divider

For FPGA Implementation:

The reference input clock from the FPGA board (Terasic DE-10 Lite) is 50 MHz. Use internal counter/s to generate a 2 Hz clock with 50% duty cycle. The reset input will reset the internal counter/s and the output signal. Connect one LED from FPGA board to the clock output pin to showcase blinking in response to 2 Hz frequency. Synthesize the design.

Make sure to include your solutions in the laboratory report. Place comments in your design entry to explain lines/block of lines with respect to your solutions.

This design shall be used in the FPGA implementations of the other design entries in Laboratory Exercise #6.

For Simulation:

Make changes in your design entry to scale down the input clock for simulation purposes. You may keep the same output frequency (2 Hz). Simulate and show the simulation waveform (timing diagram) in the laboratory report.

Test Cases:

Assert reset (**nReset**) at the start of the simulation for a couple of **Clk** edges, and keep the clock generator in the test bench produce a longer train of clock pulses (i.e., let it toggle for a while) to demonstrate the clock divider functionality.

Evaluation:

Level / Criteria	1.0 Outstanding	2.0 Competent	3.0 Marginal	5.0 Not Acceptable	Rating
CO1: Verilog Design Entry	Verilog HDL description is correct and follows specified instructions.	--	Verilog HDL description is correct but DID NOT follow the specified instructions.	NO Verilog HDL description is presented or the design entry is INCORRECT.	
CO1: Design Synthesis	Verilog HDL description is synthesized and compiled with NO issues (with 0-1 warning). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MINOR issues on constructs (with 2-3 warnings). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MAJOR issues on constructs (with 4 or more warnings). There is evidence in the lab report that supports this result.	Simulation has FAILED or there is NO evidence showing a successful simulation.	
CO2: Verilog Testbench Entry	Verilog HDL testbench is correct and follows specified instructions. ALL possible input combinations or AMPLE test stimuli are included to generate sufficient and verifiable output results.	--	Verilog HDL testbench is correct but DID NOT follow specified instructions. Possible input combinations may be INCOMPLETE or test stimuli are NOT SUFFICIENT included to generate verifiable output results.	NO Verilog testbench is presented or INCOMPLETE.	
CO2: Functional Verification	Simulation of the synthesized design is functional with NO issues and shows ALL correct and expected results. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE but are ALL correct. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE or there may be INCORRECT results. NO analysis is made with NO image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation has FAILED or there is NO evidence showing a successful simulation.	

CO3: Design Flow	Synthesized HDL-based design file was properly loaded into the FPGA with NO problems.	--	Synthesized HDL-based design file was loaded into the FPGA with A FEW technical issues.	Synthesized HDL-based design file WAS NOT PROPERLY loaded into the FPGA.	
CO3: Accuracy of Results on FPGA	Results are ALL ACCURATE as expected and recorded data is validated upon checking.	--	Results are MOSTLY ACCURATE and recorded data is validated upon checking.	Results are ERRONEOUS or recorded data CANNOT be validated upon checking.	

Exercise 6D: Hexadecimal Digit Counter

Create a hexadecimal digit counter using the 4-bit up/down counter from Exercise #6B and connect its output to a single 7-segment through the hex decoder from Exercise #5A. Use structural modeling in this design entry. Connect one 7-Segment Display from FPGA board to the output of hex decoder. Synthesize and simulate the design.

In the lab report, include a detailed block diagram to show both modules' interconnections and label them appropriately.

Test Cases:

Assert reset (**Reset**) at the start of the simulation for a couple of **Clk** edges. Design the testbench to show ALL counter operations. Prioritize the simulation waveforms (timing diagram) in the laboratory report.

FPGA Implementation:

After simulation, load the appropriate design file into the FPGA to test the functionality of the design. Refer to the onsite orientation and other attachments for this section. **Additional module needed: Clock divider (6C)**

Evaluation:

Level / Criteria	1.0 Outstanding	2.0 Competent	3.0 Marginal	5.0 Not Acceptable	Rating
CO1: Verilog Design Entry	Verilog HDL description is correct and follows specified instructions.	--	Verilog HDL description is correct but DID NOT follow the specified instructions.	NO Verilog HDL description is presented or the design entry is INCORRECT.	
CO1: Design Synthesis	Verilog HDL description is synthesized and compiled with NO issues (with 0-1 warning). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MINOR issues on constructs (with 2-3 warnings). There is clear evidence in the lab report that supports this result.	Verilog HDL description is synthesized and compiled with MAJOR issues on constructs (with 4 or more warnings). There is evidence in the lab report that supports this result.	Simulation has FAILED or there is NO evidence showing a successful simulation.	
CO2: Verilog Testbench Entry	Verilog HDL testbench is correct and follows specified instructions. ALL possible input combinations or AMPLE test stimuli are included to	--	Verilog HDL testbench is correct but DID NOT follow specified instructions. Possible input combinations may be INCOMPLETE or test stimuli are NOT SUFFICIENT included	NO Verilog testbench is presented or INCOMPLETE.	

	generate sufficient and verifiable output results.		to generate verifiable output results.		
CO2: Functional Verification	Simulation of the synthesized design is functional with NO issues and shows ALL correct and expected results. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE but are ALL correct. An analysis is made by providing image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation of the synthesized design is functional. Expected results may be INCOMPLETE or there may be INCORRECT results. NO analysis is made with NO image annotations and/or discussions of the results. There is clear evidence in the lab report that supports this.	Simulation has FAILED or there is NO evidence showing a successful simulation.	
CO3: Design Flow	Synthesized HDL-based design file was properly loaded into the FPGA with NO problems.	--	Synthesized HDL-based design file was loaded into the FPGA with A FEW technical issues.	Synthesized HDL-based design file WAS NOT PROPERLY loaded into the FPGA.	
CO3: Accuracy of Results on FPGA	Results are ALL ACCURATE as expected and recorded data is validated upon checking.	--	Results are MOSTLY ACCURATE and recorded data is validated upon checking.	Results are ERRONEOUS or recorded data CANNOT be validated upon checking.	

For the laboratory report (LR #6.2), include the following items:

- **For both Exercises 6C and 6D:**
  - Proof of successful design synthesis *(screenshot showing 0 errors)*
  - *Screenshot showing all pin assignments.*
  - Proof of successful simulation results with required number of test cases *(screenshots of simulation results with annotations or discussion of results)*
  - Proof of successful FPGA implementation *(1 sample photo of the board with sample result)*
- **For Exercises 6D block diagrams:**
  - Simulation: Detailed top module block diagram to show both modules' interconnections (4-bit up/down counter from Exercise #6B and connect its output to a single 7-segment through the hex decoder from Exercise #5A) and label them appropriately.
  - FPGA: Detailed top module block diagram to show both modules' interconnections (4-bit up/down counter from Exercise #6B and connect its output to a single 7-segment through the hex decoder from Exercise #5A) including the Clock Divider (from Exercise #6C) and label them appropriately. Include also the I/O used such as switches for parallel load, LED/s, 7-Segment Display, etc…
- All Verilog files (.v) must be submitted along with LR #6.2