Department of Computer Engineering
Digital Hardware Systems
CpE 2303L – Computer Engineering Drafting and Design

Practical Activity #4
Mechanical Design Features

Objectives:
1. Implement the electrical design considerations into the PCB Layout.
2. Use KiCAD's PCB Editor tools to implement the constraints.
3. Create a PCB layout with the electrical considerations.

Tools Required:
The following will be provided for the students:
1. Computer with KiCAD 8 installed.

Delivery Process:
The instructor will conduct a short briefing about the exercise. Knowledge from Unit V Electrical Design Considerations will be applied in this exercise, a short review of the recent chapter will be done.

Note:
Some of the contents in this manual are derived with permission from other sources. This document is a guide only. Your answers are to submitted in a separate document (lab exercise report).

Part I. Theory

Resistance

The copper printed tracks\traces on a PCB have finite resistance which introduces a voltage drop proportional to the current flowing in that particular conductor. The resistance of a conductor is considered as a metal section having a rectangular cross-section depends upon the specific resistivity of copper, which is 1.724×10^{-6} at $20℃$. A standard copper foil of $35\ \mu m$ thickness (without any plating) may be assumed. To calculate the resistance, the specific resistivity of copper is divided by cross-section of the conductor.

$$R = \frac{\rho L}{A}\Omega$$

$R = resistivity\ (\Omega - cm \times 10^{-6})$
$L = conductor\ length\ (cm)$
$A = area\ of\ cross - section\ of\ the\ conductor\ (cm^2)$

It is known that when current flows through a conductor, its temperature rises due to the joule effect (copper resistance increases with temperature). The equation to calculate the resistance at a certain temperature is shown below:

$$R_t = R_0[1 + \alpha(T_1 - T_0)]$$

$R_t = resistance\ at\ temperature\ T_1$
$R_0 = resistance\ at\ temperature\ T_0$
$\alpha = temperature\ coefficient\ of\ conductivity$

The current carrying capacity of a copper conductor depends on the thickness and width of the conductor. Table 1 shows the current carrying capacity based on conductor width and thickness in ounce per square foot.

Table 1 Current Carrying Capacity of a Conductor

Conductor Width (in)	½ oz	1 oz	2 oz	3 oz
0.005	0.13	0.50	0.70	1.00
0.01	0.50	0.80	1.40	1.90
0.02	0.70	1.40	2.20	3.00
0.03	1.00	1.90	3.00	4.00
0.05	1.50	2.50	4.00	5.50
0.07	2.00	3.50	5.00	7.00
0.10	2.50	4.00	7.00	9.00
0.15	3.50	5.50	9.00	13.00
0.20	4.00	6.00	11.00	14.00

Usually, the copper thickness is fixed therefore the PCB designer can either adjust the conductor or length to accommodate the current flowing through it.

Capacitance Between Opposite Conductors

Capacitance is parameter of considerable importance, particularly in the design of PCBs at high frequency. The capacitance comes into play in the following two situations:

- Capacitance between conductors on opposite sides.
- Capacitance between adjacent conductors.

Two PCB conductors lying one above another and separated by a dielectric (laminate) form a capacitor whose approximate capacitance can be calculated from the basic capacitor formula:

$$C = 0.886 \times \epsilon \times \frac{A}{b}\,(pF)$$

$A = total\ overlapping\ area\ (cm^2)$
$b = thickness\ of\ dielectric$
$\epsilon = relative\ dielectric\ constant, taken\ from\ manufacturer$

Capacitance Between Opposite Conductors

It is a function width, thickness and spacing as well as the dielectric constant of the board material. For all practical purposes, the value of coupling capacitance, (pF/cm) for a G-10 laminate with dielectric constant of 5.4 and conductor thickness of $35\ \mu m$ is given on the figure below.

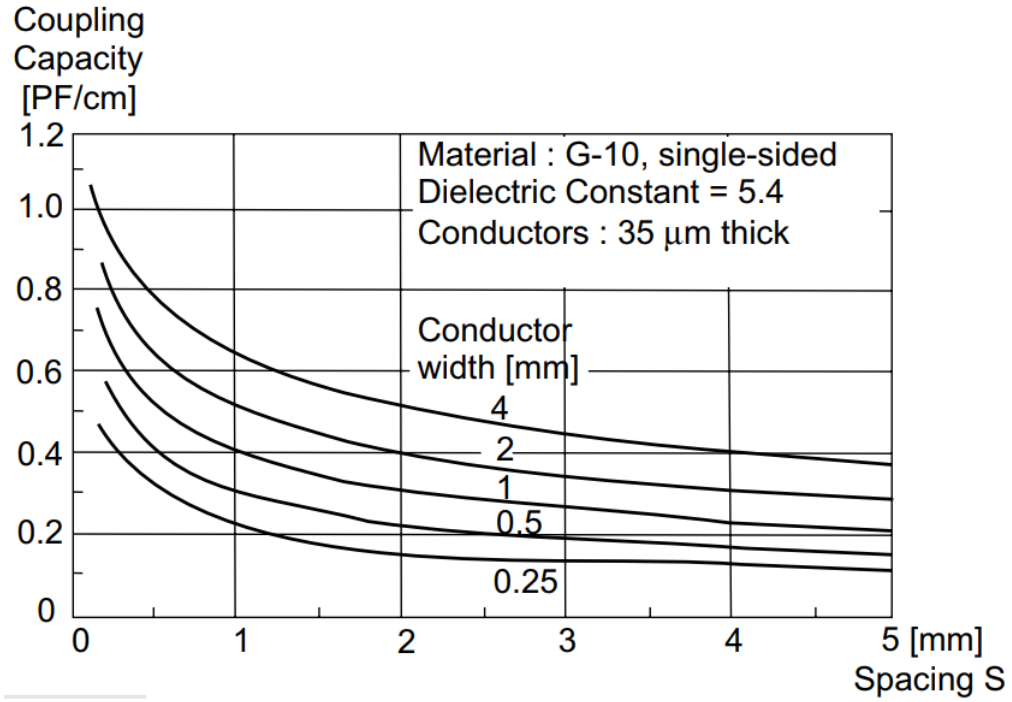

Figure 1 Capacitive Coupling between adjacent conductors as a function of spacing.

Inductance

Logic circuits with a clock rate of only 10 kHz, high frequency components of the rectangular shaped signals can often cause problems. In such situations, it is important to know the inductance of the conductor arrangement. For a given type of copper clad board having 35 um copper conductor thickness, the inductance of parallel running conductor widths can be calculated using the figure below.

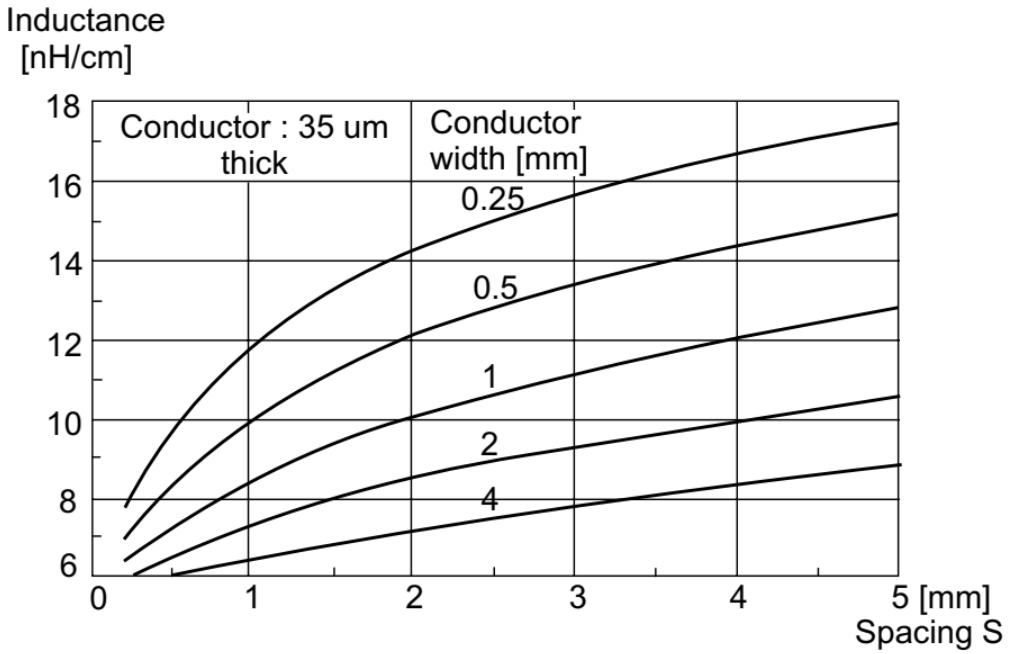

Figure 2 Inductance of Parallel Conductors

Component Placement Rules

In a highly sensitive circuit, the critical components are placed first and in such a manner as to require minimum length for the critical conductors. However, in a less critical circuit, the components are arranged exactly in the order of signal flow. This will result in a minimum overall conductor length. Also, in a circuit where a few components have considerably more connecting points than the others, these key components must be placed first and the remaining ones are grouped around them.

The general rule is to place first components, whose position is fixed for the final fitting and interconnections, e.g. connectors, heat sinks, etc. Then place the components which are connected to these fixed components. Among the components, larger components are placed first and the space in between is filled with smaller ones. All the components should be placed in such a manner that disordering of other components is not necessary if they must be replaced.

Conductor Spacing

Conductor Spacing is generally based on voltage breakdown or flashover between adjacent conductors. The conductor spacing is determined by the peak voltage difference between adjacent conductors, capacitive coupling parameters and the use of coating (mask).

Conductor Width

General reference for conductor width is:

$$W_{ground} > W_{supply} > W_{signal}$$

$W_{ground}\ is\ ground\ conductor$
$W_{supply}\ is\ supply\ (VCC, VDD) conductor$
$W_{signal}\ is\ signal\ conductor\ (bus\ or\ net)$

The ground conductor should the most copper volume to provide good grounding and protecting the circuit from power surges. For TTL circuits:

$$W_{ground} > 2 \times W_{supply}$$
$$W_{supply} > 2 \times W_{signal}$$

It is a good practice to analyze the circuit and determine the current and type of signal flowing through a conductor. This provides information on the decision for the conductor width, length and thickness.

Part II. Integrating Electrical Design Considerations to PCB Layout

Before doing the exercise, make sure that you have listened to the demonstration on implementing electrical design considerations.

Activity #1:

For this activity, use the layout in Practical Activity #3, Activity #1. (PATILUNA_PA3-1.kicad_pcb.

Instructions:

1. Analyze the circuit and identify the current and type of signal flowing through each conductor. Note your findings in a text editor and save it with a filename <LASTNAME>_PA4-1.txt.

2. Adjust the track widths of the conductors and consider resistance, capacitance and inductance. Use the data gathered step 1. Track widths should be in mm (convert from mil to mm). You may have to edit the layout to adjust the conductor spacing. You might also have to move some components.

3. Run DRC and make sure errors and warnings are addressed.

4. Edit the silkscreen and arrange the component designators (name). You may add documentation on the silkscreen to indicate the function of the connectors. On a blank portion within the bottom layer, add the following (without the quotation marks). Replace 'y' with the document number in the schematic and the 'x' with the iteration number of your design.

   "CpE 2303L-2024-yyyy Rev 1.x"

   Since this is the 3rd iteration of the layout, revision number should not be lower than 1.3. Adjust font size if necessary.

5. Save the schematic diagram and PCB layout with the same filename format: "<YOUR LAST NAME>_PA4-1.kicad_pcb". For example "PATILUNA_PA4-1.kicad_pcb".

Activity #2:

For this activity, use the PCB layout in Activity #3 (Practical Activity #2 – "MCU-based two-digit counter") with filename "PATILUNA_PA3-2.kicad_pcb".

Instructions:

1. Analyze the circuit and identify the current and type of signal flowing through each conductor. Note your findings in a text editor and save it with a filename <LASTNAME>_PA4-2.txt.

2. Change the power connector (pin header) to a Molex connector.

3. Adjust the track widths of the conductors and consider resistance, capacitance and inductance. Use the data gathered step 1. Track widths should be in mm (convert from mil to mm). You may have to edit the layout to adjust the conductor spacing. You might also have to move some components.

4. Run DRC and make sure errors and warning are addressed.

5. Edit the silkscreen and arrange the component designators (name). You may add documentation on the silkscreen to indicate the function of the connectors. On a blank portion within the bottom layer, add the following (without the quotation marks). Replace 'y' with the document number in the schematic and the 'x' with the iteration number of your design.

   "CpE 2303L-2024-yyyy Rev 1.x"

   Since this is the 4th minor iteration of the layout, revision number should not be lower than 1.4. Adjust the font size if necessary. Adjust the font size if necessary.

6. Save the schematic diagram and PCB layout with the same filename format: “<YOUR LAST NAME>_PA4-1.kicad_pcb”. For example “PATILUNA_PA4-1.kicad_pcb”.

Submissions Instructions:

Layout Printout

Print all the PCB layout by clicking Files->Print. Click “Printer” and choose “Microsoft Print to PDF” as a printer. Click “Preferences” and make sure that the orientation is landscape and the paper size if US LETTER. Click “Ok” then click “Print”. To print click “OK” and save the file to the same folder you save your schematic diagrams and PCB layouts.

Combine the three (3) PCB layouts into a single PDF file1. The filename format should be “<YOUR LAST NAME>_PA2.pdf” for example “PATILUNA _PA2.pdf”. Submit PDF to the Practical Activity #2 page in Canvas.

Schematic and Layout Files

Submit the **schematic** (.kicad_sch) and **layout** (.kicad_pcb) files for the three activities. Do not archive or zip the files.