Hanyu Wang

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414 Badenerstrasse
8004 Zurich, Switzerland

EDUCATION

09/2021 - present **Master of Science**, Electrical Engineering Information Technology
Swiss Federal Institute of Technology Zurich

09/2017 - 08/2021 **Bachelor of Engineering**, Electrical and Computer Engineering
University of Michigan-Shanghai Jiao Tong University Joint Institute
GPA: 3.79/4.00 Ranking: 4/148

EXPERIENCE

05/2020 - 11/2020 **Research Intern**, Computer Systems Laboratory
Cornell University, Ithaca, USA
Advisor: Dr. Zhiru Zhang

01/2020 - 05/2020 **Exchange Student**, Electrical and Computer Engineering
University of Wisconsin Madison, Wisconsin, USA
GPA: 4.00/4.00

06/2019 - 08/2021 **Research Intern**, Emerging Computing Technology Laboratory
Shanghai Jiao Tong University, Shanghai, China
Advisor: Dr. Weikang Qian

12/2018 - 02/2019 **Exchange Student**, German Language Program
Technical University of Berlin, Berlin, Germany

SELECTED PROJECTS

04/2021 - 09/2021 **AIG rewriting using Simulated Annealing**
Emerging Computing Technology Laboratory, Shanghai, China
- Implemented simulated annealing framework based on Berkeley ABC rewriting, refactor, and resubstitution.
- Reduced the area of EPFL benchmarks by 22% on average comparing to the powerful command compress2rs in Berkeley ABC

09/2020 - 04/2021 **Global Fanout Optimization using SAT-based rewiring**
Emerging Computing Technology Laboratory, Shanghai, China
- Reduced the fanout number on critical path by 34% based on circuits in EPFL best results.
- Developed a framework utilizing SAT-solver in Fanout Optimization.

04/2020 - 11/2020 **Distilling Arbitration Logic from Traces using Machine Learning**
Computer Systems Laboratory, Ithaca, USA
- Utilized reinforcement learning in optimizing memory banking, pre-fetching, branch prediction.
- Reduced the area of "distilled" logic learned from RL to fit SoC.

01/2020 - 04/2020 **Global Router Course Competition**, ECE556
University of Wisconsin Madison, Wisconsin, USA
- Implemented Global Router with heterogeneous Rip-up Re-Routing
- Won the 1st place in the contest 2020 with the lowest wirelength.

09/2019 - 11/2019 **5-stage In-order Pipeline Scalar Microarchitecture Implementation**
University of Michigan-Shanghai Jiao Tong University Joint Institute
- Implemented a 5-stage pipeline CPU with cache
- Emulated Verilog top module using Xilinx Vivado

HONORS & AWARD

11/2020	**Scholarship**: Sam and Daisy Wu Research Scholarship (1 out of 162)
11/2018	**Scholarship**: Yu Liming Scholarship (6 out of 325)
11/2018	**Scholarship**: Undergraduate Excellence Scholarship
09/2017	**Scholarship**: John Wu & Jane Sun Excellence Scholarship

TEACHING

05/2019 - 08/2019	**Teaching Assistant**, VE475 Introduction to Cryptography University of Michigan-Shanghai Jiao Tong University Joint Institute
09/2019 - 12/2019	**Teaching Assistant**, VP260 Honors Physics II University of Michigan-Shanghai Jiao Tong University Joint Institute
05/2019 - 08/2019	**Teaching Assistant**, VP160 Honors Physics I University of Michigan-Shanghai Jiao Tong University Joint Institute

LANGUAGE SKILLS

- Chinese: Native
- English: GRE 325 (V:155 Q:170 AW:4)
  TOEFL 109 (R:30 L:25 S:27 W:27)
- German: Goethe A2

PUBLICATIONS

C1. Y. Zhou, **H. Wang**, J. Yin, and Z. Zhang, *Distilling Arbitration Logic from Traces using Machine Learning: A Case Study on NoC*, to appear in Design Automation Conference (DAC), Dec. 2021. (Best Paper Nominee)