Hanyu WANG

(+41)79-222-6346
hanywang@student.ethz.ch
Gertrudstrasse 84
8003 Zurich, Switzerland

EDUCATION

09/2024 - Present	**PhD candidate**, Computer Science University of California, Los Angeles Interests: Quantum computing
09/2021 - 09/2024	**Master of Science**, Electrical Engineering Information Technology Swiss Federal Institute of Technology Zurich **GPA**: Core: 5.82/6.00, All: 5.53/6.00
09/2017 - 08/2021	**Bachelor of Engineering**, Electrical and Computer Engineering University of Michigan-Shanghai Jiao Tong University Joint Institute **GPA**: 3.79/4.00 Ranking: 4/148

EXPERIENCE

09/2024 - Present	**Graduate Research Assistant**, VAST Research Group University of California, Los Angeles Advisor: Prof. Jason Cong
10/2022 - 09/2024	**Research Intern**, DYNAMO Research Group ETH, Zurich, Switzerland Advisor: Prof. Lana Josipović
10/2021 - 09/2022	**Research Intern**, Integrated Systems Laboratory EPFL, Lausanne, Switzerland Advisor: Prof. Giovanni De Micheli
06/2019 - 09/2021	**Research Intern**, Emerging Computing Technology Laboratory Shanghai Jiao Tong University, Shanghai, China Advisor: Prof. Weikang Qian
05/2020 - 11/2020	**Research Intern (Remote)**, Computer Systems Laboratory Cornell University, Ithaca, USA Advisor: Prof. Zhiru Zhang
01/2020 - 05/2020	**Exchange Student**, Electrical and Computer Engineering University of Wisconsin Madison, Wisconsin, USA GPA: 4.00/4.00
12/2018 - 02/2019	**Exchange Student**, German Language Program Technical University of Berlin, Berlin, Germany

HONORS & AWARD

07/2022	**Competition**: 1st place in IWLS 2022 Contest
11/2020	**Scholarship**: Sam and Daisy Wu Research Scholarship (1 out of 162)
11/2018	**Scholarship**: Liming Yu Scholarship (6 out of 325)
11/2018	**Scholarship**: Undergraduate Excellence Scholarship
09/2017	**Scholarship**: John Wu & Jane Sun Excellence Scholarship
11/2019	**Competition**: Bronze Medal in the University Physics Competition
11/2016	**Competition**: 2nd Class Award in National Olympiad of Information (NOIP)
09/2016	**Competition**: 2nd Class Award in Chinese Physics Olympiad (CPhO)

TEACHING

06/2023 - 08/2023	**Teaching Assistant**, VLSI 4: Measurement and testing of VLSI Circuits Supervised a student project that runs Scan Chain Implemented Fault Injection using a 93000 tester.
02/2023 - 06/2023	**Teaching Assistant**, VLSI 2: Backend design, ETH Zurich Assisted 12 exercises, including DFT in Synopsys DC, Floorplanning and PnR in Cadence Innovus and DRC LVS using Mentor Calibre.
09/2022 - 12/2022	**Teaching Assistant**, VLSI 1: HDL-based design for FPGAs, ETH Zurich Assisted 8 exercises for HDL coding, FPGA deployment using Xilinx Vivado, and High-level synthesis using Vivado HLS.
05/2019 - 08/2019	**Teaching Assistant**, VE475 Introduction to Cryptography University of Michigan-Shanghai Jiao Tong University Joint Institute
09/2019 - 12/2019	**Teaching Assistant**, VP260 Honors Physics II University of Michigan-Shanghai Jiao Tong University Joint Institute
05/2019 - 08/2019	**Teaching Assistant**, VP160 Honors Physics I University of Michigan-Shanghai Jiao Tong University Joint Institute

SELECTED PROJECTS

03/2022 - 07/2022	**Minimum Circuit Size Problem Solver** EPFL, Lausanne, Switzerland ● Synthesized multi-output completely specified functions. ● Won 1st place in the global contest.
05/2022 - 07/2022	**Scan Chain Implemented Fault Injection,** VLSI4 Project ETH, Zurich, Switzerland ● Implemented SCIFI on hp93000 tester. ● Ran fault injection test on Pony.
04/2021 - 09/2021	**AIG Size Optimization using Simulated Annealing** Emerging Computing Technology Laboratory, Shanghai, China ● Implemented simulated annealing framework based on ABC rewriting, refactoring, and resubstitution. ● Reduced the area by 22% compared to the state-of-the-art logic synthesis command compress2rs in ABC.
01/2021 - 03/2021	**ReFO: Resubstitution-based Fanout Optimization for FPGA Delay Reduction** Huawei Inc, Shanghai, China ● Developed a resubstitution-based algorithm and reduced the total fanout on the critical path by 60% with a 5% area overhead.
01/2020 - 04/2020	**Global Router Competition**, ECE556 Project University of Wisconsin Madison, Wisconsin, USA ● Implemented Global Router with heterogeneous Rip-up Re-Routing ● Won 1st place in the 2020 contest with the lowest wire length.

LANGUAGE SKILLS

● Chinese:	Native	
● English:	GRE	325 (V:155 Q:170 AW:4)
	TOEFL	109 (R:30 L:25 S:27 W:27)
● German:	Goethe A2	

PUBLICATIONS

W: Workshop / **C: C**onference paper

C6. **H. Wang**, D. Tan, and J. Cong, *Quantum State Preparation Circuit Optimization Exploiting Don't Cares*, International Conference on Computer-Aided Design (ICCAD), to appear, Oct. 2024.

C5. C. Meng, M. Yu, H. Wang, and G. De Micheli, *Rarity-Reducing Logic Synthesis for Mitigating Hardware Trojan Threats*, International Conference on Computer-Aided Design (ICCAD), to appear, Oct. 2024.

W3. **H. Wang**, C. Meng, and G. De Micheli, *A Cost-generic Resubstitution Algorithm with Customizable Cost Functions*, International Workshop on Logic and Synthesis (IWLS), Jul. 2024.

C4. **H. Wang**, J. Cong, and G. De Micheli, *Quantum State Preparation Using an Exact CNOT Synthesis Formulation*, Design, Automation, and Test in Europe Conference (DATE), Mar. 2024.

C3. C. Meng, H. Wang, Y. Mai, W. Qian, and G. De Mechili, *VACSEM: Verifying Average Errors in Approximate Circuits Using Simulation-Enhanced Model Counting,* Design, Automation and Test in Europe Conference (DATE), Mar. 2024. **(Best Paper Nominee)**

C2. **H. Wang**, C. Rizzi, and L. Josipović, *MapBuf: Simultaneous Technology Mapping and Buffer Insertion for HLS Performance Optimization*, International Conference on Computer-Aided Design (ICCAD), to appear, Nov. 2023. **(Best Paper Nominee)**

W2. **H. Wang**, C. Rizzi, and L. Josipović, *MapBuf: Simultaneous Technology Mapping and Buffer Insertion for HLS Performance Optimization*, International Workshop on Logic and Synthesis (IWLS), Jul. 2022.

W1. **H. Wang**, S. Lee, and G. De Micheli, *A Cost-generic Resubstitution Algorithm with Customizable Cost Functions*, International Workshop on Logic and Synthesis (IWLS), Jul. 2022.

C1. Y. Zhou, H. Wang, J. Yin, and Z. Zhang, *Distilling Arbitration Logic from Traces using Machine Learning: A Case Study on NoC*, Design Automation Conference (DAC), Dec. 2021. **(Best Paper Nominee)**