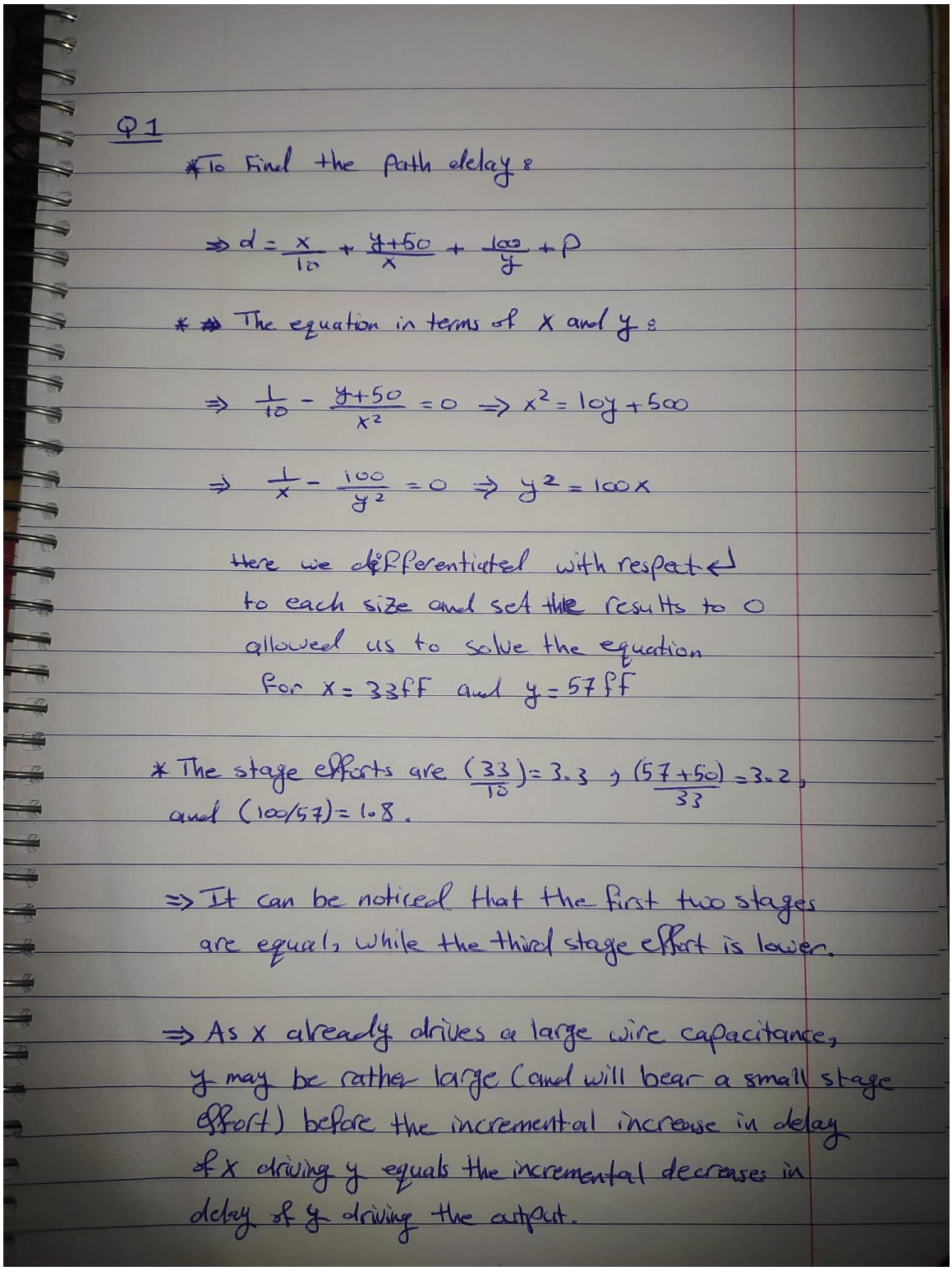
Nqaa Ladadwa-1180629

HW2-VLSI



Q1

* To Find the path delay:

$$\Rightarrow d = \frac{x}{10} + \frac{y+50}{x} + \frac{100}{y} + p$$

** The equation in terms of x and y:

$$\Rightarrow \frac{1}{10} - \frac{y+50}{x^2} = 0 \Rightarrow x^2 = 10y + 500$$

$$\Rightarrow \frac{1}{x} - \frac{100}{y^2} = 0 \Rightarrow y^2 = 100x$$

there we differentiated with respect to each size and set the results to 0 allowed us to solve the equation

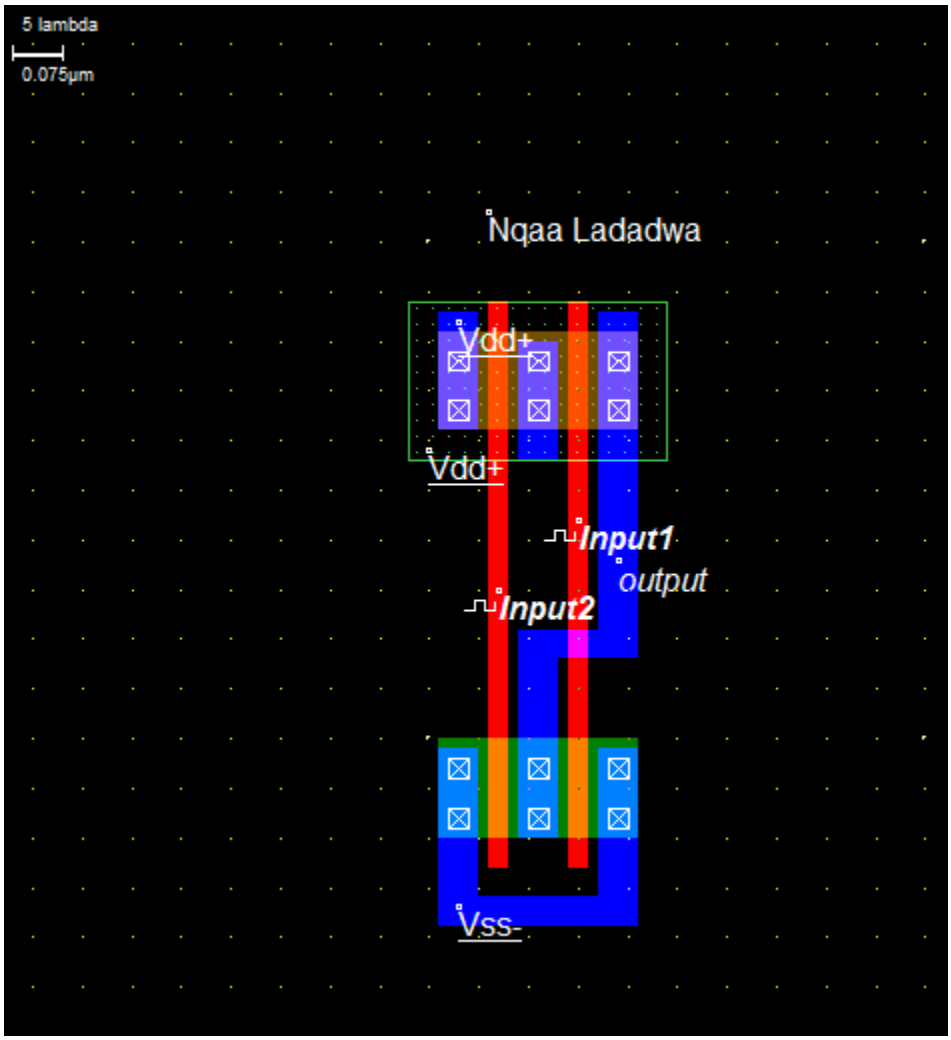
For x = 33ff and y = 57 ff

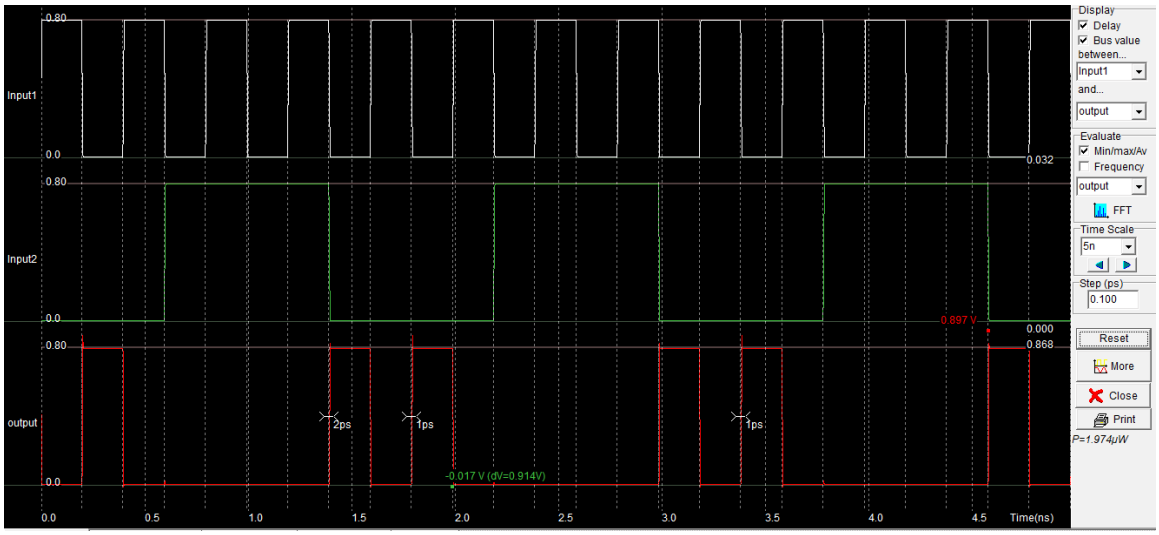
* The stage efforts are $(\frac{33}{10}) = 3.3$, $\frac{(57+50)}{33} = 3.2$, and $(100/57) = 1.8$.

⇒ It can be noticed that the first two stages are equal, while the third stage effort is lower.

⇒ As x already drives a large wire capacitance, y may be rather large (and will bear a small stage effort) before the incremental increase in delay of x driving y equals the incremental decreases in delay of y driving the output.

Q2:


5 lambda
0.075µm
Nqaa Ladadwa
Vdd+
Vdd+
Input1
output
Input2
Vss-


Input1
Input2
output
0.80
0.0
0.032
0.897 V
0.000
0.868
2ps
1ps
1ps
-0.017 V (dV=0.914V)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
Time(ns)
Display
Delay
Bus value between...
Input1
and...
output
Evaluate
Min/max/Av
Frequency
output
FFT
Time Scale
5n
Step (ps)
0.100
Reset
More
Close
Print
P=1.974µW