# Test 1

1. **What technology was used in the first embedded system developed for the MinuteMan-I Missiles?**

a. Integrated circuits and microprocessors
b. Discrete transistor logic and hard disk drive for main memory
c. Vacuum tubes and magnetic tape drives
d. Digital signal processors and solid-state drives
e. None of these

2. **What is the impact of shrinking technology nodes on processor clock rates?**

a. Smaller process nodes lead to slower switching speeds and increased gate delays.
b. Shrinking technology nodes enable faster switching speeds and improved power efficiency.
c. Smaller transistors increase clock rates but decrease processor performance.
d. All of these
e. None of these

3. **What does the Behavioural Domain in the Y-chart represent?**

a. The high-level functionalities and operations required by the embedded system, including tasks, algorithms, and control processes.
b. The different possible implementations of the system's functionalities, such as hardware and software options.
c. The allocation decisions of functionalities to hardware or software components.
d. The physical components and their layout in the embedded system.
e. None of these

4. **What is a key feature of bank-switched memory compared to dual-port memory?**

a. Bank-switched memory allows simultaneous access to different memory banks by the CPU and I/O hardware.
b. Bank-switched memory provides a single memory space that is accessed by both software and hardware.
c. Bank-switched memory has two modes of operation for exclusive access to memory banks.
d. Bank-switched memory uses a FIFO buffer for data transfer.
e. None of these

5. **What is the primary role of an RTOS in managing interrupts and tasks?**

a. To handle interrupts with fixed priority scheduling
b. To manage tasks, scheduling, and resources in real-time
c. To assign priority levels to hardware interrupts

d. To provide dynamic prioritization for ISRs only
e. None of these

6. **What advantage does a microkernel provide over a monolithic kernel?**
a. Higher performance due to all services running in kernel space
b. Greater modularity and OS-neutral abstraction with essential services only in the kernel
c. Fewer system crashes due to tight internal integration of services
d. Simplified implementation with all services in user space
e. None of these

7. **Which statement best describes a process in the context of an operating system?**
a. A process is a single sequential flow of control within a program
b. A process is a program or part of it that needs to be executed and requires system resources like CPU, memory, and I/O devices
c. A process is a lightweight thread that shares address space with other processes
d. A process is a specific set of tasks executed by a Real Time OS
e. None of these

8. **Which of the following statements is true about FLOPS?**
a. FLOPS measure the number of integer operations a processor can perform per second
b. FLOPS are used to assess the performance of a processor in complex mathematical calculations
c. FLOPS predict integer and logic performance accurately
d. All of these
e. None of these

9. **What is the main difference between pre-emptive and non-pre-emptive task management?**
a. Pre-emptive tasks run until completion, while non-pre-emptive tasks can be interrupted
b. Non-pre-emptive tasks can be interrupted in favor of higher-priority tasks, while pre-emptive tasks cannot
c. Pre-emptive tasks can be interrupted by the scheduler, while non-pre-emptive tasks continue until they voluntarily yield control
d. Non-pre-emptive tasks are managed based on priority, while pre-emptive tasks are not

10. **Which of the following is true regarding a finite state machine (FSM)?**
a. A state in an FSM only reflects the current inputs
b. In a Mealy Machine, outputs depend solely on the current state

c. A transition is triggered by fulfilling a specific condition
d. All of these
e. None of these

## Test 2

1. **In a LIN bus protocol, what does the frame header consist of?**
a. Data field and sync pattern
b. Identifier and checksum
c. Break, sync pattern, and identifier
d. All of these
e. None of these

2. **What is a cache miss?**
a. When the cache contains the information requested.
b. When the requested data is found in the cache memory.
c. When the cache does not contain the information requested and the processor needs to retrieve it from a higher-level memory.
d. All of these
e. None of these

3.**Which technique for reducing cache miss rates involves using the compiler to predict and load data into the cache before it is actually needed?**
a. Hardware prefetching
b. Compiler-controlled prefetching
c. Victim caches
d. Pseudo-associative caches
e. None of these

4. **Which type of cache miss is caused by the first access to a block that is not yet in the cache?**
a. Capacity miss
b. Conflict miss
c. Compulsory miss
d. Collision miss
e. None of these

5. **What happens during a recessive to dominant transition in a CAN bus system?**
a. A bit is automatically inserted by the receiver to maintain synchronization.
b. All nodes on the bus synchronize to the Start of Frame (SOF) bit.
c. The bus becomes idle and all nodes stop transmitting data.

d. The bit-stuffing process is initiated by the receiver.
e. None of these

6. **What is the primary goal of reducing cache miss penalty?**
a. To increase the hit rate of the cache.
b. To decrease the time required to access data from the cache.
c. To increase the size of the cache.
d. To improve the time required to replace a block in the cache from main memory.
e. None of these

7. **What is a key feature of the CAN bus MAC protocol compared to Aloha and Ethernet?**
a. CAN bus nodes use a fixed delay time to avoid collisions.
b. CAN bus nodes detect collisions based on dominant and recessive bits, allowing one node to continue transmitting while others stop.
c. CAN bus nodes do not need to listen to the bus while transmitting.
d. CAN bus nodes use acknowledgments to determine if a collision has occurred.
e. None of these

8. **What is the primary function of the DMARequest signal in a DMA operation?**
a. To indicate that the DMA Controller has completed the data transfer.
b. To signal the peripheral device to place data onto the data bus.
c. To acknowledge that the DMA Controller has gained control of the buses.
d. To request control of the system buses from the bus arbitration unit.
e. None of these.

9. **What condition must be met for the SCL line to transition from 0 to 1 during synchronization?**
a. All masters must finish their high period.
b. The longest low period must be completed.
c. The first master to finish its low period releases the SCL line.
d. All of these
e. None of these

10. **In $I^2C$ arbitration, what is the first bit transmitted after the start condition?**
a. Acknowledge bits
b. Data bits
c. Slave addresses
d. All of these
e. None of these