MetalFish: GPU-Accelerated NNUE Evaluation on Apple Silicon

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Abstract. We present MetalFish, a GPU-accelerated chess engine leveraging Apple Silicon's unified memory architecture for NNUE evaluation. Through systematic optimization and benchmarking on M2 Max, we demonstrate: (1) GPU batch evaluation achieving 268 μs median latency for single positions and 0.4 μs per position at batch size 2048, (2) true batching with up to 530× speedup over sequential dispatches, (3) SIMD-optimized kernels with 8-way unrolled accumulation, and (4) complete feature coverage with 0% position capping (supporting up to 64 features per perspective). Our implementation reduces GPU end-to-end latency by 2.75× compared to naive approaches. While dispatch overhead (139 μs) makes single-position GPU evaluation unsuitable for alpha-beta search, batch evaluation becomes throughput-competitive at $N \geq 512$, enabling efficient bulk analysis and MCTS-style evaluation.

Keywords: Chess Engine, GPU Computing, Metal, NNUE, Apple Silicon, Unified Memory

1 Introduction

Modern chess engines combine alpha-beta search with neural network evaluation (NNUE) to achieve superhuman playing strength. While GPU acceleration has proven effective for batch-oriented algorithms like Monte Carlo Tree Search in Leela Chess Zero [2], its applicability to traditional alpha-beta search remains challenging due to sequential evaluation patterns.

Apple Silicon's unified memory architecture eliminates explicit CPU-GPU memory transfers, potentially reducing the overhead that has historically limited GPU adoption in alpha-beta engines. This paper presents MetalFish, a GPU-accelerated chess engine that explores the practical limits of GPU evaluation on Apple Silicon.

1.1 Contributions

1. **Optimized GPU NNUE implementation**: We achieve 268 μs median latency for single-position evaluation and 0.4 μs per position at batch size 2048—a 2.75× improvement over naive implementations.

Table 1. NNUE Network Architecture

Component	Big Network	Small Network
Feature set	HalfKAv2_hm	HalfKAv2_hm
Input features	45,056	22,528
Hidden dimension	1,024	128
FC0 output	15 (+1 skip)	15 (+1 skip)
FC1 output	32	32
FC2 output	1	1
Layer stacks (buckets)	8	8

2. **Complete feature coverage**: Our implementation supports up to 64 features per perspective (128 total), handling 100% of chess positions without feature capping. Previous implementations capped at 32 features, affecting 75% of positions.
3. **Verified true batching**: We demonstrate single-dispatch batching achieving up to 530× speedup over sequential dispatches at batch size 1024.
4. **SIMD-optimized kernels**: We present Metal compute kernels with 8-way unrolled accumulation, dual-perspective feature transformation, and threadgroup memory optimization.
5. **Comprehensive benchmarking**: We provide detailed stage breakdowns, latency percentiles, and scaling analysis across batch sizes 1–2048.

2 Background

2.1 NNUE Architecture

Stockfish's NNUE [1, 5] uses HalfKAv2_hm features with sparse input and efficient incremental updates. Table 1 summarizes the architecture.

Feature requirements: HalfKAv2_hm generates one feature per non-king piece from each perspective. A position with 30 pieces (excluding 2 kings) generates up to 30 features per perspective. Our implementation supports 64 features per perspective, providing headroom for all legal positions.

2.2 Metal Compute Model

Apple Metal [6] provides GPU compute through command buffers with unified memory access. Key characteristics:

- **Unified memory**: CPU and GPU share the same physical memory, eliminating explicit transfers
- **Command buffer lifecycle**: Allocation, encoding, submission, and synchronization
- **Threadgroup memory**: Fast on-chip memory for inter-thread communication
- **SIMD groups**: 32-wide SIMD execution on Apple GPUs

Table 2. GPU Configuration Constants

Parameter	Value
Max batch size	4,096
Max features per perspective	64
Max total features	128
Threadgroup size	256
SIMD group size	32
Forward pass threads	64

3 System Architecture

3.1 GPU Constants and Limits

Table 2 shows the key GPU configuration parameters.

3.2 Kernel Optimizations

We implement three key optimizations in our Metal compute kernels:

1. SIMD-aware feature transformation: The feature transform kernel processes features with memory coalescing, accessing weights with stride patterns that maximize cache utilization.

2. Unrolled accumulation: The forward pass uses 8-way unrolled loops for the FC0 layer, reducing loop overhead and enabling instruction-level parallelism:

```
for (; i + 7 < hidden_dim; i += 8) {
    int8_t c0 = clipped_relu(acc[i] >> SCALE);
    int8_t c1 = clipped_relu(acc[i+1] >> SCALE);
    // ... c2-c7
    sum += c0 * weights[(i)*stride + out];
    sum += c1 * weights[(i+1)*stride + out];
    // ... 6 more
}
```

Listing 1.1. 8-way unrolled FC0 accumulation

3. Threadgroup memory for FC layers: Intermediate results (FC0 outputs, skip connections) are stored in threadgroup memory, enabling efficient inter-thread communication without global memory round-trips.

3.3 Batch Evaluation Pipeline

Algorithm 1 shows the optimized batch evaluation.

Algorithm 1 Optimized GPU Batch NNUE Evaluation

Require: Batch of N positions
Ensure: Evaluation scores for all positions

```
// Stage 1: Feature extraction (CPU)
for each position do
    Extract white/black features from bitboards
    Store in contiguous buffers with offsets
end for
// Stage 2: GPU evaluation (single command buffer)
Upload features to unified memory buffers
DispatchThreads(hidden_dim × N)                          ▷ Feature transform
Barrier
DispatchThreadgroups(N, threads=64)                      ▷ Forward pass
SubmitAndWait
return scores from output buffer
```

4 Experimental Methodology

4.1 Hardware and Software

- **Hardware**: Apple M2 Max (12-core CPU, 38-core GPU, 64GB unified memory)
- **Software**: macOS 14.0, Xcode 15.0, Metal 3.0
- **Build**: CMake, -O3, LTO enabled
- **Networks**: nn-c288c895ea92.nnue (125MB), nn-37f18f62d772.nnue (6MB)

4.2 Timing Methodology

All measurements use `std::chrono::high_resolution_clock`:

- **Warmup**: 100 iterations discarded
- **Samples**: 100–100,000 iterations depending on variance
- **Statistics**: Median, P95, P99 reported
- **GPU timing**: Blocking `waitUntilCompleted()` (synchronous)

5 Results

5.1 Feature Coverage

Table 3 shows the feature count distribution.

Our implementation handles 100% of positions without feature capping, a critical improvement over the previous 32-feature limit.

5.2 GPU Dispatch Overhead

Table 4 shows minimal-kernel dispatch overhead.

The 139 μs median dispatch overhead represents the minimum cost for any GPU operation in synchronous mode.

Table 3. Feature Count Distribution (2,048 positions)

Metric	Value
Max features observed (total)	60
Max features per perspective	30
GPU limit per perspective	64
Positions exceeding limit	0%

Table 4. GPU Dispatch Overhead—Minimal Kernel (N=1,000)

Statistic	Latency (μs)
Median	139
P95	253
P99	310

5.3 GPU Stage Breakdown

Table 5 decomposes end-to-end latency.

GPU dispatch and kernel execution dominate (>98% of total time). CPU feature extraction is negligible.

5.4 Batch Latency Scaling

Table 6 shows end-to-end latency across batch sizes.

Key findings: (1) Latency is approximately constant (267–289 μs) for batch sizes 1–128, showing dispatch dominance. (2) Per-position cost drops from 267 μs (N=1) to 0.4 μs (N=2048). (3) Latency increases gradually beyond N=512, indicating kernel compute becoming significant.

5.5 True Batching Verification

Table 7 compares sequential vs batched dispatches.

Speedups scale linearly with batch size, confirming true single-dispatch batching.

5.6 Performance Comparison

Table 8 compares our optimized implementation with the naive approach.

Our optimizations achieve 2.75× faster single-position evaluation and eliminate all feature capping.

5.7 Search Performance

The engine achieves 1.38M nodes/second using CPU NNUE evaluation:

Table 5. GPU Stage Breakdown (N=100 iterations each)

Batch Size	CPU Prep	GPU Eval	GPU %
1	0.2 μs	268 μs	99.9%
8	0.3 μs	269 μs	99.9%
512	6.0 μs	370 μs	98.4%

Table 6. GPU End-to-End Batch Latency (N=100 iterations)

Batch Size	Median (μs)	P95 (μs)	P99 (μs)	Per-Pos (μs)
1	267	349	384	267.0
8	279	510	655	34.8
32	289	513	761	9.0
128	287	463	687	2.2
512	380	512	730	0.7
1024	540	661	862	0.5
2048	848	931	1,051	0.4

6 Discussion

6.1 When GPU Evaluation Helps

GPU batch evaluation becomes throughput-competitive at $N \geq 512$ (0.7 μs/position vs CPU feature extraction at 0.04 μs). This enables:

- **Database analysis**: Evaluating thousands of positions from game databases
- **MCTS evaluation**: Monte Carlo Tree Search naturally batches leaf evaluations
- **Training data generation**: Bulk position evaluation for neural network training

6.2 Alpha-Beta Limitations

Single-position GPU evaluation (268 μs) remains >6,000× slower than CPU feature extraction (0.04 μs). Alpha-beta search evaluates positions sequentially with data-dependent pruning, making batch accumulation impractical.

6.3 Optimization Impact

Our optimizations reduced GPU latency by 2.75× through:

- SIMD-aware memory access patterns
- 8-way unrolled accumulation loops
- Threadgroup memory for intermediate results
- Increased feature buffer capacity (32 → 64 per perspective)

Table 7. True Batching Verification (N=50 iterations)

N	Sequential (N×1 CB)	Batched (1×1 CB)	Speedup
16	4,649 μs	274 μs	17.0×
64	18,738 μs	291 μs	64.3×
256	74,220 μs	327 μs	227.3×
1024	298,506 μs	563 μs	530.0×

Table 8. Performance Comparison: Naive vs Optimized

Metric	Naive	Optimized
GPU latency (N=1)	737 μs	268 μs
GPU latency (N=512)	580 μs	370 μs
Per-position (N=2048)	0.6 μs	0.4 μs
Feature cap violations	75%	0%
Max batch size	256	4,096

7 Related Work

Leela Chess Zero [2] demonstrates successful GPU acceleration through MCTS, which naturally batches evaluations. AlphaZero [3] showed neural network evaluation can replace handcrafted evaluation with batch-oriented search.

For alpha-beta, Rocki and Suda [4] explored GPU parallelization through parallel subtree evaluation. Our work extends this to unified memory hardware with optimized NNUE kernels.

Apple's Metal documentation [6, 7] recommends minimizing command buffer submissions and using threadgroup memory for intermediate results.

8 Conclusion

We presented MetalFish, a GPU-accelerated chess engine achieving:

1. **268 μs** median single-position GPU evaluation (2.75× improvement)
2. **0.4 μs** per-position cost at batch size 2048
3. **530**× true batching speedup at N=1024
4. **0%** feature capping (100% position coverage)
5. **1.38M** nodes/second search performance

GPU acceleration is effective for batch-oriented workloads (MCTS, database analysis, training) but dispatch overhead makes it unsuitable for alpha-beta's sequential evaluation pattern. Our optimized Metal kernels and increased feature capacity provide a solid foundation for GPU-accelerated chess evaluation on Apple Silicon.

Table 9. Search Benchmark (50 positions, depth 13)

Metric	Value
Total Nodes	2,477,446
Total Time	1,792 ms
Nodes/Second	1,382,503

Reproducibility

Hardware: Apple M2 Max, 64GB. **Software**: macOS 14.0, Xcode 15.0. **Build**: CMake, -O3, LTO. **Source**: https://github.com/NripeshN/MetalFish. **Benchmark**: `gpubench` UCI command.

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