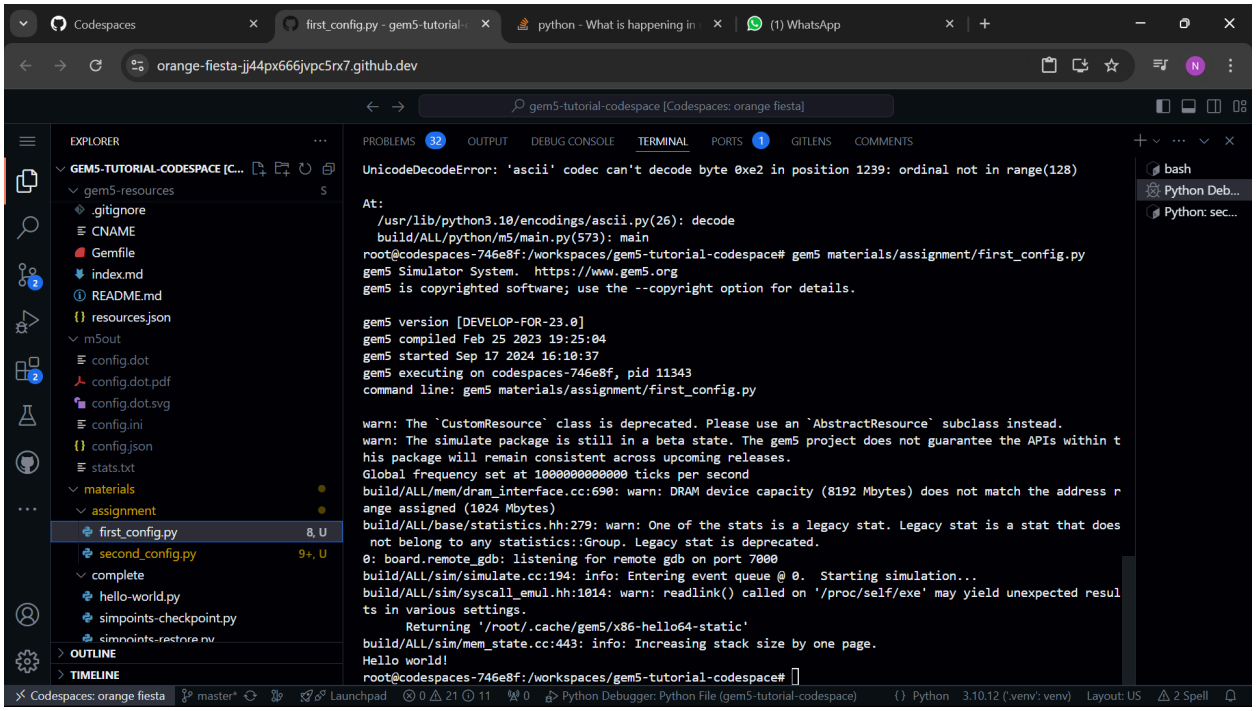
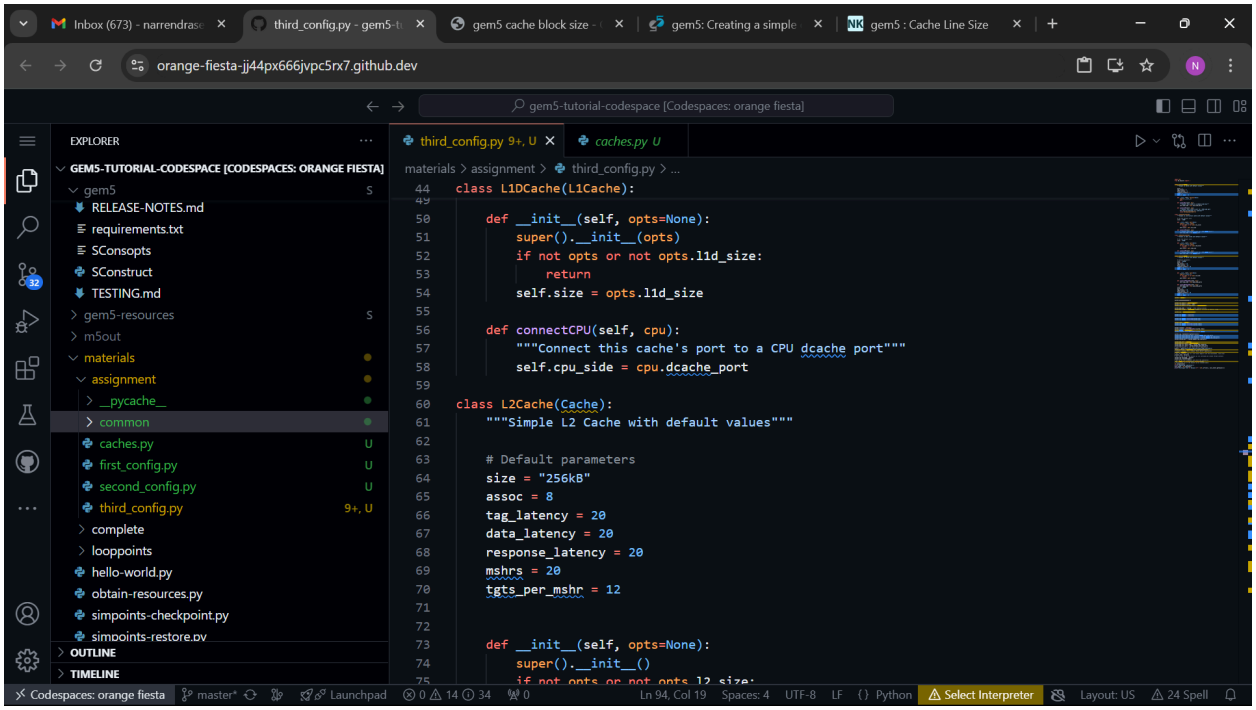
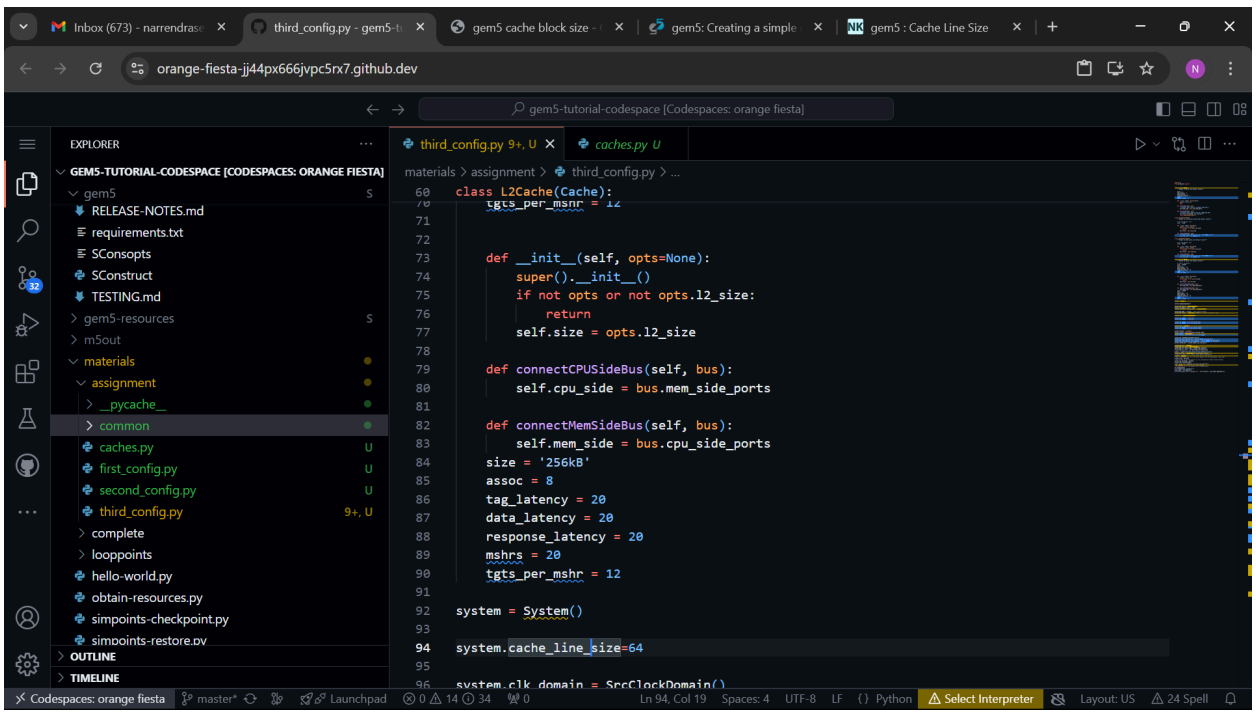
Github
https://github.com/Nrrndr/Narrendra-SKJ-Lab
.23/517555/PA/22195
Narrendra
(file ada di github)
NO1



NO2

NO 3


Inbox (673) - narrendrase
third_config.py - gem5-tu
gem5 cache block size -
gem5: Creating a simple
gem5 : Cache Line Size
orange-fiesta-jj44px666jvpc5rx7.github.dev
gem5-tutorial-codespace [Codespaces: orange fiesta]
EXPLORER
GEM5-TUTORIAL-CODESPACE [CODESPACES: ORANGE FIESTA]
gem5
RELEASE-NOTES.md
requirements.txt
SConsopts
SConstruct
TESTING.md
gem5-resources
m5out
materials
assignment
__pycache__
common
caches.py
first_config.py
second_config.py
third_config.py
complete
looppoints
hello-world.py
obtain-resources.py
simpoints-checkpoint.py
simpoints-restore.py
OUTLINE
TIMELINE
third_config.py 9+, U
caches.py U
materials > assignment > third_config.py > ...
class L1DCache(L1Cache):
def __init__(self, opts=None):
super().__init__(opts)
if not opts or not opts.l1d_size:
return
self.size = opts.l1d_size
def connectCPU(self, cpu):
"""Connect this cache's port to a CPU dcache port"""
self.cpu_side = cpu.dcache_port
class L2Cache(Cache):
"""Simple L2 Cache with default values"""
# Default parameters
size = "256kB"
assoc = 8
tag_latency = 20
data_latency = 20
response_latency = 20
mshrs = 20
tgts_per_mshr = 12
def __init__(self, opts=None):
super().__init__()
Codespaces: orange fiesta
master*
Launchpad
Ln 94, Col 19
Spaces: 4
UTF-8
LF
Python
Select Interpreter
Layout: US
24 Spell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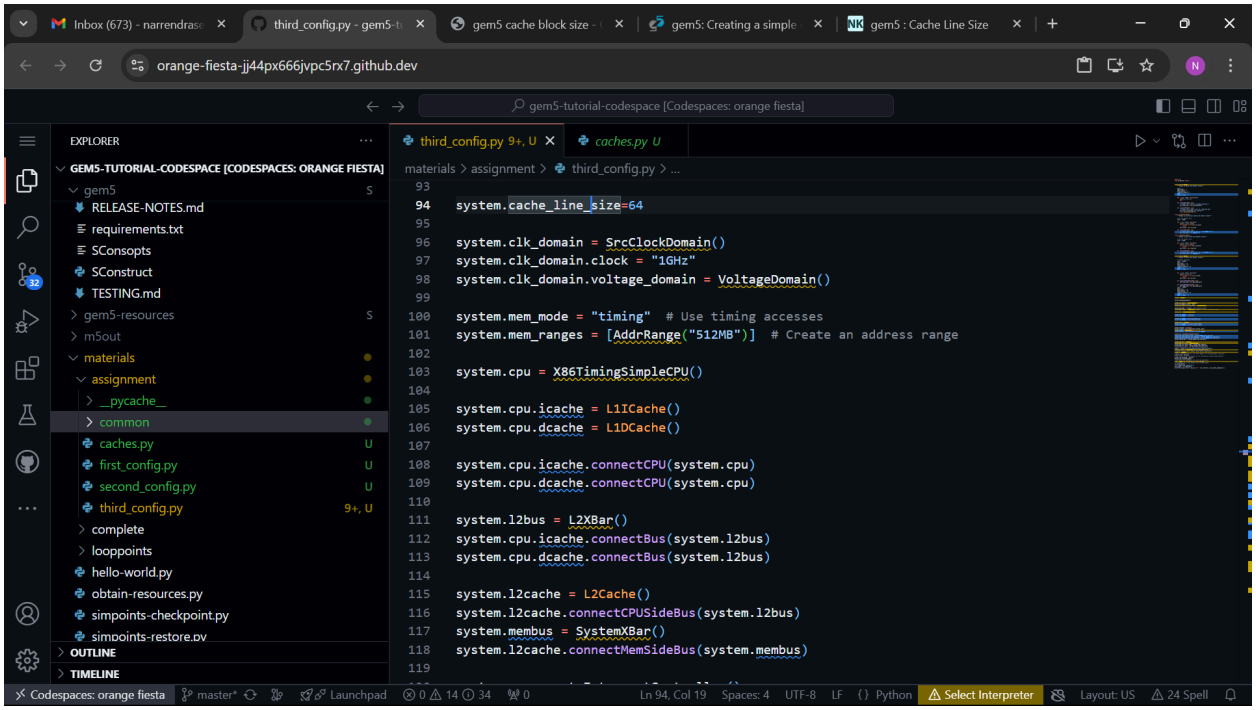
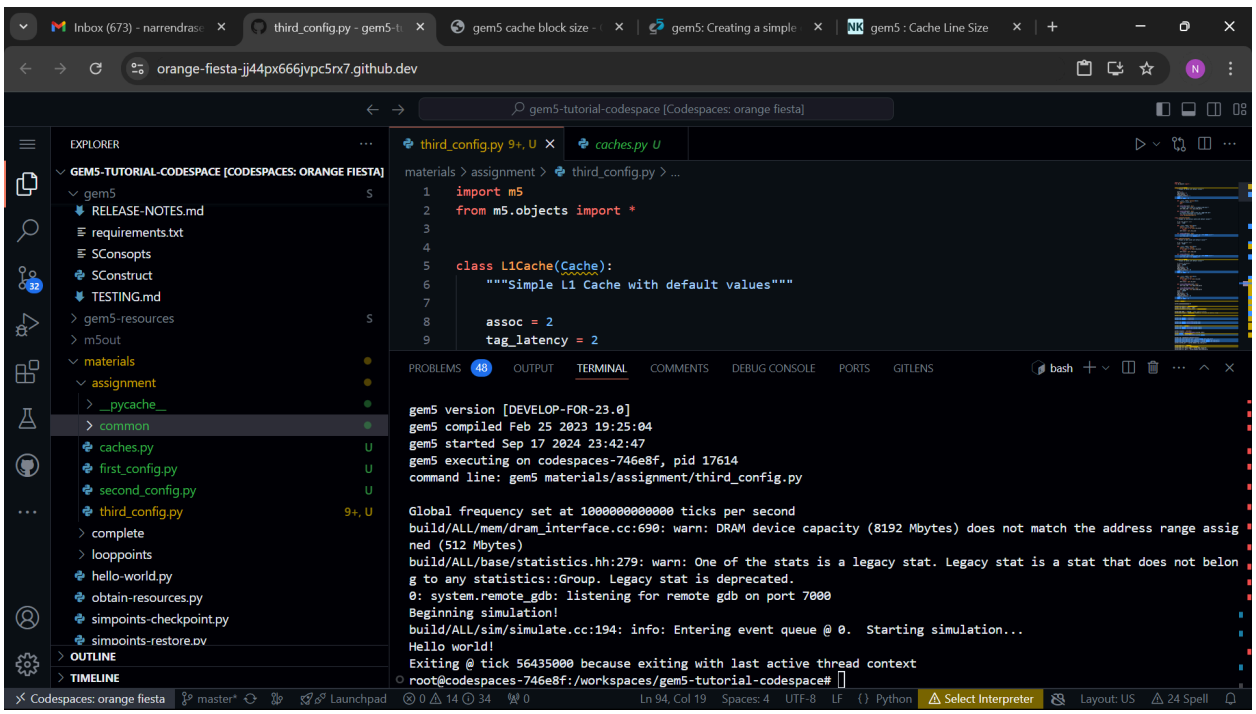
EXPLORER
GEM5-TUTORIAL-CODESPACE [CODESPACES: ORANGE FIESTA]
third_config.py 9+, U
caches.py U
materials > assignment > third_config.py > ...
class L2Cache(Cache):
def __init__(self, opts=None):
super().__init__()
if not opts or not opts.l2_size:
return
self.size = opts.l2_size
def connectCPUSideBus(self, bus):
self.cpu_side = bus.mem_side_ports
def connectMemSideBus(self, bus):
self.mem_side = bus.cpu_side_ports
size = '256kB'
assoc = 8
tag_latency = 20
data_latency = 20
response_latency = 20
mshrs = 20
tgts_per_mshr = 12
system = System()
system.cache_line_size=64
Codespaces: orange fiesta
master*
Launchpad
Ln 94, Col 19
Spaces: 4
UTF-8
LF
Python
Select Interpreter
Layout: US
24 Spell





NO 4

https://microarch.org/micro53/papers/738300a471.pdf

gem5-SALAM: A System Architecture for LLVM-based Accelerator Modeling

MAIn Objective:

To know and understand what gem5SALAM might be able to achieve compare to other alternative
finding:
Unlike the existing simulation platform, gem5-SALAM offers the run-time engine as a new Sim-Object within gem5 ecosystem to create a flexible full system simulation with many hardware accelerators

The paper also presents significant benefits of gem5-SALAM in enabling full system simulations and design space exploration for single and multiple accelerators with varying design sweeps.