

Github

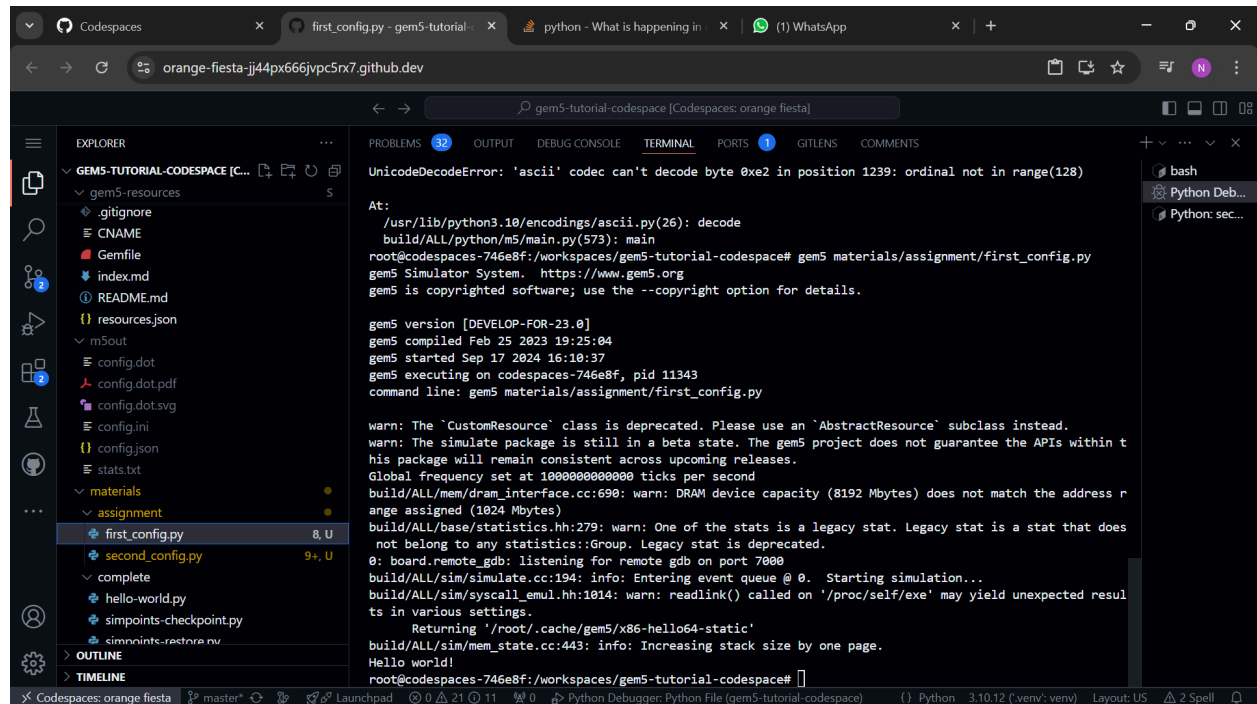
<https://github.com/Nrrndr/Narrendra-SKJ-Lab>

.23/517555/PA/22195

Narrendra

(file ada di github)

NO1



```
UnicodeDecodeError: 'ascii' codec can't decode byte 0xe2 in position 1239: ordinal not in range(128)

At:
/usr/lib/python3.10/encodings/ascii.py(26): decode
build/ALL/python/m5/main.py(573): main
root@codespaces-746e8f:/workspaces/gem5-tutorial-codespace# gem5 materials/assignment/first_config.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version [DEVELOP-FOR-23.0]
gem5 compiled Feb 25 2023 19:25:04
gem5 started Sep 17 2024 16:10:37
gem5 executing on codespaces-746e8f, pid 11343
command line: gem5 materials/assignment/first_config.py

warn: The 'CustomResource' class is deprecated. Please use an 'AbstractResource' subclass instead.
warn: The simulate package is still in a beta state. The gem5 project does not guarantee the APIs within t
his package will remain consistent across upcoming releases.
Global frequency set at 1000000000000 ticks per second
build/ALL/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address r
ange assigned (1024 Mbytes)
build/ALL/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does
not belong to any statistics::Group. Legacy stat is deprecated.
0: board.remote_gdb: listening for remote gdb on port 7000
build/ALL/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
build/ALL/sim/syscall_emul.hh:1014: warn: readlink() called on '/proc/self/exe' may yield unexpected resul
ts in various settings.
Returning '/root/.cache/gem5/x86-hello64-static'
build/ALL/sim/mem_state.cc:443: info: Increasing stack size by one page.
Hello world!
root@codespaces-746e8f:/workspaces/gem5-tutorial-codespace#
```

NO2



```
root@codespaces-746e8f:/workspaces/gem5-tutorial-codespace# gem5 materials/assignment/second_config.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version [DEVELOP-FOR-23.0]
gem5 compiled Feb 25 2023 19:25:04
gem5 started Sep 17 2024 17:11:37
gem5 executing on codespaces-746e8f, pid 42063
command line: gem5 materials/assignment/second_config.py

Global frequency set at 1000000000000 ticks per second
build/ALL/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
build/ALL/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Legacy stat is deprecated.
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/ALL/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
Hello world!
Exiting @ tick 462979000 because exiting with last active thread context
root@codespaces-746e8f:/workspaces/gem5-tutorial-codespace#
```

NO 3

```
44 class L1DCache(L1Cache):
45
46     def __init__(self, opts=None):
47         super().__init__(opts)
48         if not opts or not opts.l1d_size:
49             return
50         self.size = opts.l1d_size
51
52     def connectCPU(self, cpu):
53         """Connect this cache's port to a CPU dcache port"""
54         self.cpu_side = cpu.dcache_port
55
56 class L2Cache(Cache):
57     """Simple L2 Cache with default values"""
58
59     # Default parameters
60     size = "256kB"
61     assoc = 8
62     tag_latency = 20
63     data_latency = 20
64     response_latency = 20
65     mshrs = 20
66     tgts_per_mshr = 12
67
68     def __init__(self, opts=None):
69         super().__init__()
70         if not opts or not opts.l2_size:
71             return
72         self.size = opts.l2_size
73
74     def connectCPUSideBus(self, bus):
75         self.cpu_side = bus.mem_side_ports
76
77     def connectMemSideBus(self, bus):
78         self.mem_side = bus.cpu_side_ports
79
80     size = '256kB'
81     assoc = 8
82     tag_latency = 20
83     data_latency = 20
84     response_latency = 20
85     mshrs = 20
86     tgts_per_mshr = 12
87
88     system = System()
89
90     system.cache_line_size = 64
91
92     system.clk_domain = SrcClockDomain()
```

```
60 class L2Cache(Cache):
61     """Simple L2 Cache with default values"""
62
63     # Default parameters
64     size = "256kB"
65     assoc = 8
66     tag_latency = 20
67     data_latency = 20
68     response_latency = 20
69     mshrs = 20
70     tgts_per_mshr = 12
71
72     def __init__(self, opts=None):
73         super().__init__()
74         if not opts or not opts.l2_size:
75             return
76         self.size = opts.l2_size
77
78     def connectCPUSideBus(self, bus):
79         self.cpu_side = bus.mem_side_ports
80
81     def connectMemSideBus(self, bus):
82         self.mem_side = bus.cpu_side_ports
83
84     size = '256kB'
85     assoc = 8
86     tag_latency = 20
87     data_latency = 20
88     response_latency = 20
89     mshrs = 20
90     tgts_per_mshr = 12
91
92     system = System()
93
94     system.cache_line_size = 64
95
96     system.clk_domain = SrcClockDomain()
```

```

93
94 system.cache_line_size=64
95
96 system.clk_domain = SrcClockDomain()
97 system.clk_domain.clock = "1GHz"
98 system.clk_domain.voltage_domain = VoltageDomain()
99
100 system.mem_mode = "timing" # Use timing accesses
101 system.mem_ranges = [AddrRange("512MB")] # Create an address range
102
103 system.cpu = X86TimingSimpleCPU()
104
105 system.cpu.icache = L1ICache()
106 system.cpu.dcache = L1DCache()
107
108 system.cpu.icache.connectCPU(system.cpu)
109 system.cpu.dcache.connectCPU(system.cpu)
110
111 system.l2bus = L2X8Bar()
112 system.cpu.icache.connectBus(system.l2bus)
113 system.cpu.dcache.connectBus(system.l2bus)
114
115 system.l2cache = L2Cache()
116 system.l2cache.connectCPUSideBus(system.l2bus)
117 system.membus = SystemX8Bar()
118 system.l2cache.connectMemSideBus(system.membus)
119

```

```

1 import m5
2 from m5.objects import *
3
4
5 class L1ICache(Cache):
6     """Simple L1 Cache with default values"""
7
8     assoc = 2
9     tag_latency = 2

```

```

gem5 version [DEVELOP-FOR-23.0]
gem5 compiled Feb 25 2023 19:25:04
gem5 started Sep 17 2024 23:42:47
gem5 executing on codespaces-746e8f, pid 17614
command line: gem5 materials/assignment/third_config.py

Global frequency set at 1000000000000 ticks per second
build/ALL/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
build/ALL/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Legacy stat is deprecated.
0: system.remote_gdb: listening for remote gdb on port 7000
Beginning simulation!
build/ALL/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
Hello world!
Exiting @ tick 56435000 because exiting with last active thread context
root@codespaces-746e8f:/workspaces/gem5-tutorial-codespace#

```

NO 4

<https://microarch.org/micro53/papers/738300a471.pdf>

gem5-SALAM: A System Architecture for LLVM-based Accelerator Modeling

MAIn Objective:

To know and understand what gem5SALAM might be able to achieve compare to other alternative

finding:

Unlike the existing simulation platform, gem5-SALAM offers the run-time engine as a new Sim-Object within gem5 ecosystem to create a flexible full system simulation with many hardware accelerators

The paper also presents significant benefits of gem5-SALAM in enabling full system simulations and design space exploration for single and multiple accelerators with varying design sweeps.