NRUSINGA CHARAN GANTAYAT

(480) 743-4784 ▪ ngantaya@asu.edu ▪ Tempe, AZ 85281 ▪ www.LinkedIn.com/in/nrusinga-charan-gantayat

OBJECTIVE

Looking for internship/Co-op opportunities for Fall 2023/Spring 2024.

EDUCATION

MASTER OF SCIENCE (M.S.) IN ELECTRICAL ENGINEERING (Analog and Mixed Signals Circuit Design) **May 2024**
Arizona State University **GPA: 3.70/4**
Relevant Coursework: *VLSI Design, Digital System Circuits, Constructionist Approach to Microprocessor Design, Analog Integrated Circuits, Computer Architecture, VLSI Architecture, Fundamentals of CMOS and MEMs.*

BACHELOR'S IN ENGINEERING IN ELECTRONICS AND COMMUNICATION ENGINEERING **August 2019**
Dayananda Sagar College of Engineering **GPA: 8.6/10.0**
Relevant Coursework: *Digital CMOS VLSI circuits, Signals, and Systems, Analog communications, Fundamentals of Analog VLSI design, Embedded systems design, VLSI Lab, Digital system design using Verilog, Microcontrollers, HDL Lab.*

PROFESSIONAL EXPERIENCE

Software Engineer **KPIT Technologies Limited** **February 2020 – July 2022**

- Toyota Motor Corporation: Worked closely with offshore teams at Magna Electronics, Japan to develop TMC rear camera and all-around sensor display HMI software on Vector AUTOSAR stack.
- Worked closely with the customer to understand the new change requests for the software and implement them.
- Specifically responsible for the HMI's voice recognition and camera washer feature. Also maintained a few variants of the SW by defect fixing and unit testing.

SKILLS

EDA Tools: Cadence: Virtuoso, Spectre, Innovus, Synopsys: Design Compiler,VCS, Hspice; Mentor Graphics: Calibre (DRC, LVS), Catapult, ModelSim

Programming Languages: C/C++, SystemC, Python, Verilog, SystemVerilog, UVM Framework(1.2), Labview, SystemC, Matlab.

PROJECT EXPERIENCE

ASIC Acceleration for Graph Convolutional Neural Networks (GCNs) **EEE525**
Arizona State University

- Designed a three-staged graph convolutional network using Verilog. Synthesized the design using Design Complier and performed APR using innovus. Performed functional verification at each design stage. (RTL, post Synthesis, post-APR).
- Performed LVS and DRC checks to ensure there are no violations. Latency=20ns, Power= 27.93mW

Design of 4-bit mirror adder architecture(RTL to GDSII flow) **EEE 425/591**
Arizona State University

- Designed an optimized 4-bit adder that has a minimal area, power, and delay. Performed the layout of the same in Virtuoso Layout editor.
- Performed DRC and LVS checks to ensure there are no violations. Area=31.39um2, Delay=108ps.

Developed Universal Verification Components for YAPP_PACKETS (YAPP: Yet Another Packet Protocol)
Arizona State University

- Created a YAPP packet using UVM library. Created a driver, a simple sequencer, and a simple monitor.
- Created a driver to build the above three components. Also encapsulated all the components into UVC top level.
- Build and connect methods to create and join hierarchy. Instantiated the UVC in testbench and generated packets and viewed the log files.

Static Timing Analysis Implementation using STL in C++

- Static Timing Analysis was performed to find the delays of the logical circuits present in the "ISCAS'85 High-Level benchmark Models". Worst case run time of 0.12s and 0.43s was achieved for c17 and c7552 benchmark files respectively.
- The arrival time, slew and slack of every gate was computed and the critical path was found and tested in C++.

Generated UVM sequences

- Declared YAPP sequences for various stimulus goals: simple, nested, property controlled, and directed.
- Leveraged UVM factory and override functions to modify default behavior.
- Developed tests for dynamic packet generation.

Developed verification components for a 4-port switch design **EEE591**
Arizona State University

- A SystemVerilog project was developed, utilizing randomization, conditional constraints, inheritance, and polymorphism to create packets and enhance the design. Validation was conducted using xrun, and an infrastructure for the verification component was established using aggregate classes.
- The functionality of the verification component was verified with the Design Under Test (DUT) through an interface. After successful validation for a single port, the design was expanded by creating three additional instances of the switch and conducting further testing.

RESEARCH

Arizona State University

- Presently, I am engaged in the field of High-Level Synthesis (HLS) utilizing System C and Matchlib libraries, under the guidance of Professor Jeff Zhang. The project's focus involves creating an accelerator through HLS using System C.