



nucurrent
ADVANCED WIRELESS POWER

Getting Started with Slotted Power Development Kit

Rev 1.1

23-Sep-2020

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2 Revision History

Revision	Description	Date
1.0	Initial Draft	8/06/2020
1.1	Ki FW Support	9/23/2020

3 Purpose

The purpose of this document is to describe the basic setup and operation of the NuCurrent Slotted Power Development Kit, SPDK.

The NuCurrent SPDK is targeted for medium to high power applications that require simultaneous NFC communication and wireless power transmission. The kit is designed for OEMs developing both Wireless Power Consortium (WPC) Qi Cordless Kitchen Standard (Ki) and Medium Power Standard applications.

For more information on either of these standards, please see the WPC website: www.wirelesspowerconsortium.com.

4 What is included in the NuCurrent SPDK?

Hardware	Key Features / Functionality	Qty
NFC Core Module (NC03-T228M01-PCBA-P0B)	Supports NFC communication via NXP® PN7362. The Core Module supports: 1) Bi-directional data transfer 2) Output power levels up to 500mW	2
NFC Power Amplifier (NC03-T230M01-PCBA-P1C)	1) Receives DC power ($4.5V \leq V_{\text{Digital}} \leq 5.5V$, $5V \leq V_{\text{PA}} \leq 24V$) 2) Supplies 5V power to T228M, Core Module 3) Amplifies the standard NFC power & data from the Core Module from 500mW to >2.5W. 4) Transmits amplified NFC power and data to NFC coil. 5) Receives and passes NFC data from NFC coil to Core Module	1
NFC Power Harvester (NC03-R229M01-PCBA-P1B)	1) Receives wireless power at 13.56MHz. 2) Converts power to DC 3) Regulates and delivers up to 1.25W of DC power.	1
21cm TX Coil (NC03-T237K32-PCBA-P1A)	21 cm NFC transmit coil, based on Ki “Black Dot” 6/7/8.	1
8cm RX Coil (NC03-R237K23-PCBA-P1A)	8 cm NFC receive coil, based on Ki “Black Dot” 1	1
Generic Tuning Board (NC03-T237K40-PCBA-P1A)	Generic tuning board, used for connecting customer coil to NuCurrent SPDK.	2

5 Hardware Setup

The following section describes the initial hardware setup steps required for the NuCurrent SPDK.

5.1 Power Amplifier

The Power Amplifier system is composed of the following:

1. NC03-T230M01-PCBA-P1C, Power Amplifier (qty 1)
2. NC03-T228M01-PCBA-P0B, Core Module (qty 1)

The primary function of the Core Module is for modulating and demodulating the communication signals. The primary function of the Power Amplifier is to increase the power out levels from the Core Module from ~500mW to over 2.5W. The NuCurrent SPDK ships with the Core Module already installed into the Power Amplifier, and requires no customer actions.

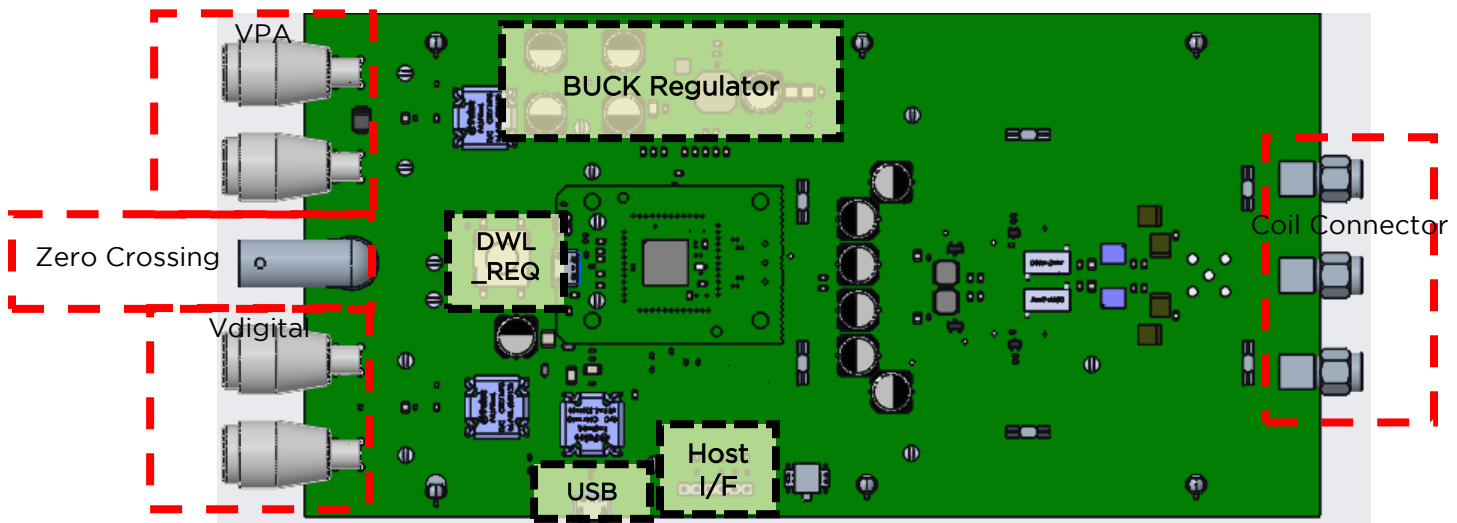


Figure 1: Power Amplifier Interface Location

5.1.1 Board Configuration

The following section describes the customer configurable areas of the Power Amplifier design.

5.1.1.1 Power In

Power connections for the Power Amplifier is accomplished via the standard 4mm banana jacks located on the left side of the PCB, see Figure 1

5.1.1.1.1 Vdigital

The Core Module (PN7362) only requires a single input voltage of 5V +/- 0.5V. The current requirement on Vdigital is ~500mA. Therefore, it is recommended that the power supply for Vdigital is set to 5V, 1A.

5.1.1.1.2 VPA

The discrete differential class E power amplifier resident on the T230M Power Amplifier board is designed to support various supply voltage levels. Voltage to the class E can be supplied in 2 methods:

5.1.1.1.2.1 Banana plugs (AS SHIPPED)

As shipped from NuCurrent, power from the banana plugs is routed directly to the discrete differential class E amplifier. This is accomplished by:

1. Remove jumper on HDR300, see Figure 2
2. Remove jumper on HDR301, see Figure 2
3. Install jumper wire from HDR300 pin 1 to HDR301 pin 2, see Figure 2

NOTE: Power on banana plug is connected directly to the class E differential amplifier, and can be set / adjusted by the user.

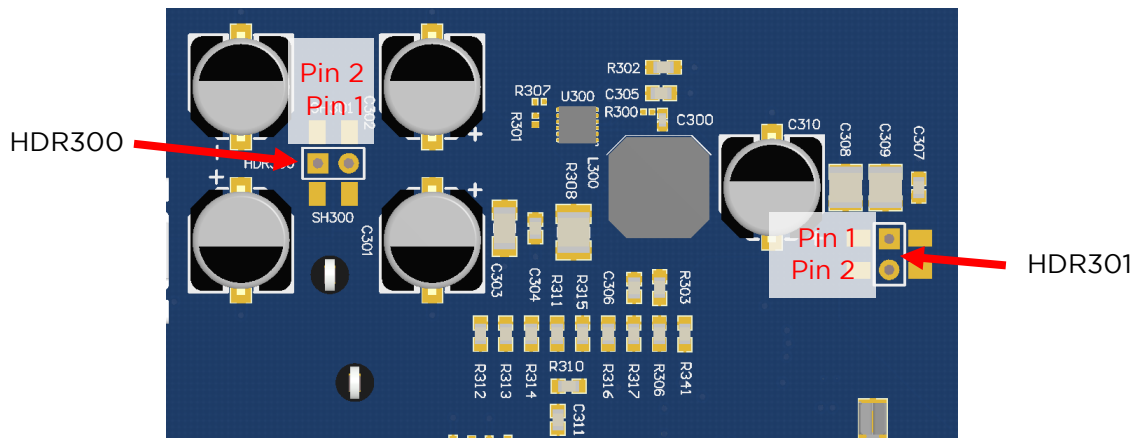


Figure 2: PA BUCK Circuit

5.1.1.1.2.2 On-board BUCK regulator.

The power amplifier board also contains a LMR23615 Buck regulator, that is capable of producing output voltages between 6.1V and 19.5V. Use of the on-board regulator REQUIRES use of:

1. NuCurrent Ki FW, version **<TBD>** or greater.
2. Voltage on VPA banana plugs of 24V.

The following hardware configuration are also required to use the on-board regulator.

1. Remove jumper wire from HDR300 pin 1 to HDR301 pin 2, Figure 2
2. Install jumper on HDR300, see Figure 2
3. Install jumper on HDR301, see Figure 2

NOTE: Power on banana plug is connected to an on-board LMR23615 regulator, and can only be set / adjusted via FW.

5.1.1.2 Zero Crossing (Comm Valid)

In a full Ki® system, the “Zero Crossing” or “Communication Valid” signal is an INPUT to the Power Amplifier, and is used to indicate when the High Power / Low Frequency field is OFF, and the NFC Slotted Power subsystem can transmit / receive data. In the NuCurrent SPDK, the Zero Crossing signal connection is made on a BNC connector, see Figure 1

This signal is captured at the GPIO number 7 on the Core Module (PN7362).

The electrical characteristics of the Zero Crossing (Comm Valid) signal are:

- Connection Type: BNC
- Voltage Level: 0V - 3.3V

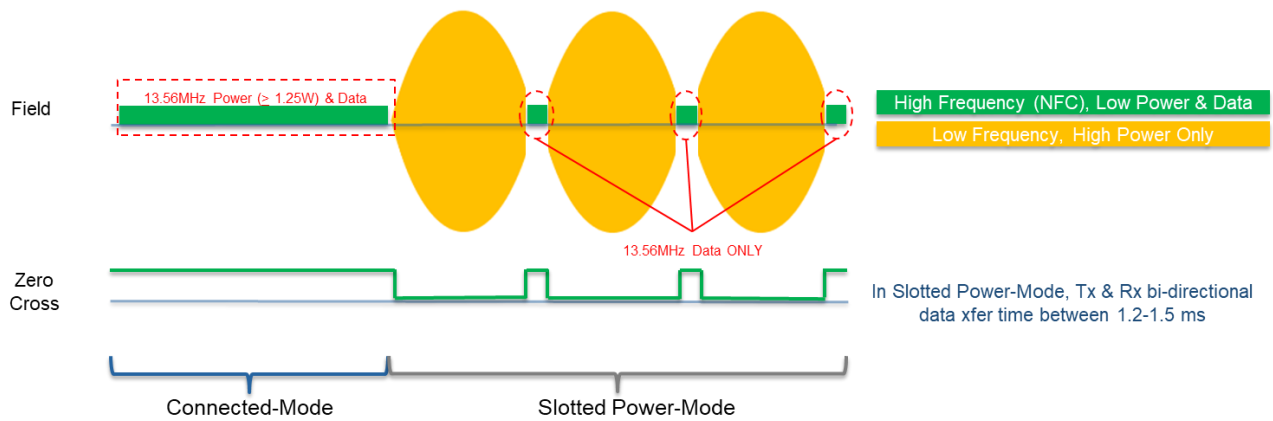


Figure 3: Slotted Power Field Sequence

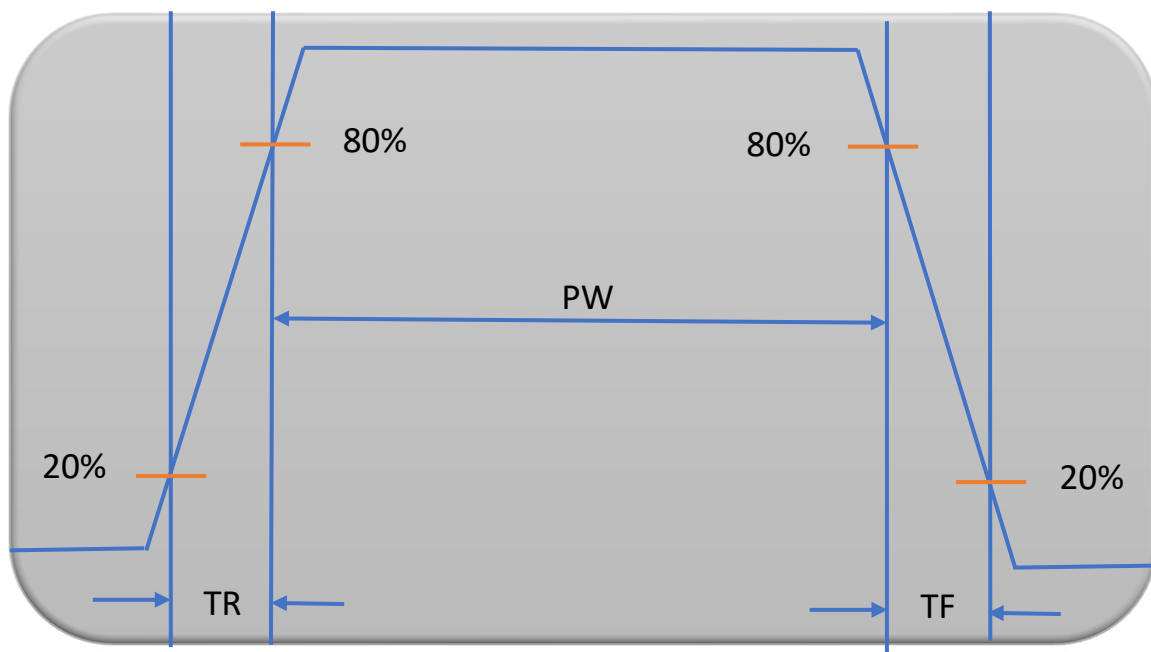


Figure 4: Trigger Signal Waveform

Timings	Time	Comment
TR (Rise Time)	Min: 1.0ns Max: 3.5ns	This is the rise time of the trigger signal. The Power Transmitter can turn on the 135.56MHz field when the trigger signal reaches 80% of its active high voltage.
PW (Pulse Width)	1500μs	The pulse width (end of rising time until start of falling time) shall be at least 1500μs and represents the time slot for the Slotted NFC Communications.
TF (Fall Time)	Min: 1.0ns Max: 3.5ns	This is the fall time of the triggering signal. The Power Transmitter must initiate turning off the 13.56MHz field when this signal reaches 80% of its active high voltage.

5.1.1.3 Coil / Antenna

The NuCurrent SPDK utilizes SMA connectors to allow maximum flexibility of coil connections. The SPDK ships with 2 coils that represent the size and shape the end customer would expect to see in a Slotted Power application.

To ensure proper operation, the coil connections must be fully tightened to 80–120 N·cm. NuCurrent recommends the use of Radiall 8mm torque wrench ([R282.320.000](https://www.radiall.com/en/produit/8mm-torque-wrench)), for tightening SMA connectors.



Figure 5: PA Coil Connector

5.1.1.4 Host Interface

The NuCurrent SPDK host interface is available on header J250, a 6 pin, 100-mil header, located at the bottom of the Power Amplifier board (see Figure 1). The following hardware interfaces are options (but not are all supported in FW):

Table 1: PA Host I/F Support

HW Interface	Settings	Firmware Support
UART (2/4-wire)	460,800. 8-N-1	Supported
	115,200, 8-N-1	Not Supported
SPI	TBD	Not Supported
I2C	100/400kHz	Not Supported
USB slave	12Mbps	Not Supported

5.1.2 Mounting in the Fixture <Optional>

These optional fixtures were designed to:

- Provide a consistent user experience by fixing & flattening the large 21 cm diameter coil, NC03-T237K32-PCBA-P1A.
- Reduce stress on coil PCB, specifically at the SMA connectors.
- Reduce stress on the Power Amplifier PCB, specifically at the SMA connectors.

Below are the detailed assembly instructions.

- 1) Place the TX coil, NC03-T237K32-PCBA-P1A, onto the Base

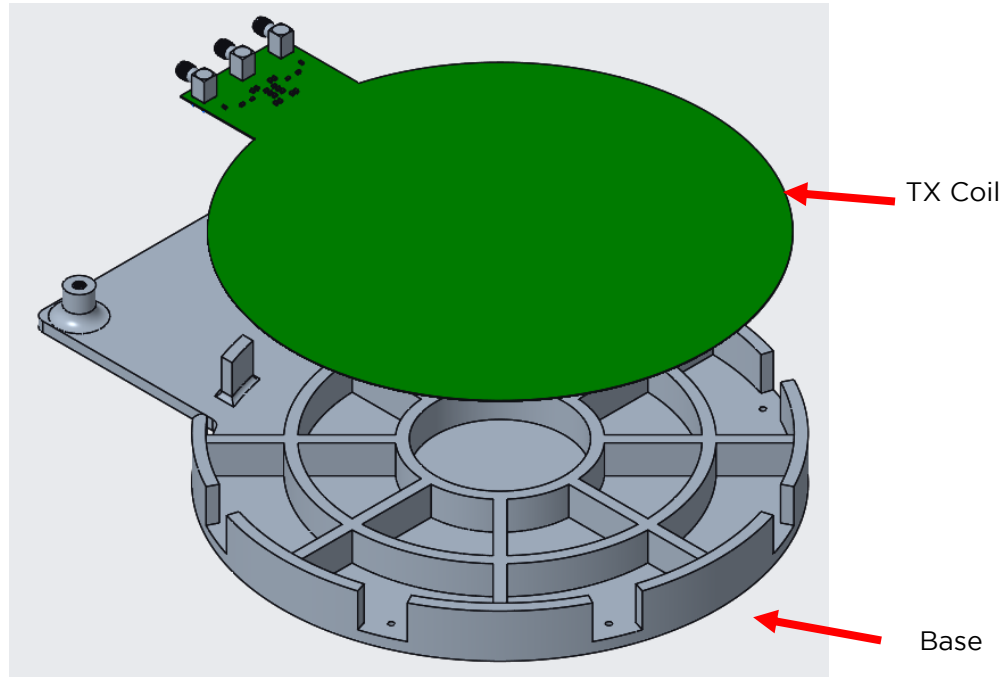


Figure 6: PA Fixture + Coil

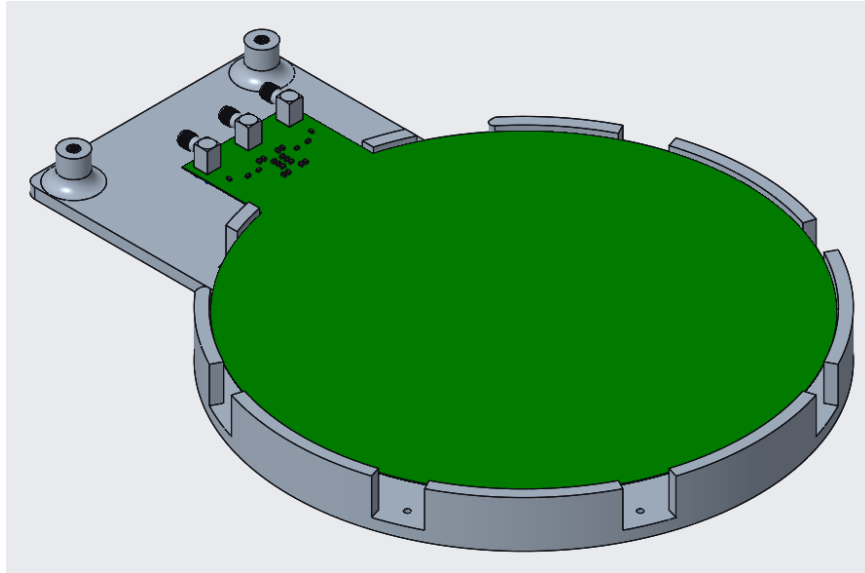


Figure 7: PA Fixture Coil Seated

- 2) Slide the 6 clamps into the cutout region of the base and screw it using M2x8mm screws.

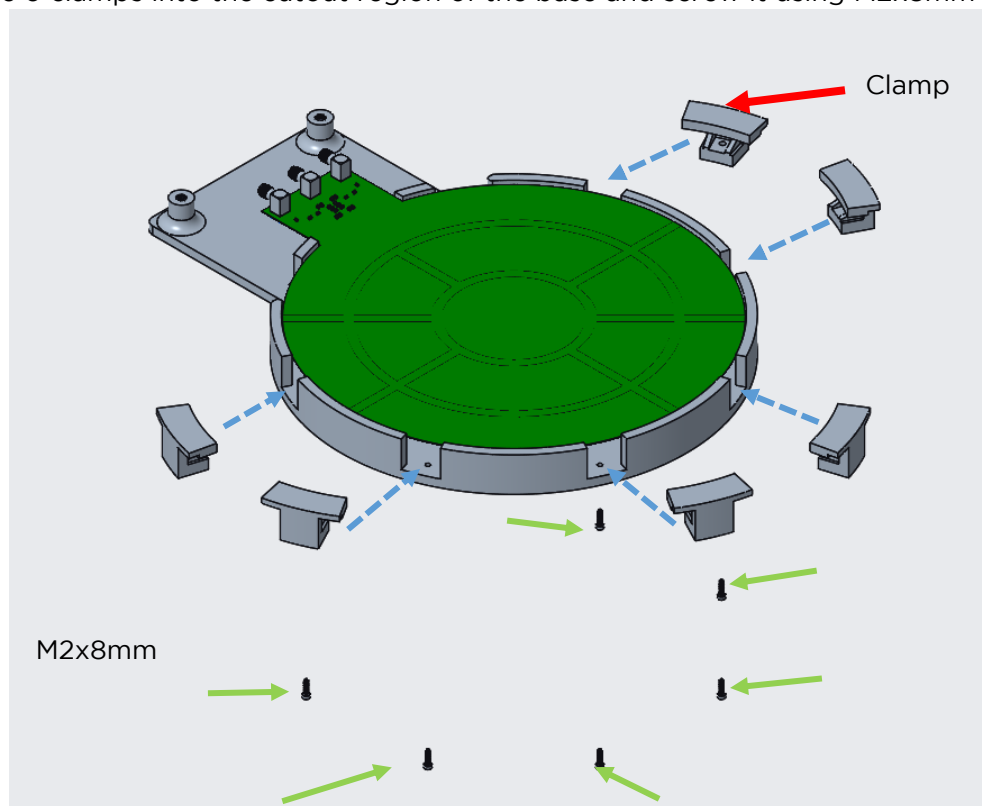


Figure 8: PA Fixture Clamp Assy

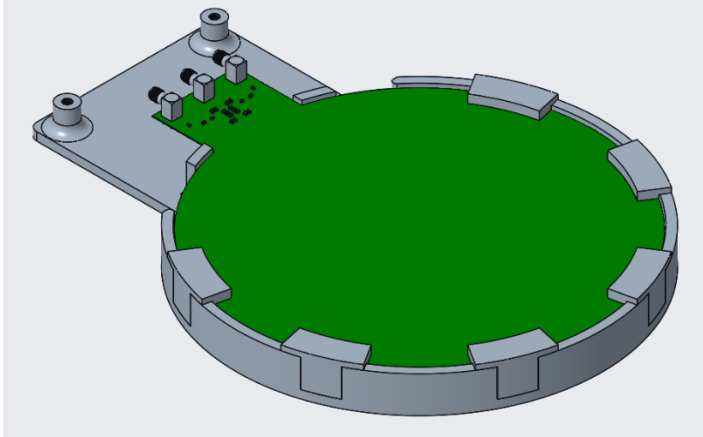


Figure 10: PA Fixture Coil Assembled TOP

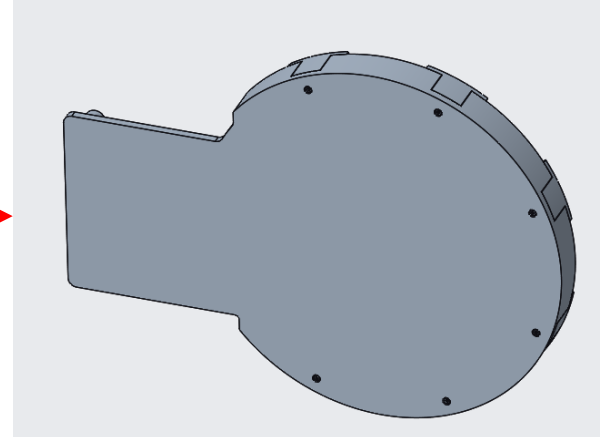


Figure 9: PA Fixture Coil Assembled BOTTOM

- 3) Assemble 4 stand-offs at the back 4 through holes of the TX PCBA.
- 4) Connect the TX coil to the TX PCBA, screw the TX PCBA and the base at the front 2 through holes using M3.5x8mm screws.

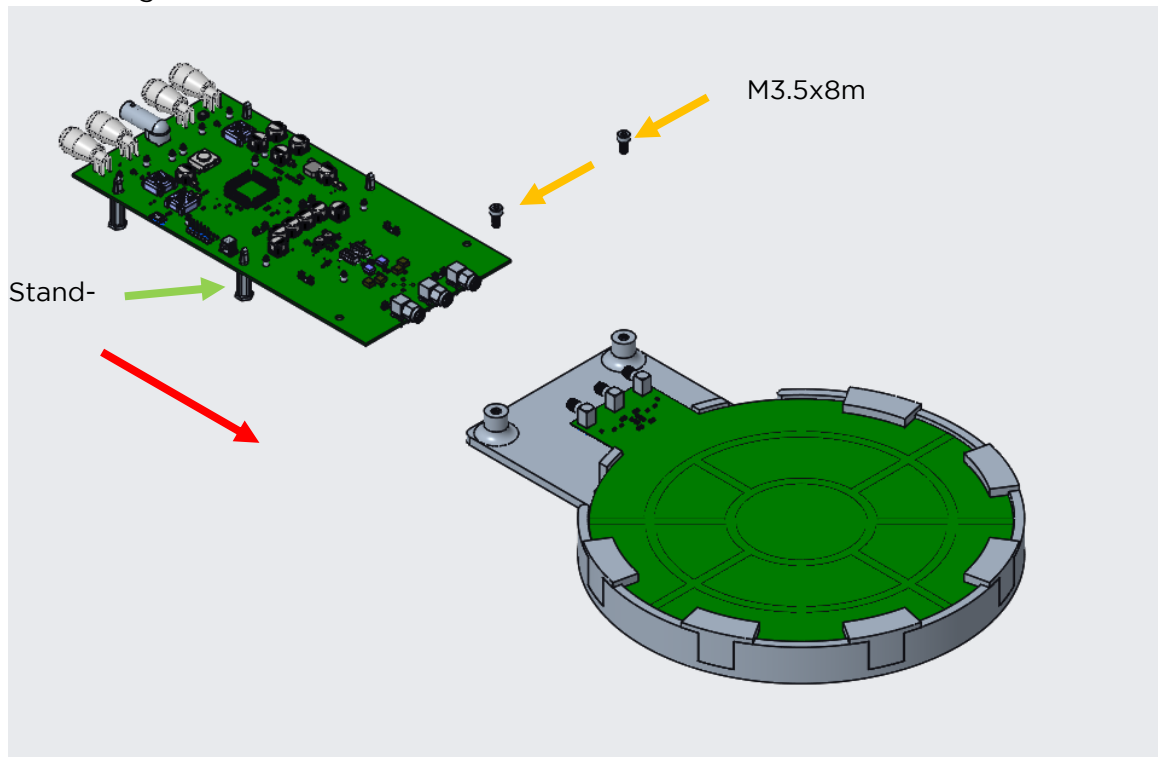


Figure 11: PA Fixture Coil Connection

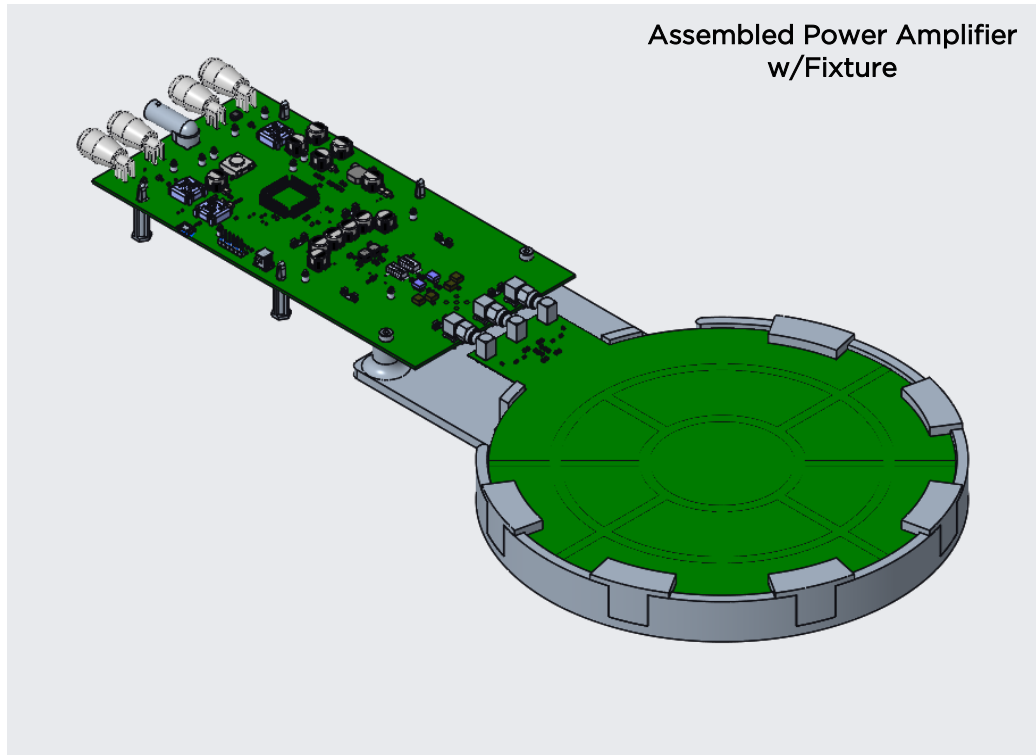


Figure 12: PA Fixture Fully Assembled

5.2 Power Harvester

The Power Harvester system is composed of the following:

1. NC03-R229M01-PCBA-P1B, Power Harvester (qty 1)
2. NC03-T228M01-PCBA-P0B, Core Module (qty 1)

The primary function of the Core Module is for modulating and demodulating the communication signals. The primary function of the Power Harvester is to harvest, rectify and regulate the 13.56MHz wireless power and deliver up to 1.25W of 5V DC power. NOTE: The Power Harvester has been optimized for 1.25W, but may provide higher power based on the transmitted power and efficiency.

The NuCurrent SPDK ships with the Core Module already installed into the Power Harvester, and requires no customer actions.

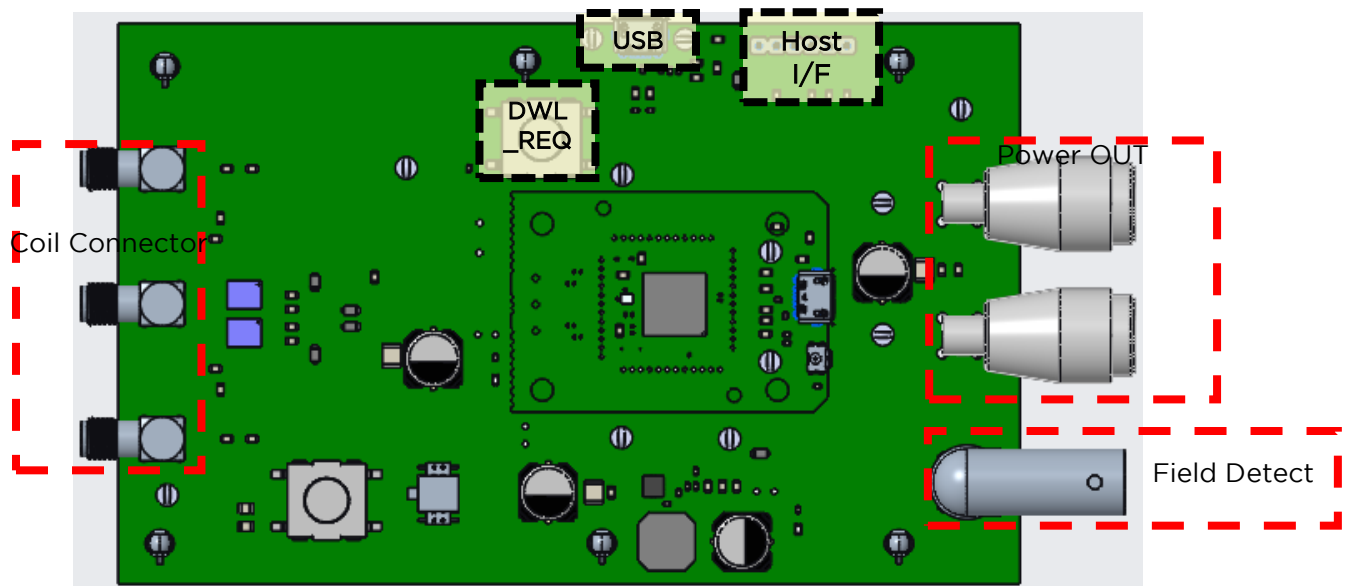


Figure 13: Power Harvester Interface Location

5.2.1 Board Configuration

The following section describes the customer configurable areas of the Power Harvester portion of the NuCurrent SPDK.

5.2.1.1 Power Out Connections

When the Power Harvester assembly is in the presence of the magnetic field provided by the Power Amplifier assembly, the Power Harvester provides a fixed 5V DC voltage @ 250mA (1.25W).

5.2.1.2 Field Detect

In a full Ki® system, the “Field Detect” signal is an OUTPUT from the Power Harvester, and is used to indicate when the Power Harvester is in the presence of a wireless field operating at 13.56MHz. In the NuCurrent SPDK, the Field Detect signal connection is made on a BNC connector, see Figure 13.

This signal is captured by GPIO number 7 on the Core Module (PN7362).

The Field Detect signal indicates when the Power Harvester system is in the presence of a 13.56MHz signal, with enough energy to power up the Core Module (PN7362).

The electrical characteristics of the Field Detect signal are:

- Connection Type: BNC
- Voltage Level: 0V - 3.3V
- Rise / Fall Time: <1mS

5.2.1.3 Coil / Antenna

See 5.1.1.3.

5.2.1.4 Host Interface

The NuCurrent SPDK host interface is available on header J760, a 6 pin, 100-mil header, located in the Top Right area of the Power Harvester board (see Figure 13). The following hardware interfaces are options (but not are all supported in FW):

Table 2: Power Harvester Host I/F Support

HW Interface	Settings	Firmware Support
UART (2/4-wire)	460,800, 8-N-1	Supported
	115,200, 8-N-1	Not Supported
SPI	TBD	Not Supported
I2C	100/400kHz	Not Supported
USB slave	12Mbps	Not Supported

5.2.2 Mounting in the Fixture <Optional>

These optional fixtures were designed to:

- Provide a consistent user experience by fixing & flattening the 8 cm diameter coil, NC03-R237K23-PCBA-PIA.
- Reduce stress on coil PCB, specifically at the SMA connectors.
- Reduce stress on the Power Harvester PCB, specifically at the SMA connectors.
- Ensure a minimum of 1.2 cm of Z distance between the TX and RX coil.
- Provide a method for quickly and repeatably testing at either 1.2 cm or 4.0 cm coil-to-coil distances.

Below are the detailed assembly instructions.

- 1) Assemble the 4 stand-offs (2 at the middle and 2 at the rear through holes) to the Power Harvester PCBA
- 2) Connect the RX coil to the Power Harvester PCBA

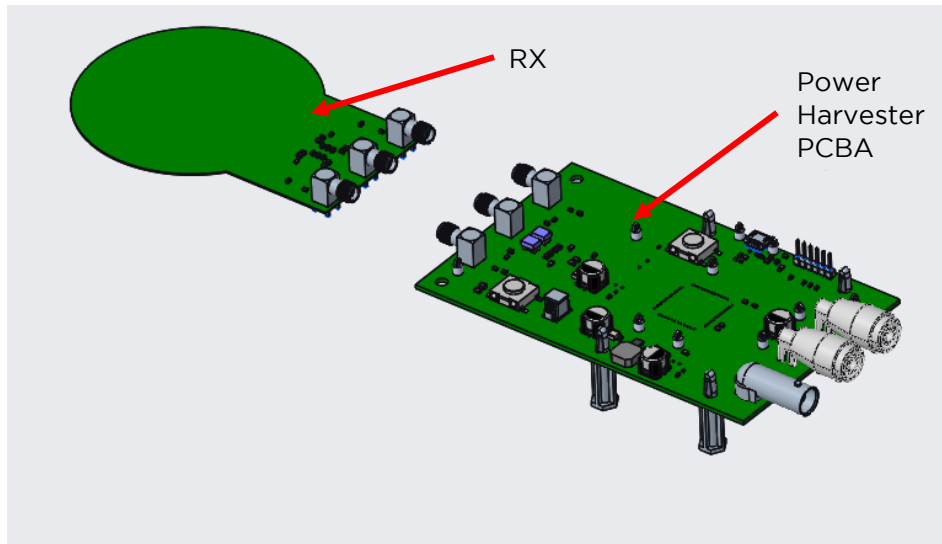


Figure 14: PH Fixture Coil & Standoffs Assy

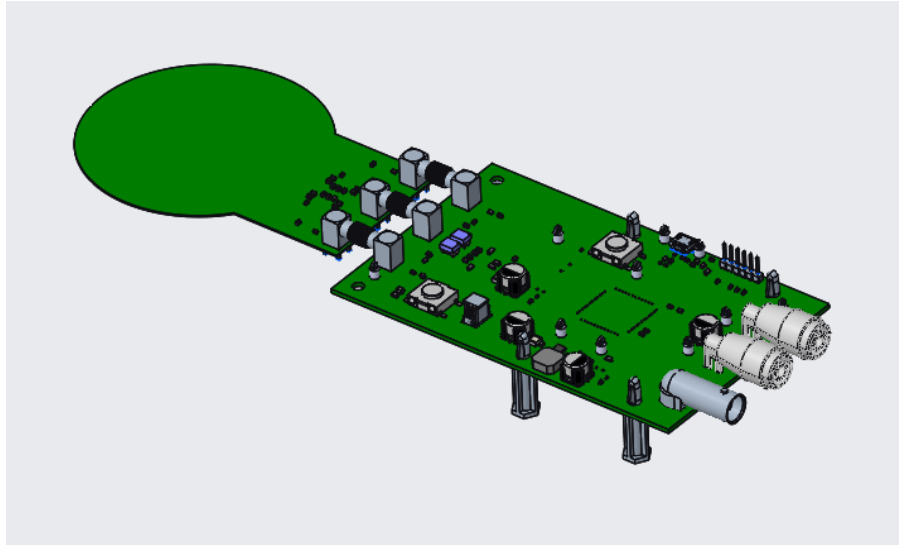


Figure 15: PH Fixture Coil & Standoffs Assembled

- 3) Slide the spacer underneath the RX coil and place the 2 bosses under the RX PCBA such that they are lined up with the front 2 through holes of the RX PCBA.
- 4) Screw the spacer to the RX PCBA using M3.5mmx8mm screw.

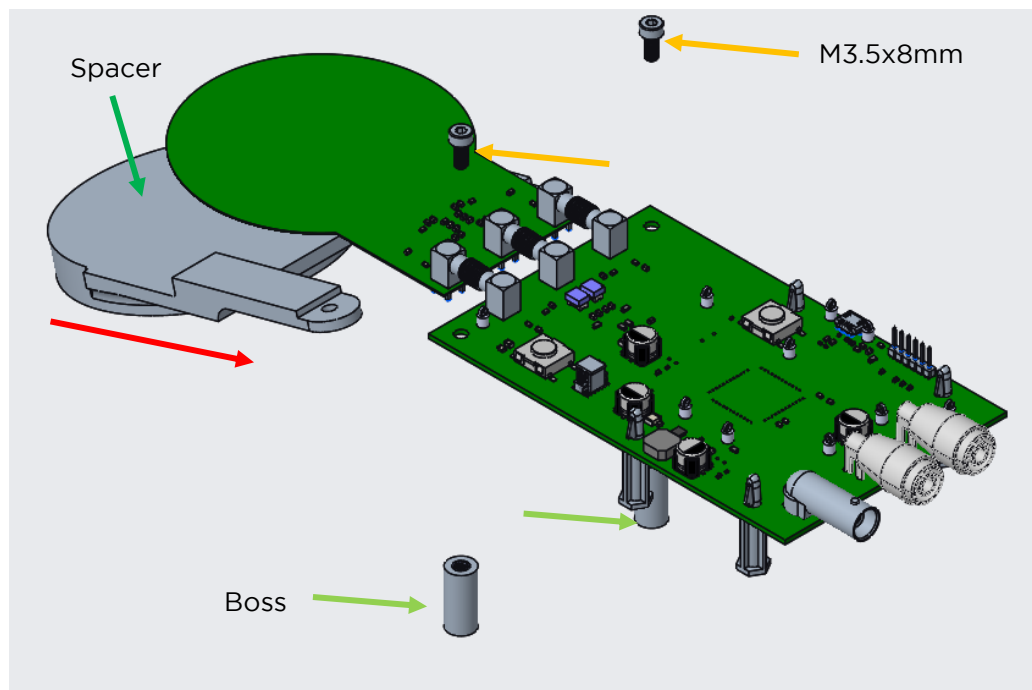


Figure 16: PH Fixture Spacer & Boss Assy

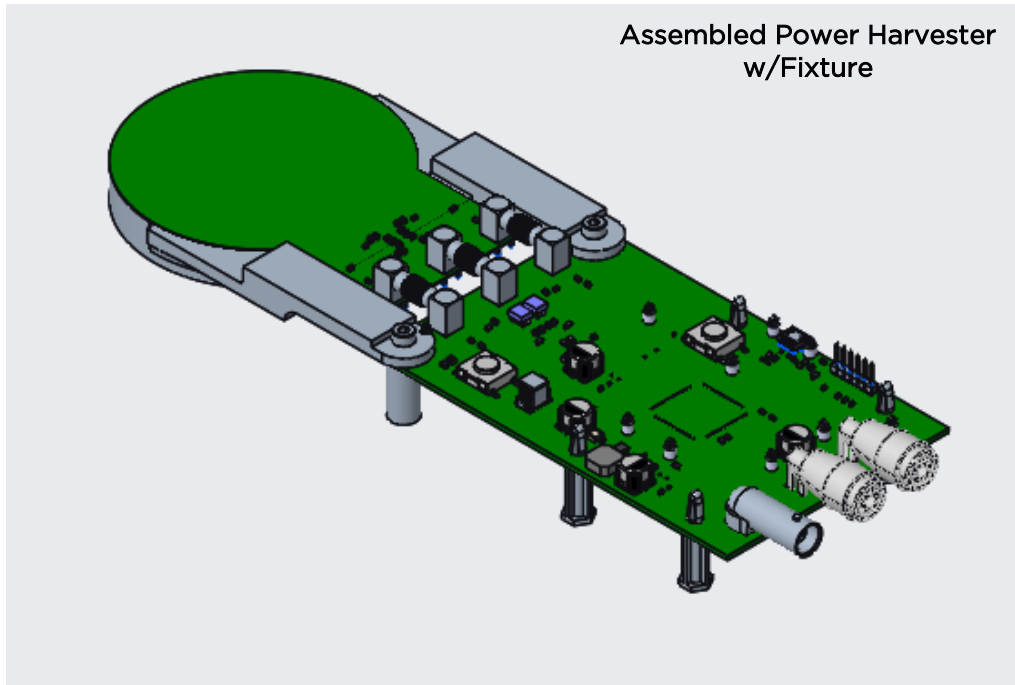


Figure 17: PH Fixture Fully Assembled

- 5) Place the assembled RX system on top of the spacer (1.2cm or 4cm).

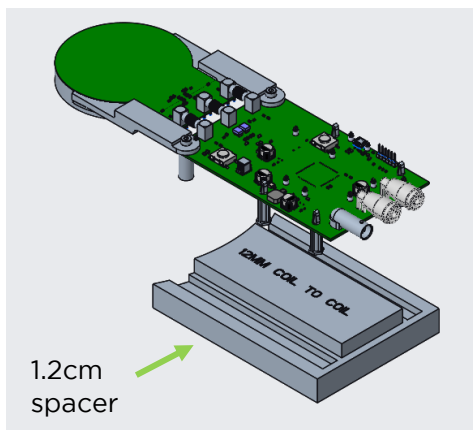


Figure 18: PH 1.2cm Spacer Assy

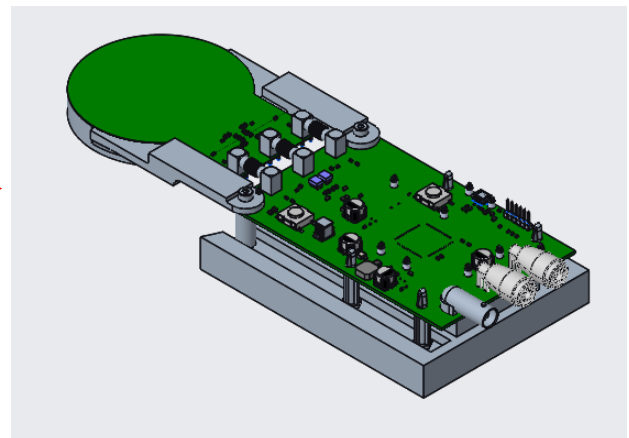


Figure 19: PH 1.2cm Spacer Assembled

6 Programming Firmware

The PN7362 requires 2 binary images for proper operation: EEPROM & Application.

The EEPROM image contains parameters used for configuring the PN7362 HW, as well as FW configurable parameters.

The Application image contains the code for high-level features, i.e. NFC stack, Host Interface, Command Parser, etc.

There are 2 approved methods for programming Firmware into the NuCurrent SPDK:

- 1) USB (Preferred method for Ki FW)
- 2) Serial Wire Debug, SWD via J-Link Commander

6.1 USB Download Mode

The NFC Core Module can enumerate as a USB mass storage device thru use of the DWL_REQ button (see Figure 1 / Figure 13).

The following procedure is used for programming using USB D/L mode:

- 1) Remove ALL power to Power Amplifier
- 2) Disconnect Host Interface connections, i.e. UART/Serial.
- 3) Depress and hold DWL_REQ button
- 4) Insert USB data cable

In Windows®, a USB mass storage device should appear (see Figure 20).

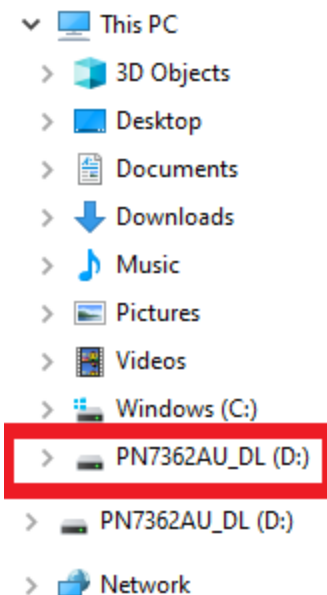


Figure 20: Windows USB Mass Storage Device

- 5) Erase EEPROM image
 - a. DELETE DRP_00.DAT

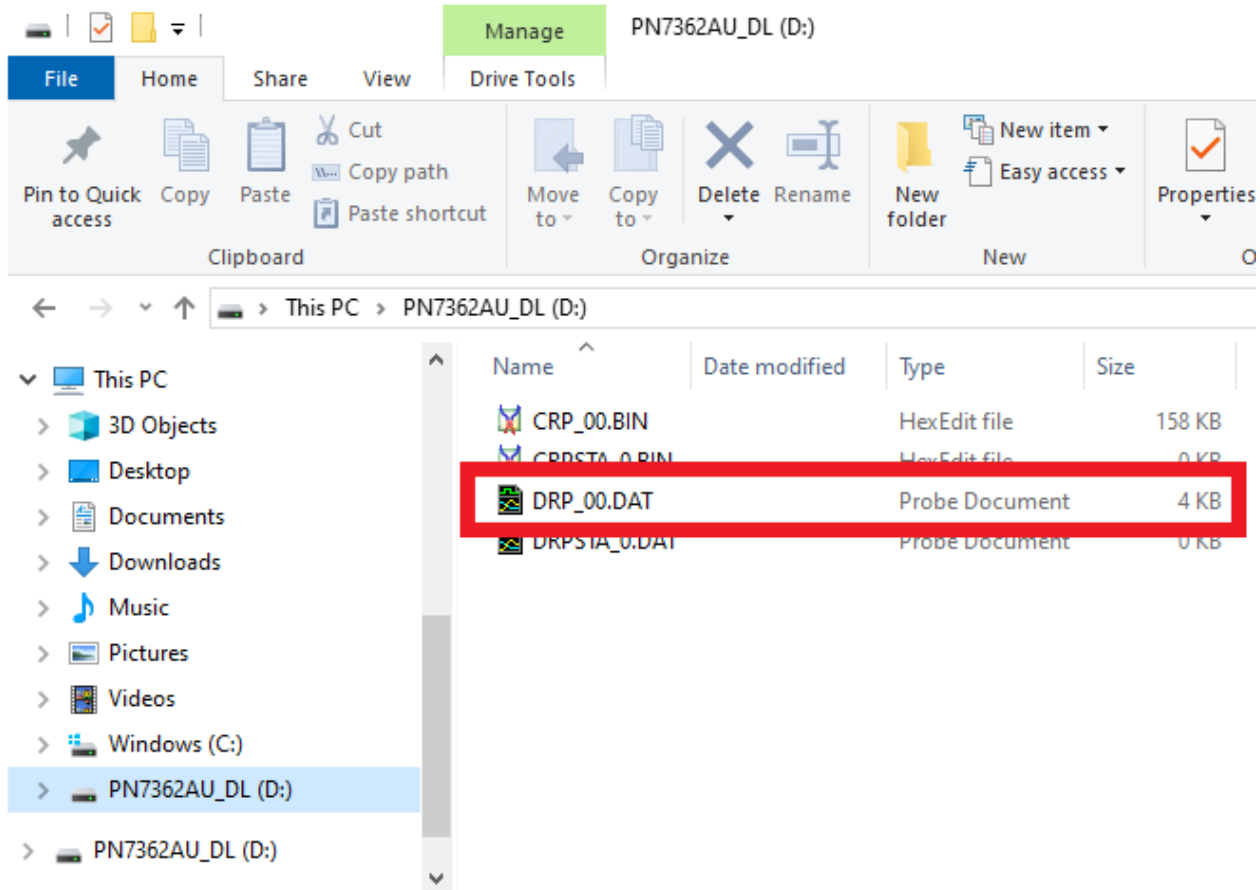


Figure 21: USB Mass Storage - EEPROM Image

- 6) Program EEPROM image
 - a. Copy **<EEPROM>.bin** to D:\.
 - b. NOTE: Windows Explorer should restart when copy to D:\ is complete. This is expected behavior.
 - c. NOTE: PN7362 ROM code will automatically rename **<EEPROM >.bin** to DRP_00.DAT during the flashing process. Therefore, **<EEPROM>.bin** will “disappear”, and DRP_00.DAT will “appear” after the Window Explorer restart / PN7362 reboot.
- 7) Erase APPLICATION image
 - a. DELETE CRP_00.DAT

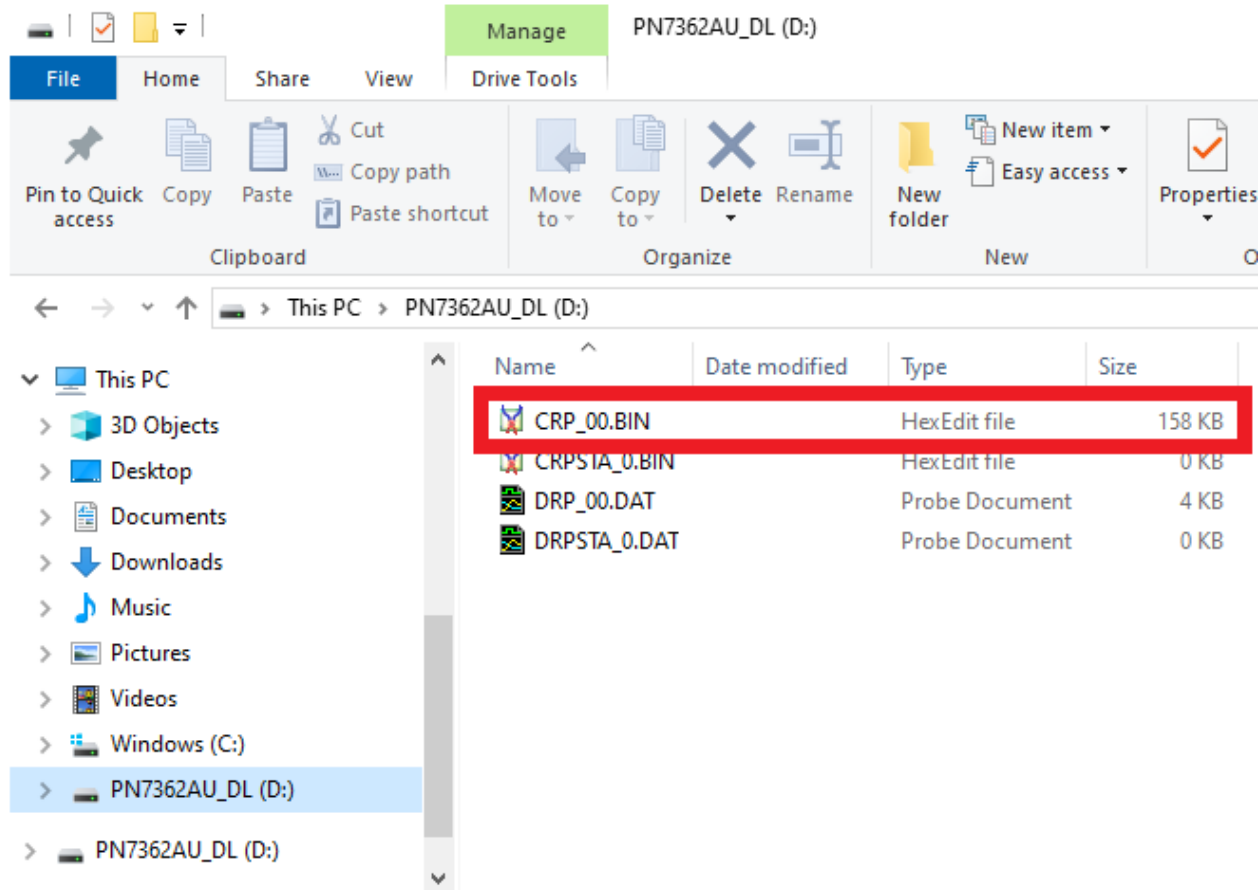


Figure 22: USB Mass Storage - Application Image

- 8) Program APPLICATION image
 - a. Copy **<application>.bin** to D:\.
 - b. NOTE: Windows Explorer should restart when copy to D:\ is complete. This is expected behavior.
 - c. NOTE: PN7362 ROM code will automatically rename **<application>.bin** to CRP_00.DAT during the flashing process. Therefore, **<application>.bin** will “disappear”, and CRP_00.DAT will “appear” after the Window Explorer restart / PN7362 reboot.
- 9) Remove USB data cable (REQUIRED to take Core Module out of USB D/L mode)

6.2 J-Link

J-Link EDU hardware & software is available through Segger @ <https://www.segger.com/products/debug-probes/j-link/models/j-link-edu/>. While there are no expected incompatibilities expected with different versions of J-Link HW and FW, NuCurrent has validated the following HW / FW version:

SEGGER J-Link Commander V6.12f (Compiled Jan 13 2017 16:38:21)

DLL version V6.12f, compiled Jan 13 2017 16:37:50

Firmware: J-Link V10 compiled Jan 7 2020 16:51:47

Hardware version: V10.10

S/N: <XXXXXXXXXX>

License(s): FlashBP, GDB

OEM: SEGGER-EDU

Figure 23: J-Link Version Information

6.2.1 J-Link Programming Procedure

Below is the procedure required for programming using J-Link.

- 1) Remove power to the target system
- 2) Connect J-Link programmer to PC.
- 3) Connect J-Link programmer to target system. (Connector P/N: FTSH-107-01-L-DV)

Table 3: J-Link Connector Pinout

<u>J-Link Sig Name</u>	<u>J-Link Pin #</u>	<u>NuCurrent SPDK Prog Conn Pin #</u>	<u>Target Sig Name</u>
VDD	1	9	VDD
VDD	2	9	VDD
GND	3	8	GND
GND	4	8	GND
GND	5	8	GND
GND	6	8	GND
SWD_DIO	7		NFC_SWD_IO
GND	8	8	GND
SWD_CLK	9		NFC_SWD_CLK
GND	10	10	GND
Not Connected	11		
GND	12	10	GND

<u>J-Link Sig Name</u>	<u>J-Link Pin #</u>	<u>NuCurrent SPDK Prog Conn Pin #</u>	<u>Target Sig Name</u>
Not Connected	13		
GND	14	10	GND
Reset_N	15	3	NFC_RSTn
GND	16	10	GND
Not Connected	17		
GND	18	10	GND
Not Connected	19		
GND	20	10	GND

- 4) Apply power to Core Module
 - a. Option A: Insert USB data cable
 - b. Option B (Power Amplifier ONLY): Apply 5V/1A to Vdigital
- 5) Launch J-Link Commander

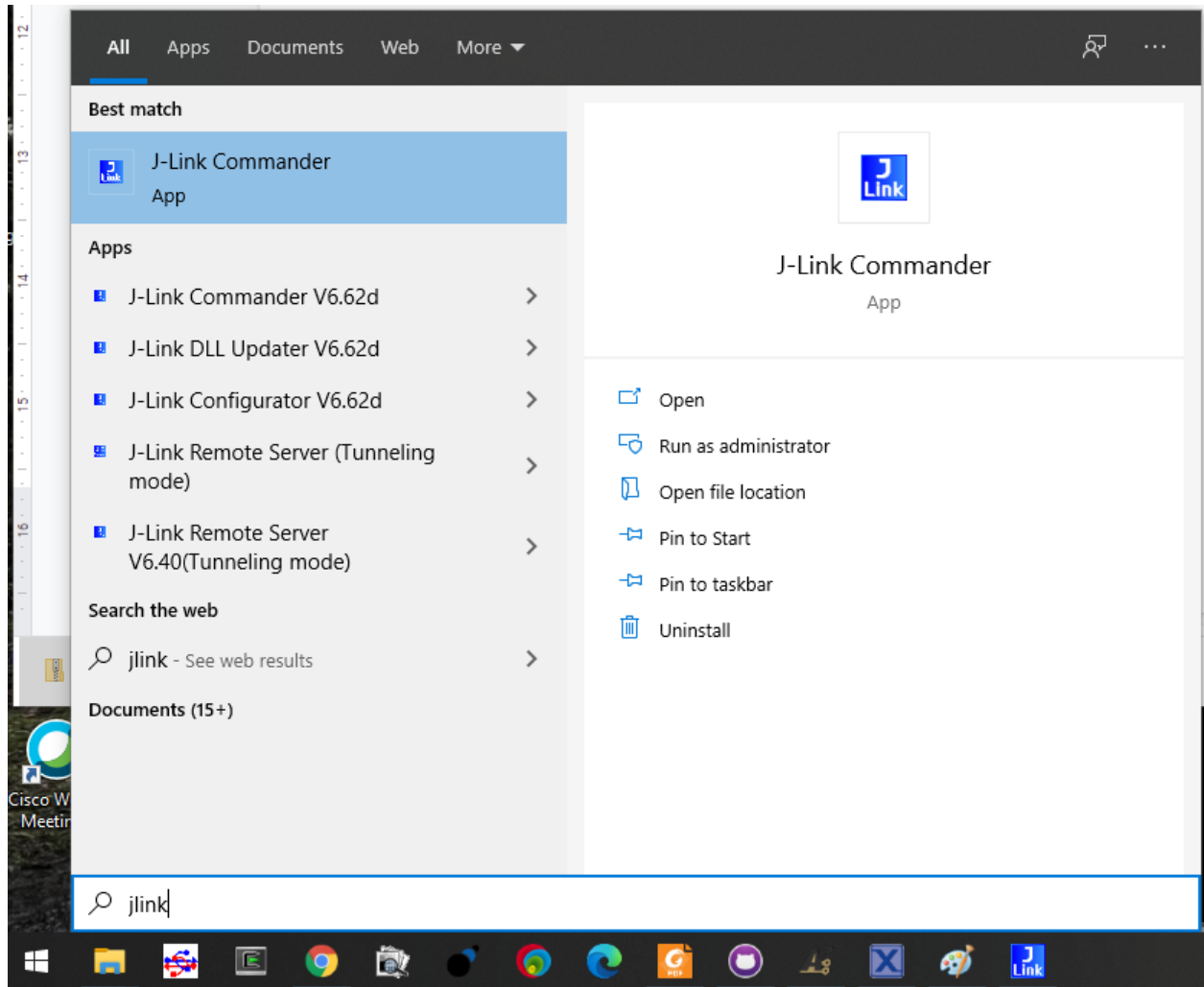


Figure 24: J-Link Commander

- 6) Set interface = SWD
 - a. Type "si swd"
- 7) Set device = PN7362
 - a. Type "device PN7362AU"
- 8) Set target interface speed = 4000
 - a. Type "speed 4000"
- 9) Connect to to target
 - a. Type "connect"
- 10) Halt the target
 - a. Type "h"
- 11) Program the EEPROM binary image.
 - a. Type "loadbin <full dir path>\<EEPROM>.bin,201200"
- 12) Program the APPLICATION binary image.

- a. Type "loadbin <full dir path>\<APPLICATION>.bin,203000"
- 13) Reset the target
 - a. Type "r"
- 14) Run the target
 - a. Type "g"
- 15) Exit J-Link Commander
 - a. Type "exit"

6.2.2 J-Link Expected Output

Table 4: J-Link Expected Output

Step	J-Link Commander Terminal
1	SEGGER J-Link Commander V6.12f (Compiled Jan 13 2017 16:38:21) DLL version V6.12f, compiled Jan 13 2017 16:37:50 Connecting to J-Link via USB...O.K. Firmware: J-Link V10 compiled Jan 7 2020 16:51:47 Hardware version: V10.10 S/N: 260109954 License(s): FlashBP, GDB OEM: SEGGER-EDU VTref = 4.900V Type "connect" to establish a target connection, '?' for help
2	J-Link> si swd Selecting SWD as current target interface.
3	J-Link> device PN7362AU
4	J-Link> speed 4000 Selecting 4000 kHz as target interface speed
5	J-Link> connect Device "PN7362AU" selected. Found SWD-DP with ID 0x0BB11477 AP-IDR: 0x04770021, Type: AHB-AP AHB-AP ROM: 0xE00FF000 (Base addr. of first ROM table) Found Cortex-M0 r0p0, Little endian. FPUnit: 4 code (BP) slots and 0 literal slots CoreSight components: ROMTbl 0 @ E00FF000 ROMTbl 0 [0]: FFF0F000, CID: B105E00D, PID: 000BB008 SCS

	ROMTbl 0 [1]: FFF02000, CID: B105E00D, PID: 000BB00A DWT ROMTbl 0 [2]: FFF03000, CID: B105E00D, PID: 000BB00B FPB Cortex-M0 identified.
6	J-Link>h PC = FFFFFFFE, CycleCnt = 00000000 R0 = 00000000, R1 = 00030000, R2 = 00203000, R3 = 00000003 R4 = 00000004, R5 = 00030000, R6 = 000050C0, R7 = 00000001 R8 = 48008020, R9 = 04082084, R10= 009011C8, R11= 00020842 R12= 00000128 SP(R13)= FFFFFFFD8, MSP= FFFFFFFD8, PSP= 00102868, R14(LR) = FFFFFFF9 XPSR = C1000003: APSR = NZcvq, EPSR = 01000000, IPSR = 003 (HardFaultMemManage) CFBP = 00000000, CONTROL = 00, FAULTMASK = 00, BASEPRI = 00, PRIMASK = 00
7	J-Link>loadbin <full dir path>\<EEPROM>.bin,201200 Downloading file [<full dir path>\<EEPROM>.bin]... J-Link: Flash download: Flash programming performed for 1 range (2240 bytes) J-Link: Flash download: Total time needed: 0.128s (Prepare: 0.018s, Compare: 0.004s, Erase: 0.000s, Program: 0.102s, Verify: 0.000s, Restore: 0.002s) O.K.
8	J-Link>loadbin <full dir path>\<APPLICATION>.bin,203000 Downloading file [<full dir path>\<APPLICATION>.bin]... J-Link: Flash download: Flash programming performed for 1 range (67328 bytes) J-Link: Flash download: Total time needed: 1.324s (Prepare: 0.040s, Compare: 0.041s, Erase: 0.000s, Program: 1.215s, Verify: 0.004s, Restore: 0.022s) O.K.
9	J-Link>r Reset delay: 0 ms Reset type NORMAL: Resets core & peripherals via SYSRESETREQ & VECTRESET bit. NXP PN7 reset: Halting CPU before performing reset... NXP PN7 reset: Halted CPU before reset.
10	J-Link>g
11	J-Link>exit

6.3 NXP NFC Cockpit (As Shipped)

The NuCurrent SPDK ships with standard NXP NFC Cockpit FW pre-loaded into the Power Amplifier.

6.3.1 Power Amplifier (NFC Cockpit)

NXP NFC Cockpit is available @

<https://www.nxp.com/products/rfid-nfc/nfc-hf/nfc-readers/nfc-cockpit-configuration-tool-for-nfc-ics:NFC-COCKPIT>

NuCurrent ships the SPDK with the following FW images pre-installed:

Table 5: NuCurrent Power Amplifier FW Images

Power Amplifier - EEPROM	NxpNfcCockpit_28_00_00_EEPROM.bin
Power Amplifier - APPLICATION	NxpNfcCockpit_03_04_00_Flash.bin

6.3.2 Power Harvester (Card Emulator)

The NuCurrent SPDK, Power Harvester ships with the following images pre-installed:

Table 6: NuCurrent Power Harvester FW Images

Power Harvester - EEPROM	user_ee.bin
Power Harvester - APPLICATION	NfcrdlibEx8_HCE_T4T.bin

6.4 Ki Firmware

The NuCurrent SPDK can be loaded with NuCurrent provided firmware images that support the protocol requirements of the Ki eco-system.

6.4.1 Errata's

Version B0.00.01.00 of the NuCurrent Ki FW has the following known limitations that will be resolved in future releases:

	<u>Known Issue</u>
1	Zero Crossing positive duty cycle ≥ 2 ms.
2	Zero Crossing period limited to 10mS (50Hz emulation)
3	Data transfer in Power Transfer mode limited to 106 & 212Kbps
4	Payload size @ 106Kbps limited to 6 bytes
5	Full system power cycle required if Power Amplifier stops responding to NuCurrent Command-line utility

6.4.2 Power Amplifier

The NuCurrent SPDK Power Amplifier firmware binaries are available @ <https://github.com/NuCurrent/NFC-Slotted-Power-Dev-Kit>

Table 7: NuCurrent Power Amplifier FW Images

Power Amplifier - EEPROM	EEPROM_SPDK_T230M_vAlpha.bin
Power Amplifier - APPLICATION	Application_SPDK_T230M_vB0.00.01.00.bin

6.4.3 Power Harvester (Card Emulator)

The NuCurrent SPDK Power Harvester firmware binaries are available @ <https://github.com/NuCurrent/NFC-Slotted-Power-Dev-Kit>

Table 8: NuCurrent Power Harvester FW Images

Power Harvester - EEPROM	EEPROM_SPDK_R229M_vAlpha.bin
Power Harvester - APPLICATION	Applicaition_SPDK_R229M_vB0.00.01.00.bin

7 System Operation

7.1 Power Transfer

Here are the steps required to establish power transfer.

- 1) Place your assembled Amplifier module on a flat surface & connect a microUSB cable and power supply to your Amplifier as shown in Figure 25.

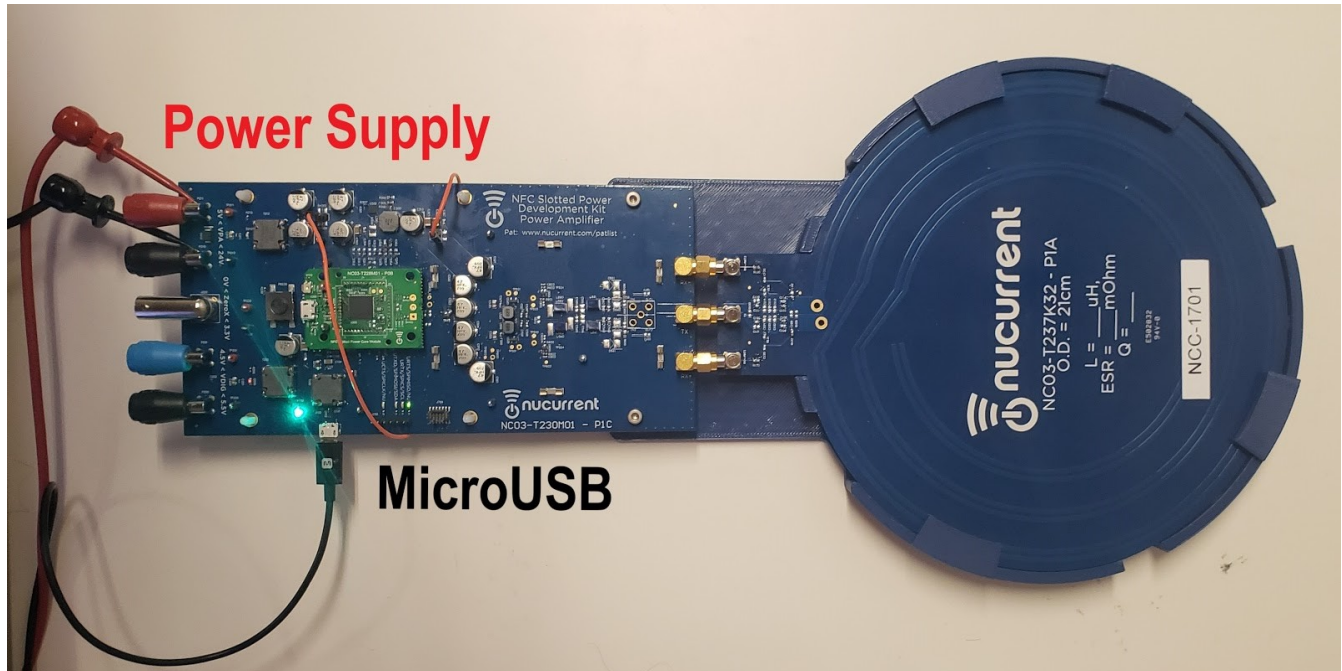


Figure 25: Power Amplifier Setup

- 2) Set the power supply voltage source to 17V, 1A, see Figure 26.

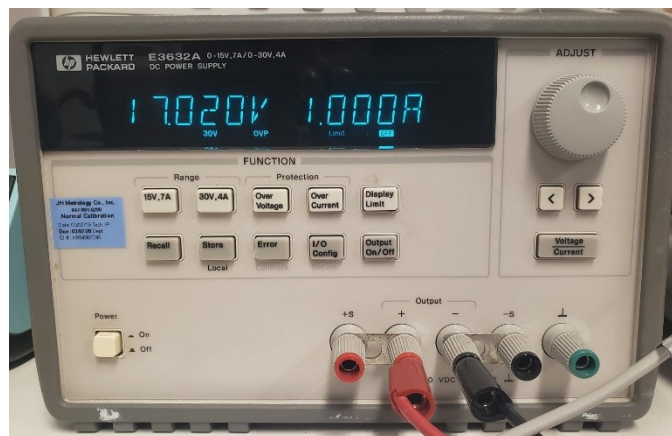


Figure 26: Power Amplifier VPA Setting

- 3) Launch NFC Cockpit application.
- 4) Once the Amplifier is detected, the window shown in Figure 27 will appear.

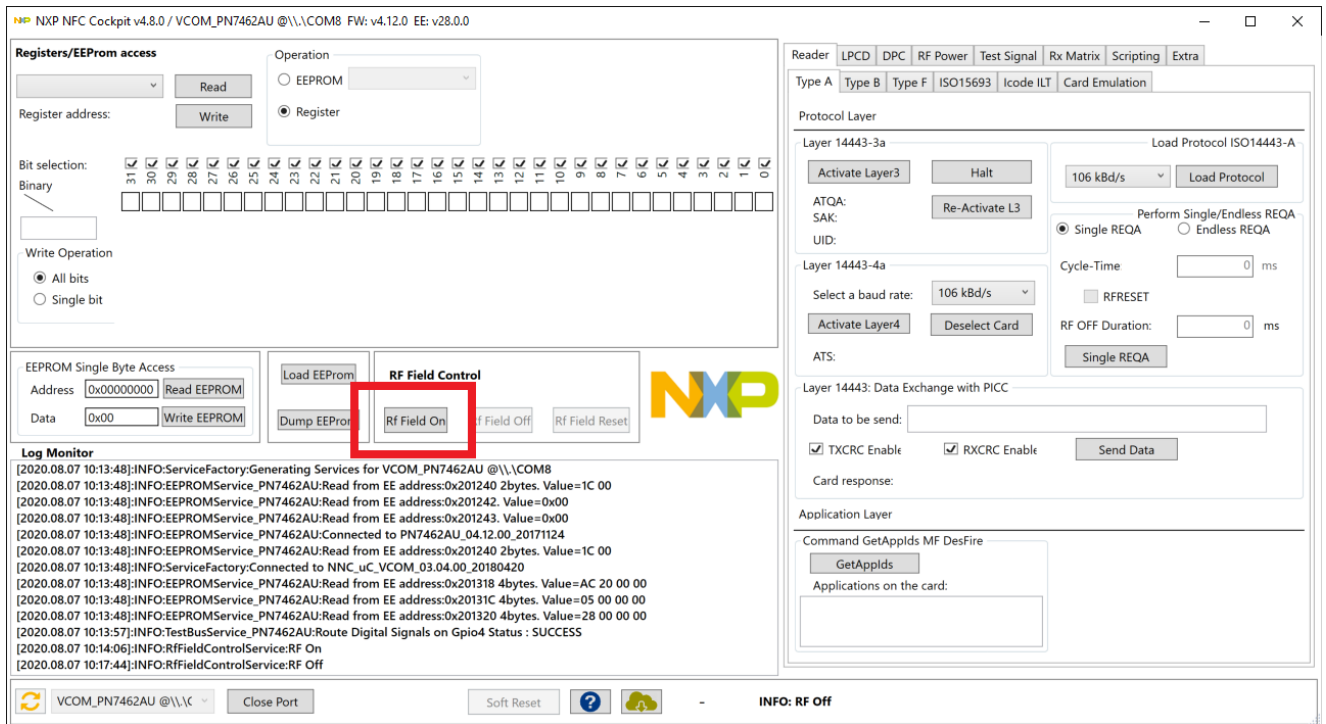


Figure 27: NXP NFC Cockpit Amplifier Detection Screen

- 5) To establish power transfer on the Amplifier, turn on the RF field by clicking on the RF Field On button (see Figure 27). NOTE: A current draw of ~200mA on VPA will be observed.

The harvester module already ships with card emulation software and does not require NFC Cockpit.

- 1) Place the assembled Harvester module on top of the Amplifier module as shown in Figure 28. NOTE: VRECT and VREG LEDs on the Harvester should now light up.
- 2) Connect an Electronic load to the Harvester module across the Vreg (Blue) and Ground (Black) banana jacks, as shown in Figure 28 and draw up to 1.25W of power.

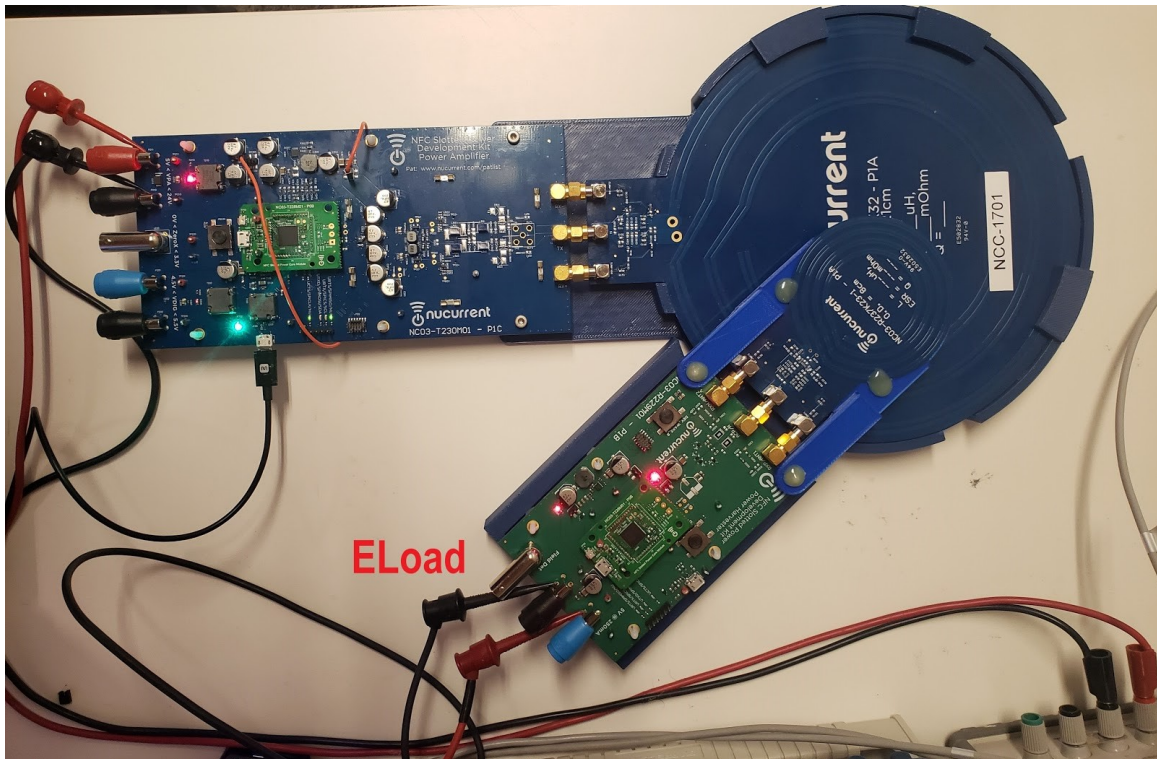


Figure 28: Power Harvester Placement

7.2 Data Transfer

Once power transfer has been successfully verified, the system is ready for data transfer. Using NFC Cockpit, the following steps are used to observe data transfer.

7.2.1 NFC Cockpit (Standard NFC Mode)

Data transfer is ensured over:

- Power loading conditions from 0W to 1.25W,
- Physical coil locations within the operating volume.

Note: If the transmitter is unable to support the load on the receiver, a drop in voltage on the receiver's regulator to 0V is observed. Immediately turn-off the load to prevent stress on the system.

7.2.1.1 106Kbps Data Transfer

Below are the steps required to verify data transfer @ 106Kbps using the NFC Cockpit.

- 1) Load 106KBd/s protocol
- 2) Select Endless REQA
- 3) Configure 1mS delay between data transfers (required for Card communication timing)
- 4) Start Data Transfer.

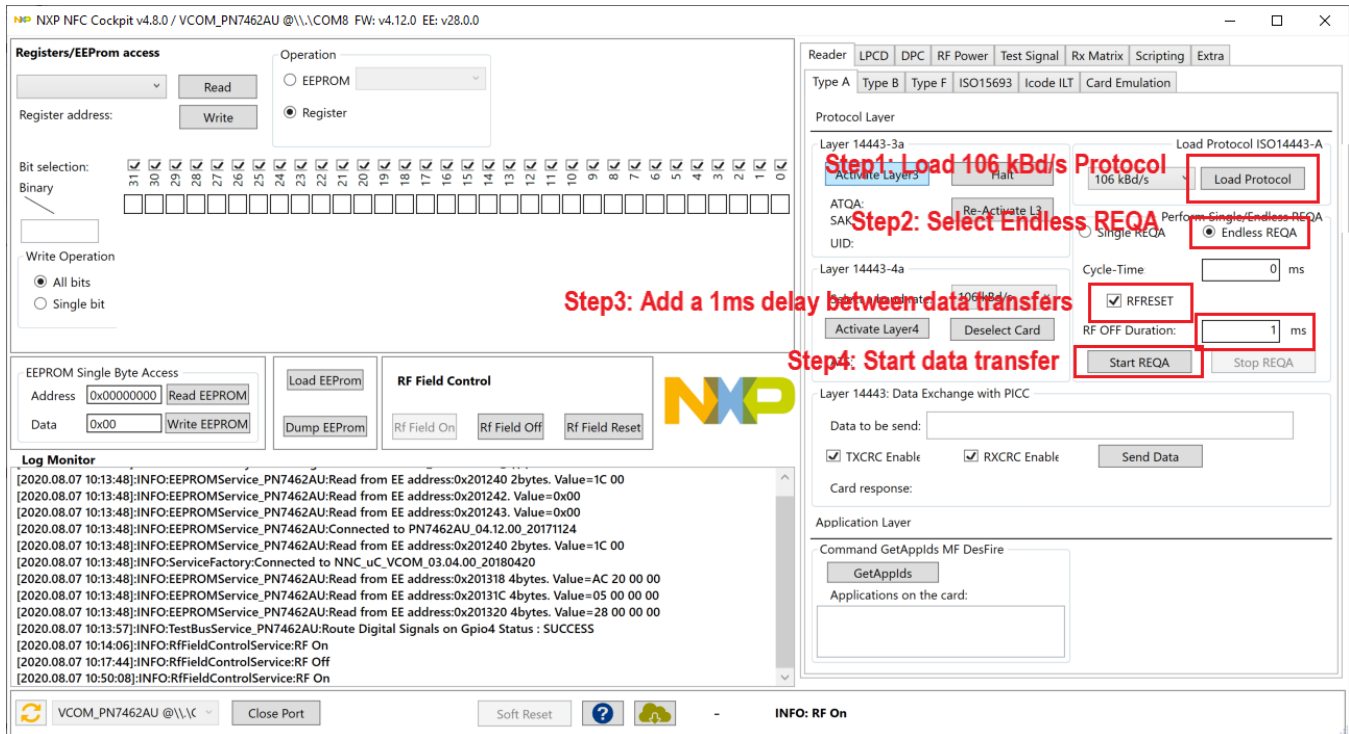


Figure 29: NFC Cockpit Configuration - 106Kpbs

Attached below is a screenshot of successful and failed data transfer observed on NFC Cockpit

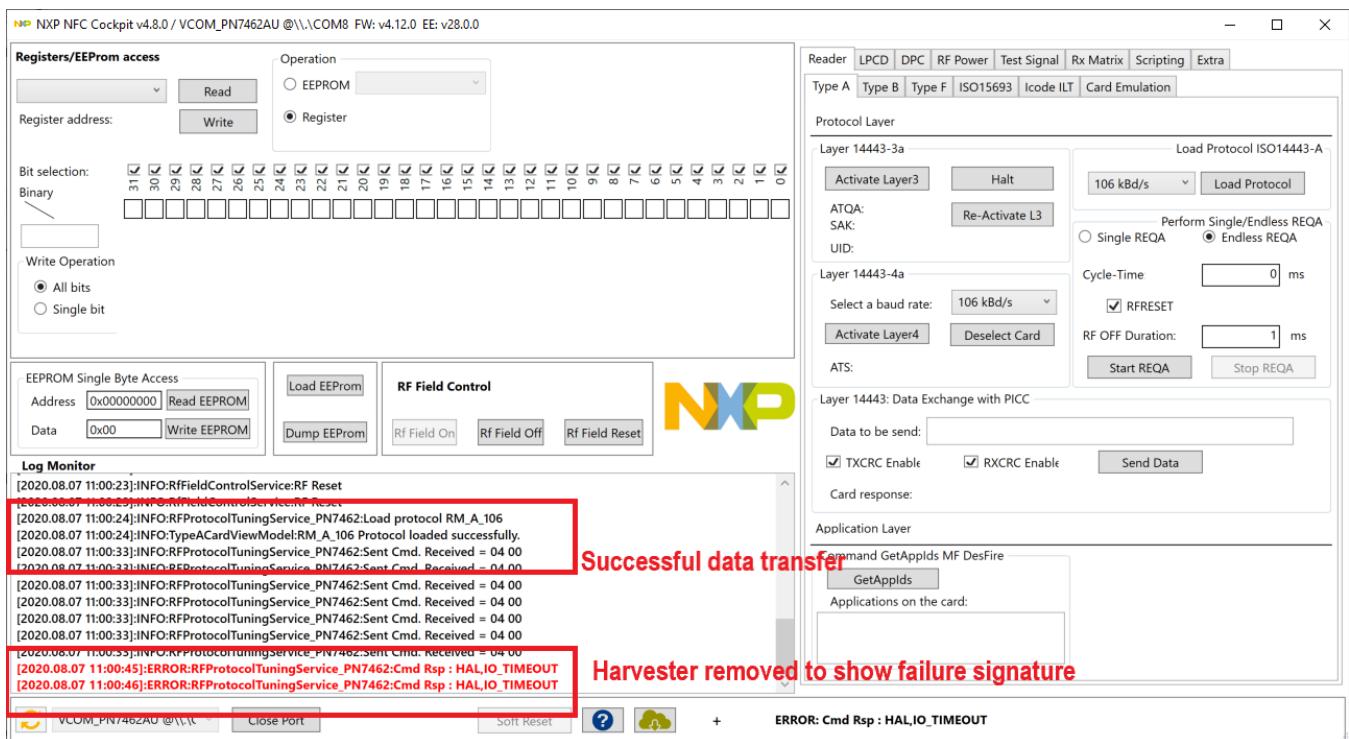


Figure 30: NFC Cockpit Configuration - 106Kbps Logs

7.2.1.2 424Kbps Data Transfer

Once 106Kbps operation has been verified, 424Kbps can be verified.

- 1) Reset RF Field 5 times. Resetting 5 times is required for NXP NFC Cockpit stability.
- 2) Activate Layer3
- 3) Set baud rate to 424KBd/s
- 4) Activate Layer 4
- 5) Send desired data

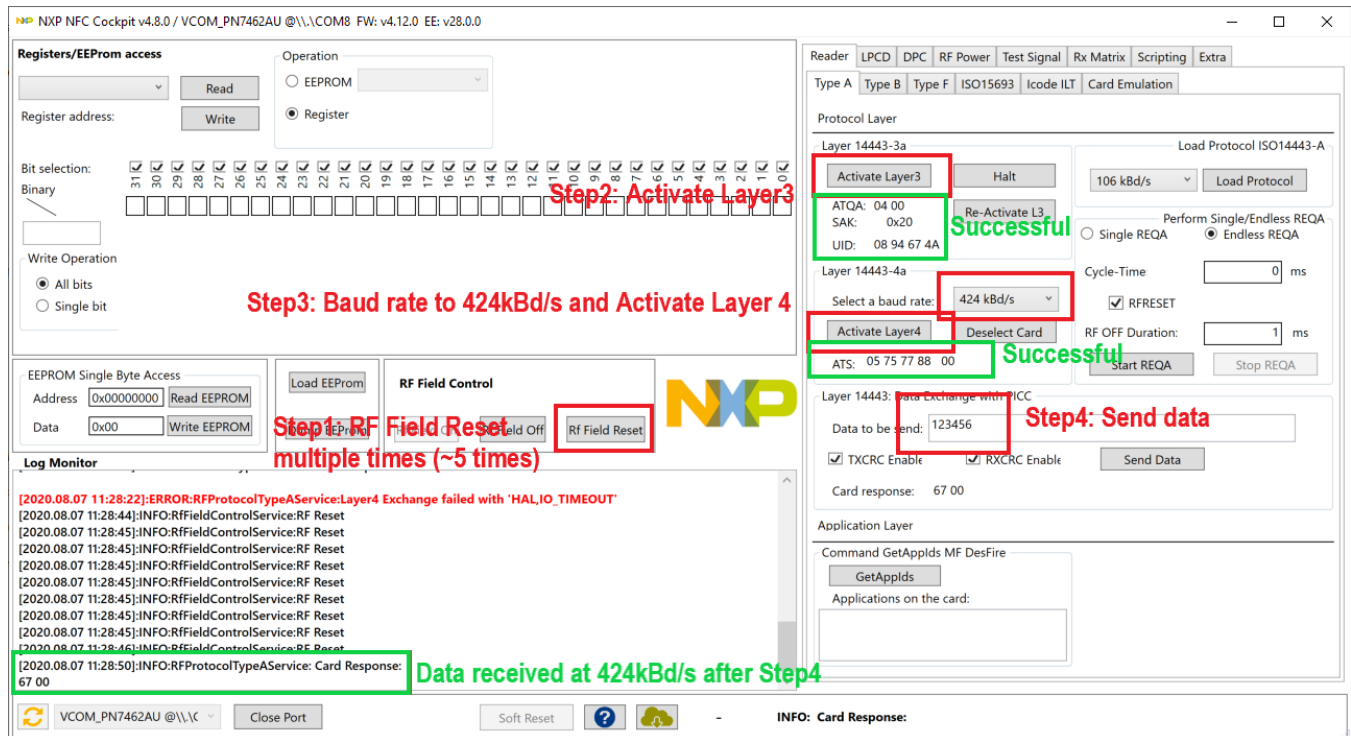
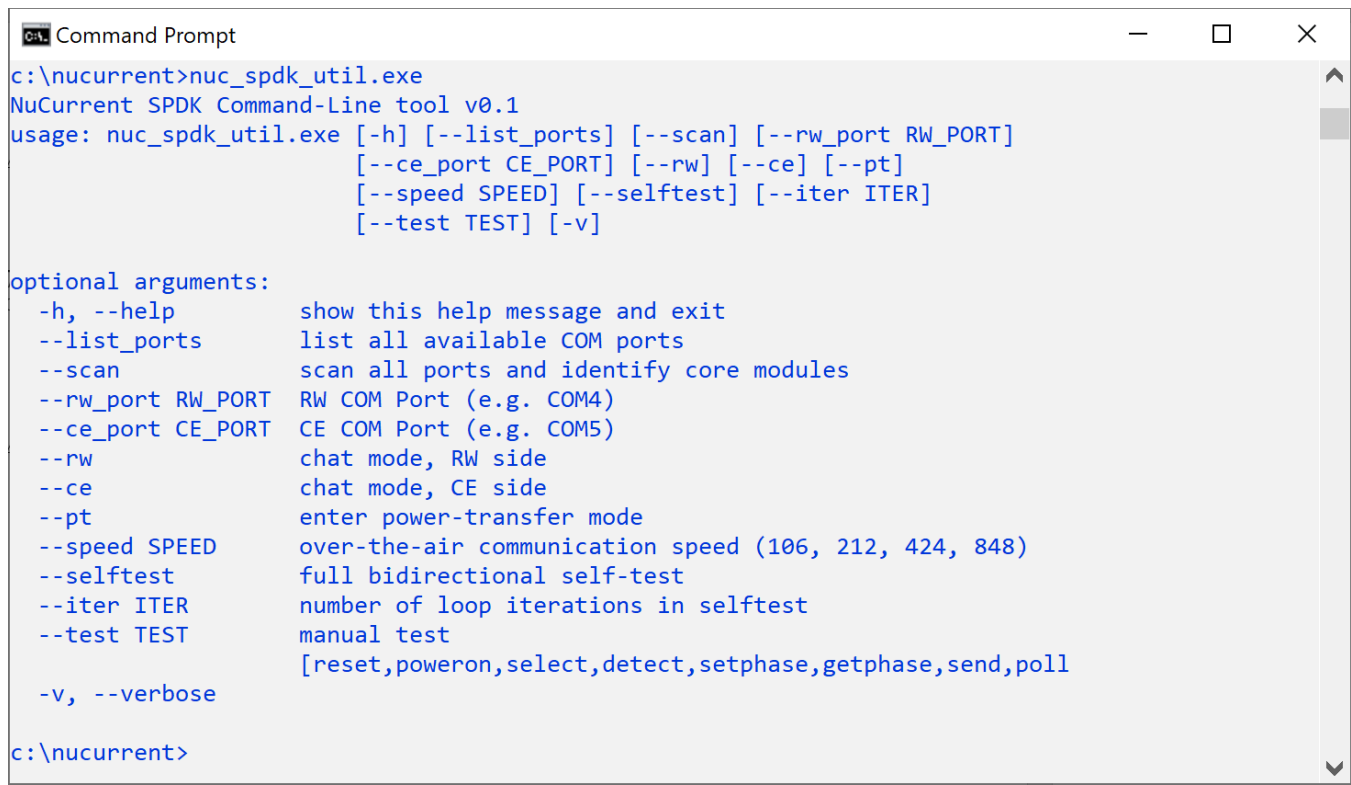


Figure 31: NFC Cockpit Configuration - 424Kbps

7.2.2 NuCurrent Command-line Tool

A command-line utility is provided to demonstrate serial communication and control over the SPDK functionality. This application communicates over the UART interfaces described in sections 5.1.1.4 and 5.2.1.4. This section assumes that serial connections to a host computer have been made to both the Power Harvester and Power Amplifier.

Launch the **nuc_spdk_util.exe** application in a Command Prompt window. The menu of options will appear as shown in Figure 32.



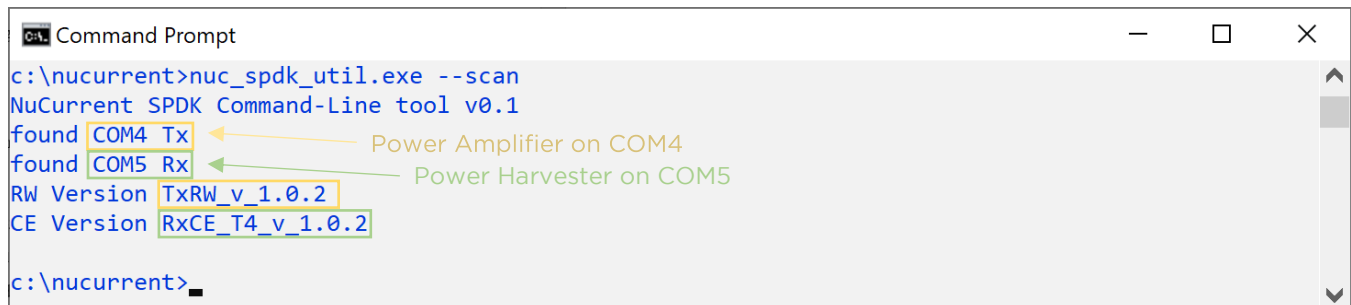
```
C:\> Command Prompt
c:\nucurrent>nuc_spdk_util.exe
NuCurrent SPDK Command-Line tool v0.1
usage: nuc_spdk_util.exe [-h] [--list_ports] [--scan] [--rw_port RW_PORT]
                        [--ce_port CE_PORT] [--rw] [--ce] [--pt]
                        [--speed SPEED] [--selftest] [--iter ITER]
                        [--test TEST] [-v]

optional arguments:
  -h, --help            show this help message and exit
  --list_ports          list all available COM ports
  --scan               scan all ports and identify core modules
  --rw_port RW_PORT    RW COM Port (e.g. COM4)
  --ce_port CE_PORT    CE COM Port (e.g. COM5)
  --rw                chat mode, RW side
  --ce                chat mode, CE side
  --pt                enter power-transfer mode
  --speed SPEED        over-the-air communication speed (106, 212, 424, 848)
  --selftest          full bidirectional self-test
  --iter ITER         number of loop iterations in selftest
  --test TEST         manual test
                     [reset,poweron,select,detect,setphase,getphase,send,poll]
  -v, --verbose

c:\nucurrent>
```

Figure 32: nuc_spdk_util.exe utility menu

Verify the host computer can identify connected Core Modules using the **--scan** option:



```
C:\> Command Prompt
c:\nucurrent>nuc_spdk_util.exe --scan
NuCurrent SPDK Command-Line tool v0.1
found COM4 Tx
found COM5 Rx
RW Version TxRW_v_1.0.2
CE Version RxCE_T4_v_1.0.2

c:\nucurrent>
```

Figure 33: core modules identified with --scan

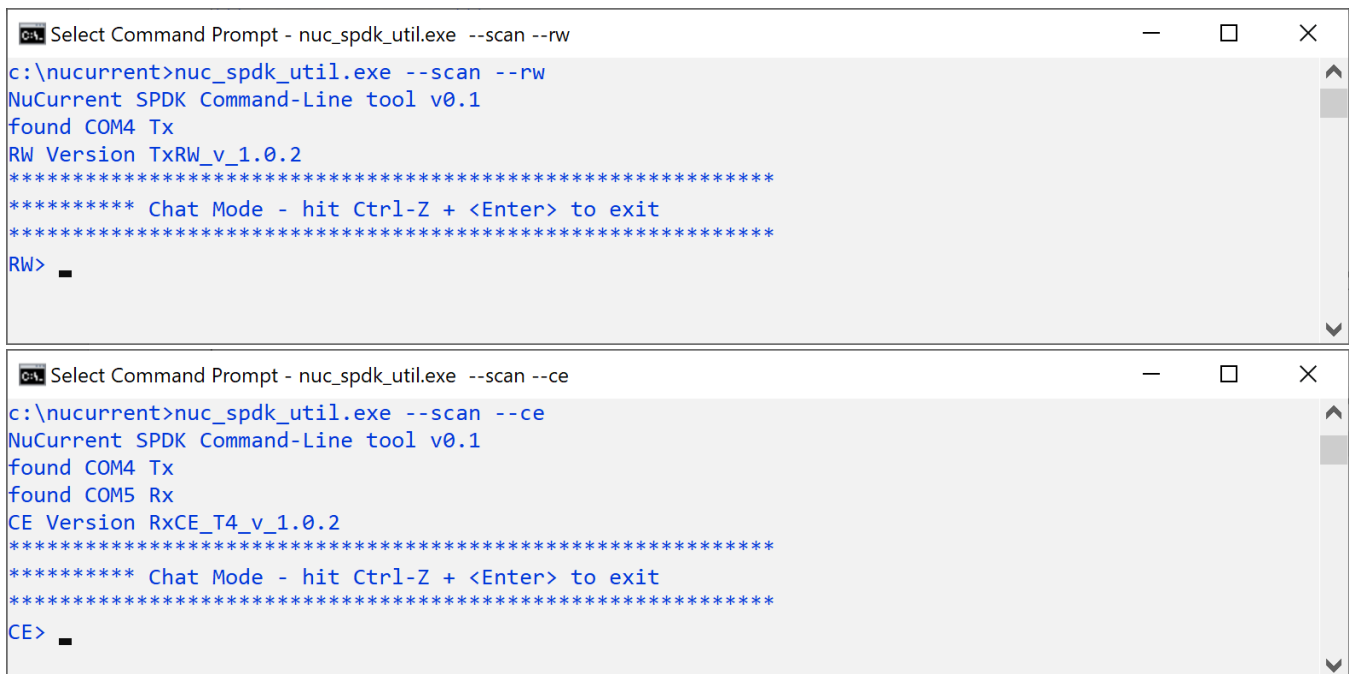
Perform a simple self-test by issuing the **--selftest** command. Adding **--pt** will perform the test in power transfer mode, and **--speed=212** will make the over-the-air connection at 212kbps as opposed to the default 106kbps.

```
Command Prompt
c:\nucurrent>nuc_spdk_util.exe --scan --selftest
NuCurrent SPDK Command-Line tool v0.1
found COM4 Tx
found COM5 Rx
RW Version TxRW_v_1.0.2
CE Version RxCE_T4_v_1.0.2
** PERFORMING BI-DIRECTIONAL TEST **
*****
***** TURNING ON POWER PLATFORM
*****
***** POLLING FOR DEVICE
*****
***** PLACE APPLIANCE
*****
***** CONNECTED PHASE
*****
*** TEST MSG 0 RW->CE ***
*** TEST MSG 0 CE->RW ***
*** TEST MSG 1 RW->CE ***
*** TEST MSG 1 CE->RW ***
*** TEST MSG 2 RW->CE ***
*** TEST MSG 2 CE->RW ***
*** TEST MSG 3 RW->CE ***
*** TEST MSG 3 CE->RW ***
*** TEST MSG 4 RW->CE ***
*** TEST MSG 4 CE->RW ***
c:\nucurrent>
```

Figure 34: self-test

A simple “chat” mode is included to showcase the transfer of manually-entered messages. Two instances of the application are used. They can be on separate PC’s, or both on the same PC in separate Command Prompt windows.

Both instances of **nuc_spdk_util.exe** can be launched with the **--scan** option, but one should have the **--rw** option and the other will have the **--ce** option.



```
Select Command Prompt - nuc_spdk_util.exe --scan --rw
c:\nucurrent>nuc_spdk_util.exe --scan --rw
NuCurrent SPDK Command-Line tool v0.1
found COM4 Tx
RW Version TxRW_v_1.0.2
*****
***** Chat Mode - hit Ctrl-Z + <Enter> to exit
*****
RW> _

Select Command Prompt - nuc_spdk_util.exe --scan --ce
c:\nucurrent>nuc_spdk_util.exe --scan --ce
NuCurrent SPDK Command-Line tool v0.1
found COM4 Tx
found COM5 Rx
CE Version RxCE_T4_v_1.0.2
*****
***** Chat Mode - hit Ctrl-Z + <Enter> to exit
*****
CE> _
```

Figure 35: chat mode

Messages typed in one window should show up in the other. Note: the 212kbps option (`--speed=212`) should be used in conjunction with power transfer mode (`--pt`) when demonstrating communication in power transfer mode.

8 Glossary

Ki

❖ Ki Cordless Kitchen Standard which is maintained by the Wireless Power Consortium

“This standard defines transmitters and versatile cooktops that wirelessly deliver up to 2200 watts of power to smart cordless kitchen appliances – allowing them to operate without the clutter of cords. These small appliances, such as rice cookers, toaster, blenders, coffee makers, air fryers and more, are powered by simply placing them over power transmitters installed in enabled induction cooktops or neatly hidden beneath any standard non-metal countertop surface, cooktop or table. The appliances are then powered by inductive power transfer with no cords to get in the way.”

For more information on the standard please see the homepage of the Ki Cordless Kitchen Standard

(<https://www.wirelesspowerconsortium.com/kitchen/>).

NFC

Near Field Communications. This is the 13.56MHz communications and power transfer technology used by the Ki Cordless Kitchen.

The NFC Forum (<https://nfc-forum.org/>) is responsible for the high level communications in conjunction with several ISO standards (14443, 15693, 18000, 7816) [<https://www.iso.org/home.html>]

Power Harvester

Subsystem in the NuCurrent SPDK that receives the 13.56MHz NFC communications from the Power Transmitter.

This subsystem operates on the harvested power from the 13.56MHz NFC field.

Other terms for this are Power Receiver, Listener, Card Emulator.

Power Amplifier

Subsystem in the NuCurrent SPDK that drives the 13.56MHz field for low power delivery (1.25W) and communications.

Other terms for this are Power Transmitter, Poller, Reader/Writer.