



LIGHTNING FAST AI

BARQ-V2

Starter Kit Datasheet

Made in the Emirates

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BARQ V2 Starter Kit Datasheet

BARQ-V2 Starter Kit is officially released by Barqtech Trading FZCO, Dubai Silicon Oasis, Dubai, UAE. The BARQ-V2 Starter Kit is a **high-performance AI acceleration card designed to deliver real-time inference for convolutional neural networks.**

BARQ-V2 Starter Kit provides a plug-and-play experience for software developers through standard **ONNX Runtime APIs**. With built-in support for INT8 quantized models, a dedicated PCIe Gen3 x8 interface, and onboard DDR4 memory, the BARQ-V2 enables efficient edge and desktop deployment of AI workloads including image classification, object detection, and segmentation.

Designed primarily as a development and evaluation platform, the **BARQ-V2 allows engineers to prototype, integrate, and validate their AI pipelines** using Barq's acceleration technology. It serves as a convenient way to **test AI workflows** on desktop or server systems ahead of deployment to production-ready BARQ hardware.

The core board uses Xilinx's Kintex Ultrascale+ chip xcku5pffvb676 solution, which is mounted with two 1GB high-speed DDR4 SDRAM chips and two 256Mb QSPI FLASH chips. Additionally there are a wealth of peripheral interfaces for users, such as 1 PCIe3.0x8 interface, 1 FMC HPC interface, 1 Gigabit network interface, 1 MIPI input interface, 1 UART serial interface, 1 SD card interface, 1 40-pin expansion interface and so on.



Figure 1: BARQ-V2 Starter Kit

Part 1: BARQ V2 Starter Kit Acceleration Card Introduction

The BARQ V2 AI Accelerator Starter Kit is an industrial-grade edge AI processing module designed for high-performance inference workloads in smart cities, surveillance, robotics, and industrial automation. Built on the AXKU5 FPGA platform (Xilinx Kintex UltraScale+), this accelerator delivers high-efficiency AI processing with low-latency execution, making it ideal for mission-critical applications.

The PCIe-based accelerator is engineered for real-time AI inferencing, featuring an optimized FPS-per-Watt ratio for energy-efficient deployments.

Part 1.1 System Architecture Overview

The BARQ V2 Accelerator Card is composed of three main components: a PCIe Gen3 x8 interface, a Kintex UltraScale+ FPGA device (XCKU5P), and dual-channel DDR4 memory. The architecture is optimized for low-latency AI inference workloads by offloading compute-intensive operations entirely to hardware.

The host system communicates with the FPGA via PCIe using DMA transactions. Input data, models, and control signals are sent from the host application to the accelerator through this interface.

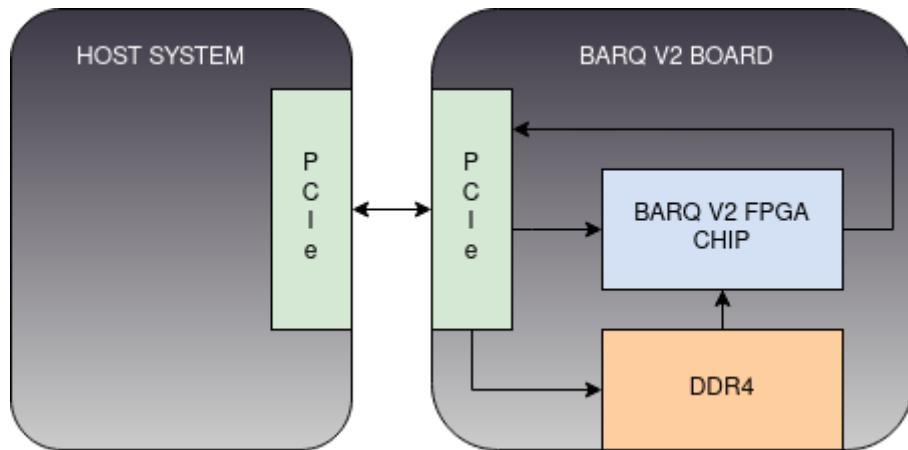


Figure 2: System overview

Once data is received on the FPGA:

- A lightweight DMA engine handles transfers between host memory and onboard DDR4.
- The DDR4 memory serves as a temporary buffer for input feature maps, intermediate results, and optionally preloaded weights.

- The accelerator logic — implemented in FPGA fabric — includes a custom INT8 processing pipeline composed of:
 - A data controller and buffer manager
 - A vector splitter/combiner and scheduler
 - A multiply-accumulate array to accelerate matrix multiplication
 - Requantization and activation logic
- The final inference results are returned to the host via PCIe.

Part 1.2 Operating Frequency

The BARQ V2 accelerator operates across three main clock domains, each selected to balance data throughput, timing closure, and external memory interfacing.

- **500 MHz Core Clock:** The main accelerator pipeline, including internal buffers, controller and compute datapath runs at 500 MHz.
- **250 MHz PCIe:** The logic responsible for PCIe DMA communication with the host operates at 250 MHz.
- **333 MHz DDR Controller Clock:** The external memory interface subsystem, including the DDR controller and interface FIFOs, runs at 333 MHz. A CDC (Clock Domain Crossing) module bridges the DDR domain with the internal logic to enable safe, asynchronous data transfers.

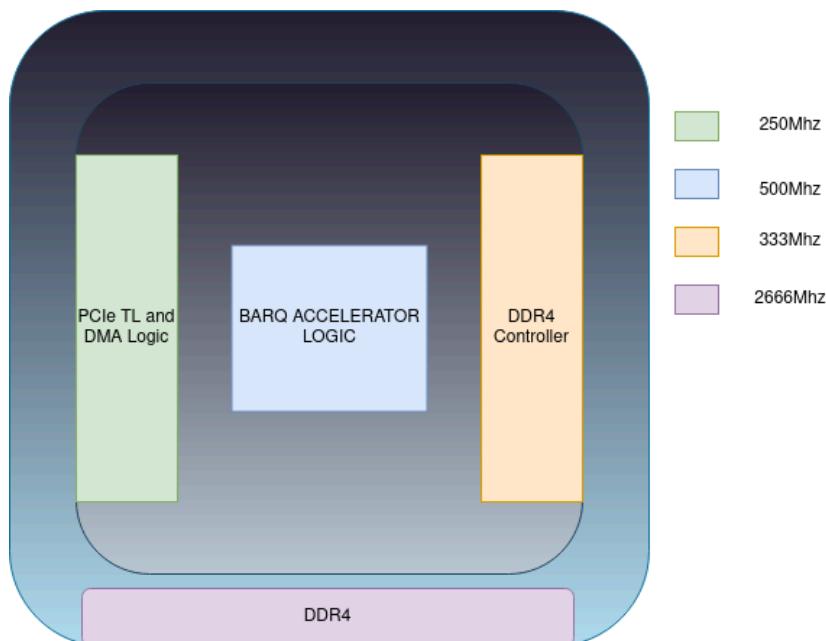


Figure 3: Clock Domains

Part 1.3 Memory Subsystem

The BARQ V2 accelerator includes **2 GiB of DDR4 memory** connected directly to the FPGA. This memory runs at **2666 MT/s** with a 64-bit data bus, providing a peak bandwidth of approximately **21.3 GB/s**.

This external memory is memory mapped to the host system through a 512 MB 32-bit prefetchable BAR. The following table shows the mapping of the BAR address space:

Start Address	End Address	Mapped Resource
0x00000000	0xC7FFFFFF	Weights
0xC8000000	0xF9FFFFFF	Biases
0XFA00000	0x1FFFFFFF	Reserved

Table 1: PCIe BAR memory map

Data is streamed from DDR4 to the accelerator core using a dedicated memory controller and internal buffering system. Memory access and synchronization are handled transparently by the hardware pipeline — no configuration is required from the user.

Part 1.4 PCIe Interface

The BARQ V2 Starter Kit communicates with the host system over a **PCI Express Gen3 x8** interface, offering a theoretical maximum throughput of up to **7.88 GB/s** in each direction.

This high-bandwidth link is used for:

- Transferring input data from the host to the accelerator
- Returning inference results back to the host
- Managing control signals and synchronization

The **dedicated DMA engine** on the FPGA handles all data movement, performing memory-to-memory transfers between host and board without involving the host CPU. The PCIe interface also serves as the **sole power source** for the board. No external power supply is required.

Part 1.5 Power Supply and Consumption

The BARQ V2 board is fully powered through the **PCIe edge connector**, requiring no external power supply. All internal voltage rails, including those for the FPGA core, auxiliary domains, transceivers, DDR4 interface, and peripherals, are derived from the 12 V PCIe supply using on-board DCDC converters.

Typical power consumption during inference is approximately **3 W**, though actual usage depends on the workload and model size. The **peak power** draw during high-throughput operation can reach up to **5.5 W**, while **idle power** is typically around **0.4 W**, depending on host-side activity and link state.

For detailed information on voltage rails, sequencing, regulator selection, and protection features, refer to **Section 2.7: Power Supply Design**.

Part 1.6 Thermal Management

The BARQ V2 board includes an **integrated active cooling system** consisting of a low-profile heatsink and fan mounted directly on the FPGA. This cooling solution is sufficient for all supported workloads under typical ambient conditions.

The fan is powered from the onboard regulators and runs continuously while the board is active. No user configuration or external airflow is required.

The system has been validated to operate reliably at ambient temperatures up to **50 °C** under full load.

Part 1.7 Startup and Reset Behavior

On power-up, the BARQ V2 board automatically initializes the FPGA configuration and enters a ready state. The PCIe link is established as part of this process, and no user interaction is required.

A dedicated **reset button (KEY1)** is available on the board to issue a **hot reset**. This reset:

- Affects only the accelerator logic
- Does **not** reset the PCIe link or the DDR4 controller
- Is intended for recovery or development use

The hot reset completes in exactly **30 ns** after the button is released. Power-on reset for the full system completes in approximately **100 µs**.

Part 1.8 Device Status Indication

The BARQ-V2 board includes seven LEDs.

- **User LEDs:** Four onboard user LEDs to be used as indicators for debugging and troubleshooting.
- **System LEDs:** Three additional LEDs. Their function is documented in **Part 2.6 LED Light**.

The first **user LED** is active (red stable light) when the PCIe link status is on.

The following table lists the **user LEDs** and their functions:

LED	Color	Function
LED1	Red	PCIe link status
LED2	Red	Reserved
LED3	Red	Reserved
LED4	Red	Reserved

Table 2: LEDs functions

Note: LED are on to indicate a good state. Reserved LEDs are always off.

Part 2: Kintex UltraScale+ AXKU5 technical specifications

Part 2.1: FPGA Development Board Introduction

ACKU5 (SoM model, the same below) core board, FPGA chip is based on Xilinx FPGA Kintex Ultrascale+ main chip xcku5pffvb676 design. The SoM connects two DDR4 memory chips to the HP port of the FPGA to form 32-bit data bandwidth, and each DDR4 capacity is up to 1GB. The memory bandwidth on the HP side is up to 85Gb/s. In addition, the core board is also integrated with two 256MBit QSPI FLASH, used to start storage configuration and system files.

The SoM uses a board-to-board connector to expand 179 IO, and the level of the outgoing IO can be modified by replacing the LDO chip on the baseboard to meet the user's requirements of non-level interface; In addition, the SoM has been expanded to 16 pairs of high-speed transceiver interfaces. For users who need a lot of IO, this core board will be a good choice. In addition, the IO connection part, the wiring between the FPGA chip and the interface is isometric and differential processing, and the SoM size is only 80*60 (mm), which is very suitable for secondary development.

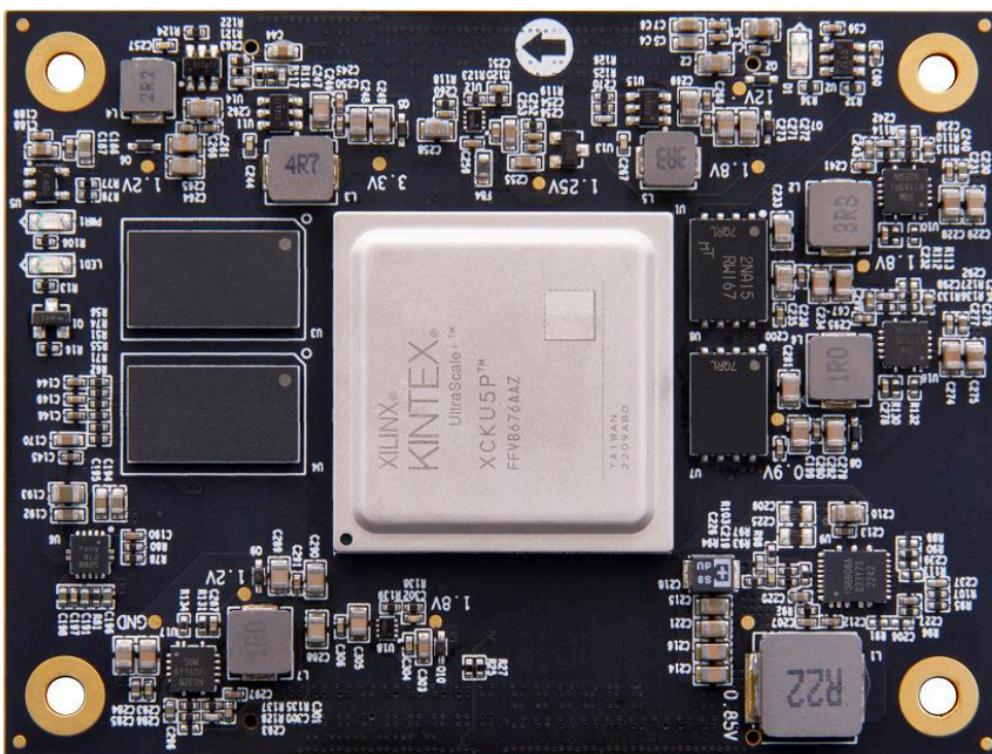


Figure 4: Front view of ACKU5 board

Part 2.2: FPGA Chip

As mentioned above, the FPGA model we used is xcku5pffvb676, belonging to Xilinx Company's Kintex Ultrascale+ series products, speed class 6, temperature class industrial. This model is in FFVB676 package with 676 pins. The chip naming rules of Xilinx Kintex Ultrascale+ FPGA are as follows:

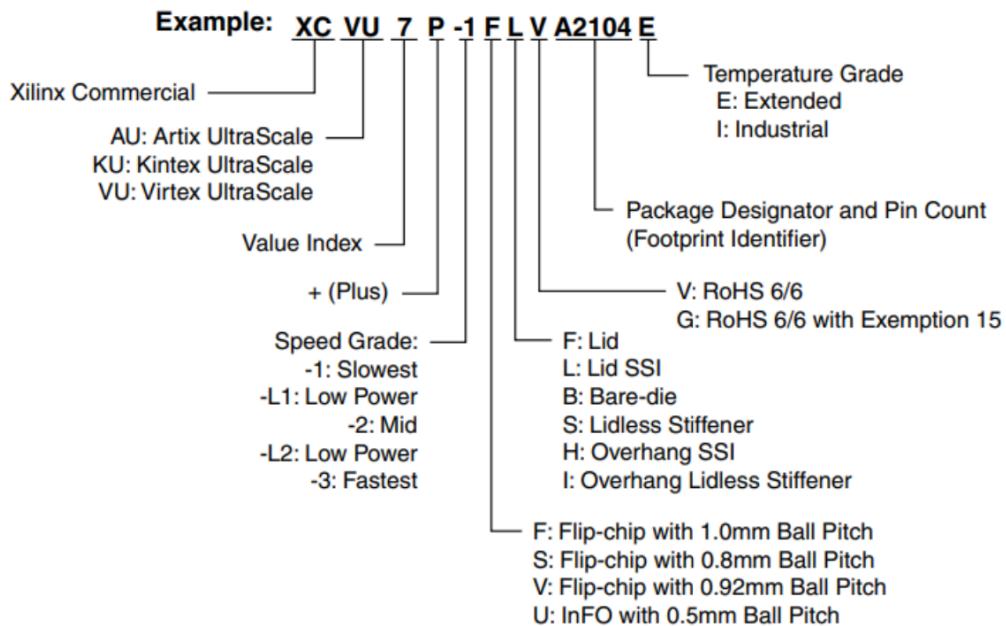


Figure 5: is the physical diagram of the FPGA chip used in the starter kit



Figure 6: FPGA Chip

Part 2.3: DDR4

The ACKU5 development board is equipped with two Micron 1GB DDR4 chips, model MT40A512M16LY-062E, connected to the HP end of the FPGA, composed of 32-bit data bus bandwidth and 2GB capacity. DDR4 SDRAM has a maximum operating data rate of 2666Mbps on the FPGA side



Figure 7: photo of two DDR4 DRAM pieces of the starter kit

Part 2.4: QSPI Flash

The SoM board is equipped with two 256MBit Quad-SPI FLASH chips, model MT25QU256ABA1EW9, which uses the 1.8V CMOS voltage standard.

Part 2.5: Clock Configuration

A 200Mhz 2-channel differential active clock is provided on the core board for the FPGA system. The differential clock source is provided for the FPGA logical part.

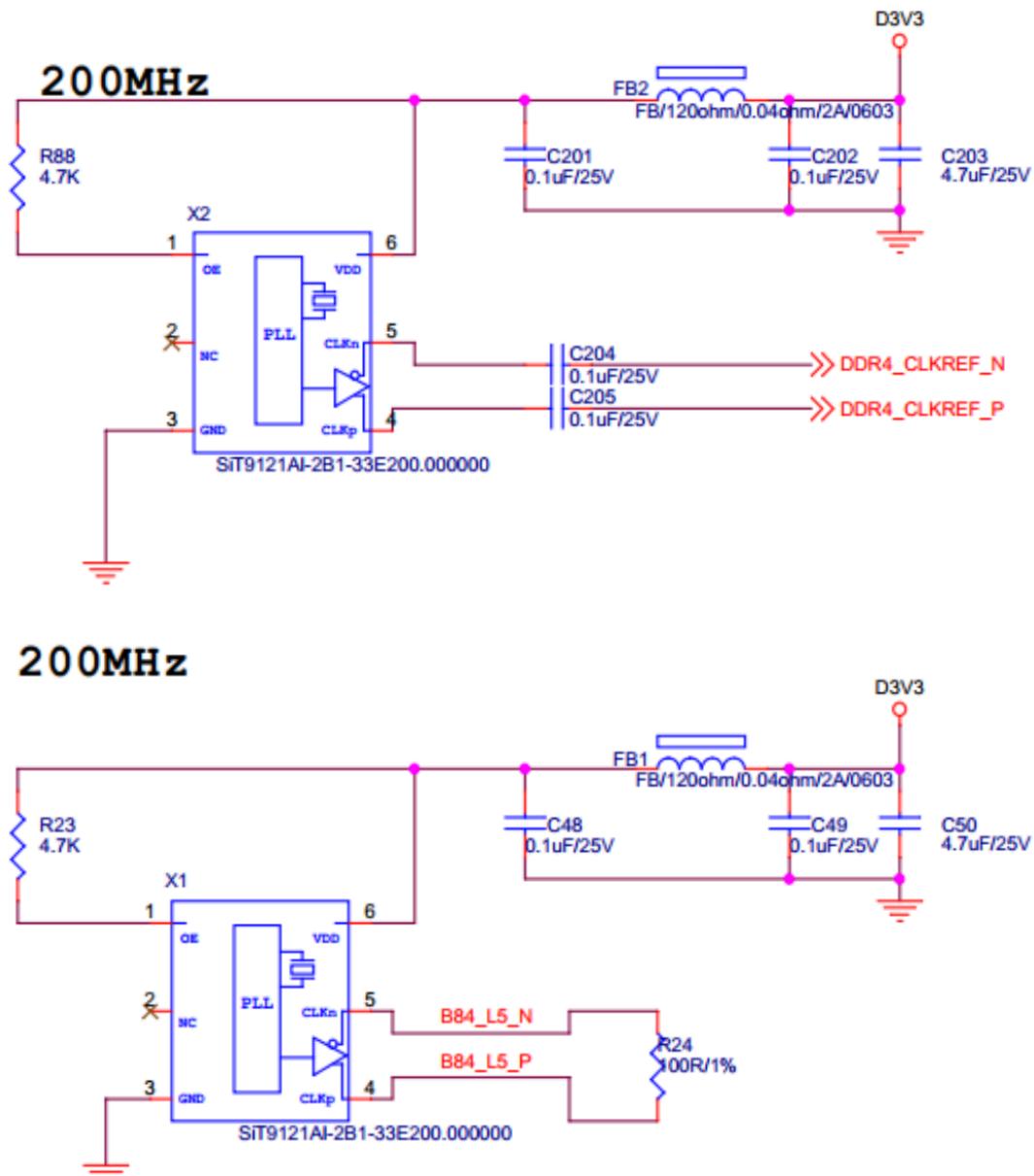


Figure 8: System clock source

Part 2.6: LED Light

The ACKU5 SoM board has three red LED lights, of which 1 is a power indicator (PWR1), 1 is a configuration LED (D1), and a user indicator (LED1). The indicator light will light up when the core is powered on; When the FPGA is configured, the configuration LED lights up.

Part 2.7: Power Supply

2.7.1 Power Supply SOM

The power supply voltage of the ACKU5 SoM board is +12V, which is connected to the mainboard. The power supply design diagram on the board is shown below:

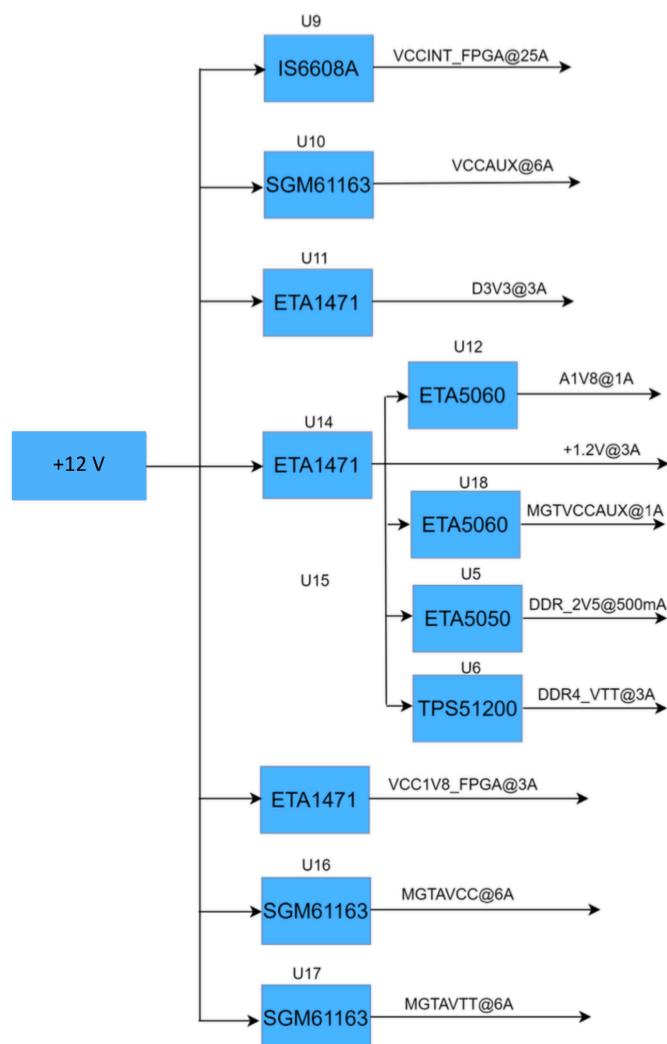


Figure 9: Schematic diagram of the power interface

+12V generates FPGA core power supply through DCDC power chip IS6608, with output current up to 25A, which can meet the current requirements of core voltage. +12V power supply and then through 3 DCDC chips SGM61163 to generate VCCAUX, MGTAVCC, MGTAVTT power supply to FPGA auxiliary power supply and high-speed transceiver power supply.

At the same time, the +12V power supply is generated by the DCDC chip ETA1471 to generate +1.2V, VCC1V8_FPGA, D3V3 power supply to the peripherals of DDR4 and FPGA. In addition, D3V3 generates the auxiliary power supply of the high-speed transceiver and the ADC power supply of the FPGA through two LDO chips, ETA5060, +1.8V; The VTT and DDR2V5 voltages for DDR4 are generated by the TPS51200 and ETA5050.

Due to the requirements of the power-on sequence of the power supply of the FPGA, in the circuit design, we have designed in accordance with the power supply requirements of the chip to ensure the normal operation of the chip.

2.7.2 Power Supply Board

The input voltage power of the development board is 12V DC. You can supply power to the development board through the PCIE slot or external +12V power supply. Use the own power supply with the development board for external power supply. Do not use other power supplies to avoid damage to the development board. The external input power supply on the carrier board is protected by 1-way voltage chip, and the DC/DC power supply chips ETA8156, ETA1471 and SGM61163 are converted into +5V, +V_ADJ and +3.3V three-way power supplies respectively. At the same time, the +3.3V output provides the voltage required by the multiple output.

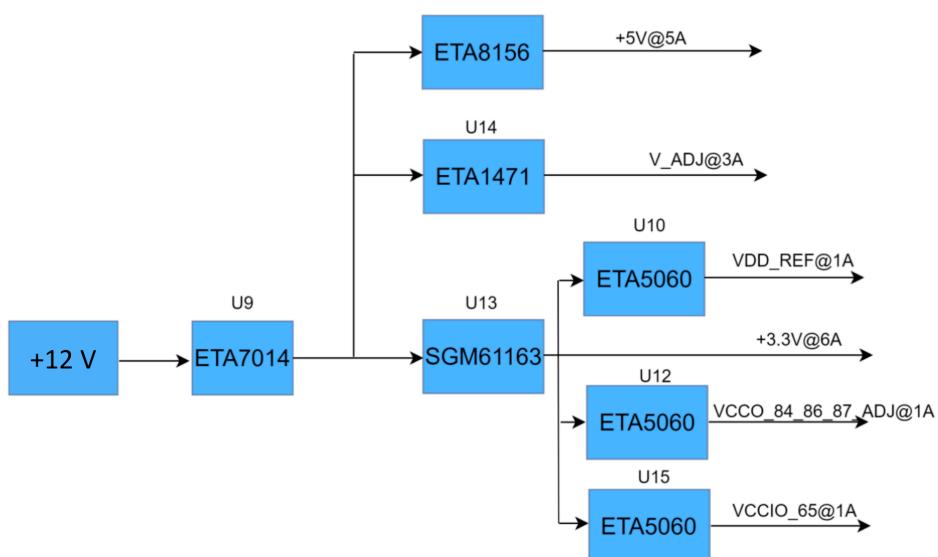


Figure 10: Schematic diagram of the power interface

The following table describes the power distribution functions:

Power Supply	Function
+5.0V	Power supply for the expansion module
V_ADJ	FPGA Voltage
+3.3V	Carrier board peripheral power supply
VDD_REF	JTAG power supply
VCCIO_65	FPGA Voltage
VCCO_84_86_87_ADJ	FPGA Voltage

Table 3: Power distribution functions

Part 2.8: Size Dimension

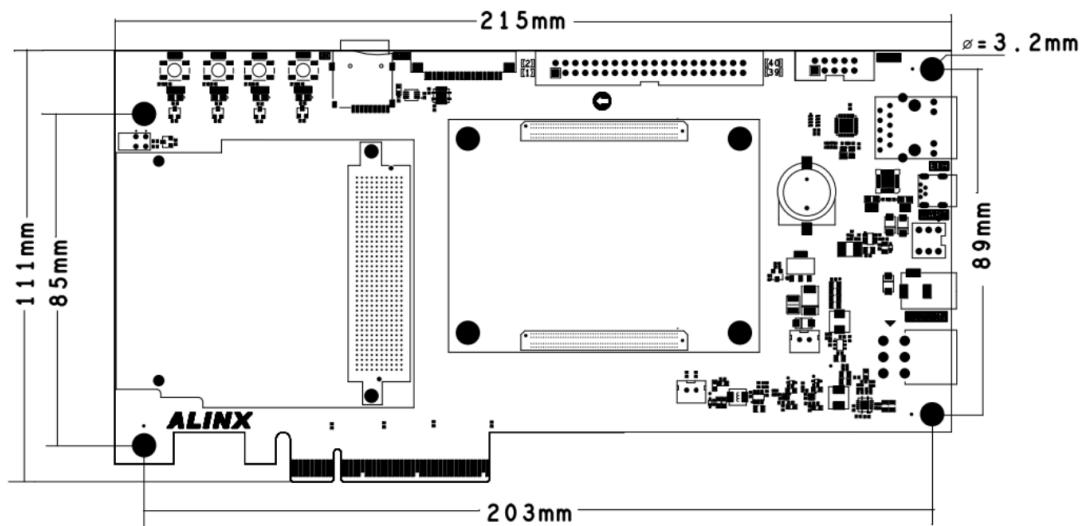


Figure 11: Starter Kit Top View

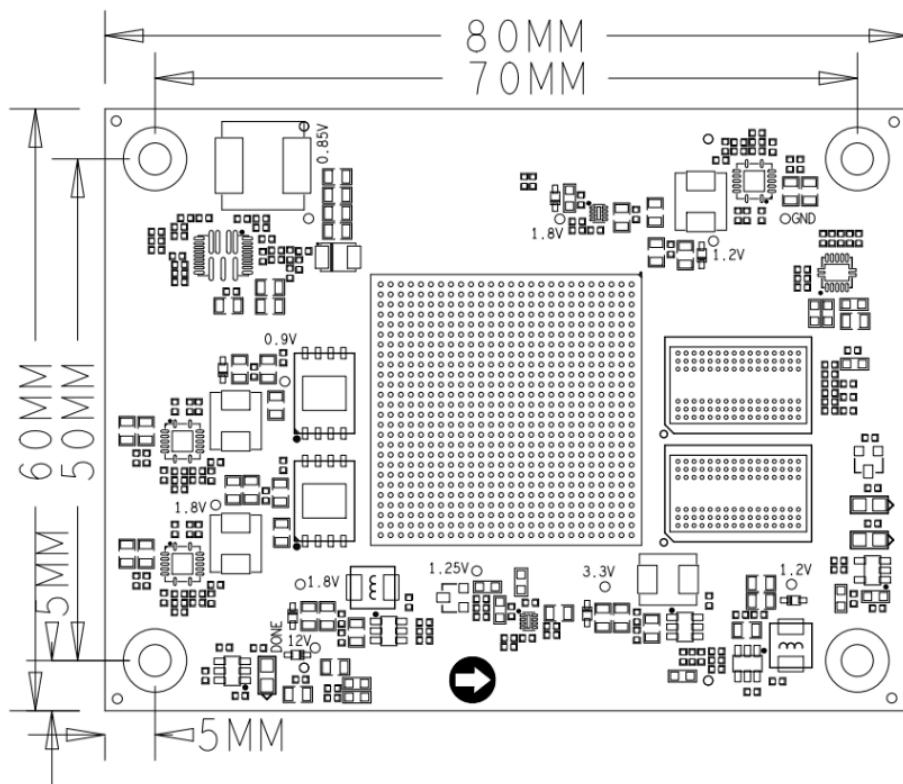


Figure 12: ACKU5 SOM Board Top View

Part 2.9: PCIe slots

The AXKU5 expansion board has a PCIe x8 interface that supports the PCIe Gen3.0 protocol, and the 8-pair transceiver is connected to the golden finger of the PCIEx8 for data communication.

The receiving and sending signals of the PCIe interface are directly connected to the FPGA transceivers, and the 8 TX signals and RX signals are connected to the FPGA transceiver in the way of differential signals, and the single-channel communication rate can be as high as 8G bit bandwidth.

The design diagram of the PCIe interface of the development board is shown in

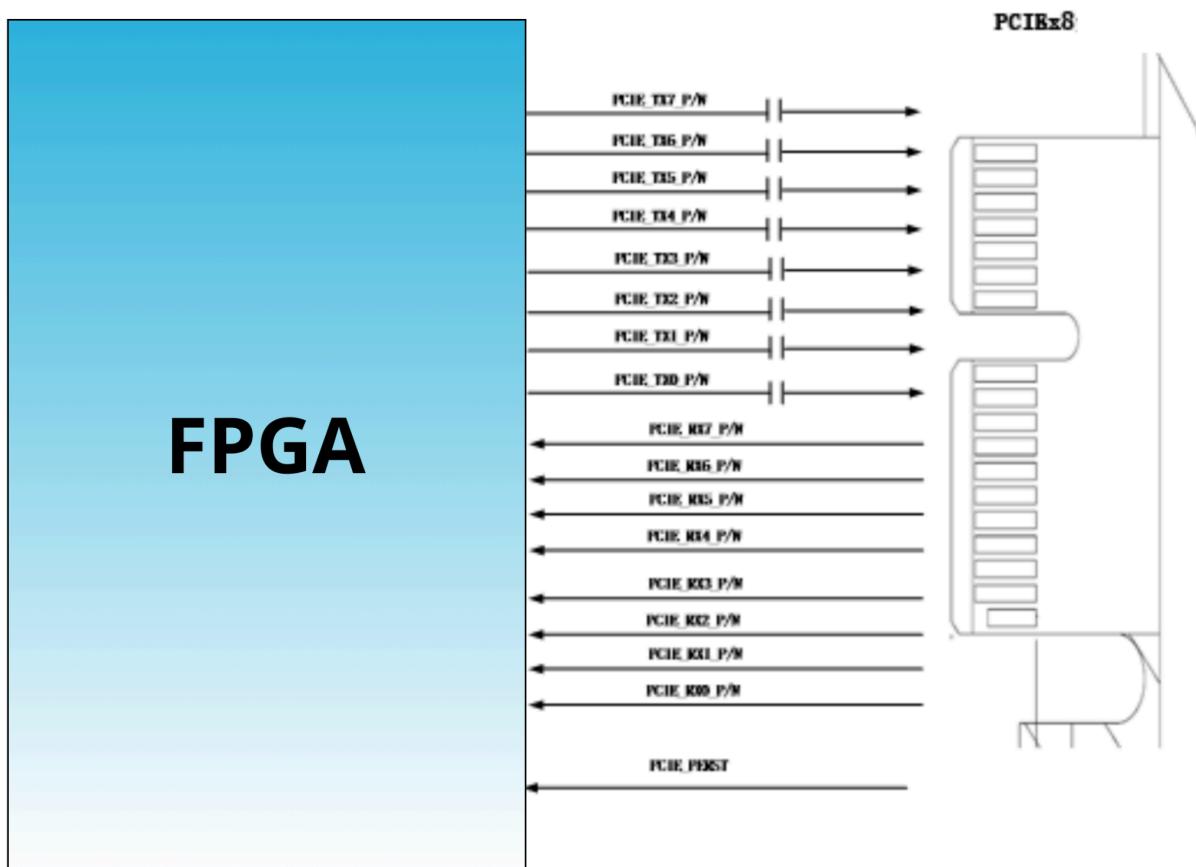


Figure 13: PCIe slot design

Part 3.3: Gigabit Ethernet Interface

There is one Gigabit Ethernet interface on the AXKU5 development board. The GPHY chip uses the JL21221D chip to provide users with network communication services. The Ethernet PHY chip is connected to the IO interface of the FPGA. The JL21221D chip supports 10/100/1000 Mbps network transmission rate and communicates with the FPGA through the RGMII interface. JL21221D chip supports MDI/MDX adaptation, various speed adaptation, Master/Slave adaptation, and supports MDIO bus for PHY register management.

When the JL21221D is powered on, it detects some specific IO level states to determine its own working mode. Table 3-2-1 describes the default Settings of the GPHY chip after it is powered on.

When the network is connected to Gigabit Ethernet, the data transmission of the FPGA and PHY chip JL2121 is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling sample of the clock.

When the network is connected to 100 Gigabit Ethernet, the data transmission of the FPGA and PHY chip JL2121 is communicated through the RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock.



Figure 14: Shows the physical diagram of the Ethernet PHY chip

Part 3.4: FMC HPC Interface

The development board has 1 FMC HPC expansion port, which can be connected to XILINX or various FMC modules of our ALINX (HDMI input and output module, binocular camera module, high-speed AD module, etc.).

Part 3.5: MIPI Interface

1-channel onboard MIPI lanex4 input port, with a maximum rate of 2.5Gb/s, is used to connect to the MIPI camera module.

Part 3.6: USB to Serial Port

The AXKU5 expansion board is equipped with a Uart to USB interface for system debugging. The conversion chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface, which can be connected to the USB port of the upper PC with a USB cable for separate power supply of the core board and serial data communication.

Part 3.7: SD Card Slot

The AXKU5 carrier board includes a Micro SD card interface in order to provide user's access to SD card memory for user data files. The SDIO signal is connected to the IO signal of the FPGA, supports SPI mode and SD mode, and uses a MicroSD card. 1-channel Micro SD card used to store operating system images and file systems.

Part 3.8: 40 Pin Expansion port

The carrier board reserves a 40-pin expansion port J8 with 2.54mm standard pitch, which is used to connect each module of black gold or the external circuit designed by the user. The expansion port has 40 signals, including 1 5V power supply, 2 3.3V power supply, 3 ground channels, and 34 IO ports. The IO of the expansion port connects to the IO of the FPGA. The default value is 3.3V.

Part 3.9: Keys and LED Lights

The carrier board of AXKU5 has 7 LED and 1 power indicator; 2 serial communication indicators, 4 user LED lights. When the development board is powered on, the power indicator will light up; The 4 LED lights are connected to the IO of the FPGA, and the user can control the on and off through the program. When the IO voltage of the connected user LED lamp is high, the user LED lamp will be on, and when the connected IO voltage is low, the user LED will be off. In addition, there are 4 user keys on the board, the default key signal is high, and the key level is low when the key is pressed

Part 3.10: JTAG Debugging port.

A 10PIN JTAG interface is reserved on the AXKU5 backboard for downloading FPGA programs or curing programs to FLASH. In order to avoid the damage to the FPGA chip caused by live plugging, we add a protection diode to the JTAG signal to ensure that the voltage of the signal is in the range accepted by the FPGA.

JTAG Connector

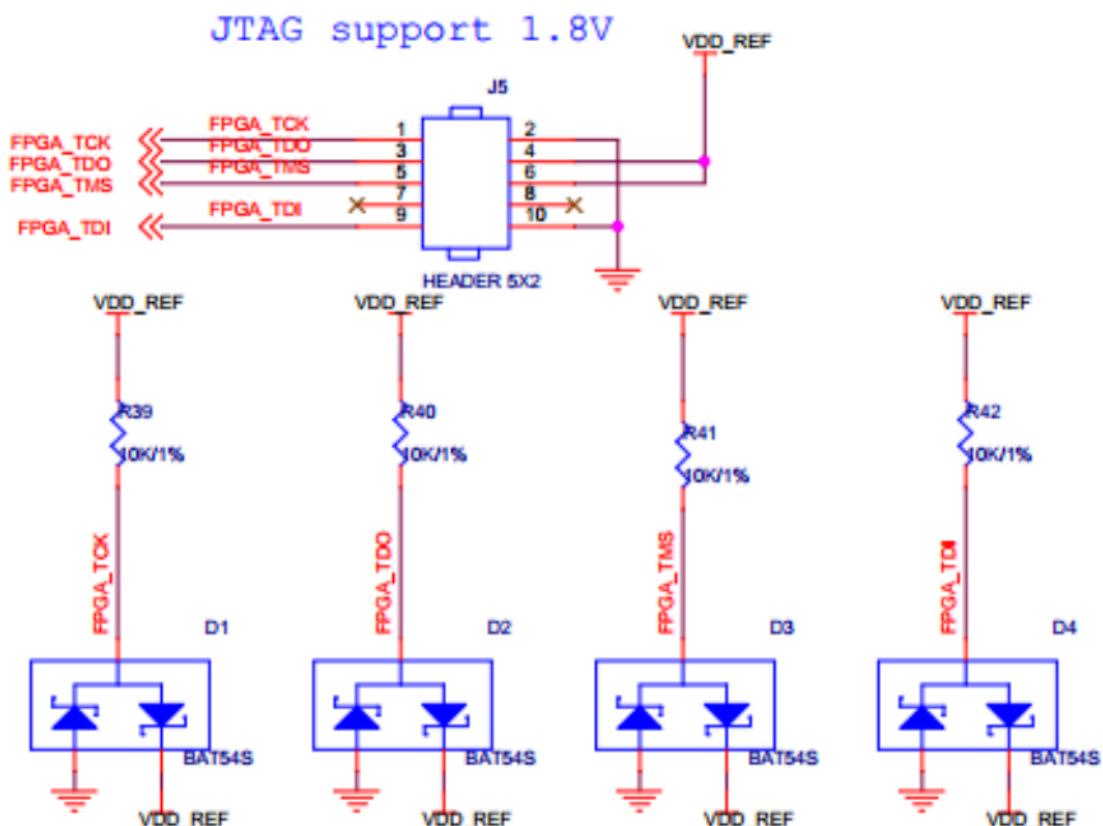


Figure 15: Schematic diagram JTAG interface