Serial data equalization

DesignCon 2007

Serial Data Equalization

Bryan Casper, Intel

Peter Pupalaikis, LeCroy

Jared Zerbe, Rambus

Abstract

Equalization is an important aspect of serial data systems. This TecForum provides a basic overview of the serial data transmission problem and the goals of equalization, along with a brief history of how it has been used in the past. We will explore the topology of an equalized system presenting key types of equalizers such as linear receive equalizers, transmitter pre-emphasis, and the decision feedback equalizer, along with the pros and cons of each type; more important, we show how various equalizer components can be used together to mitigate each other's weaknesses. Equalizers will be presented from various viewpoints, including effectiveness and practical circuit design. We will also cover modeling and optimization of equalized systems.

Author(s) Biography

Jared Zerbe joined Rambus Inc in 1992 where he has since specialized in the design of high-speed I/O, PLL/DLL clock-recovery, and SerDes circuits. He has authored multiple papers and patents in the area of high-speed clocking and data transmission. He has guest lectured and taught courses at Berkeley and Stanford in link design and is currently a Technical Director where he is focused on development of future signaling technologies.

Bryan Casper received the M.S. degree in electrical engineering from Brigham Young University, Provo UT. He currently leads the high-speed signaling research group of Intel's Circuit Research Lab, based in Hillsboro, Ore. In 1998, he worked on the development of the Pentium 4 and Xeon processors. Since 2000, he has been a circuit researcher responsible for the research, design, validation and characterization of high-speed mixed signal circuits and I/O systems.

Peter Pupalaikis received the B.S. degree in electrical engineering from Rutgers University, College of Engineering, Piscataway, NJ. His interests and responsibilities are in the areas of digital signal processing and microwave technologies. He is currently Principal Technologist at LeCroy Corporation where he has worked for the past eleven years in the design of high-speed real-time waveform digitizing systems.

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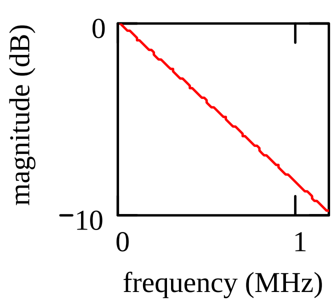
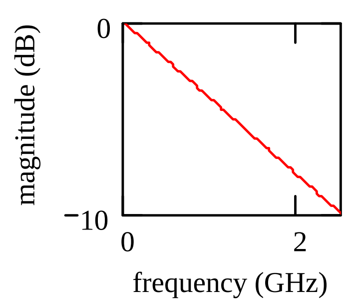
The Equalization Problem (simplistic view)

$$Q = \left[\frac{loss}{length \cdot frequency} \right]^{-1}$$

$$speed \cdot length = loss_{acceptable} \cdot Q$$

$$2.5 \cdot GHz \cdot 30 \cdot in \approx 1 \cdot MHz \cdot 1 \cdot mi$$





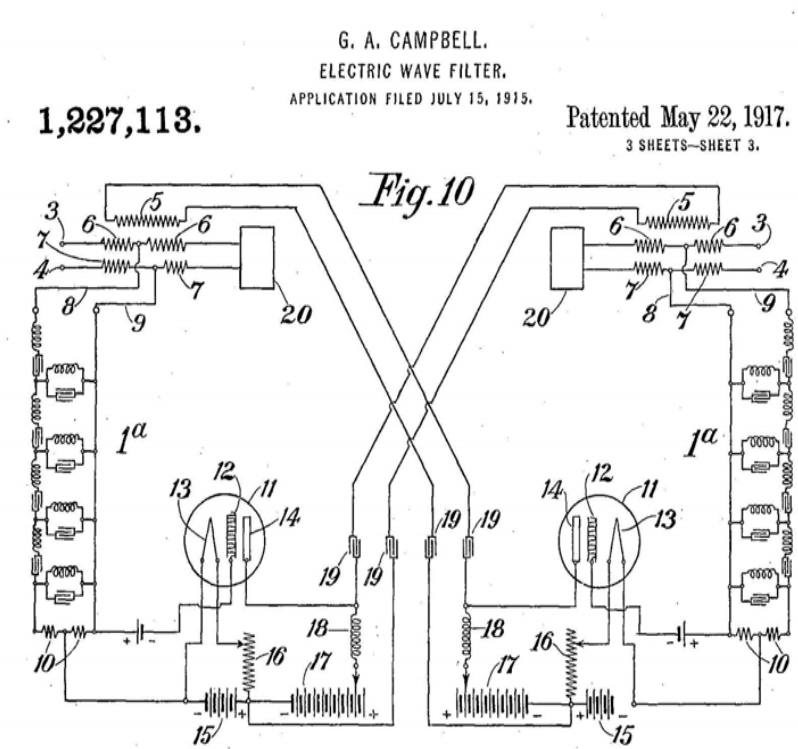
- **For a given frequency, loss is proportional to length**
- **For a given length, loss is proportional to frequency.**

- **Channel quality depends on loss characteristics vs. frequency and length**
- **2.5 GHz over 30 in. is same problem as 1 MHz over 1 mi.**

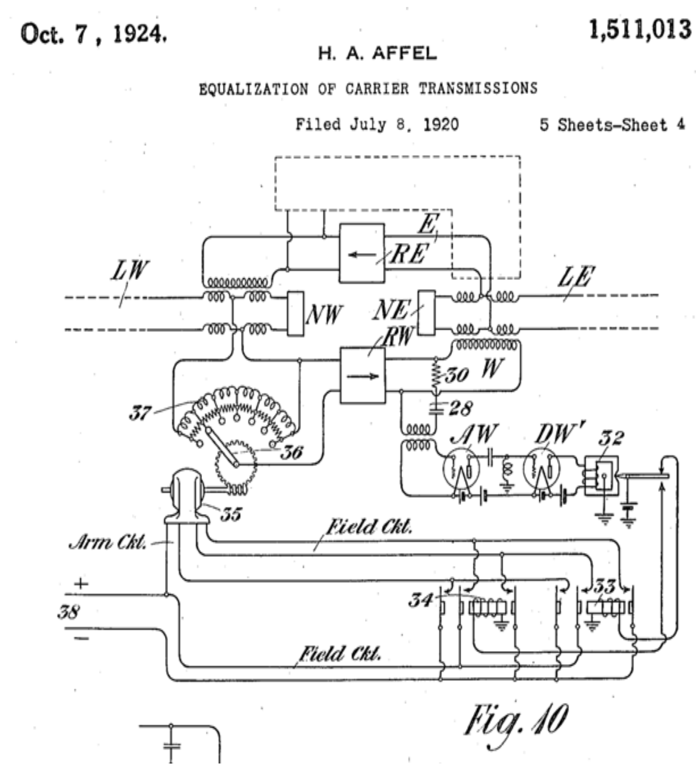
Equalization increases the acceptable loss number, thereby increasing either speed or length or both

Equalizer History

Electric Wave Filter, 1915



Adjustable Equalizer, 1920



Courtesy of Clark Foley, Maxim Corp. and the U.S. Patent Office

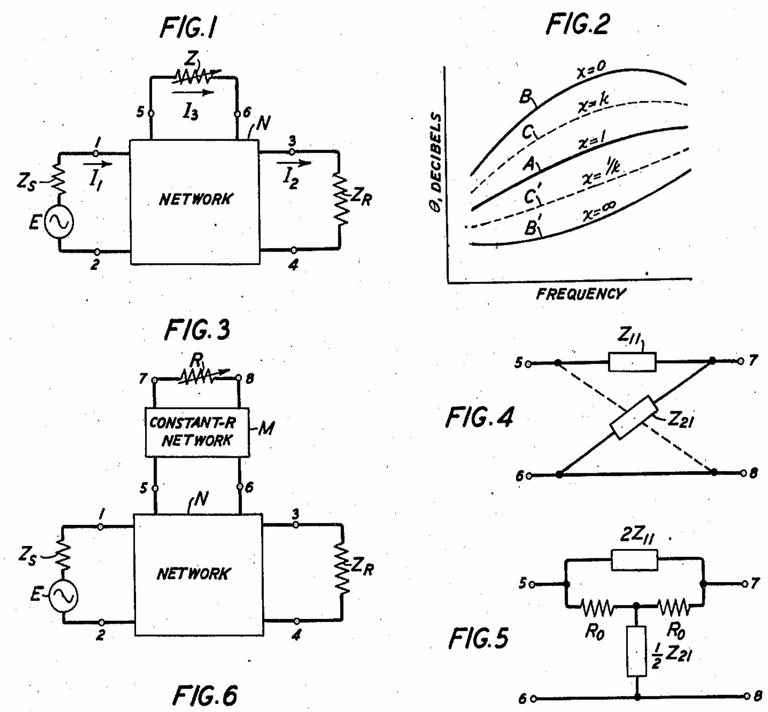
Equalizer History

Constant R and Repeaters 1936, 1939

Oct. 19, 1937. H. W. BODE 2,096,027

ATTENUATION EQUALIZER

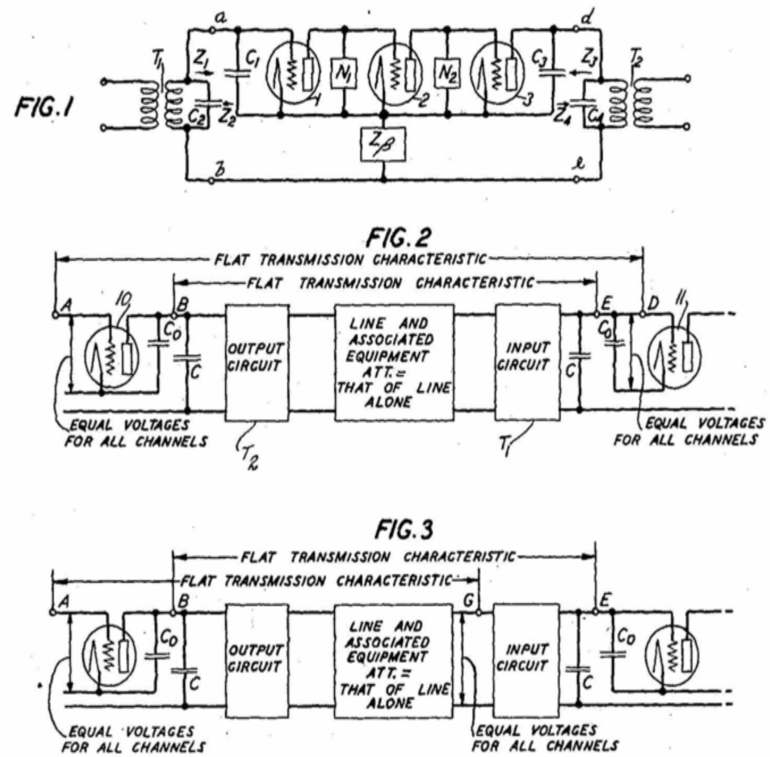
Filed Jan. 30, 1936 4 Sheets-Sheet 1



May 20, 1941. H. W. BODE 2,242,878

DESIGN OF BROAD BAND REPEATERS

Filed Sept. 29, 1939 9 Sheets-Sheet 1



Courtesy of Clark Foley, Maxim Corp. and the U.S. Patent Office

Equalizer History

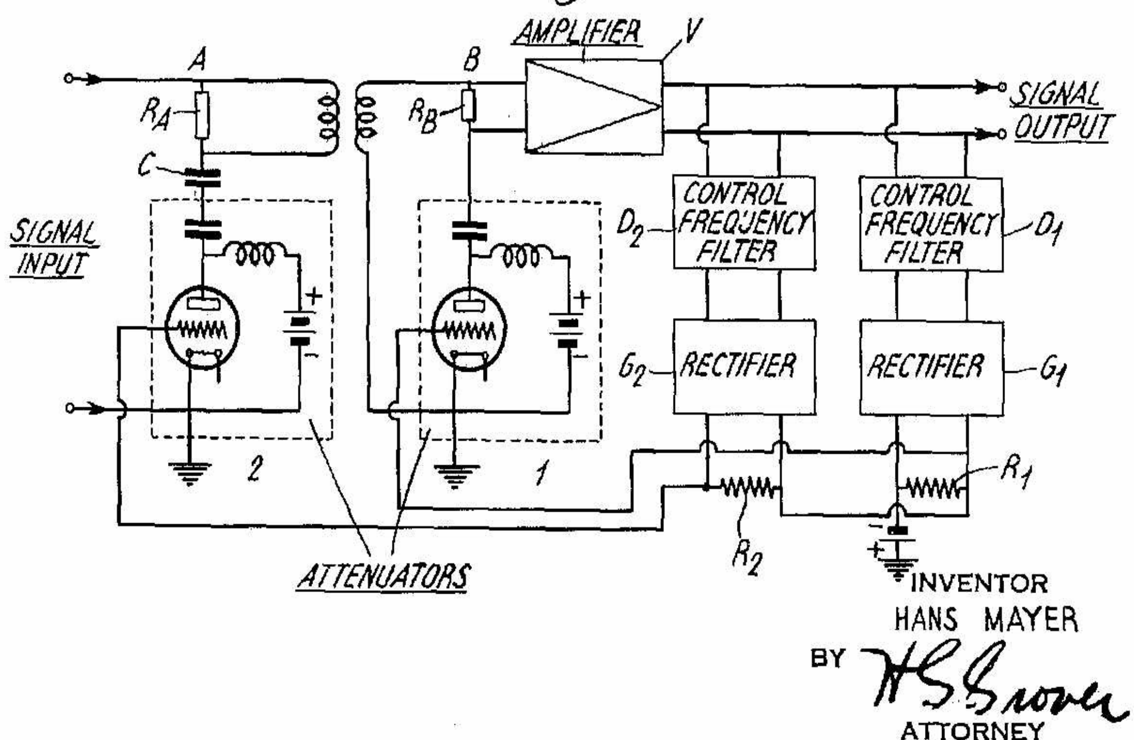
Automatic/Adaptive, 1935

Sept. 15, 1936. H. MAYER 2,054,657

AUTOMATIC SELECTIVE FADING CONTROL CIRCUITS

Filed Feb. 28, 1935

Fig. 3



Courtesy of Clark Foley, Maxim Corp. and the U.S. Patent Office

The Undersea Cable System (1956)

TABLE I

Submarine Cable Summary

	SB	SD	SF	SG	(?)[a]
Service Date of First Installation	1956	1963	1968	1976	1983-1985
Top Freq. (MHz)	0.164	1.05	6	30	125
No. of Channels (3 kHz)	48	138	845	4000	16 000
Coax Dia.	5/8″	1″	1.5″	1.7″	2¼″
Repeater Spacing (nmi)	38	20	10	5	2½
Max. Length Capability	2000	4000	4000	4000	4000
No. of Rptrs. in Max. Length	58	210	420	815	1660
Length of Ocean Block (Spacing Between Ocean Block Equalizers)	200	192	192	150	75
Repeater Gain (Top Freq.)	60	50	40	41	38
Approx. Relative First Cost/ Channel-Mile ($)[b]	1	1/4	1/10	1/30	1/60
Type of Rptr.	Physical 4-wire (2 Cables)	Equiv. 4-wire (1 Cable 1 A)	Equiv. 4-wire (1 Cable 1 A)	Equiv. 4-wire (1 Cable 1 A)	Equiv. 4-wire (1 Cable 2 A)
Active Device	Tube	Tube	Germanium Transistor	Silicon Transistor	Silicon Transistor
Type of Cable (Deep Sea)	Armored	Armorless	Armorless	Armorless	Armorless
Repeater Housing	Flexible	Rigid	Rigid	Rigid	Rigid
Max. Terminal Voltage (Including Earth Potential)	2600	6000	4200	7000	?

[a]Planning estimates.

[b]Cost relative to the first (SB) system.

[1]The SG Submarine Cable System is a joint development, with the French Post Office having primary responsiblity for the cable, and the Bell System having primary responsibility for repeaters and equalizers. More generally, the British, French, and Japanese have been active in the submarine cable field throughout.

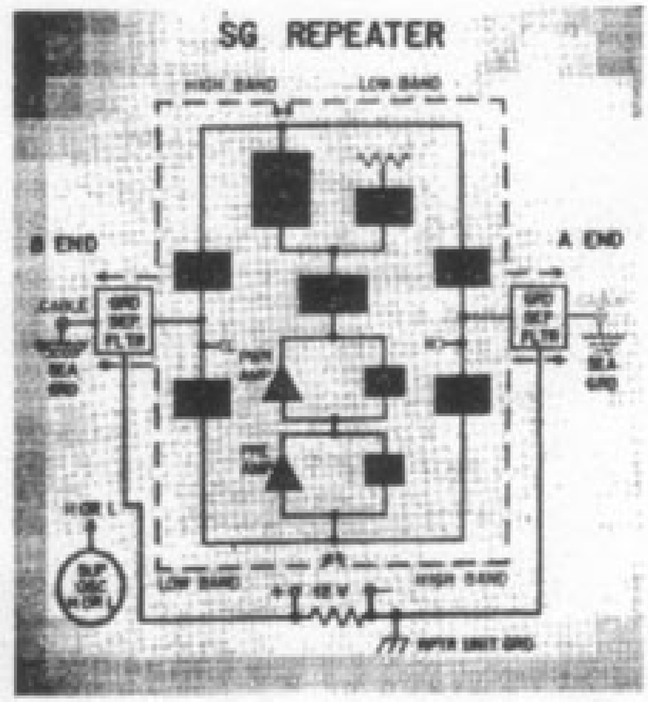


Fig. 3. Functional block diagram of undersea repeater.

- Robert L. Easton. Undersea cable systems--a survey, or, Explanation to an unknown lady in Philadelphia. IEEE Communications Society XIII(5):12-15, September 1975.

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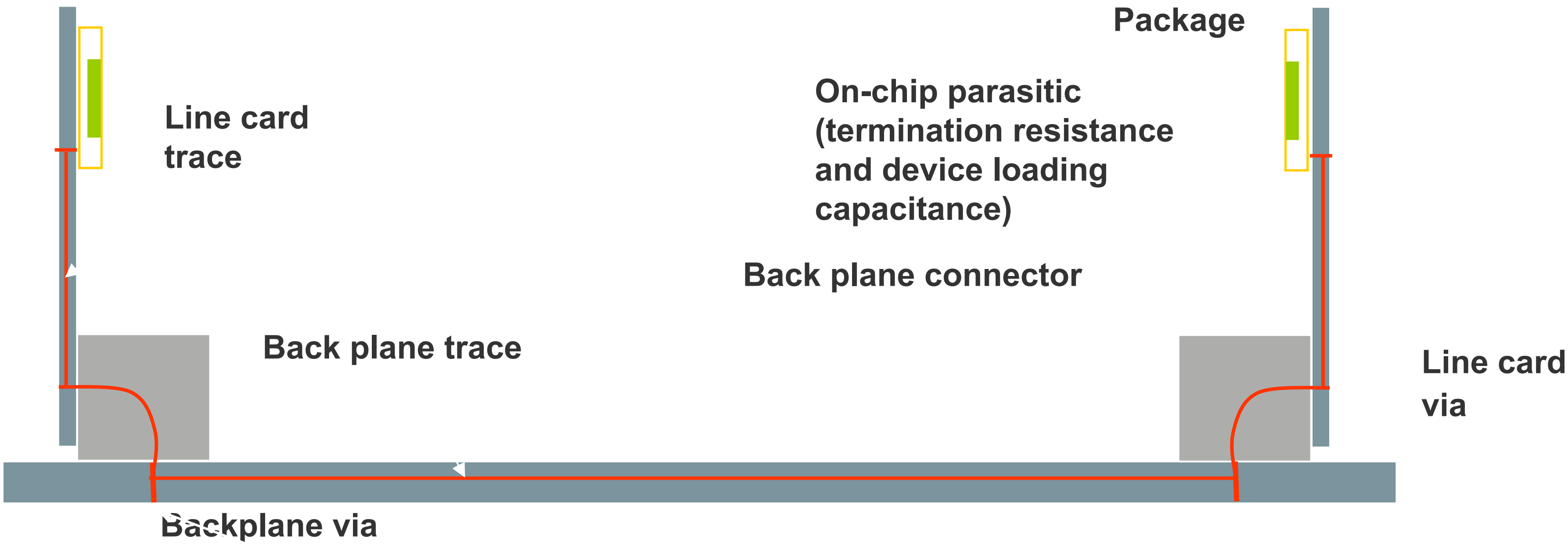
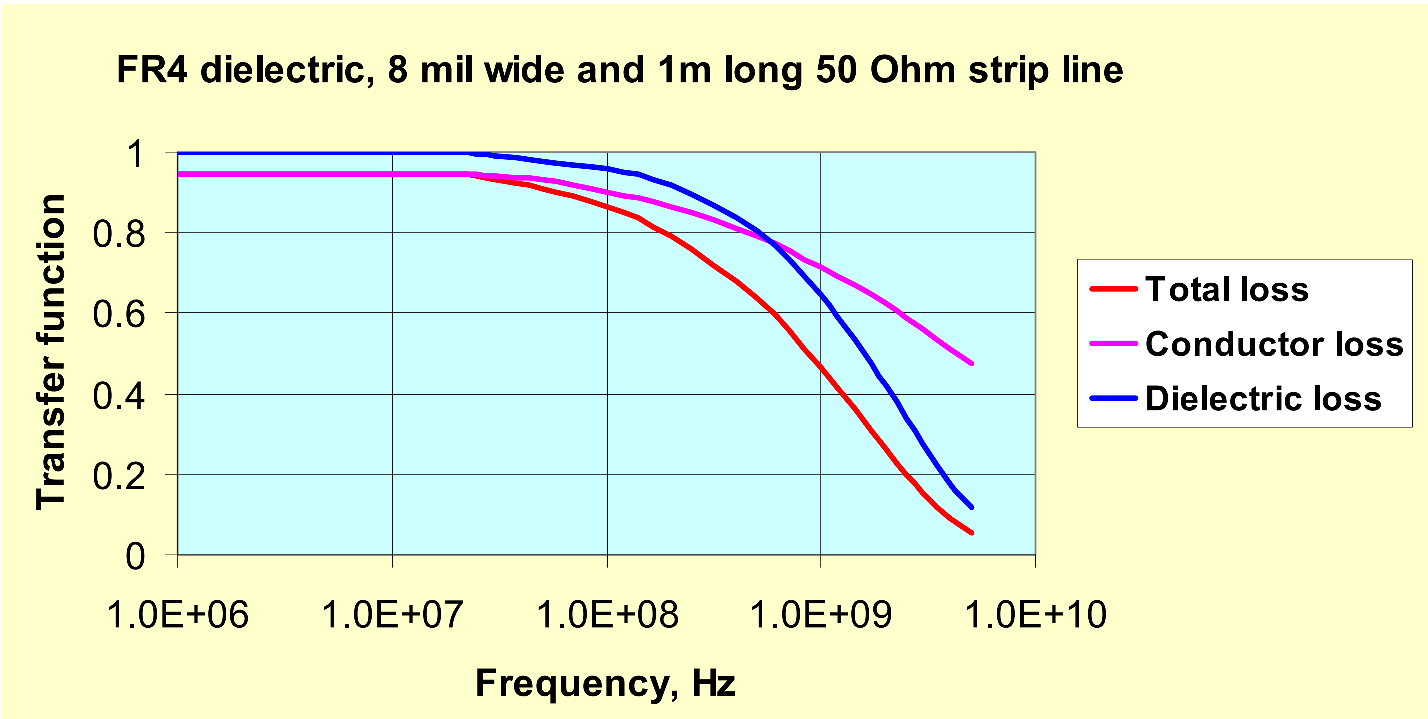
Example : The Backplane Environment



- Critical issues to account for:
  - loss, reflections, crosstalk, skew
- In a backplane there are many sources of Z and thus many possible sources of reflections

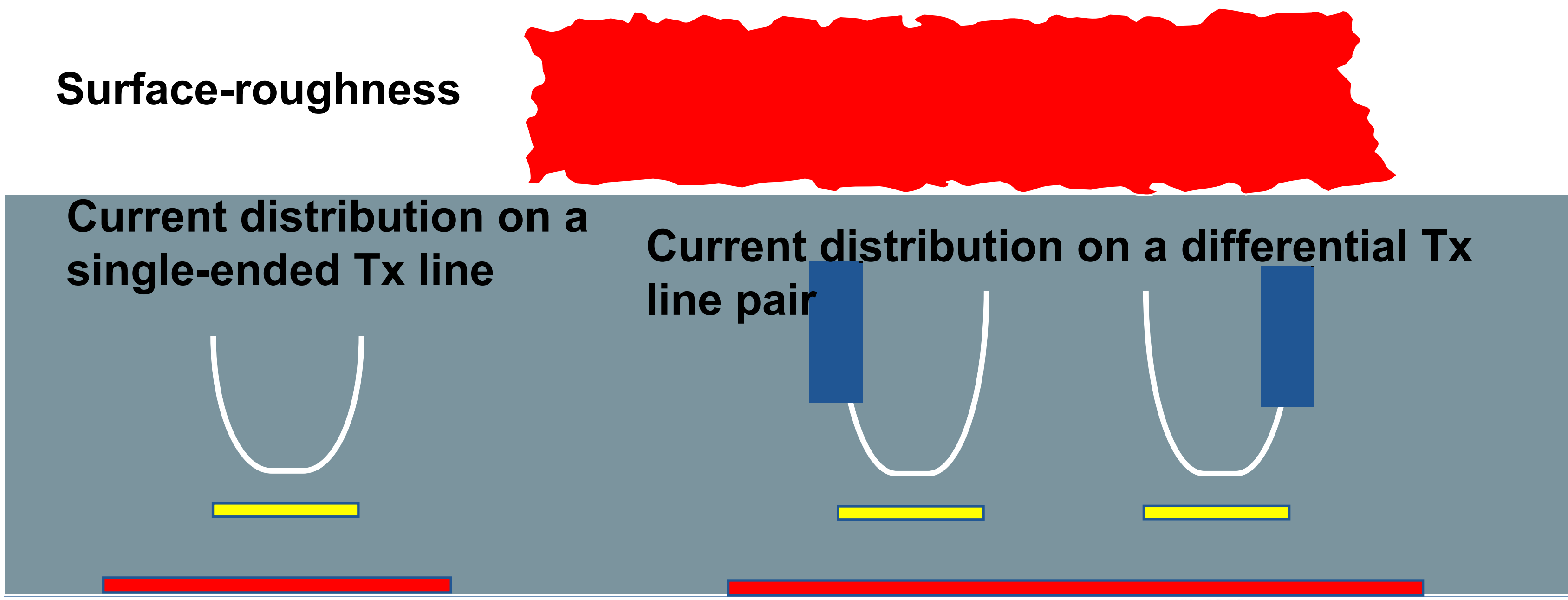
Conductor and Dielectric Losses

- **Loss in dB/unit length = 4.35 [R(f)/Z_0 + G(f) Z_0]**
  - **Resistance of the conductor, R(f) = R_0 + R_s (f)**
  - **Conductance of the dielectric, G(f) = G_0 + 2 π f δ C**



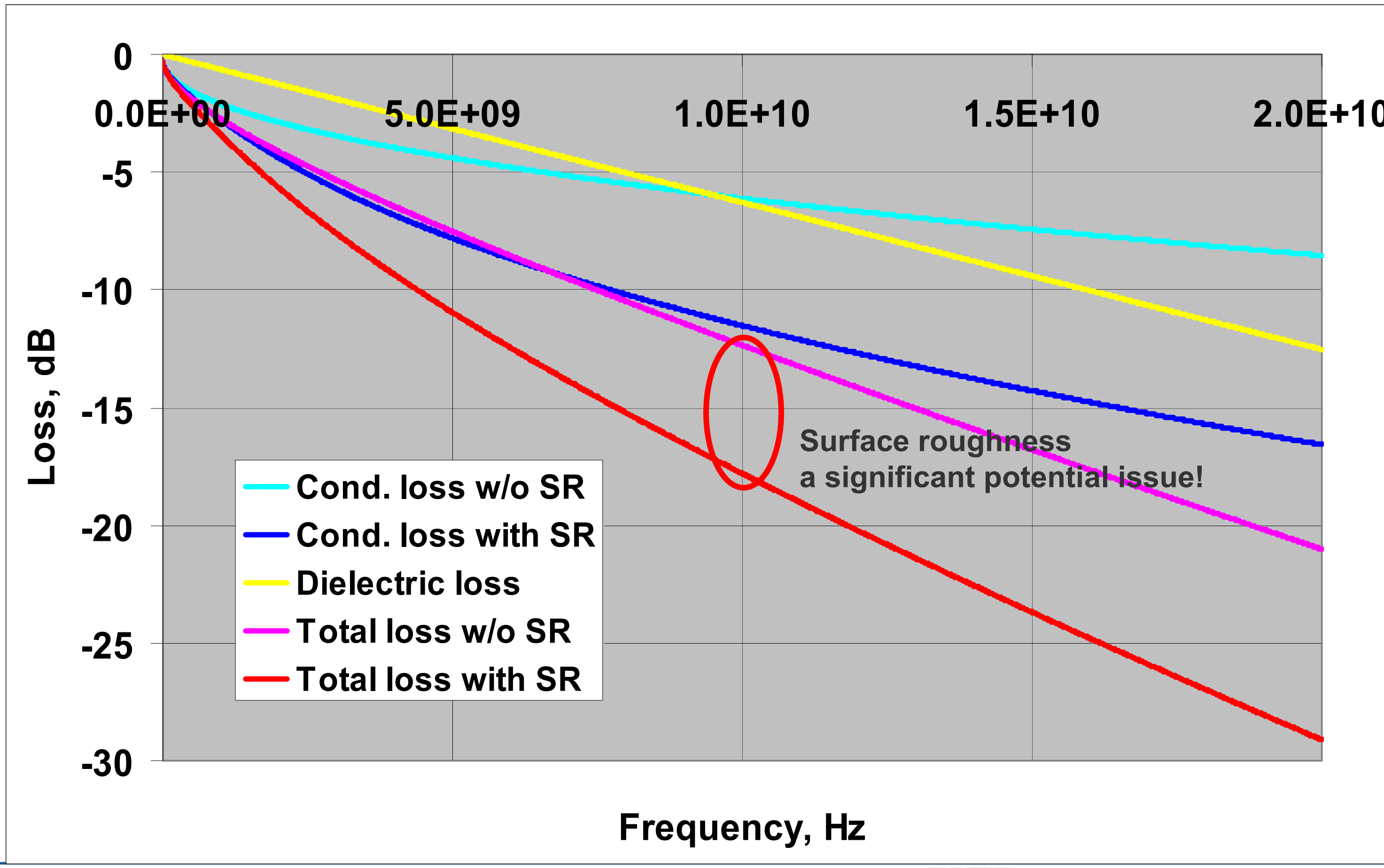
Modeling of Conductor Losses

- Conductor surface is assumed to be uniform
- Current distribution is assumed to be uniform
- Surface-roughness increases resistance by as much as 50% as skin depth approaches and eventually becomes smaller than surface-roughness



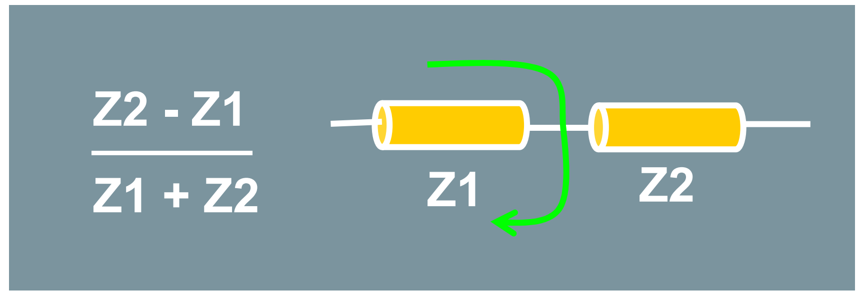
Decomposition of Trace Loss for a Low Loss Dielectric Material (Tanδ = 0.007)

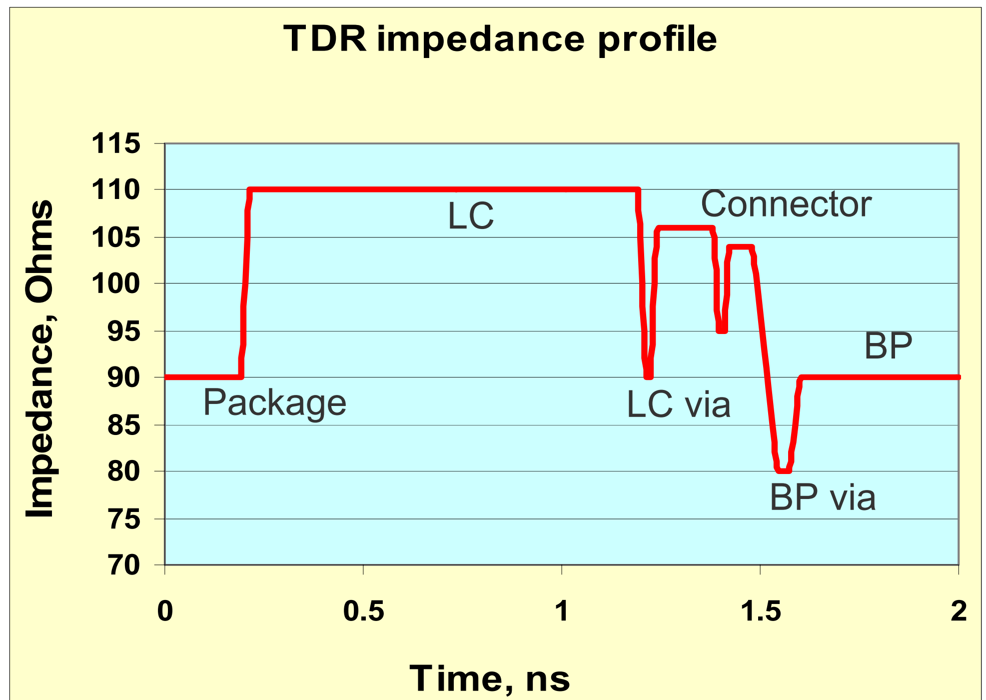
- 20" long, 6 mil wide and ½ Oz thick 50Ω trace
- RMS surface roughness: 1.3 μm

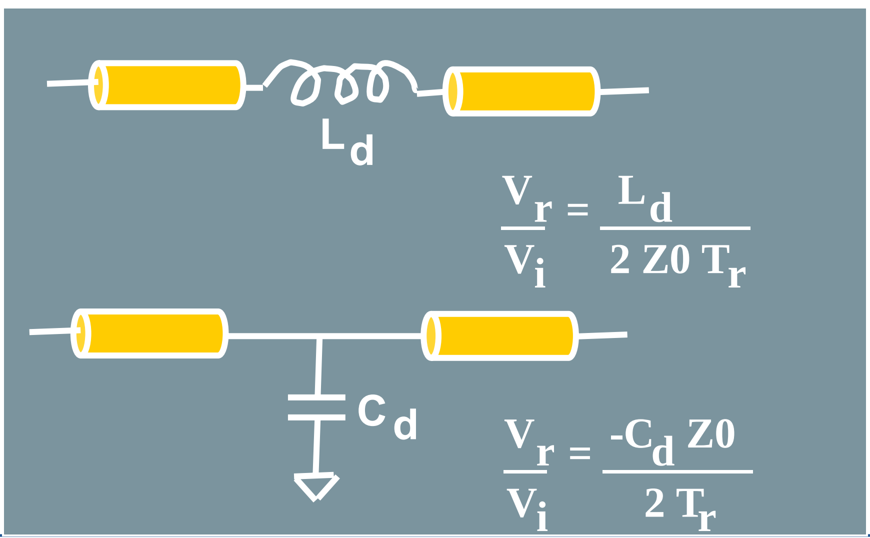


Reflections

- **Sources of Reflections : Z - Discontinuities**
  - **PCB Zs**
  - **Connector Zs**
  - **Vias (through) Zs**
  - **Package Zs**
  - **Termination Zs**





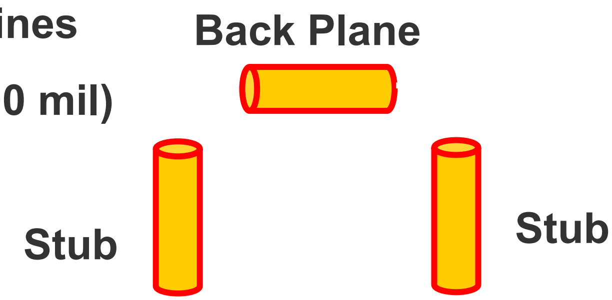


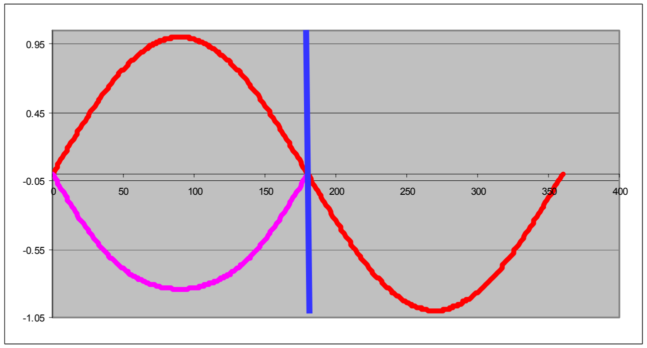
Resonance Notches
Due to Via Stub Reflections

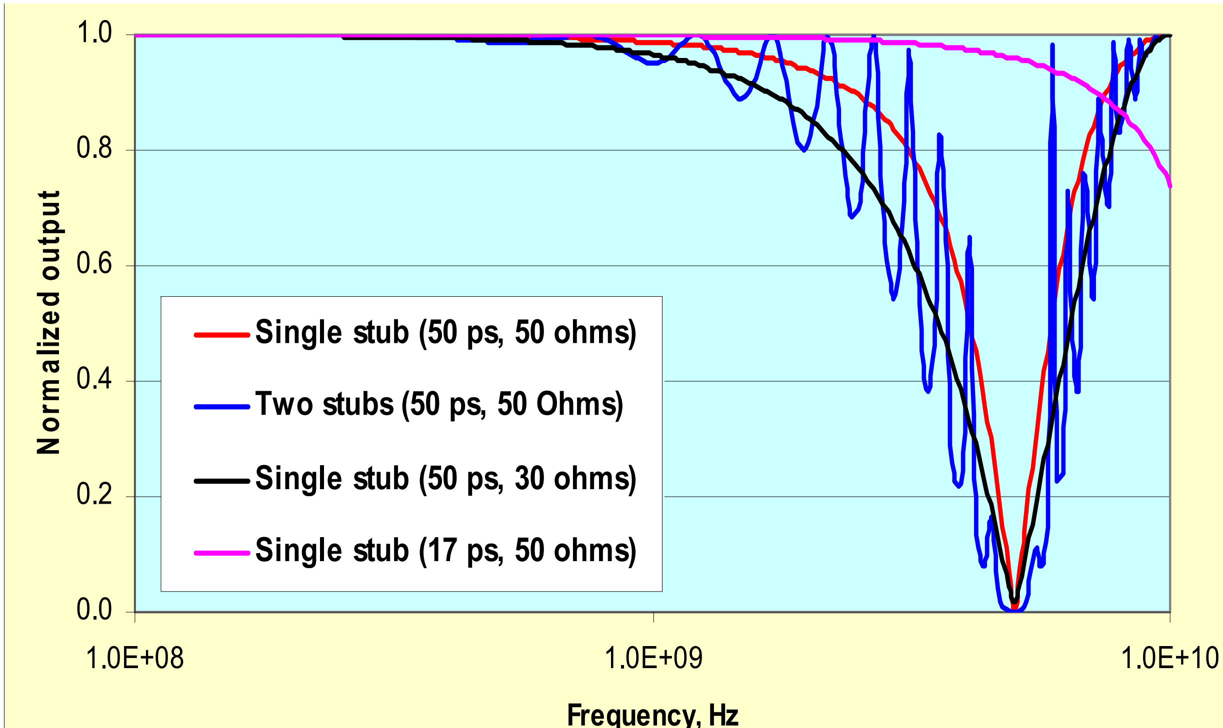
Loss less transmission lines

Stub length = 7.5 mm (300 mil)

Stub delay = 50 ps





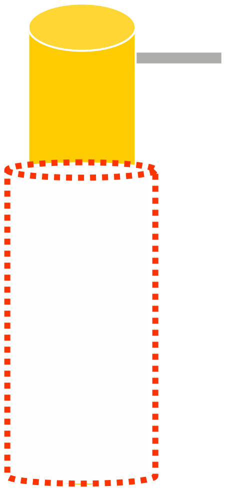


Stub length:

2.5mm

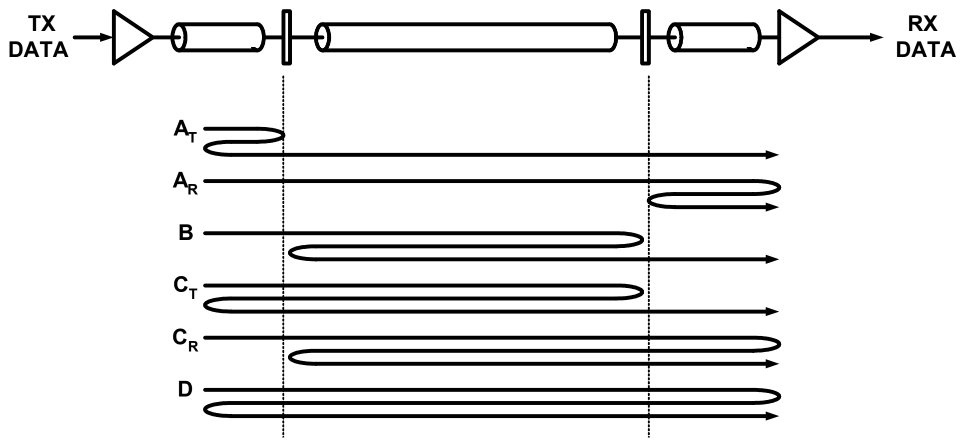
Backdrilling

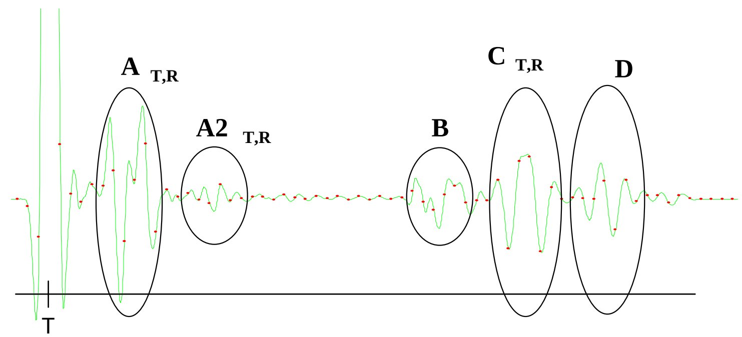
depth: 5mm



- **Surface mount connector with through-hole vias still dies not solve the problem**

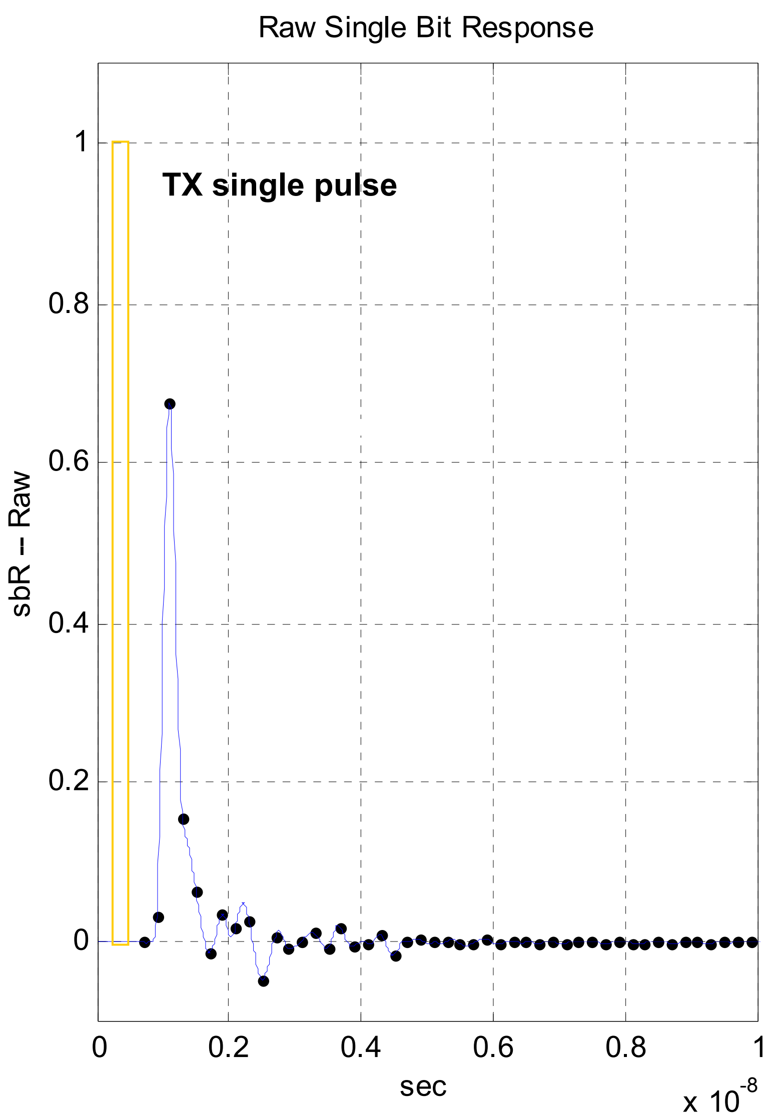
Reflections In Time : Multi-Path





- **Primary reflection sources are at the connector/backplane transition**
  - **Can be grouped in time – as a function of backplane length**

The Single Bit Response (SBR)



- What is observed at the receiver when the transmitter sends an unequalized single-bit pulse
  - Usually normalized at TX
  - Each dot is a symbol sample
- Can be very helpful in understanding nature of the system
  - Attenuation : reduction in amplitude of main pulse
  - Dispersion : spreading of the narrow pulse
  - Reflections : ripples off of Z-discontinuities

What Equalization Can & Can't Do

- Equalization is not a panacea…
  - Can't solve all signaling problems
  - Generally most powerful for
    - Dispersion
    - Attenuation
  - Sometimes useful for
    - Reflections (but takes a lot of taps)
  - In some cases can make worse
    - Crosstalk
      - αL*di/dt (inductive coupling) crosstalk can actually get worse relative to signal swing in TxEQ systems
- Equalization must be taken in context with the entire signaling problem

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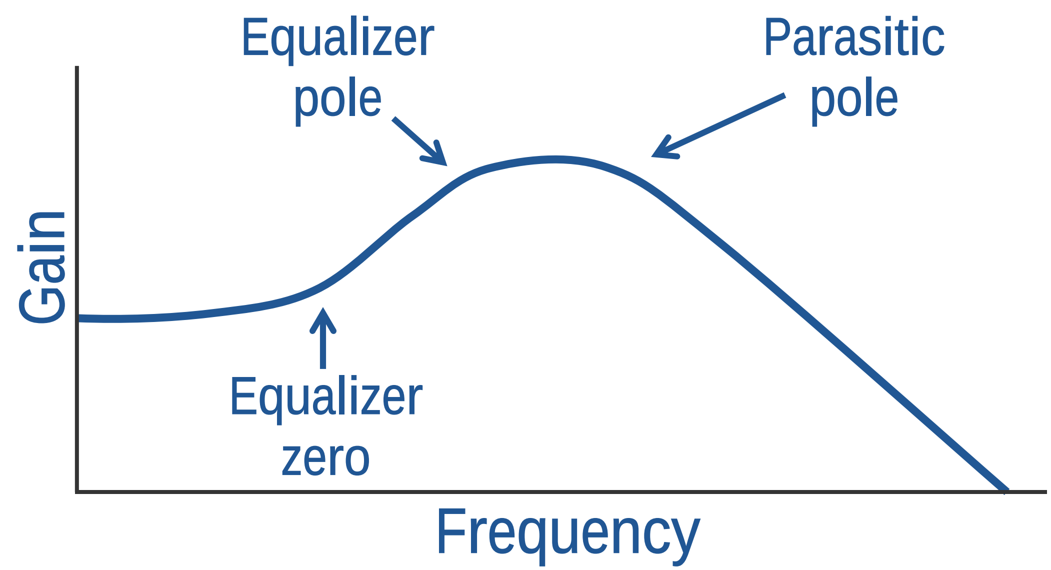
Equalizer overview

- **Linear**
  - **Unsampled**
    - **Continuous-time (CTLE)**
    - Transversal FIR
  - Sampled
    - Rx FIR
    - Tx FIR
- Non-linear
  - Decision Feedback Equalization (DFE)



PRO	• No Tx jitter amplification • Low power • Simple implementation • Xtalk amplification
CON	• Low order, limited flexibility • Limited range • Limited gain BW

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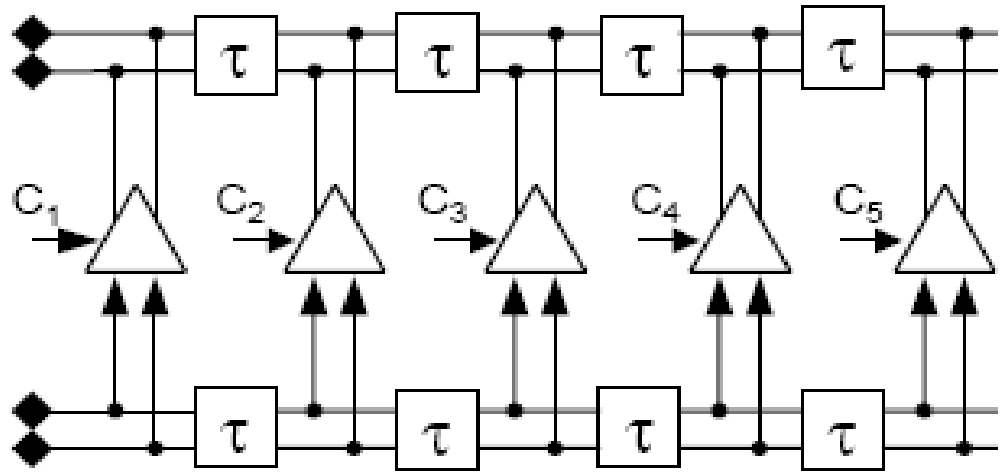

PRO	• No Tx jitter amplification • High-order, T/N equalizers feasible • Adaptivity doesn't require backchannel • Provides gain (peak power constraint)
CON	• Amplifies Xtalk and noise • Stringent LTI requirements for delay cells and amplifiers • Tuned to specific frequency

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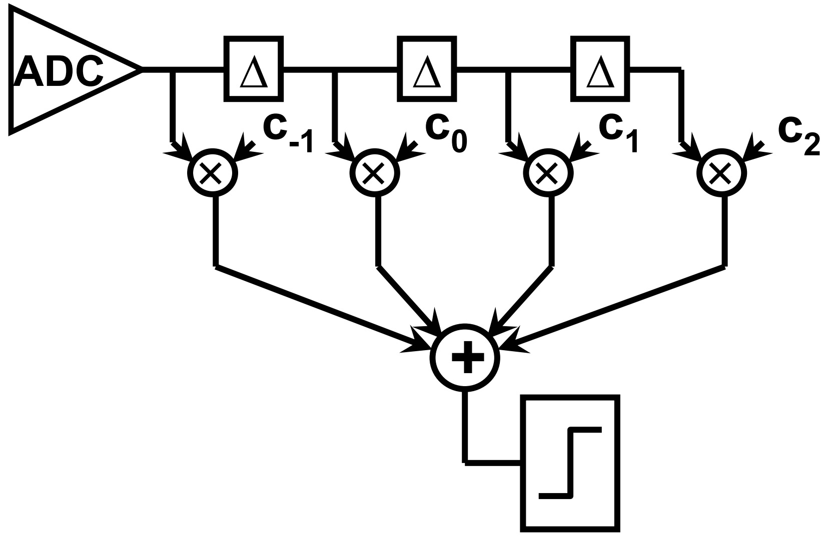

PRO	• No Tx peak power constraint as with Tx FIR
CON	• Implementation is challenging • Filter multiply and delay stages are analog signals or multi-bit digital signals • Higher power than Tx FIR

Equalizer overview

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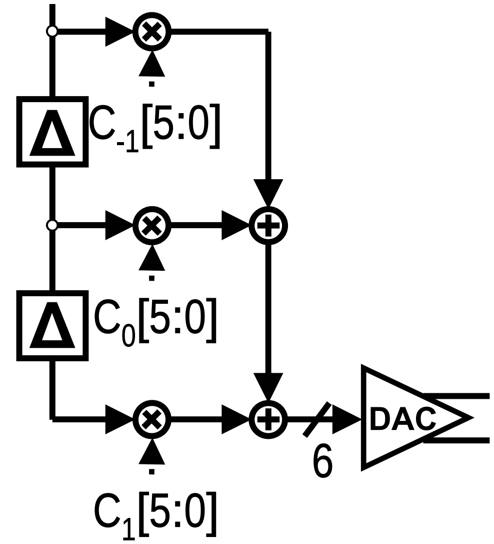

PRO	• Simple implementation • Lower power than Rx FIR • Multiply and delay stages are 1 bit wide • Good for “well-behaved” channels
CON	• Tx peak power constraint to prevent clipping • Backchannel required for adaptivity

Equalizer overview

- Linear
  - Unsampled
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    - Rx FIR
    - Tx FIR
- **Non-linear**
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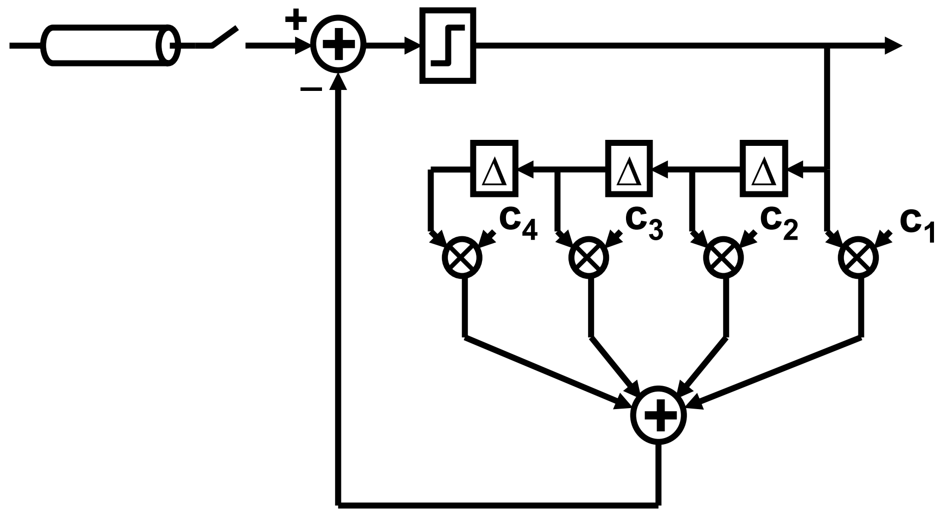

PRO	• **No noise or crosstalk amplification** • **Best for discontinuous channels**

CON	• **Speedpath from filter to slicer causes:**
	  • **Frequency limitations**
	  • **Redundant look-ahead filters resulting in high power & complexity**
	• **Error propagation**
	• **LE is usually still required**

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Most commonly used equalizers (focus of this presentation)

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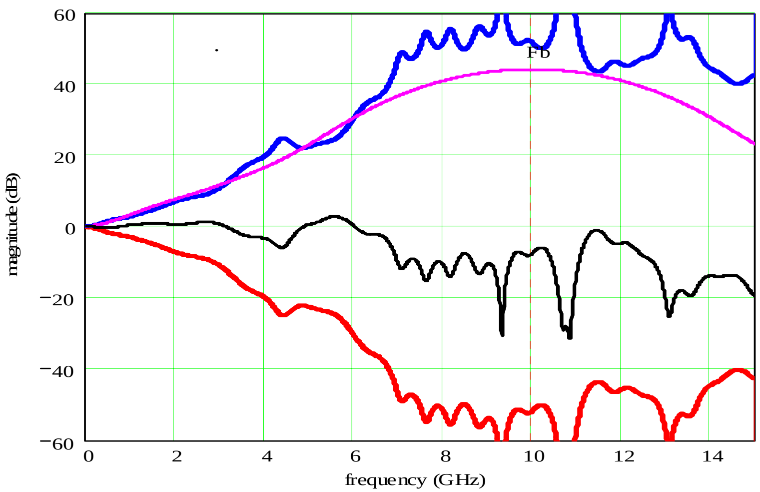
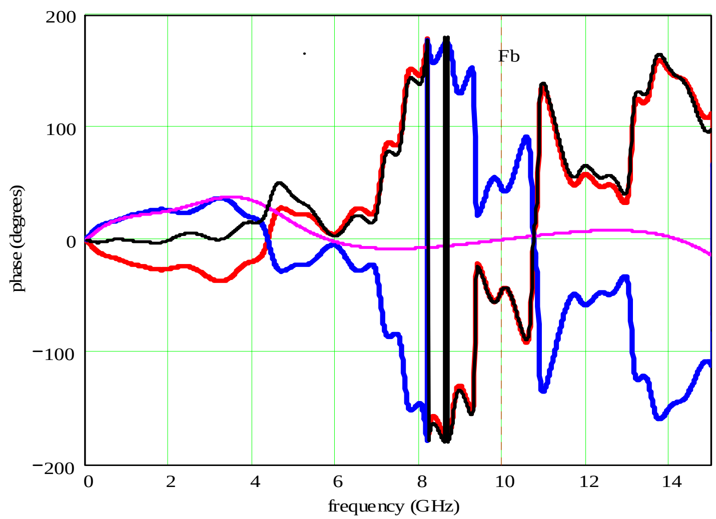
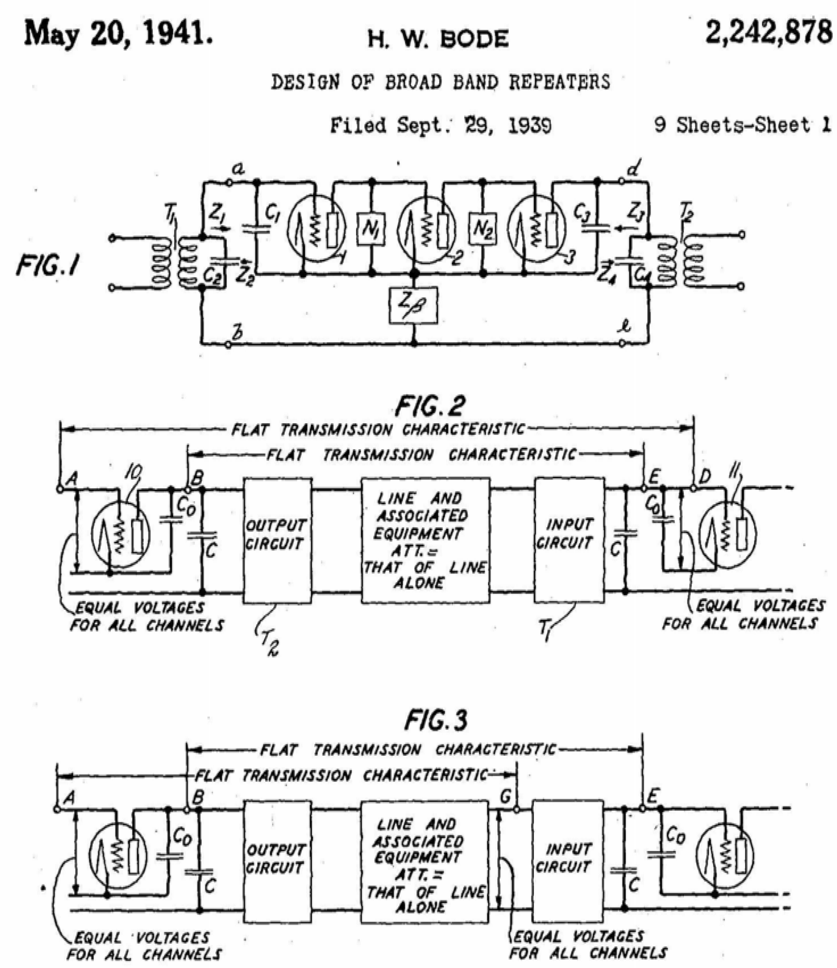
Views of Equalization Optimization

- Frequency Response Compensation (Opposing Channel Effects)
- ISI elimination (Zero Forcing)
- Mean-Squared Error Minimization (Deterministic "Noise" Minimization)
- Bit-Error Rate (Ratio) Reduction

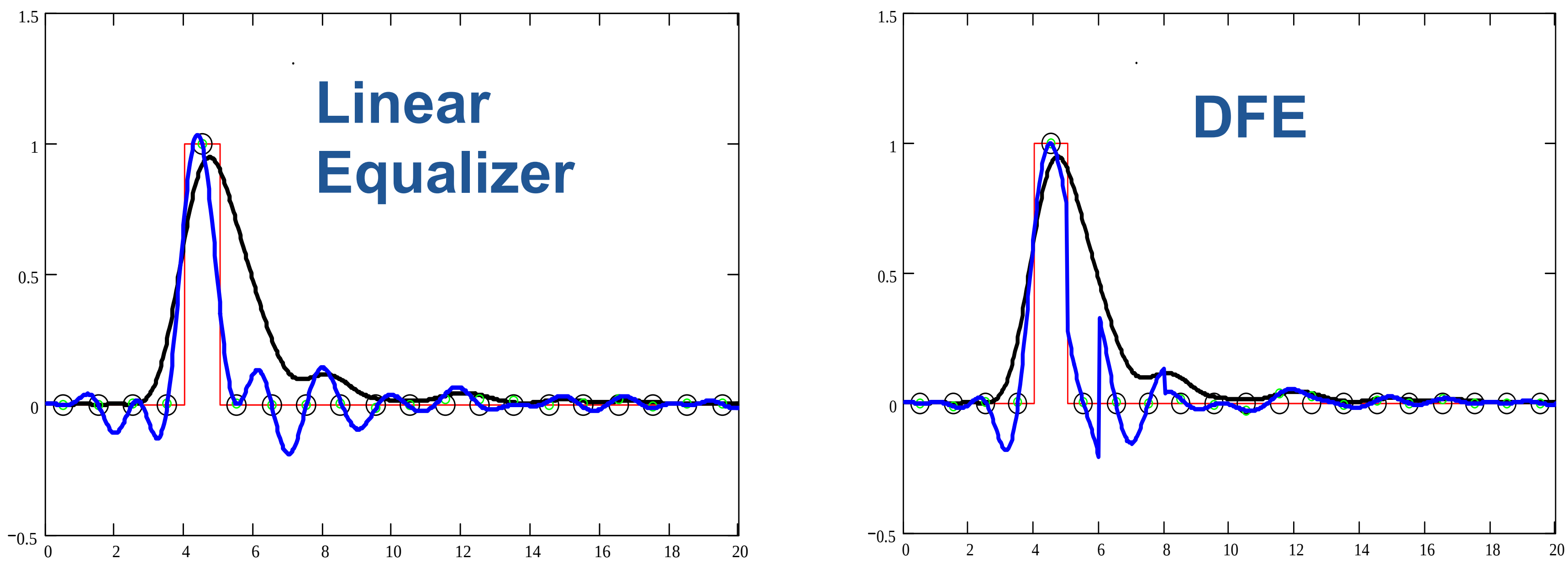
Frequency Response Compensation





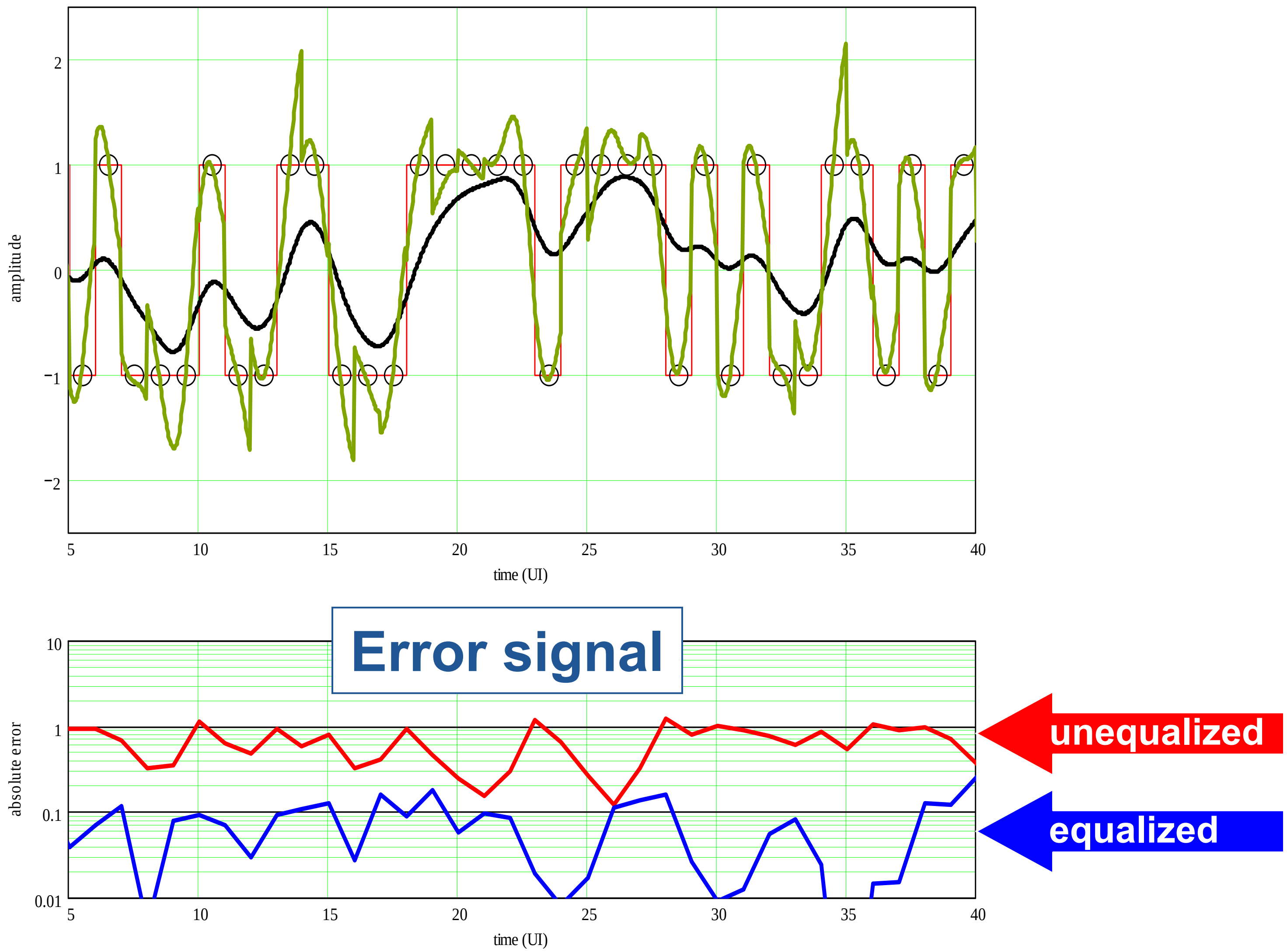


Zero Forcing Optimization



- Isolated pulse response is “forced” to go through zero in all bit positions other than the position of the isolated bit
- Can be implemented in a least-squares sense
- Zero forcing does not dictate an equalizer topology

Minimum Mean-Squared Error



LMS Algorithm Derivation

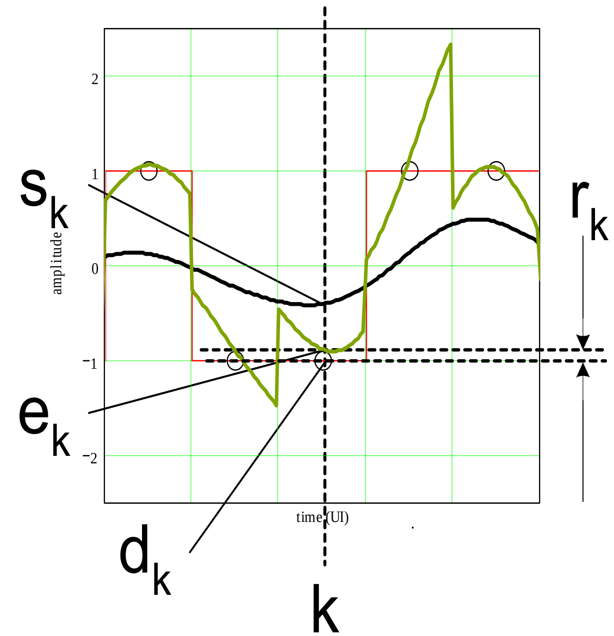
- **k is the index of a waveform point at the decision point**
- **s_k – sample of waveform**
- **d_k – ideal value of waveform**
- **e_k – sample of equalized waveform**
- **r_k – residual error**
- **w_k - weight**

$$e_k = E(k \cdot UI)$$

Equalizing Function – Also a function of coefficients a_m.

perhaps a function of s_k and or d_k

$$r_k = e_k - d_k$$



- **Goal is to minimize weighted mean-squared error.**

$$mse = \sum_k w_k \cdot r_k^{\,2}$$

Newton's Method in Multiple Variables

- **weighted mean-squared error is minimized when gradient is zero for all equalizer filter coefficients.**

$$F(a) = \frac{\partial}{\partial a_m} \sum_k w_k \cdot r_k^{\ 2} = 0$$

$$F(a_0 + \Delta a_0, a_1 + \Delta a_1, \ldots) =$$

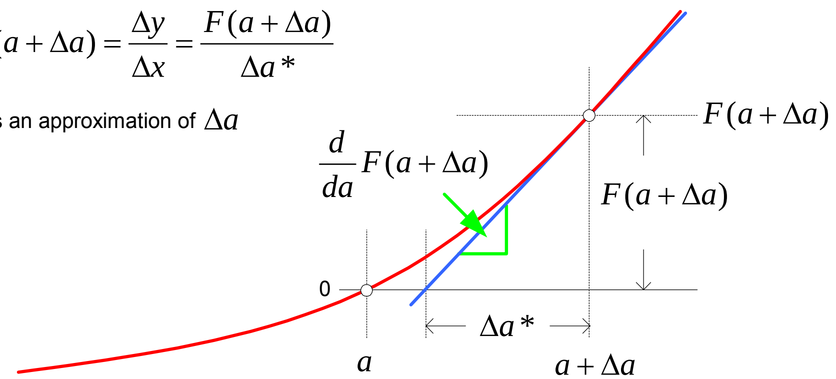
$$F(a_0, a_1, \ldots) + \Delta a_0 \frac{\partial}{\partial a_0} F(a_0, a_1, \ldots) + \Delta a_1 \frac{\partial}{\partial a_1} F(a_0, a_1, \ldots) + \ldots + O(\|\Delta a\|^2)$$

$$F(a^* + \Delta a) \cong F(a^*) + \sum_n \Delta a_n \cdot \frac{\partial}{\partial a_n} F(a^*)$$

$$\frac{d}{da} F(a + \Delta a) = \frac{\Delta y}{\Delta x} = \frac{F(a + \Delta a)}{\Delta a^*}$$

Δa^* is an approximation of Δa

$$F(a) \cong \sum_n \Delta a_n \cdot \frac{\partial}{\partial a_n} F(a)$$



Iterative LMS method

$$F(a) = \frac{\partial}{\partial a_m} \sum_k w_k \cdot r_k^{\ 2} = 0 \qquad F(a) \cong \sum_n \Delta a_n \cdot \frac{\partial}{\partial a_n} F(a)$$

$$\frac{\partial}{\partial a_m} \sum_k w_k \cdot r_k^{\ 2} = \sum_n \Delta a_n \cdot \frac{\partial}{\partial a_n} \left(\frac{\partial}{\partial a_m} \sum_k w_k \cdot r_k^{\ 2} \right)$$

- **Take a guess at a, solve for Δa, subtract Δa from a to obtain a better guess at a. Do this over and over again.**

Linear Algebraic Solution

$$\frac{\partial}{\partial a_m}\sum_k w_k \cdot r_k^{\,2} = \sum_n \Delta a_n \cdot \frac{\partial}{\partial a_n}\left(\frac{\partial}{\partial a_m}\sum_k w_k \cdot r_k^{\,2}\right)$$

$$\Downarrow$$

$$\sum_k w_k \cdot r_k \cdot \frac{\partial}{\partial a_m} r_k = \sum_n \Delta a_n \cdot \left(\sum_k w_k \cdot \left(r_k \cdot \frac{\partial^2}{\partial a_n \partial a_m} r_k + \frac{\partial}{\partial a_n} r_k \cdot \frac{\partial}{\partial a_m} r_k\right)\right)$$

$$J_{k,m} = \frac{\partial}{\partial a_m} r_k \quad \Leftarrow \quad \boxed{\text{Jacobian Matrix}} \qquad W_{k,k} = w_k \quad \Leftarrow \quad \boxed{\text{Weights Matrix}}$$

$$H_{n,m} = \sum_k w_k \cdot \left(r_k \cdot \frac{\partial^2}{\partial a_n \partial a_m} r_k + \frac{\partial}{\partial a_n} r_k \cdot \frac{\partial}{\partial a_m} r_k\right) \quad \Leftarrow \quad \boxed{\text{Hessian Matrix}}$$

$$g = J^T \cdot W \cdot r = H \cdot \Delta a \qquad \Delta a = H^{-1} \cdot \left(J^T \cdot W \cdot r\right)$$

Simplified Solution

$$H_{n,m} = \sum_k w_k \cdot \left(\cancel{r_k \cdot \frac{\partial^2}{\partial a_n \partial a_m} r_k} + \frac{\partial}{\partial a_n} r_k \cdot \frac{\partial}{\partial a_m} r_k \right)$$

Hessian Matrix

$$H_{n,m} \approx \sum_k w_k \cdot \left(\frac{\partial}{\partial a_n} r_k \cdot \frac{\partial}{\partial a_m} r_k \right) = J^T \cdot W \cdot J$$

Approximate Hessian Matrix

$$\Delta a = H^{-1} \cdot g \approx \left(J^T \cdot W \cdot J\right)^{-1} \cdot J^T \cdot W \cdot r$$

The Levenberg-Marquardt Algorithm

$$\Delta a = H^{-1} \cdot g = \left(J^T \cdot W \cdot J\right)^{-1} \cdot J^T \cdot W \cdot r$$

$$H \rightarrow H + \lambda \cdot D$$

- **D – matrix containing diagonal elements of H, zero elsewhere**
- **λ – scalar steering parameter.**

λ small favors Newton-Gauss	λ large favors gradient walk
$H + \lambda \cdot D \approx H$	$H + \lambda \cdot D \approx \lambda \cdot I$
$\Delta a = H^{-1} \cdot g$	$\Delta a \approx \frac{1}{\lambda} \cdot g$

- **On successful iterations λ is divided by 10.**
- **On Unsuccessful iterations λ is multiplied by 10.**

$$mse = \frac{r^T \cdot W \cdot r}{K}$$

- **Success defined as reduction of weighted mean-squared error.**

Equalization Functions

$$E(k) = FFE(k) + DFE(k)$$

Linear Feed-Forward Equalizer
(LE, FFE, transversal filter,
tapped delay line filter)

Decision Feedback Equalizer
(DFE)

$$FFE(k) = \sum_{i=0}^{TF-1} v(k \cdot UI - TD_i) \cdot b_i$$

$$DFE(k) = \sum_{j=0}^{DF-1} dm_{k-1-j} \cdot c_j$$

- **In decision-directed learning, dm_k is determined by decoding the bit.**
- **Otherwise, dm_k can be replaced by d_k – the known ideal voltage (training sequence).**
- **TD is the tap delay**
- **b is a vector of FFE filter coefficients**
- **c is a vector of DFE filter coefficients**

Partial Derivatives

$$J_{k,n} = \frac{\partial}{\partial a_n} r_k = \frac{\partial}{\partial a_n}(e_k - d_k) = \frac{\partial}{\partial a_n} e_k$$

$$\frac{\partial}{\partial b_i} e_k = v(k \cdot UI - TD_i) \qquad \frac{\partial}{\partial TD_i} e_k = -b_i \frac{d}{dt} v(k \cdot UI - TD_i)$$

- **Usually, TD is fixed and set to either 1 or ½ of the unit interval (UI).**

$$FFE(k) = \sum_{i=0}^{TF-1} s_{k-i+pre} \cdot b_i \qquad DFE(k) = \sum_{j=0}^{DF-1} dm_{k-1-j} \cdot c_j$$

$$\frac{\partial}{\partial b_i} e_k = s_{k-i+pre} \qquad \frac{\partial}{\partial c_j} e_k = dm_{k-1-j}$$

General Purpose LMS Algorithm

$$E(k) = \sum_{i=0}^{TF-1} s_{k \cdot SPB - i + pre} \cdot b_i + \sum_{j=0}^{DF-1} d_{k-1-j} \cdot c_j$$

$$S_{k,i} = s_{k \cdot SPB - i + pre}$$

$$D_{k,j} = d_{k-1+j}$$

$$a = \begin{pmatrix} b \\ c \end{pmatrix}$$

$$J = \begin{pmatrix} S & D \end{pmatrix}$$

$$W_{k,k} = w_k$$

INPUTS

a is a vector containing the filter tap weights (DFE and FFE), K is the number of decision bits.
J is the matrix formed by augmenting S with D (sampled and ideal voltages).
W is the weights matrix.
lambda constains the steering value to steer between gradient walk and Newton-Gauss.

$r = J \cdot a - d$		Calculate the equalized samples
$H = J^T \cdot W \cdot J$		Calculate the approximate Hessian Matrix
$D_{m,m} = H_{m,m} \qquad m \in 0 \ldots L-1$		Calculate the matrix with the diagonal elements of H
$\Delta a = (H + \lambda \cdot D)^{-1} \cdot J^T \cdot W \cdot r$		Calculate error
$mse_{initial} = r^T \cdot W \cdot r$		Calculate the initial mean-squared error (could have been retained from last iteration)
$mse_{final} = (SD \cdot (a - \Delta a) - d)^T \cdot W \cdot (SD \cdot (a - \Delta a) - d)$		Calculate the mean-squared error after correction
$mse_{final} < mse_{initial}$? true	false	Make changes to a and lambda depending on whether the iteration results in a reduction of the weighted mean-squared error
$\lambda = \lambda / 10$	$\lambda = \lambda \cdot 10$	If the iteration succeeds, make the correction an reduce lambda (favor Newton-Gauss convergence). If the iteration fails, keep the old mean-squared error and increase lambda (favor steepest decent).
$a = a - \Delta a$	$mse_{final} = mse_{initial}$	

OUTPUTS

a is the potentially adjusted, better estimate of the optimum values of the filter tap weights
lambda has been adjusted to favor Newton-Gauss convergence of steepest decent
mse_{final} is the mean-squared error after this iteration

Special LMS Algorithm

$$\Delta a = H^{-1} \cdot g = \left(J^T \cdot W \cdot J\right)^{-1} \cdot J^T \cdot W \cdot r$$

$$r = J \cdot a - d$$

$$\Delta a = \left(J^T \cdot W \cdot J\right)^{-1} \cdot J^T \cdot W \cdot (J \cdot a - d)$$

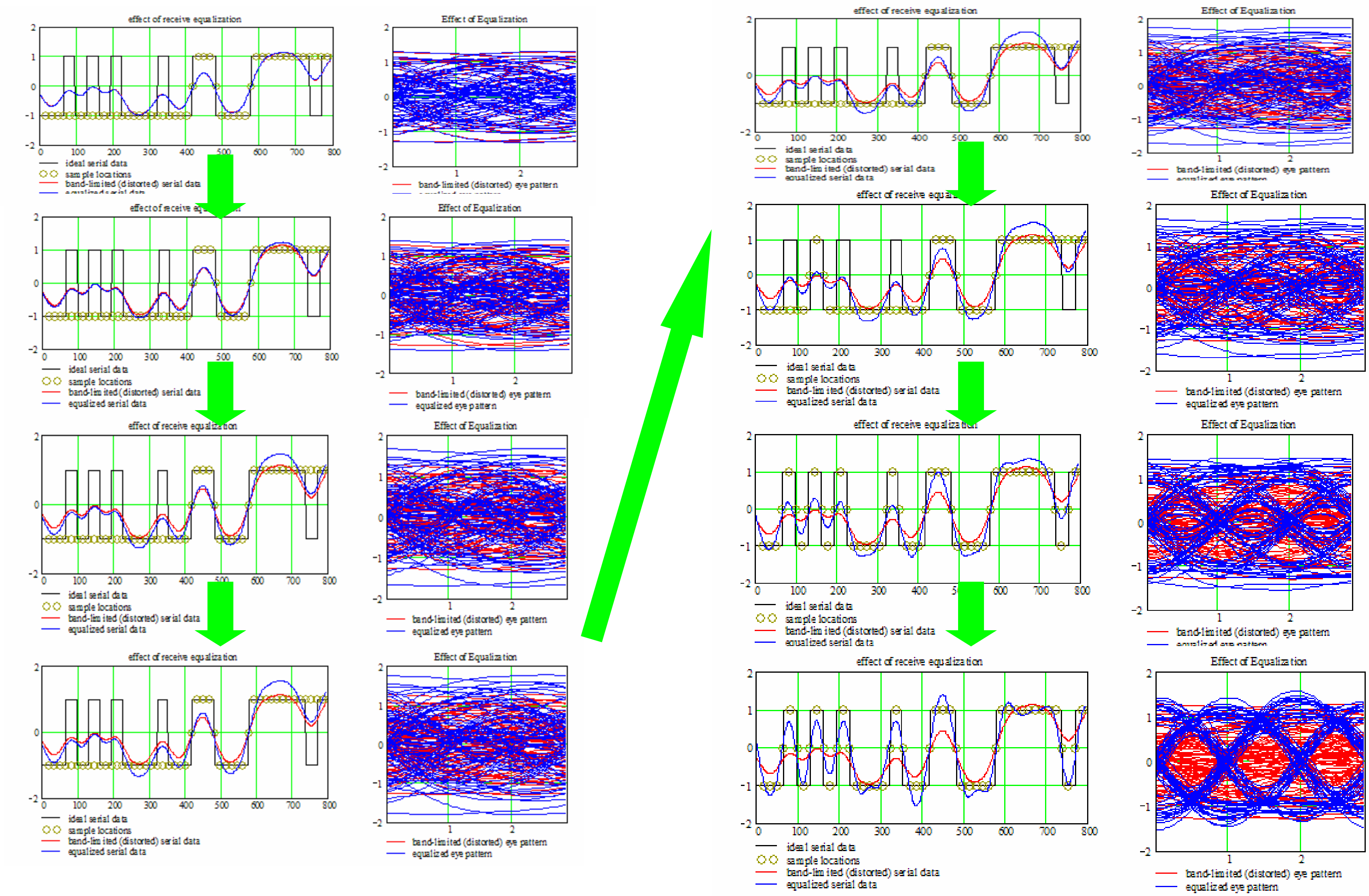
$$\Delta a = a - \left(J^T \cdot W \cdot J\right)^{-1} \cdot J^T \cdot W \cdot d$$

$$a^* = a - \Delta a = \left(J^T \cdot W \cdot J\right)^{-1} \cdot J^T \cdot W \cdot d$$

Works when:

- **Equalization function is linear.**
- **Tap Delays fixed**
- **Decision directed learning not employed.**
- **Clock recovery not considered**
- **Same as Zero Forcing when d vector contains isolated pulse**

Decision Directed Learning
(Blind Adaptation)

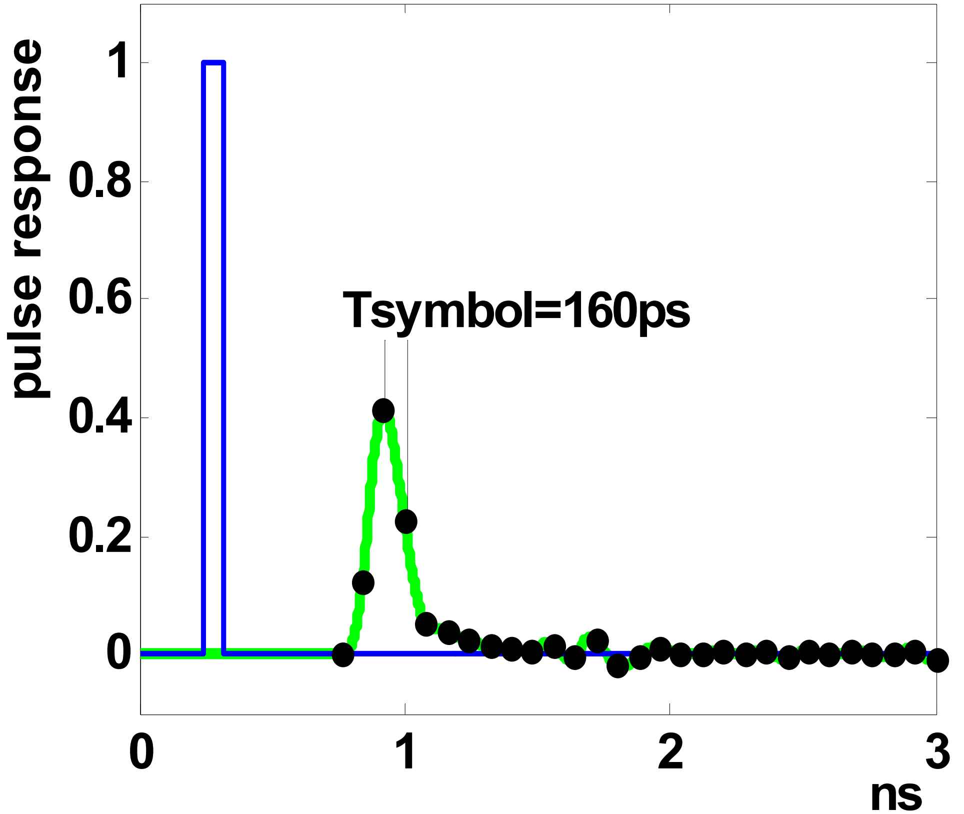


Serial Equalization *TechForum2007*

- (0:05) Scope of presentation
- (0:15) Background/history : goals, how have things been done
- (0:10) System environment issues for equalization
- (0:10) Equalization classification & qualitative tradeoffs
- (0:15) Communication theory
- **(0:30) Implementation issues I**
  - **Circuit implementation issues & tradeoffs : Rx LinEQ, Tx FIR, DFE**
  - **Clock recovery effects**
- (0:15) Break
- (0:15) Implementation issues II
- (0:40) Equalizer performance tradeoffs
- (0:10) Modeling methodology for equalization, adaptation
- (0:15) Measurement & instrumentation
- Summary & conclusions

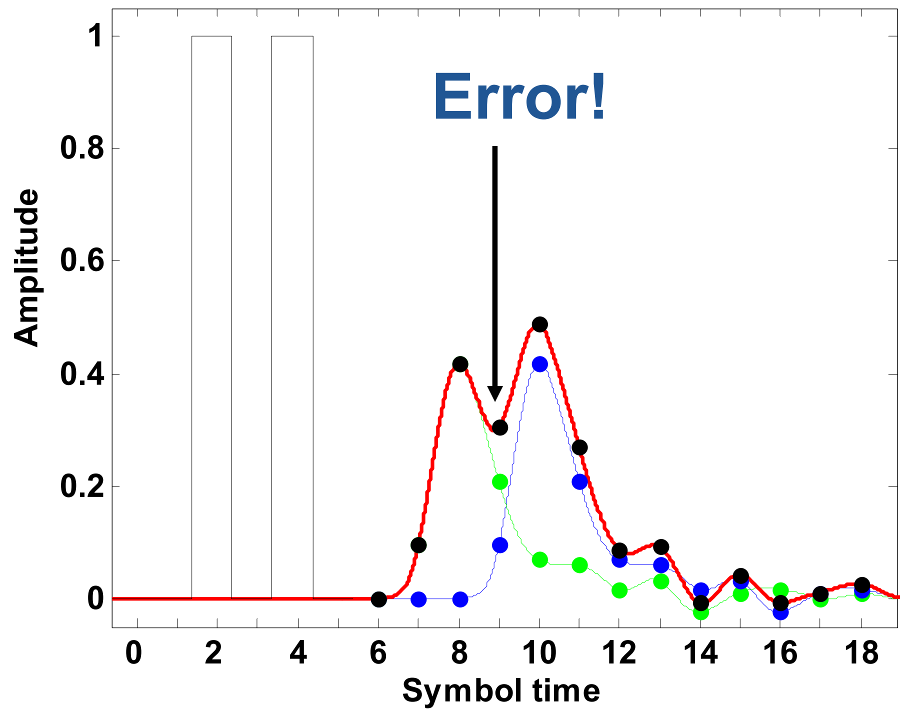
Dispersion Causes ISI

- Band-limited channels mean dispersion
  - Our nice short pulse gets spread out



- Dispersion – short latency (skin-effect, dielectric loss)
- Reflections – long latency (impedance mismatches – connectors, via stubs, device parasitics, package)

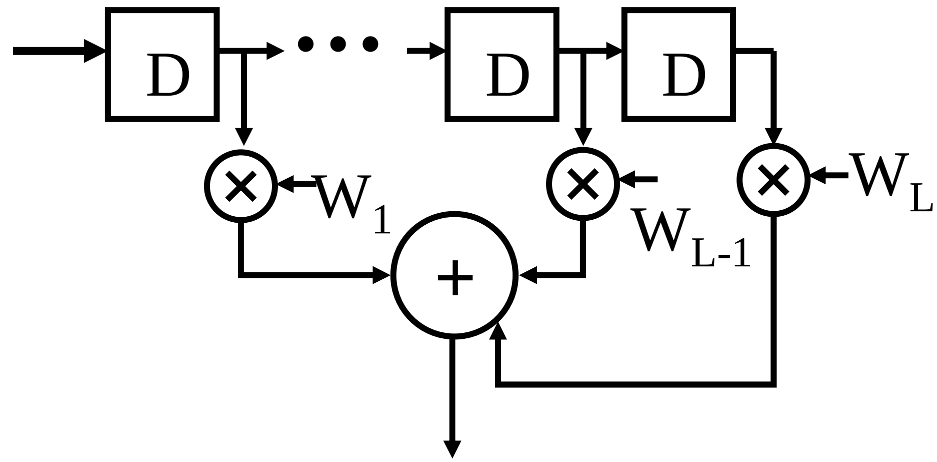
ISI Leads to Bit Failures

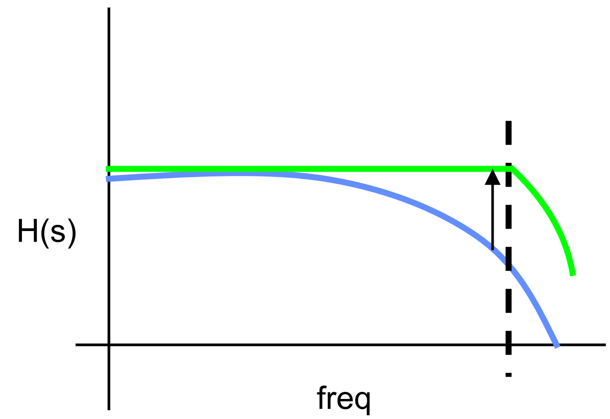


- Middle sample is corrupted by 0.2 trailing ISI (from the previous symbol), and 0.1 leading ISI (from the next symbol) resulting in 0.3 total ISI
- As a result middle symbol is detected in error

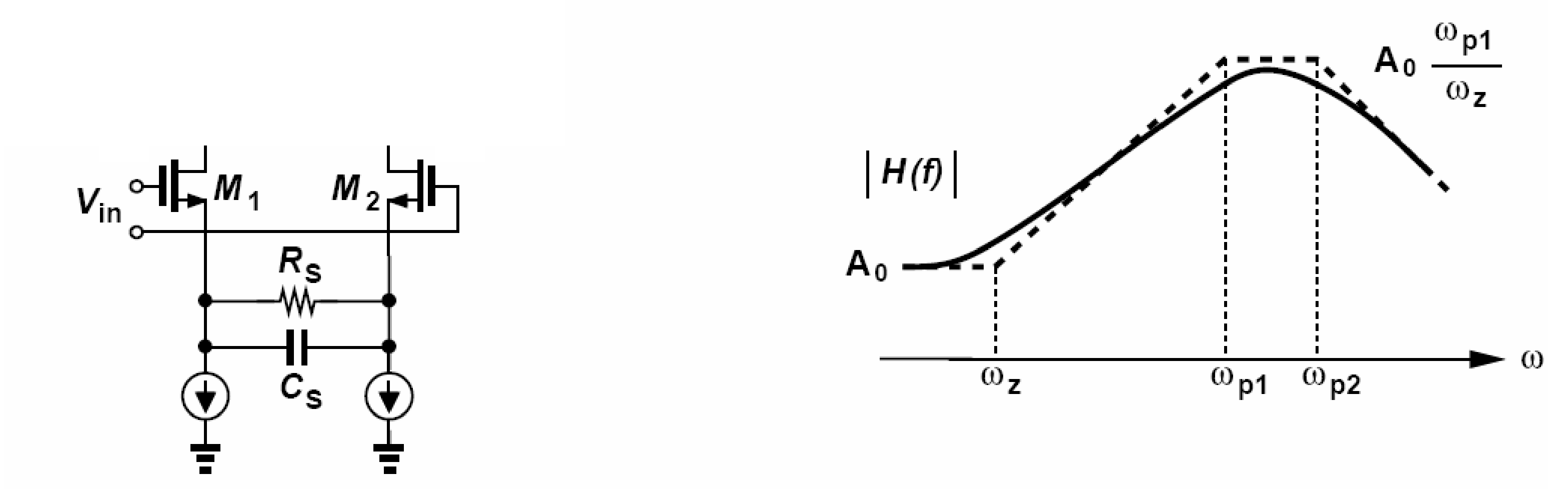
Receive Equalizer

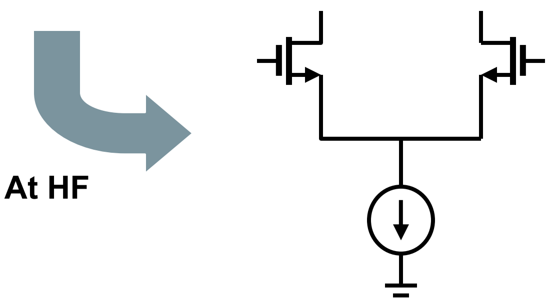
- Amplifies high-frequencies attenuated by the channel
- Pre-decision
- Digital or Analog FIR filter
- Issues
  - Also amplifies noise!
  - Precision
  - Tuning delays (if analog)
    - Not efficient for most SerDes
  - Setting coefficients
    - Adaptive algorithms such as LMS





Rx Linear Equalizer Implementation

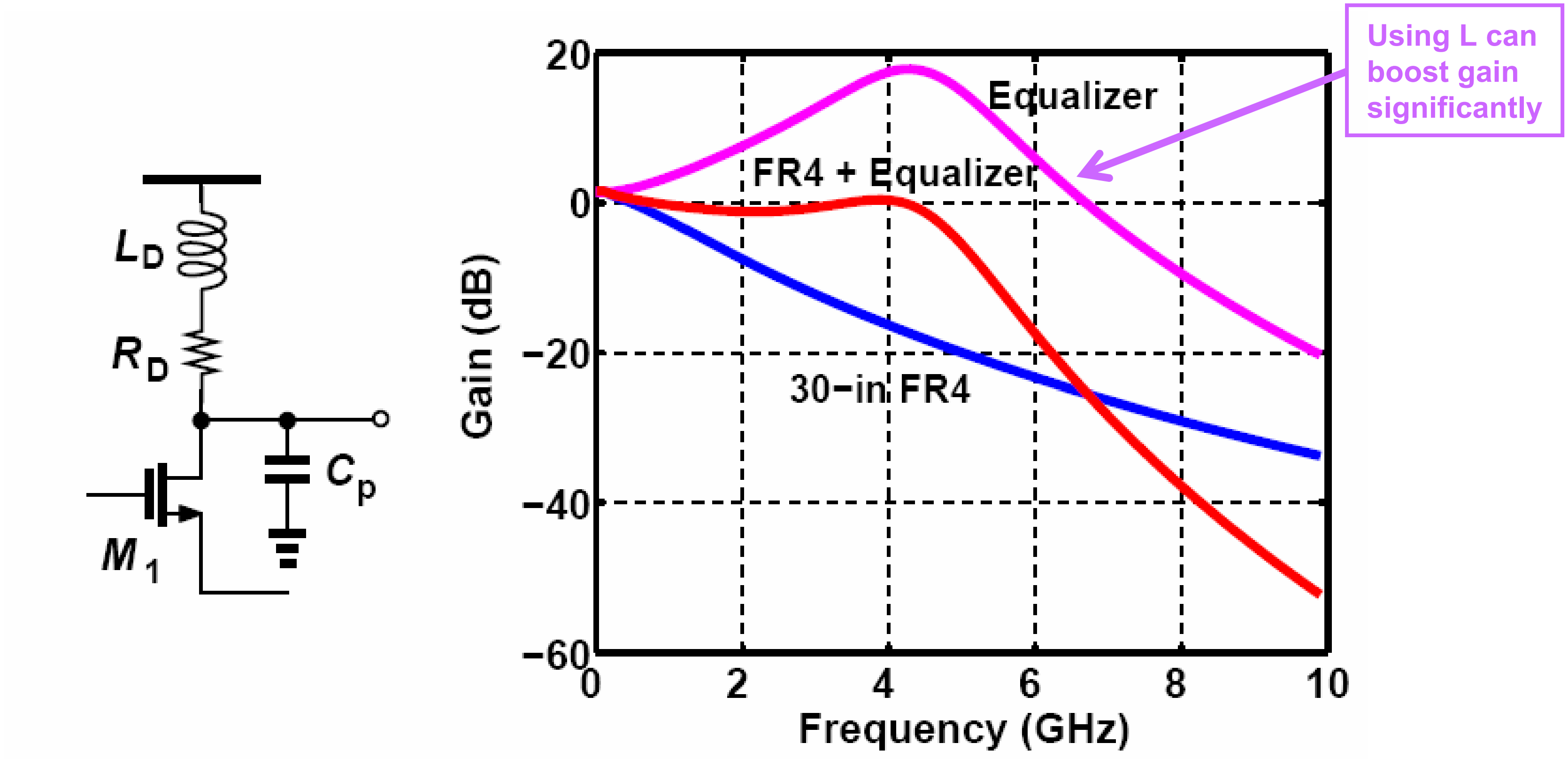




- **Source-connected RC-pole**
  - **Capacitor becomes a short at high-frequencies, increasing gain**

- **NOTE: Max gain still limited by Gain*BW product of source-coupled differential pair**

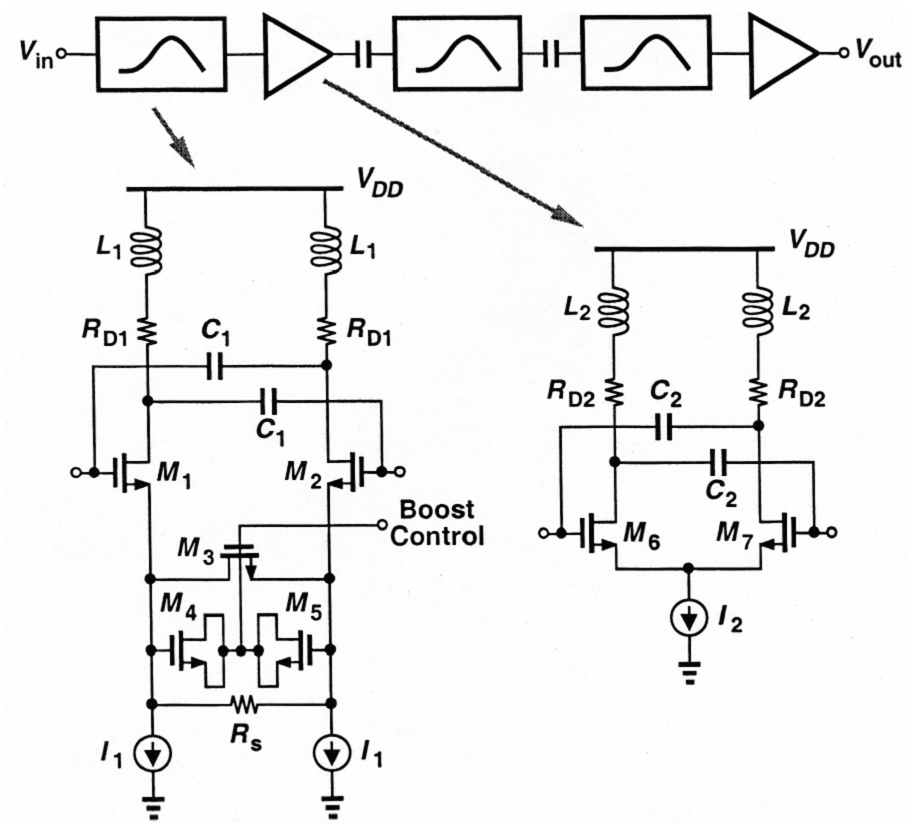
Rx Linear Equalizer Implementation → Getting More Gain



- **Build peaking amplifier by use of inductors**
  - **Area intensive**

Ref: Gondi, Razavi et.al. ISSCC 2005

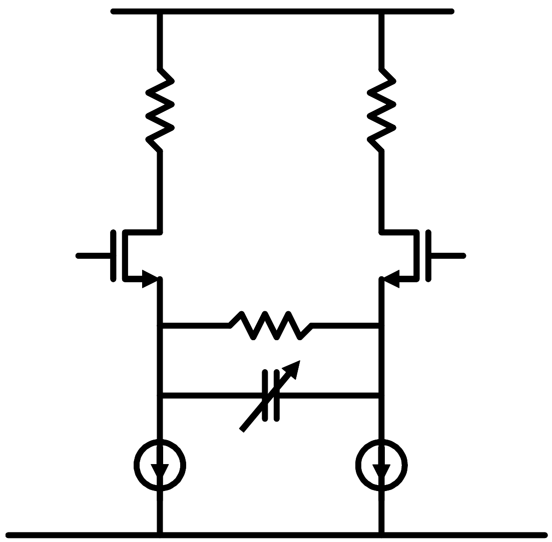
Rx Linear Equalizer : More Gain Thru Reverse Scaling!

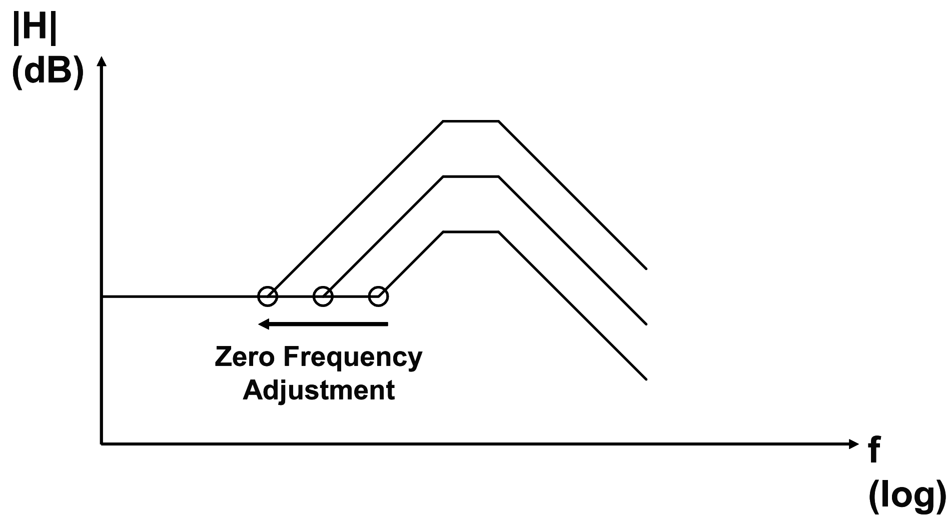


- **Multi-stage Rx LineEQ with reverse-scaling**
  - **Deals with gain-bw problem by *pushing it back onto the 50Ω line*!**
- **AC-coupling caps; common-mode issues otherwise**

Ref: Gondi, Razavi et.al. ISSCC 2005

Rx Linear Equalizer Implementation





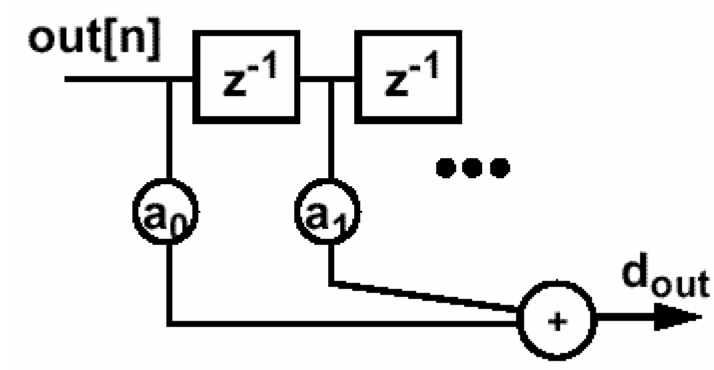
- **Deal with process variation by tuning C & therefore tuning zero location**

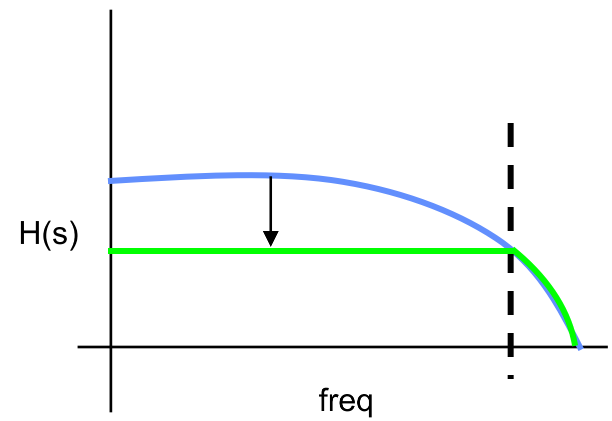
Rx LinEQ Implementation Issues

- Linearity a challenge
  - Especially when input swings vary greatly in amplitude
- Limited by gain-bw of diff-pair stage
  - Limited tuning range; rarely matches channel
  - Sensitive to PVT variations
  - Sensitive to device mismatch, linearity
  - Difficult to offset cancel, calibrate
- Multi-stage issues
  - High gain can lead to clipping in multi-stage design
  - Original design issues become even more difficult
  - Tuning is tricky
- Performance results
  - In 90nm, can generally get ~4-6dB of gain/stage at 10Gb/s if you do things right
  - Not a lot of gain – leads to multi-stage & inductively peaked designs

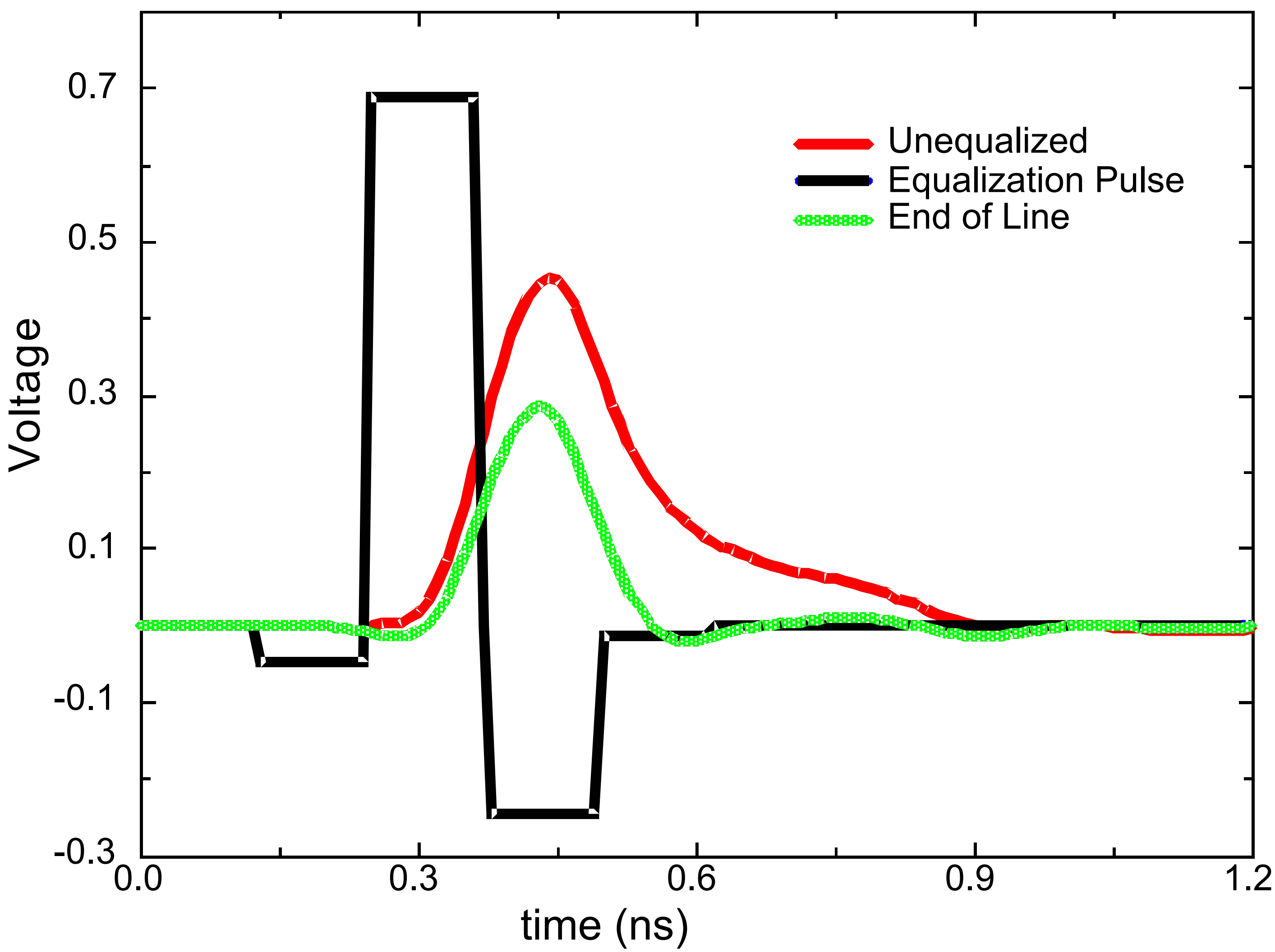
Transmit Linear Equalizer

- Attenuates low-frequencies
  - Need to be careful about output amplitude : limited output power
    - If you could make bigger swings, you would
    - EQ really attenuates low-frequencies to match high frequencies Also FIR filter : D/A converter
- Can get better precision than RX
- Issues
  - How to set EQ weights?
  - Doesn't help loss at f

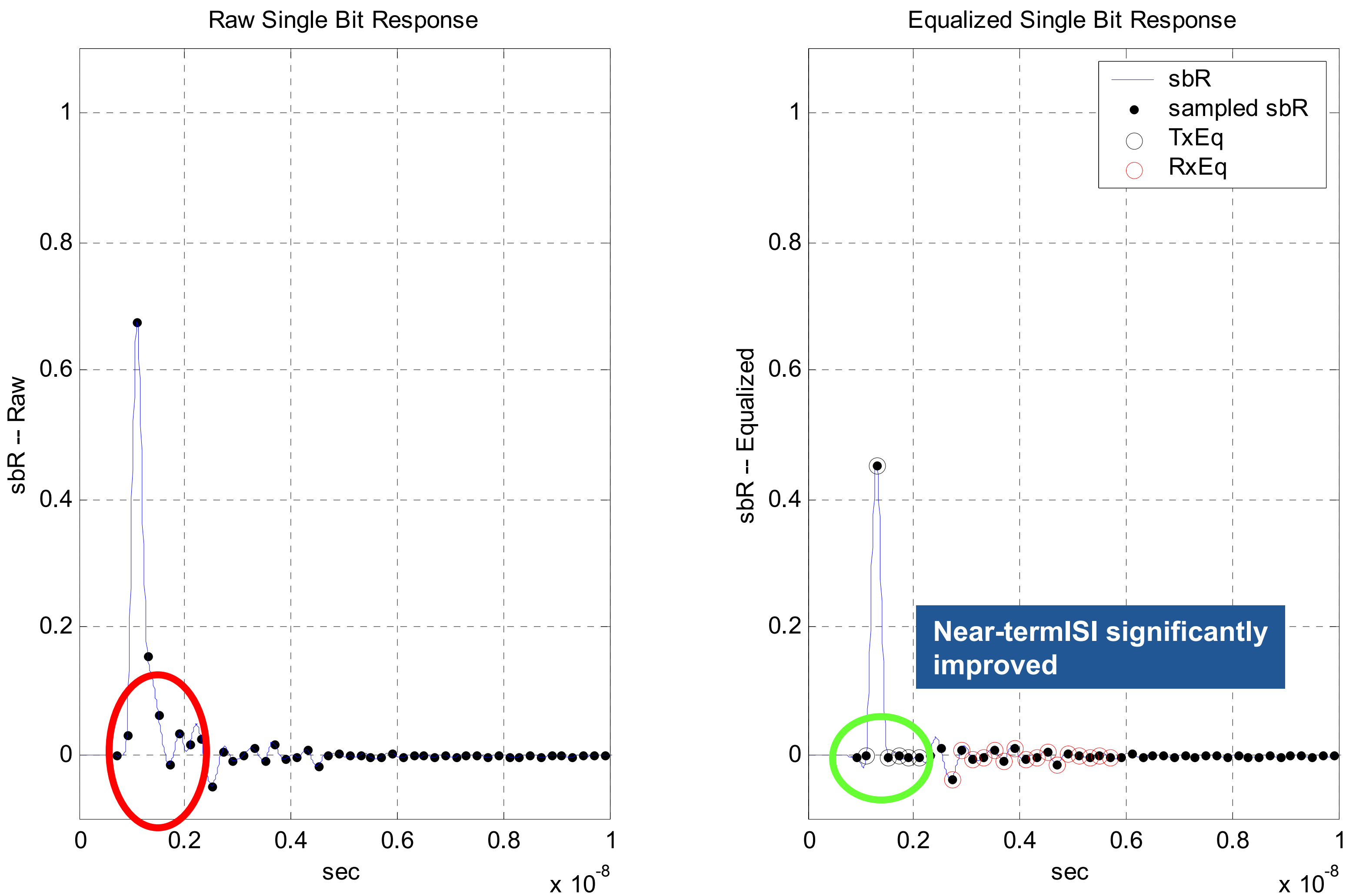




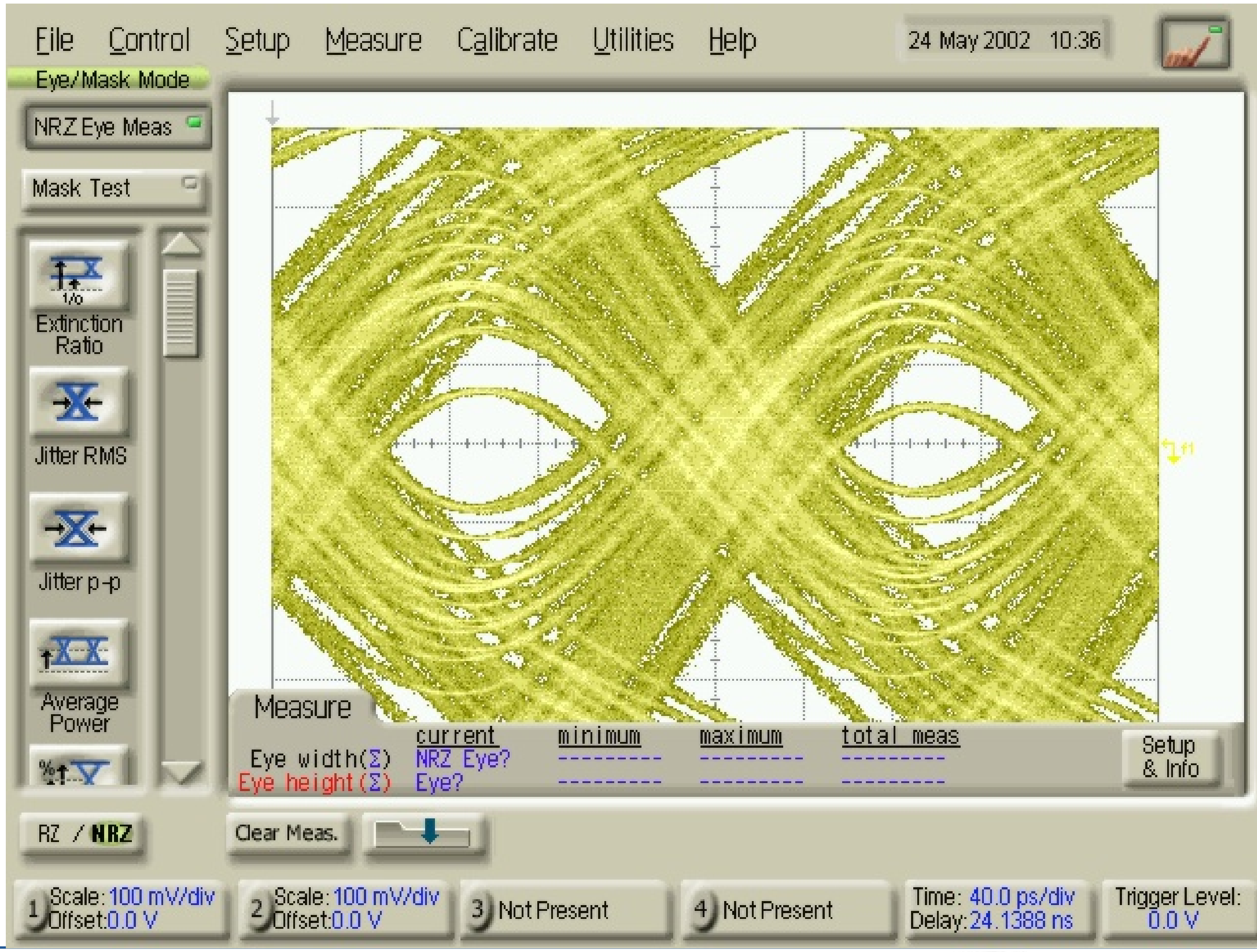
Transmit FIR : Single Bit Response



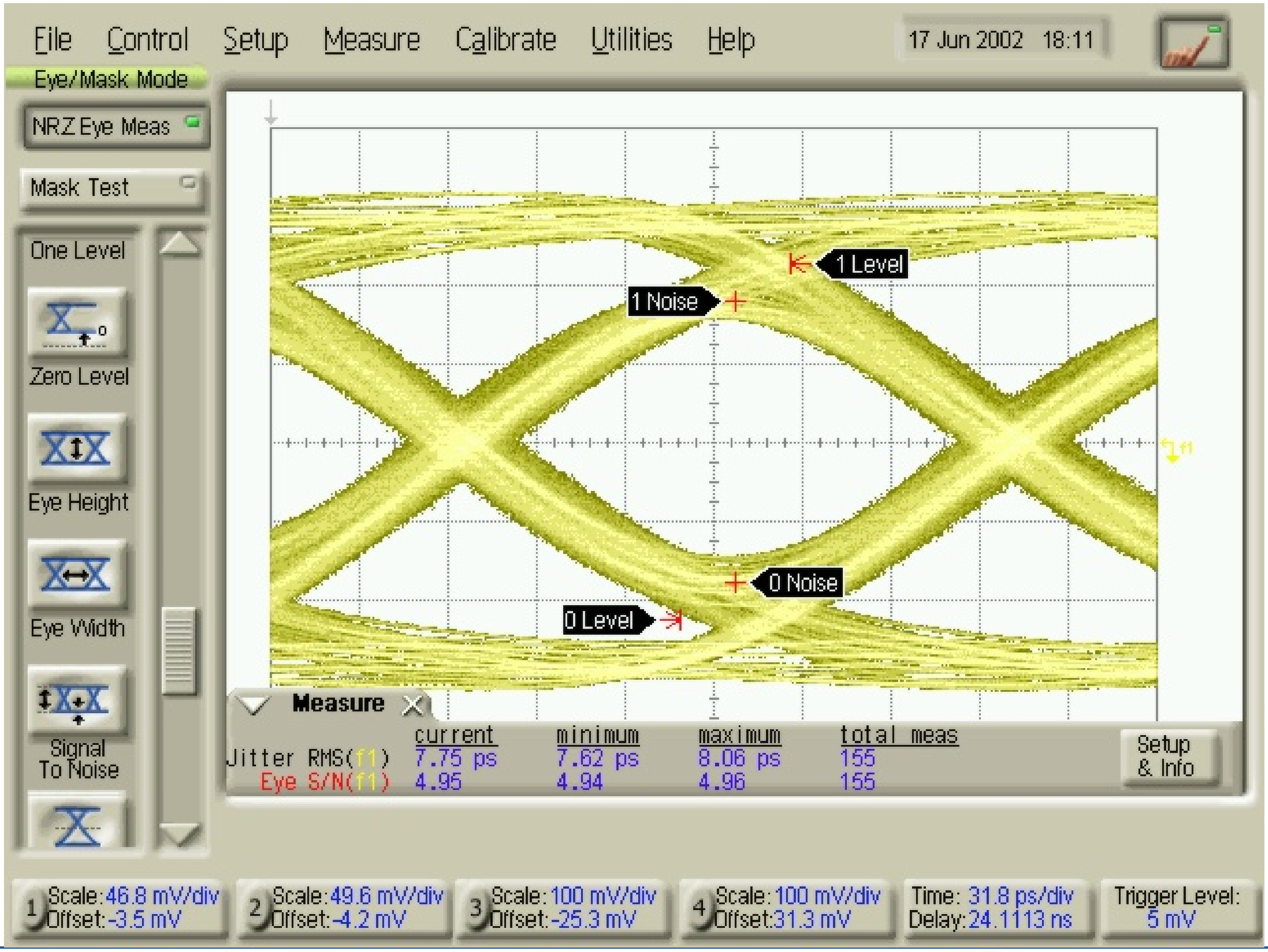
Before & After Transmit Equalization



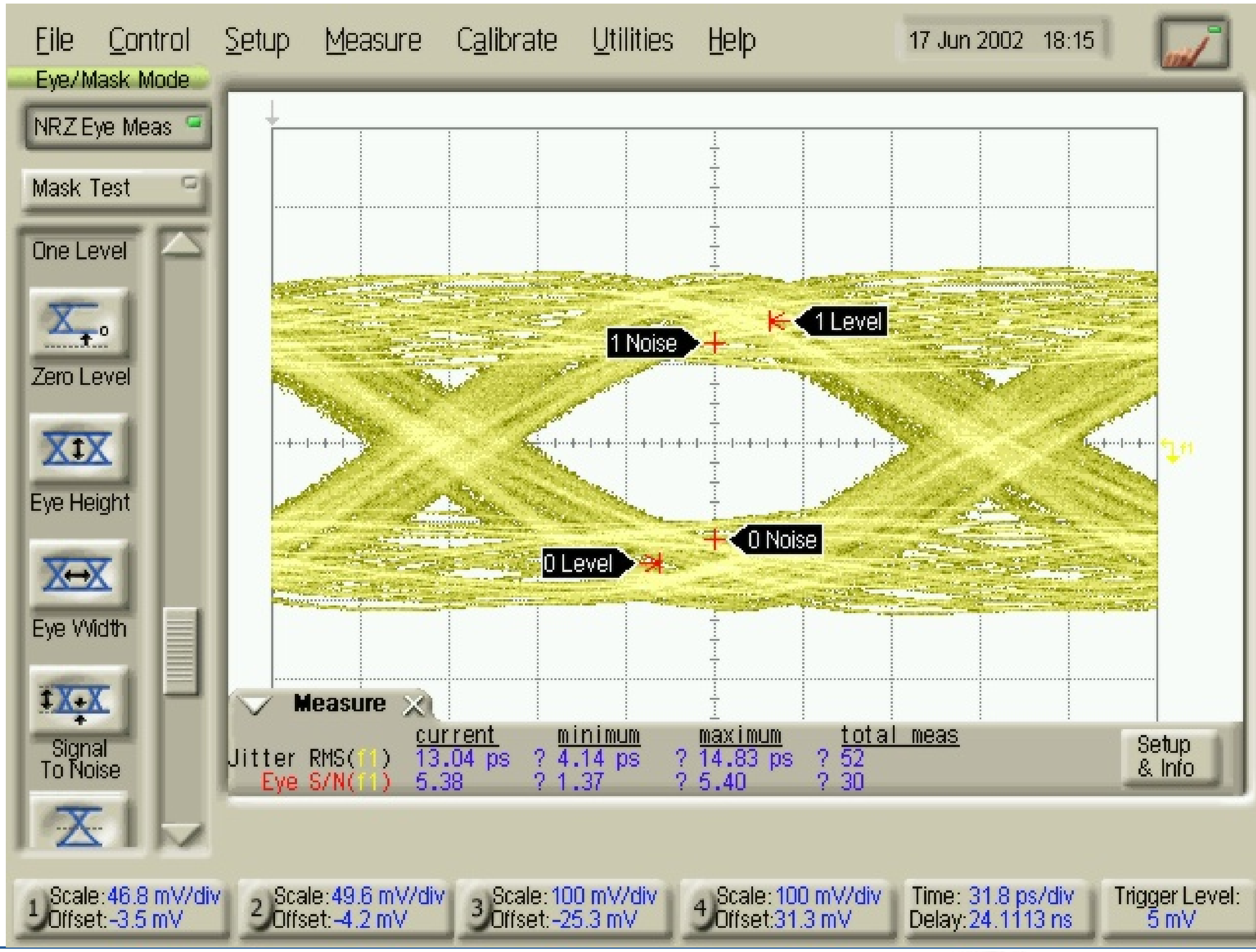
Example : 5Gbps Over 26" of FR4 NoEq



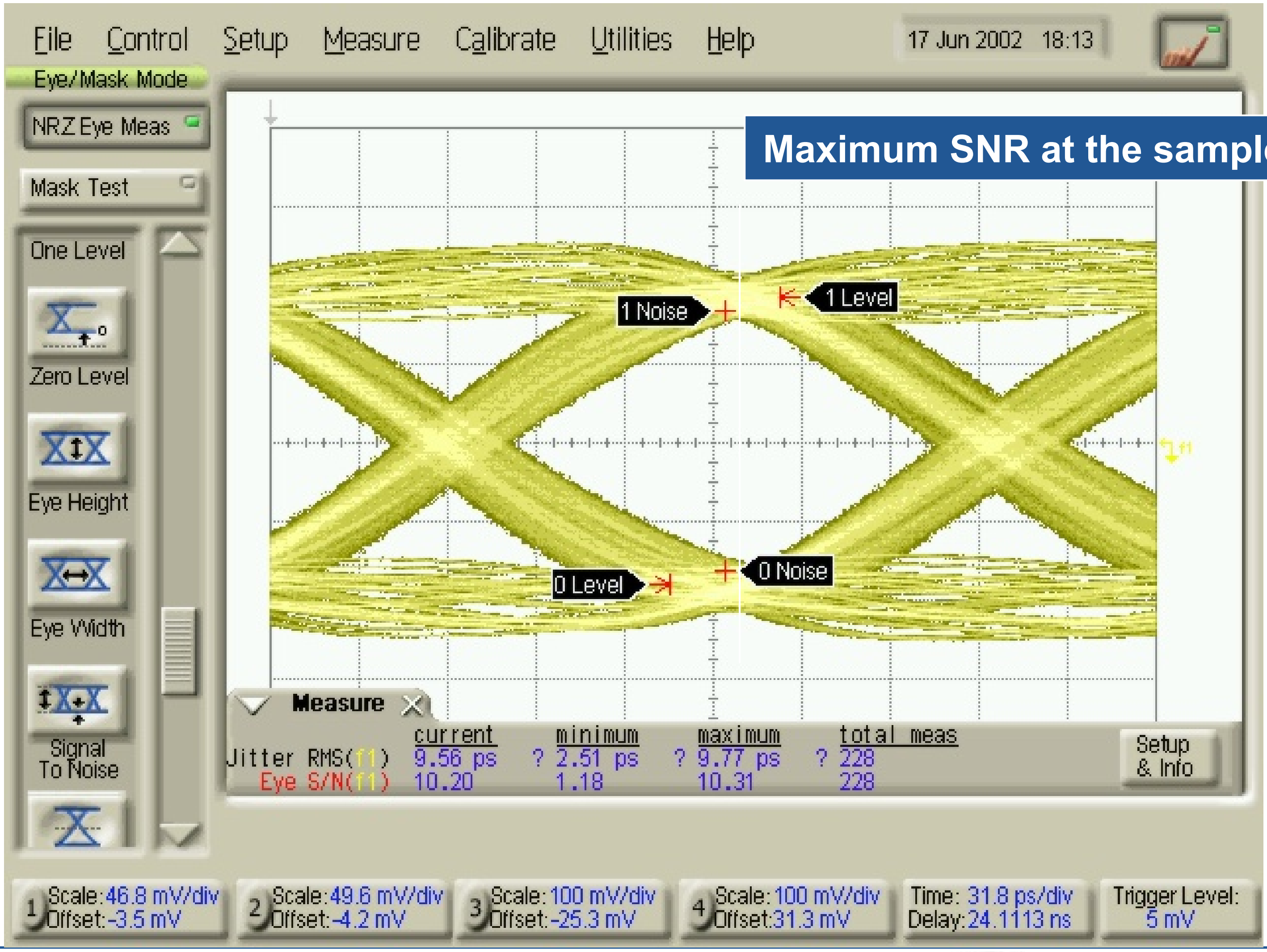
Example : 5Gbps Over 26" of FR4 Under Equalized



Example : 5Gbps Over 26” FR4 Over Equalized

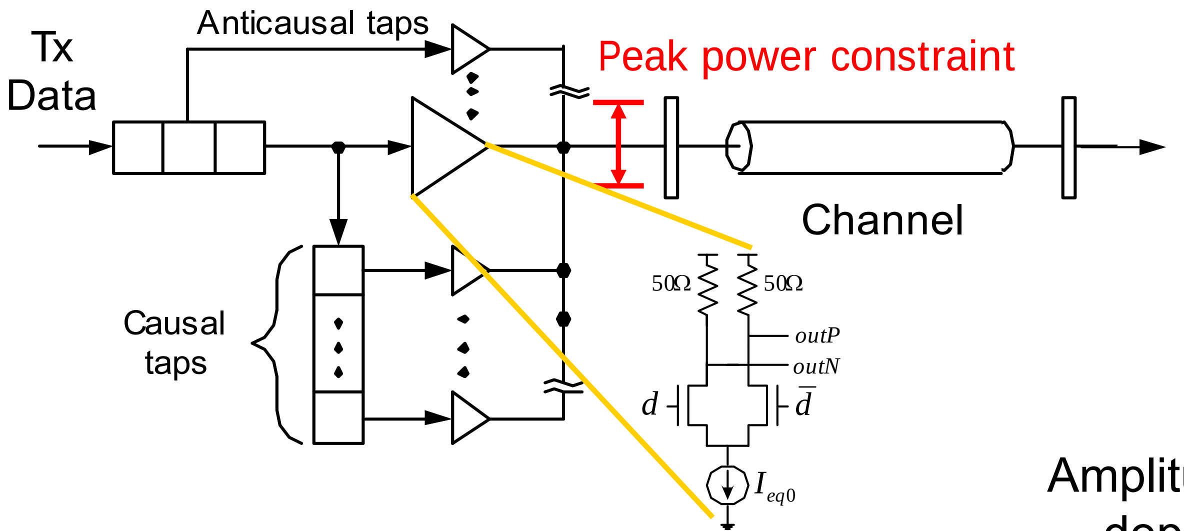


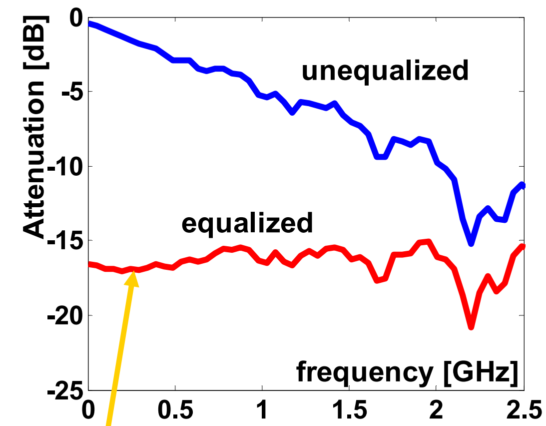
Example : 5Gbps Over 26" FR4 Correct Tx Equalization



Maximum SNR at the sample point

Transmit Equalization Implementation: Headroom Constraint

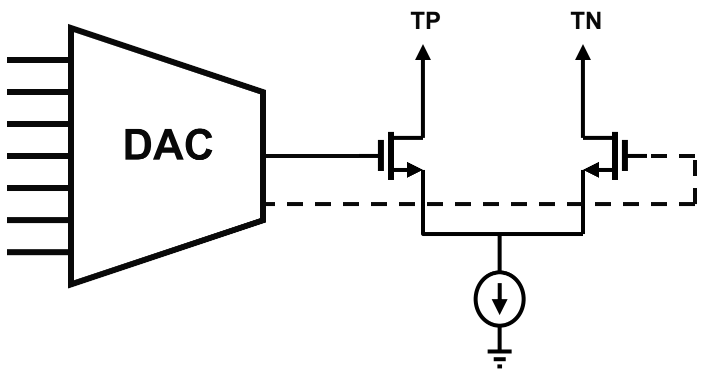




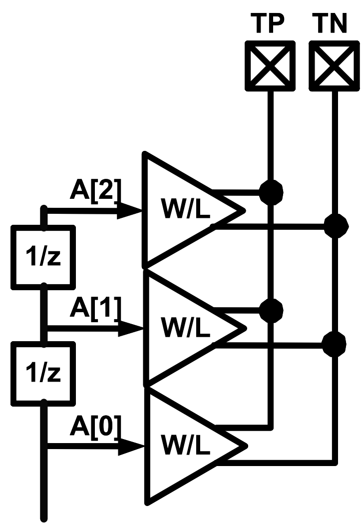
Amplitude of equalized signal depends on the channel

- **Transmit output stage has limited voltage headroom**
  - **More swing puts current sources out of saturation**
- **Tx Eq attenuates the signal**
  - **Doesn't help your attenuation at Nyquist frequency**

Two Extremes of TxEq Architectures : DAC/Direct FIR EQ

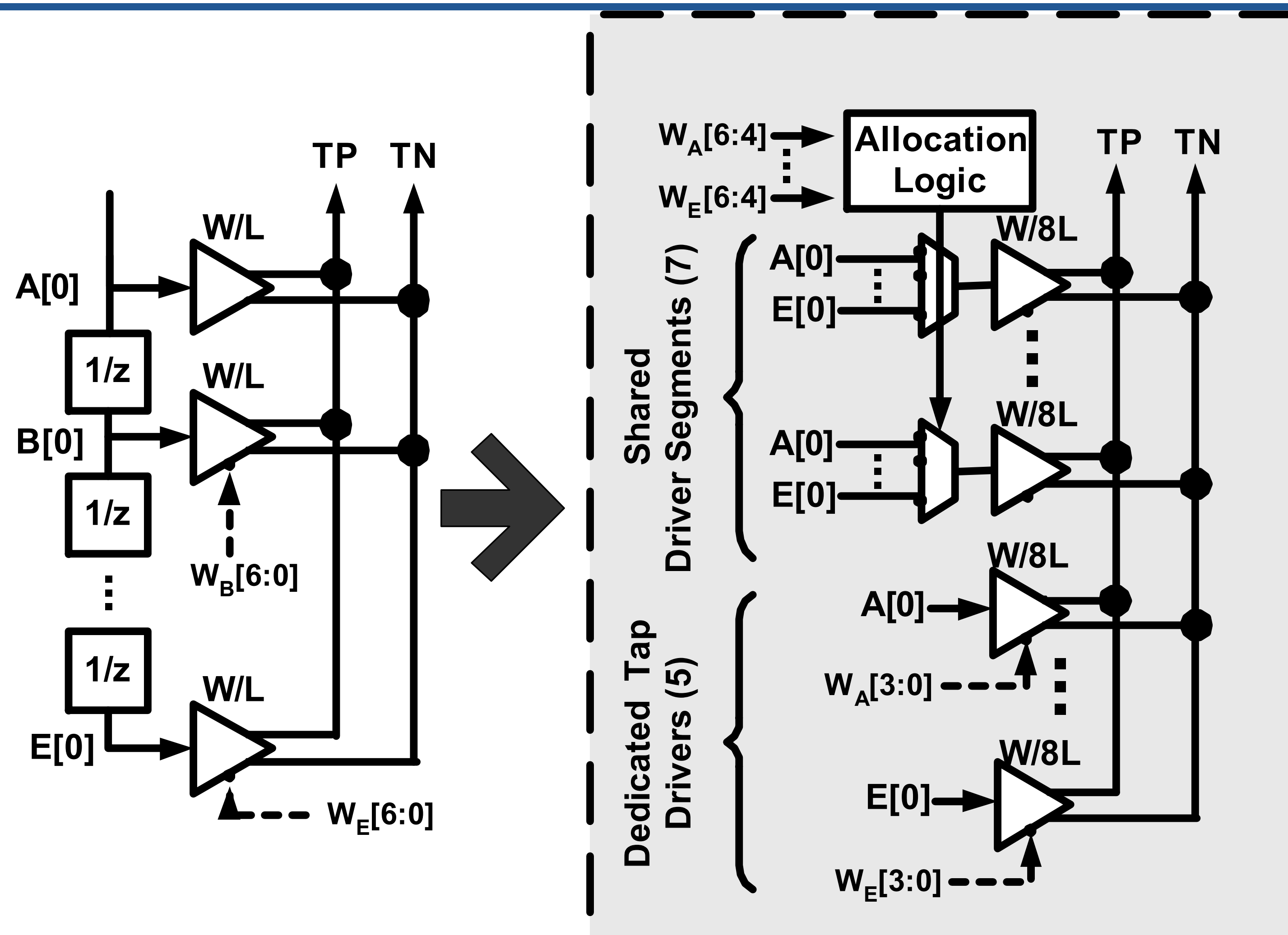


- DAC : Lowest Ci
  - Output xtors are minimum required to drive current
  - Best parasitics
  - Highest power, area, complexity
    - Requires coefficient mapping table
    - Most flexible wave-shaping



- Direct FIR: Lowest power, area
  - More output xtor W than required to drive full-swing
    - → Higher Ci
  - Direct tap coefficient application
  - Easy multiplication of data X coeff
    - Simple
    - Lowest power, area

5-Tap Shared Transmitter Compromise



Total gate = 3(5) = 15W/L

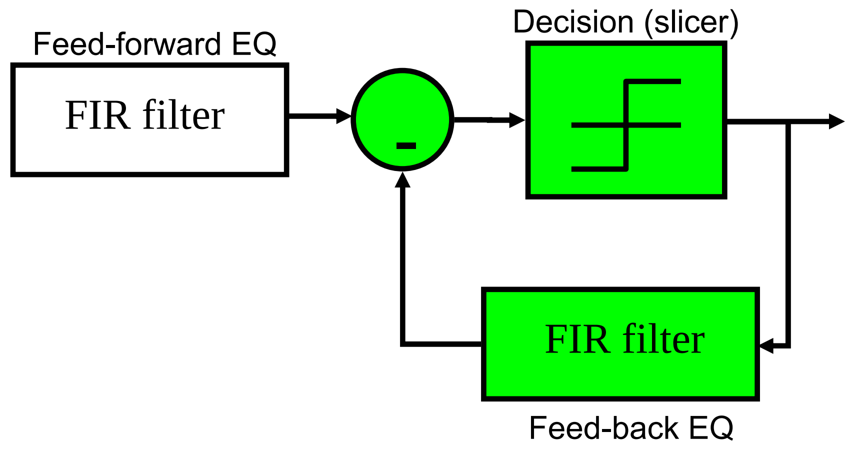
Total gate = 3(7/8+5/8) = 4.5W/L

TX LinEQ Implementation Issues

- Relatively simple to implement but…
- Attenuates the low-frequencies
  - Peak power constraint
    - Additional taps & range <u>reduce</u> signal swing
    - Too much TxEQ can collide with receiver overdrive requirements → end up with open eye which is too small
    - Use of RxLinEQ to recover eye size won't compensate for noise issues
- Setting TX coefficients is tough
  - Fundamental information is at the receiver
  - Coefficients through back-channel
    - Requires use of some bandwidth somehow…
      - Dedicated adjacent channel bw
      - Signaling through an alternate mode (CM)

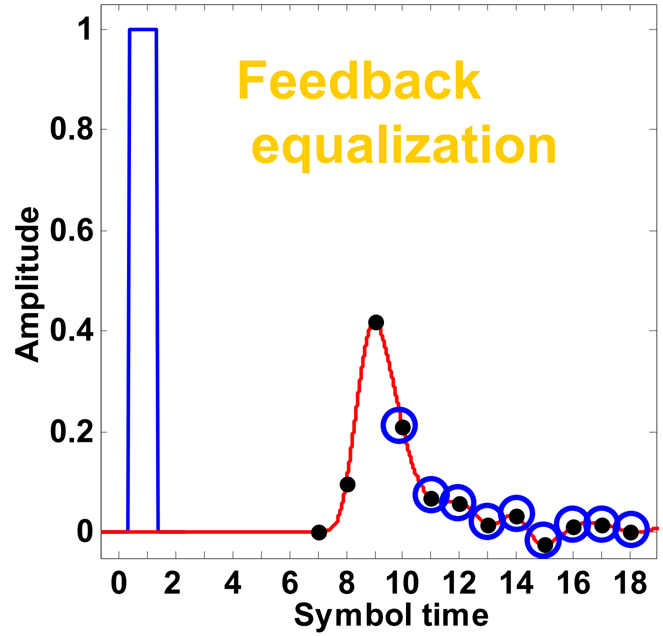
Decision Feedback Equalization

- Don't invert channel… just remove ISI
  - Know ISI because already received symbols
  - Doesn't amplify noise
  - No peak-power constraint issues
  - Has error accumulation problem
    - Less of an issue in links where random noise small
- Requires a feed-forward equalizer for precursor ISI
  - Reshapes pulse to eliminate precursor
- Timing to first tap feedback is brutal

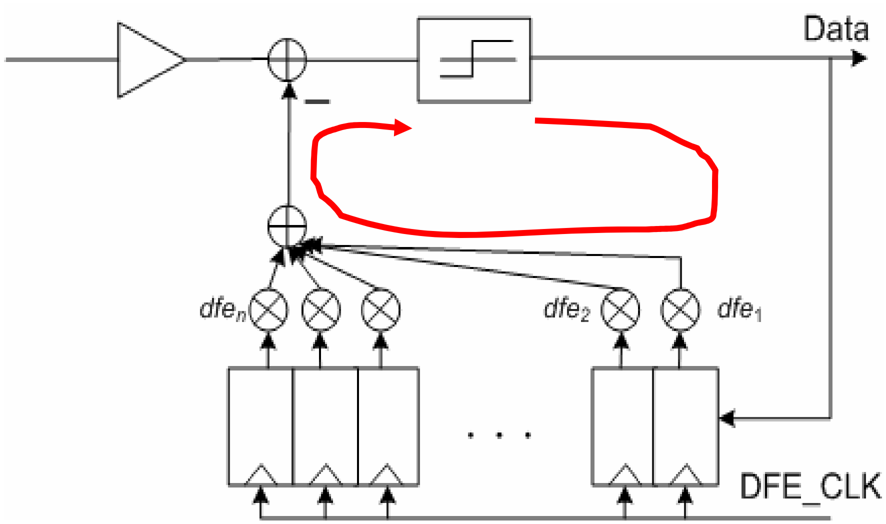


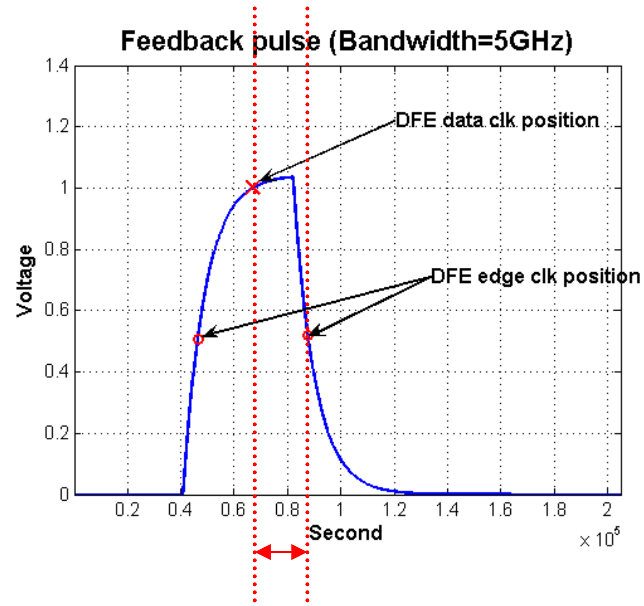
Including DFE

- Problems with DFE
  - ISI must be causal
  - Latency in the decision circuit
    - Receive latency + DAC settling < bit time
  - Can increase allowable time by loop unrolling
    - Receive next bit before the previous is resolved



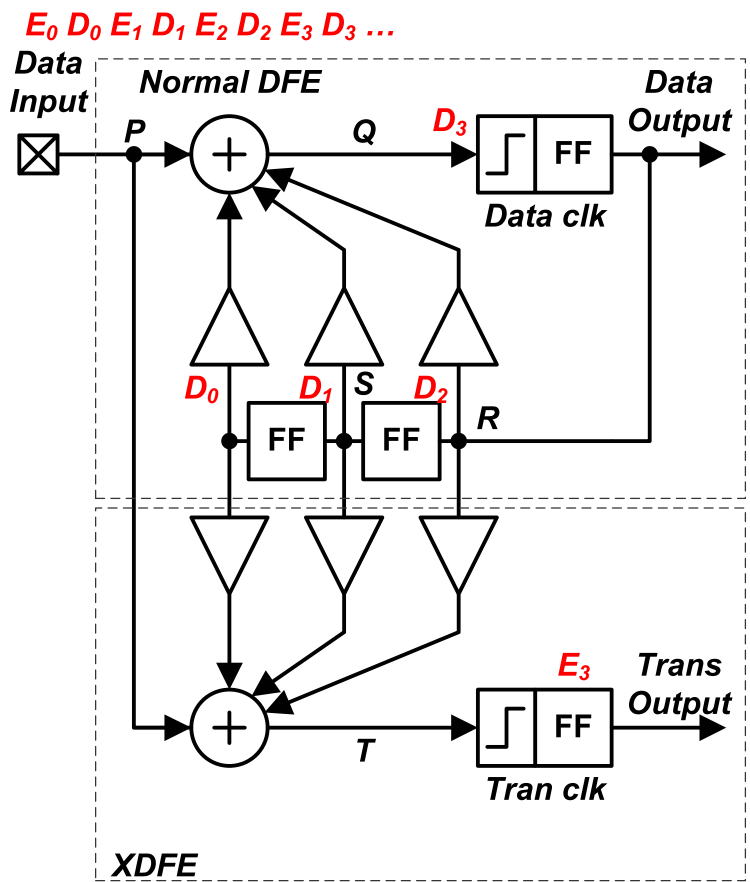
DFE Challenges : Loop Timing





- **Feedback loop timing is *extremely* tight!**
  - **Ideally you will resolve the bit, multiply by coefficient and analog sum in 0.5UI!**
    - **Otherwise affect coefficient setting/linearity**
    - **Or edge position**
  - **This is what makes DFE's hard for serial links**

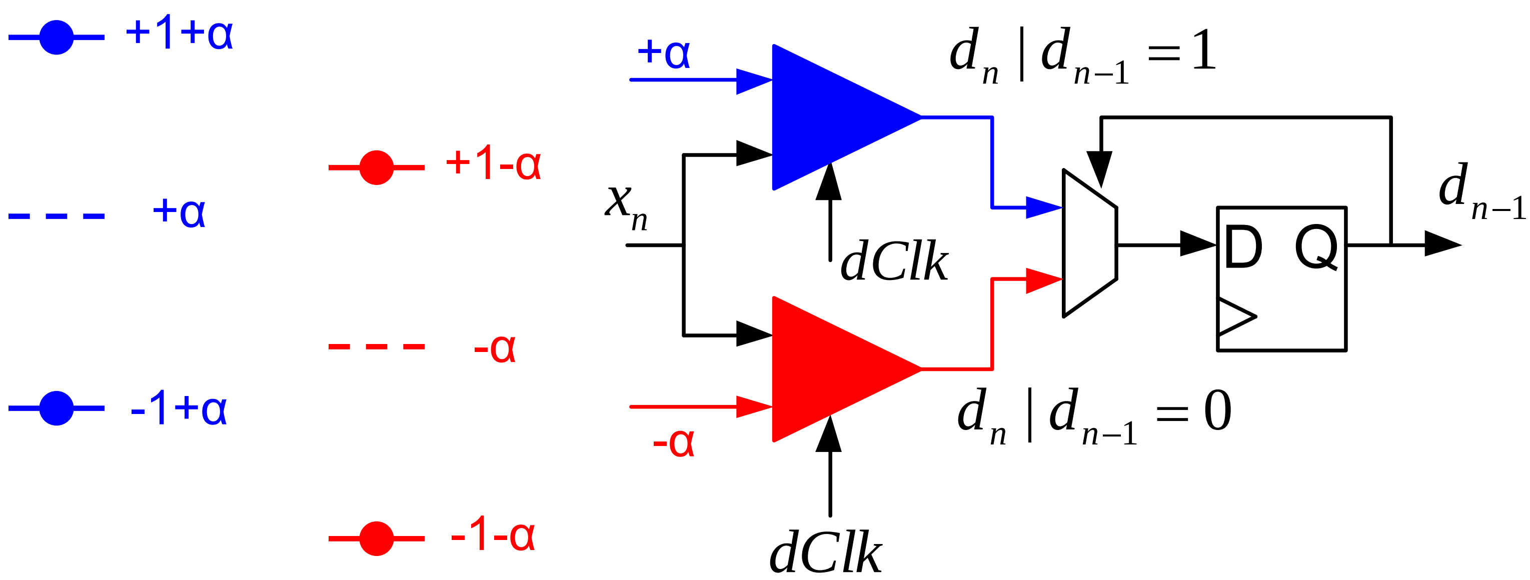
DFE Feedback Timing : Splitting Edge & Data



- **Separate data & edge feedback & summers**
  - **Still need to make 1UI data timing – still very tight**
  - **Allows separate coefficients & 'edge-DFE'**

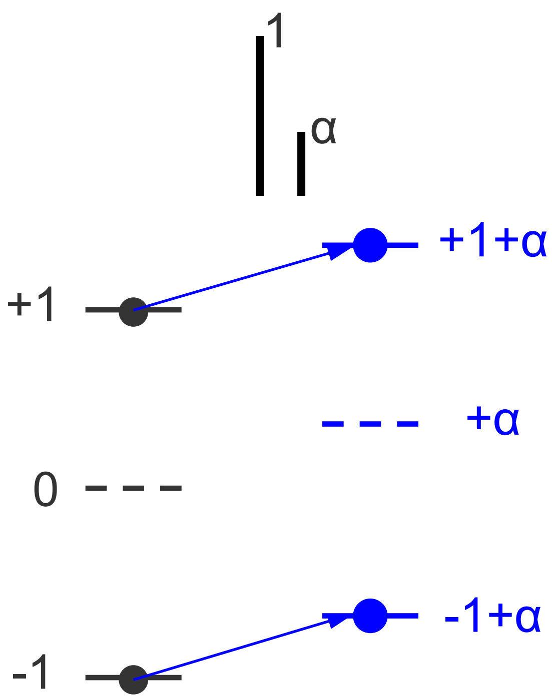
Courtesy E.Chen, K. Yang UCLA

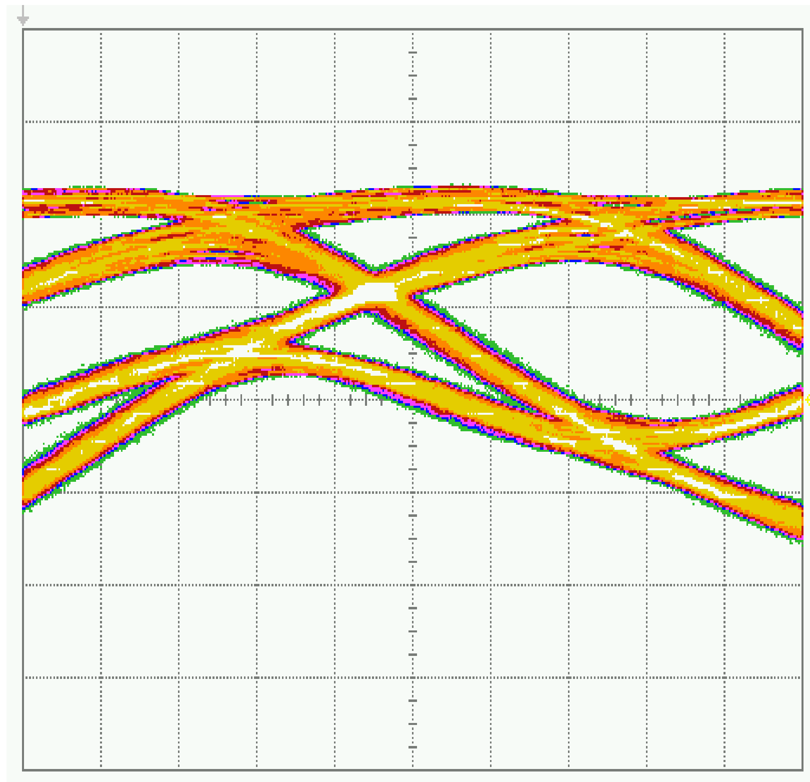
Partial Response DFE (prDFE) Via Loop Unrolling



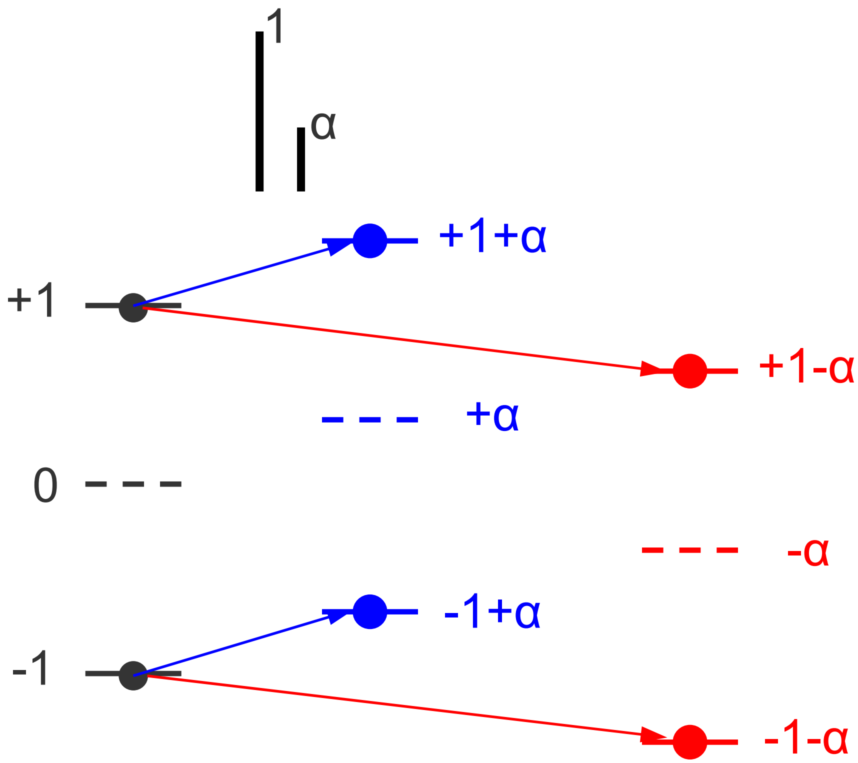
- **Instead of subtracting the error**
  - **Move the slicer level to include the noise**
  - **Slice for each possible level, since previous value unknown**
  - **Gets you to 1.5 – 2UI timing**
  - **Requires proper calibration of offset levels**

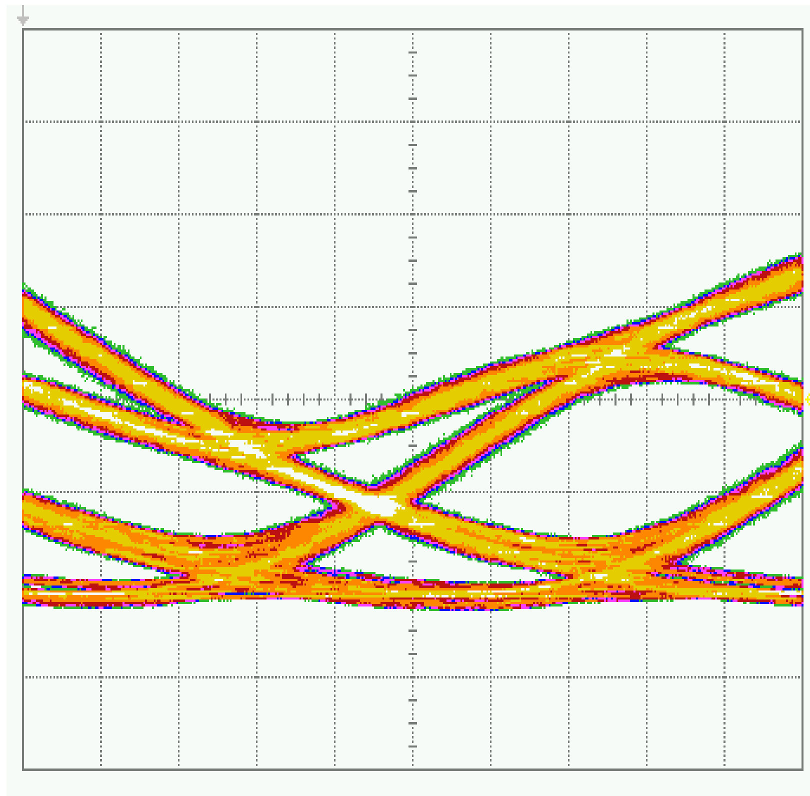
Partial Response DFE (prDFE) Via Loop Unrolling



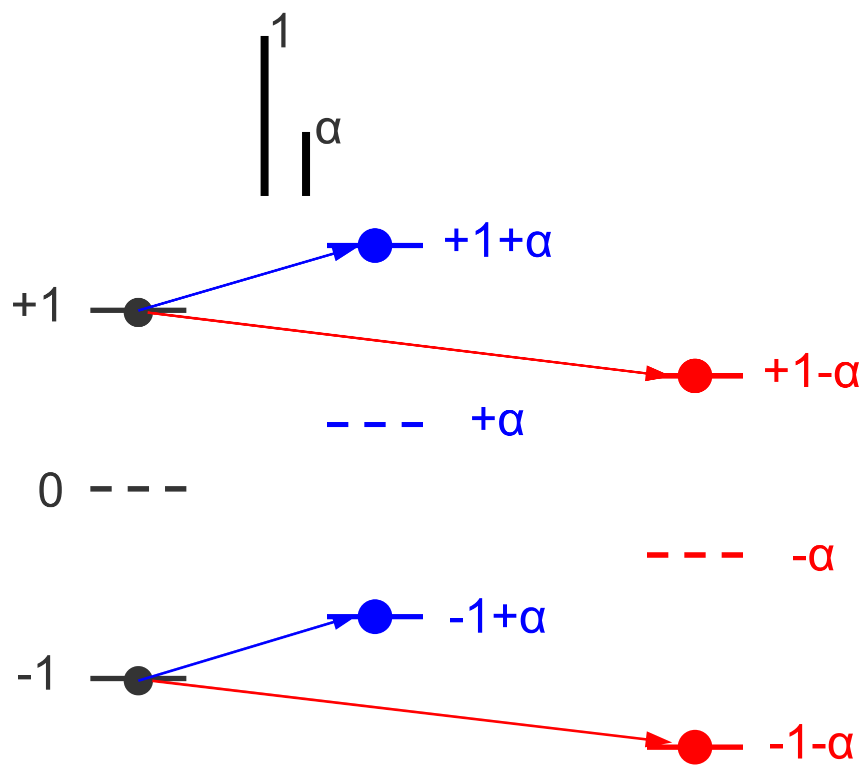


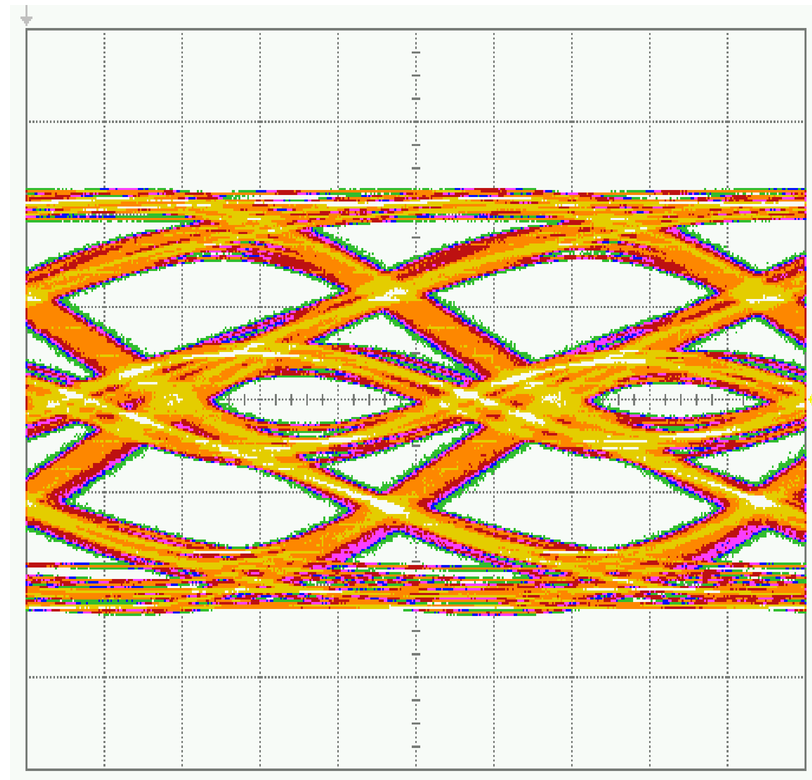
Partial Response DFE (prDFE) Via Loop Unrolling





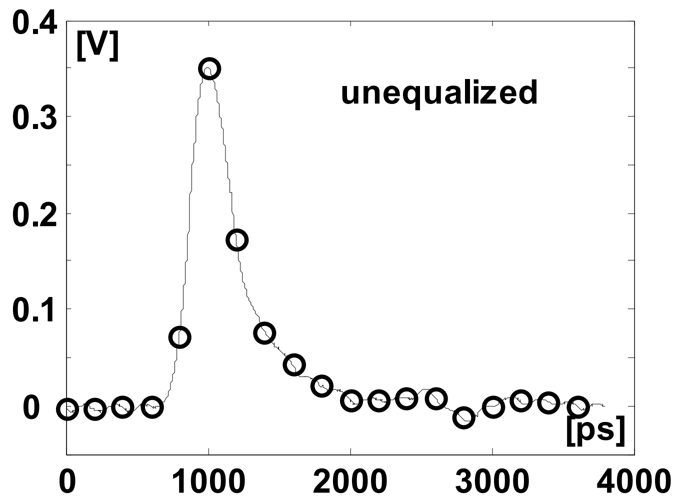
Partial Response DFE : Both Sides

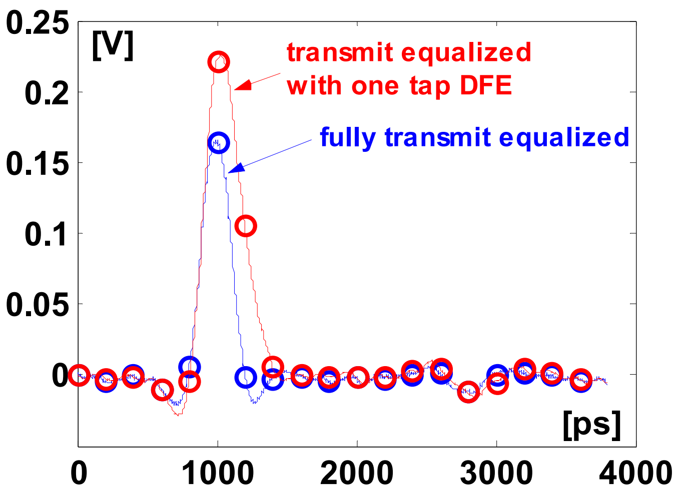




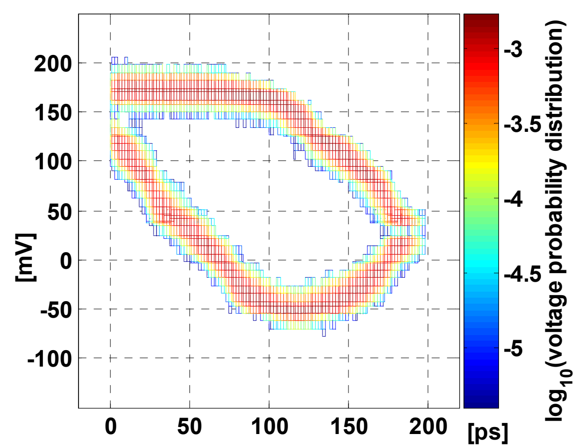
- **Final result is 4-levels when including first postcursor, α**

prDFE Effectiveness Measurement





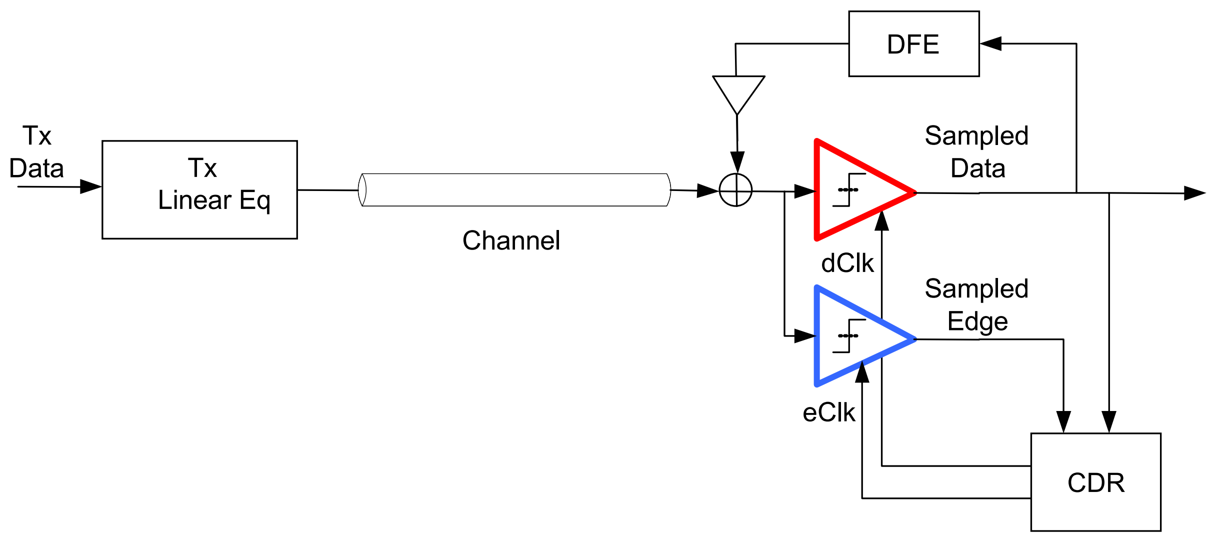
- TxEQ is power constrained
- Use of 1-bit of prDFE relieves the transmit equalizer of having to cancel the first-post-cursor by taking energy from the *main* bit



DFE Implementation Issues

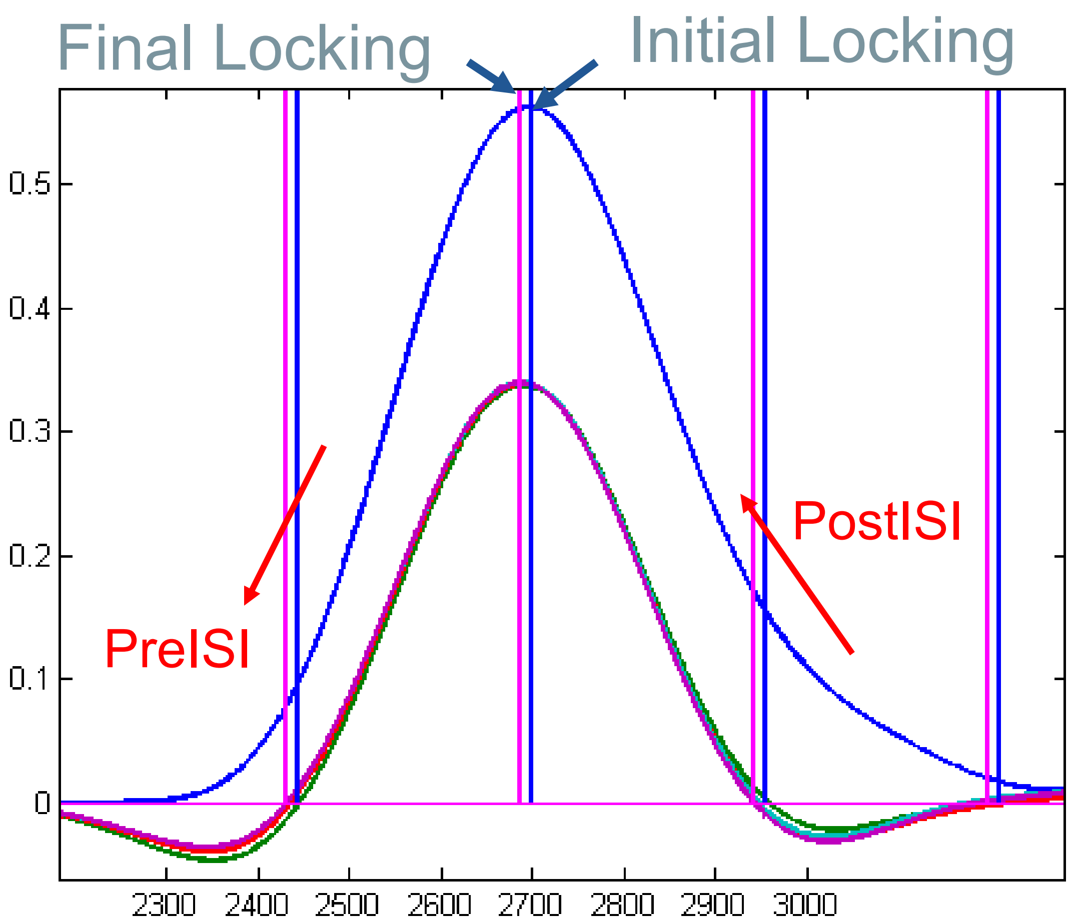
- Loop timing is very difficult
- prDFE relieves loop timing but…
  - Complexity grows by 2^N
    - Additional sampler parasitics, power grow rapidly beyond a single-stage
  - Requires offset levels
    - Adding to signal path without bad effects
    - Avoiding noise injection can be tricky
    - Need to calibrate/interpolate
  - Clock recovery challenging with prDFE

CDR & EQ – General Issues



- **Fundamental issue – conditioning signal edges effects CDR edge-position…**
- **CDR edge-position effects observed ISI**
  - **Can effect both Tx & Rx coefficients**
  - **What is best solution for lowest BER???**

TxEQ Wave-Shaping Effects On CDR Lock Position

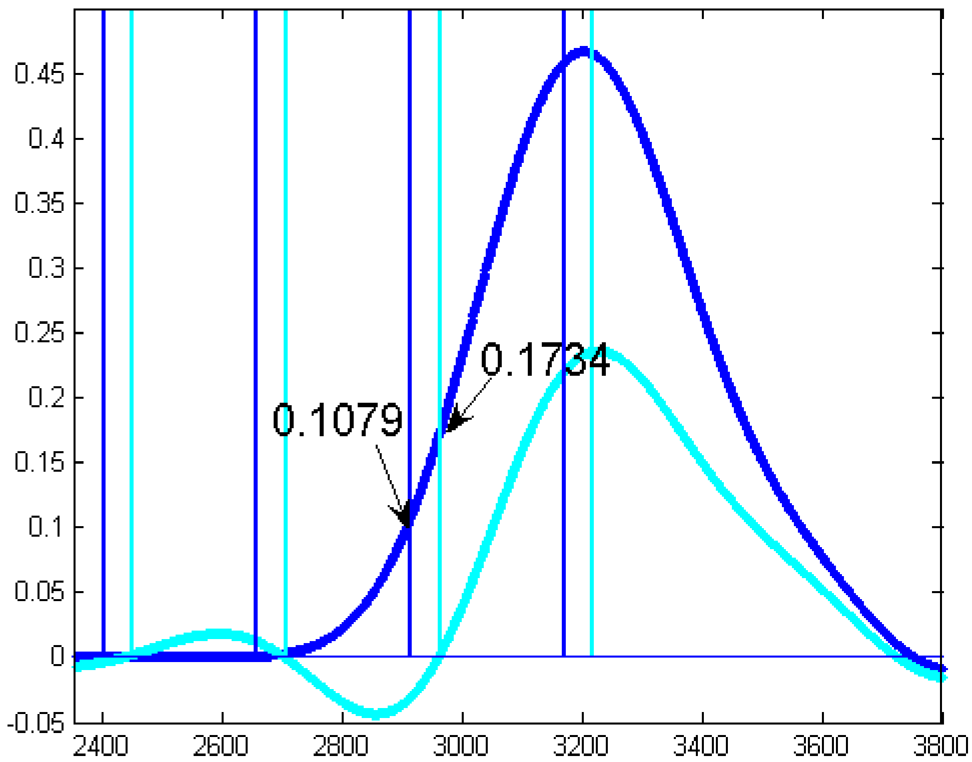


Blue: Raw single bit response

Purple : Final result with adaptation & CDR locking

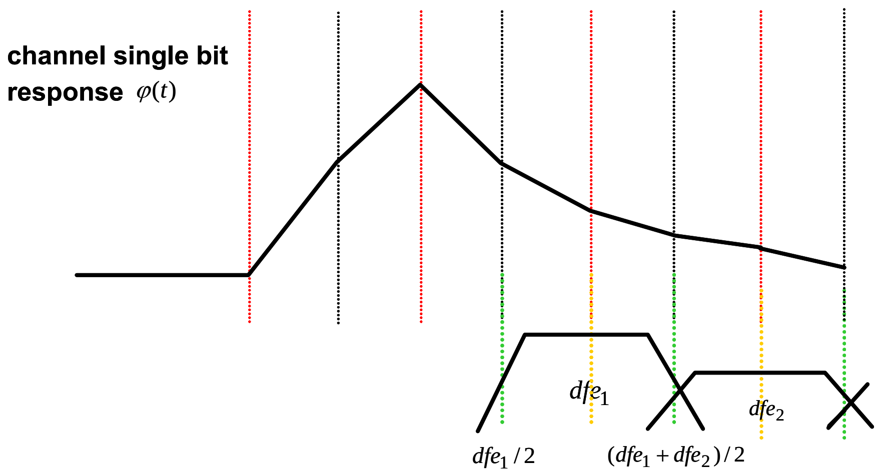
- **Effect depends on TxEQ taps**
  1 pre-cursor taps, 1 main, 2 post-cursor taps

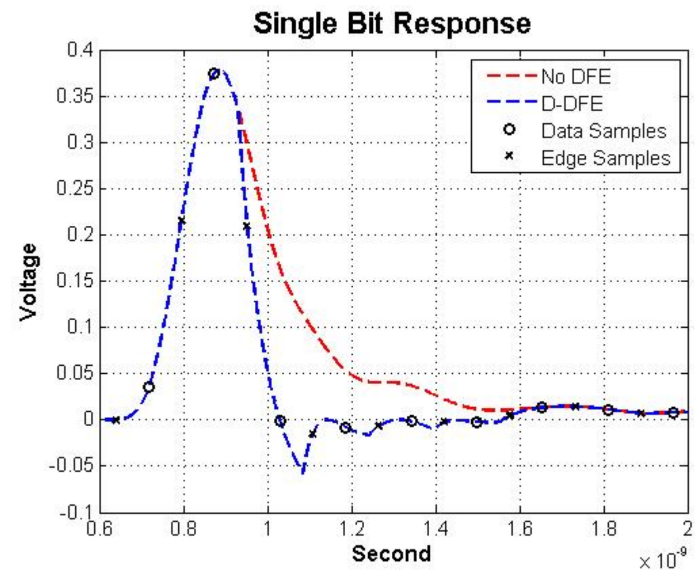
TxEQ Wave-Shaping & CDR Precursors Only



- **3 pre-cursor taps, 1 main, 0 post-cursor taps**
- **Significant phase-shift in lock position is observed**

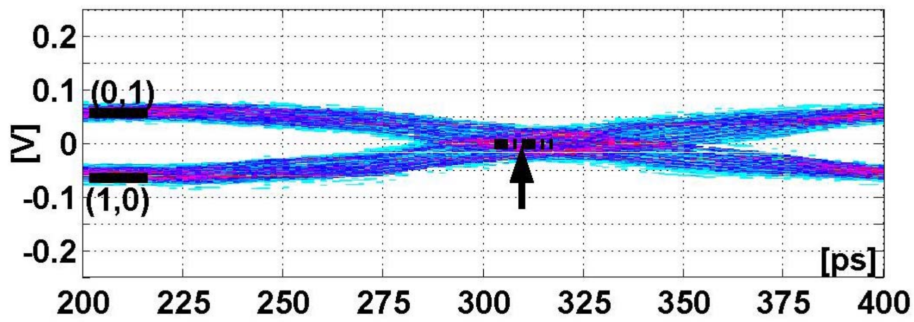
CDR & DFE : Feedback Pulse Timing

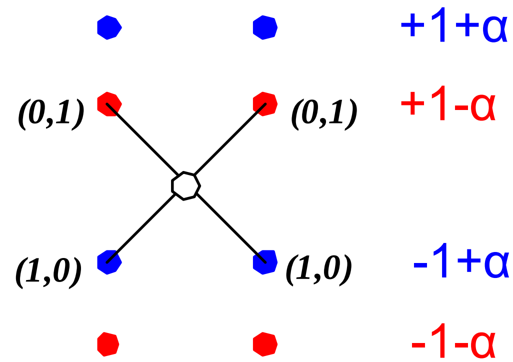




- Edge/DFE interaction with first post-cursor tap ; will move lock point
  - Proper prDFE implementation can avoid this entirely
- Unlike TxEq, since not convolved with channel taps 2-N do not interact with CDR

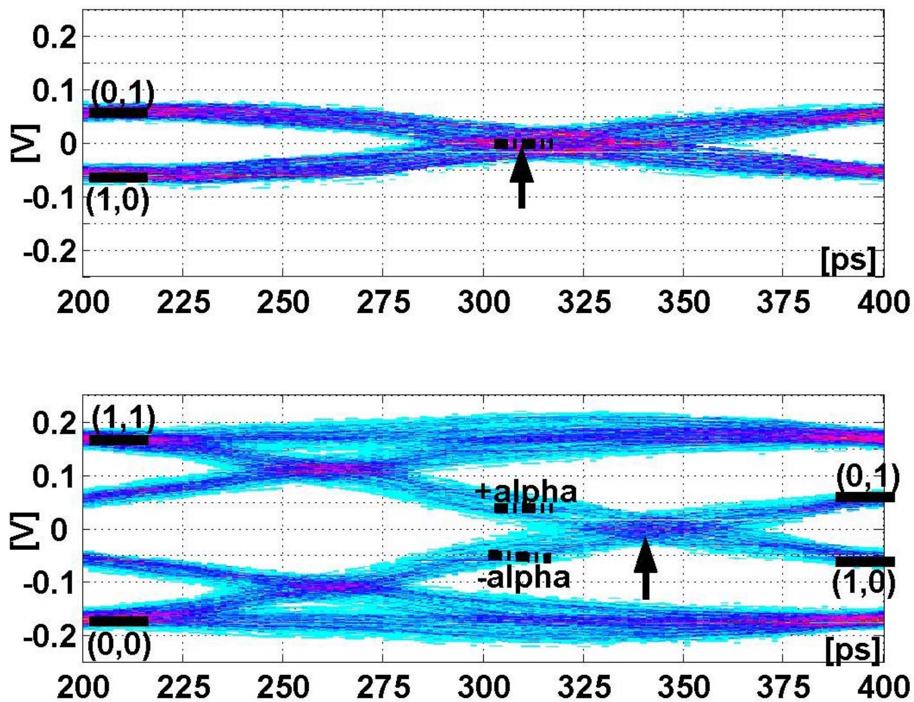
Partial Response DFE & CDR

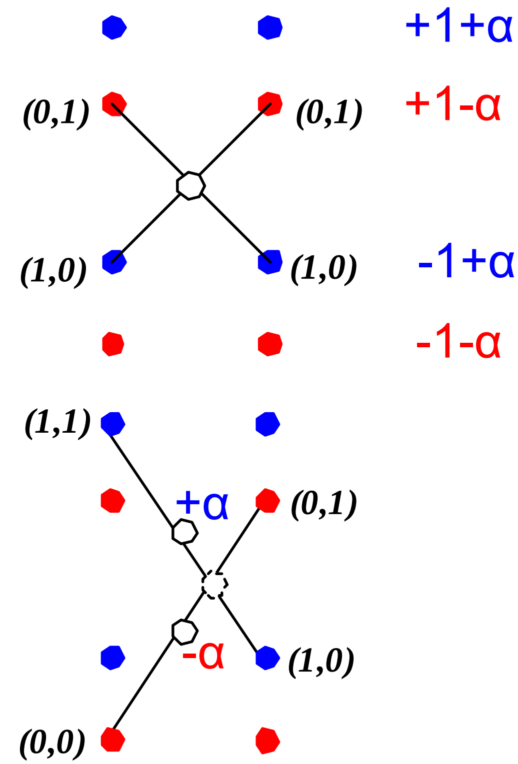




- **Four signal levels**

Partial Response DFE & CDR





- Four signal levels
- Offset edge samplers for transitions with ISI
  - Otherwise timing error
- Need to filter edges – similar to PAM4

Serial Equalization TechForum2007

- (0:05) Scope of presentation
- (0:15) Background/history : goals, how have things been done
- (0:10) System environment issues for equalization
- (0:10) Equalization classification & qualitative tradeoffs
- (0:15) Communication theory
- (0:30) Implementation issues I
- (0:15) Break
- **(0:15) Implementation issues II**
  - Setting coefficients
- (0:40) Equalizer performance tradeoffs
- (0:10) Modeling methodology for equalization, adaptation
- (0:15) Measurement & instrumentation
- Summary & conclusions

Three Basic Methods for Setting Equalization Coefficients

1. Lookup table 'set and forget'
   - Simple, based on lab measurement
   - Subject to manufacturing and environment variations
2. Adapt once on power-up
   - More complex
   - Subject to environment variation
3. Continuous adaptation
   - Most complex
   - Most complete

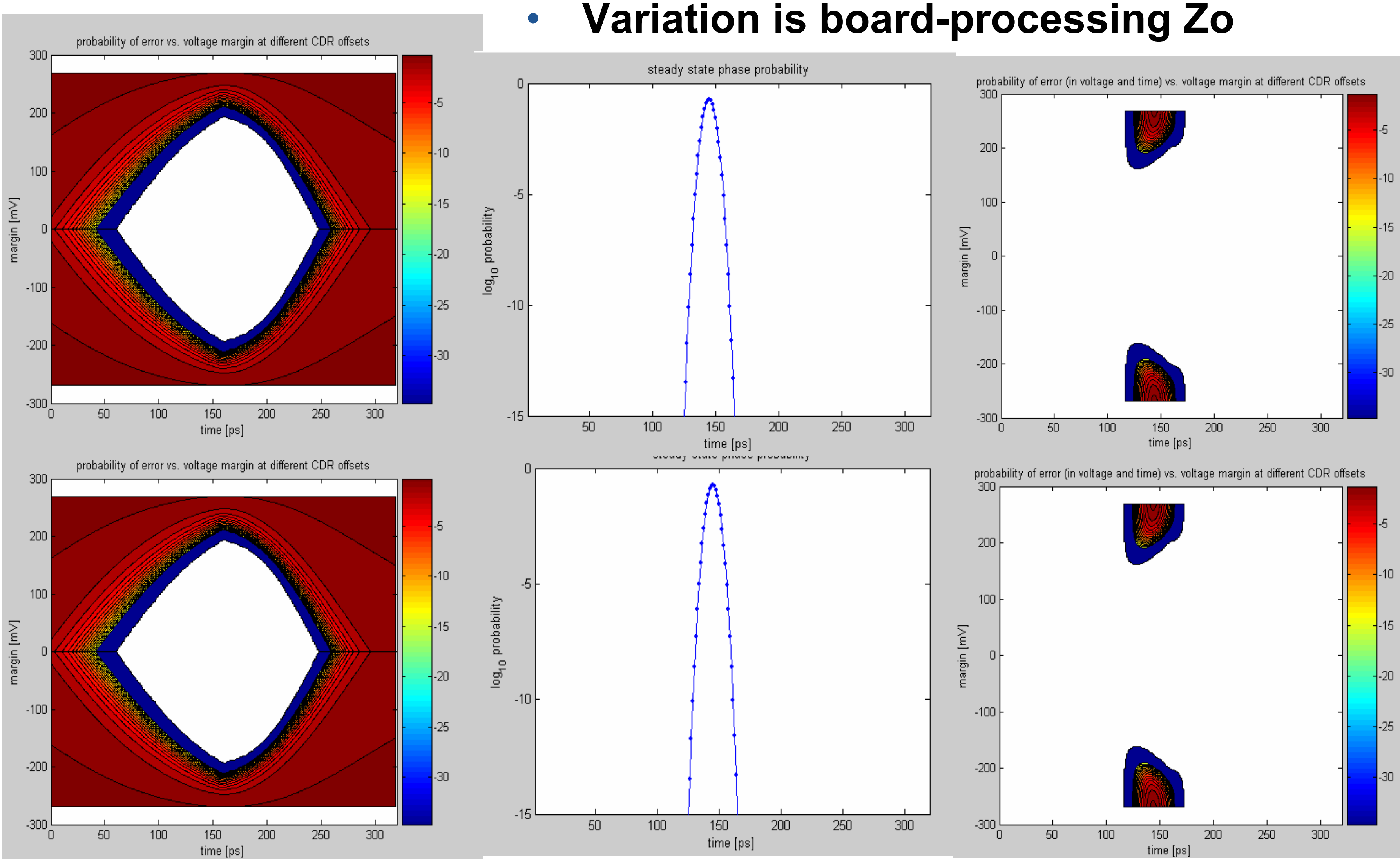
- What is really needed?

Simulation : 3.2G NRZ Set & Forget vs. Adapt Once S&F optimized @ Zo, Both Sims @ hhh Corner

- **Variation is board-processing Zo**

Set & forget

Adapt once



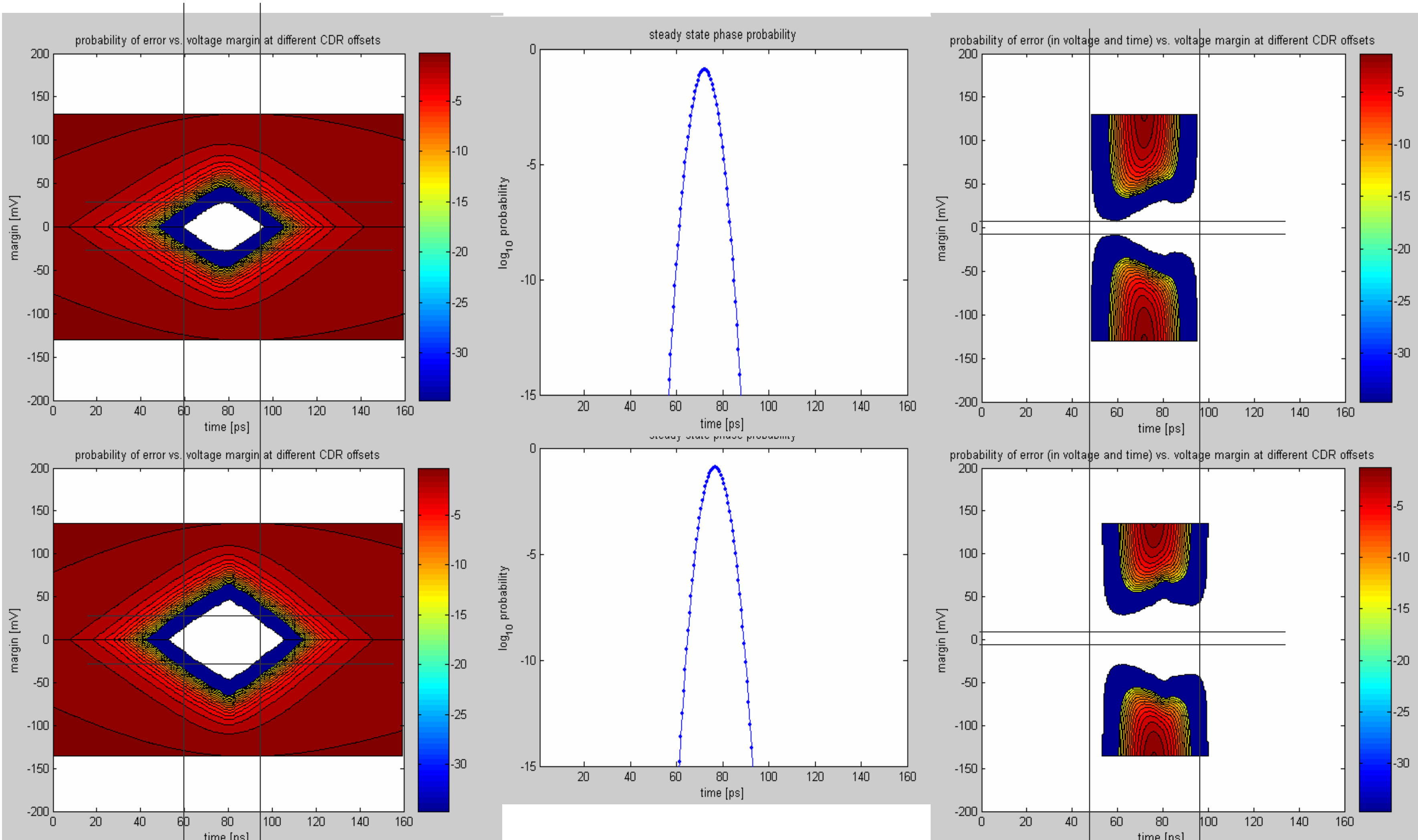
(a) (b) (c)

intel LeCroy Rambus

Simulation : 6.4G NRZ Set & Forget vs. Adapt Once S&F optimized @ Zo, Both Sims @ hhh Corner

Set & forget

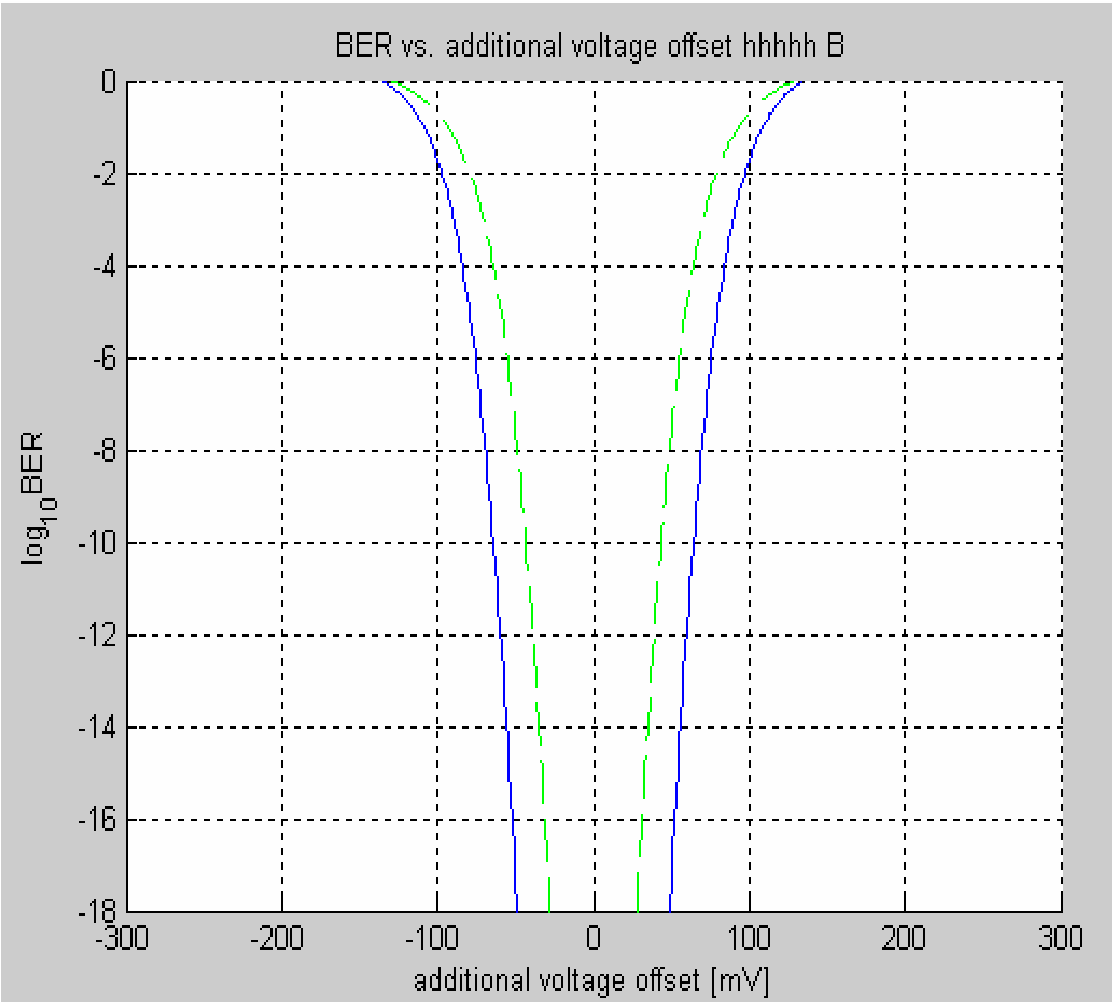
Adapt once



(a) (b) (c)

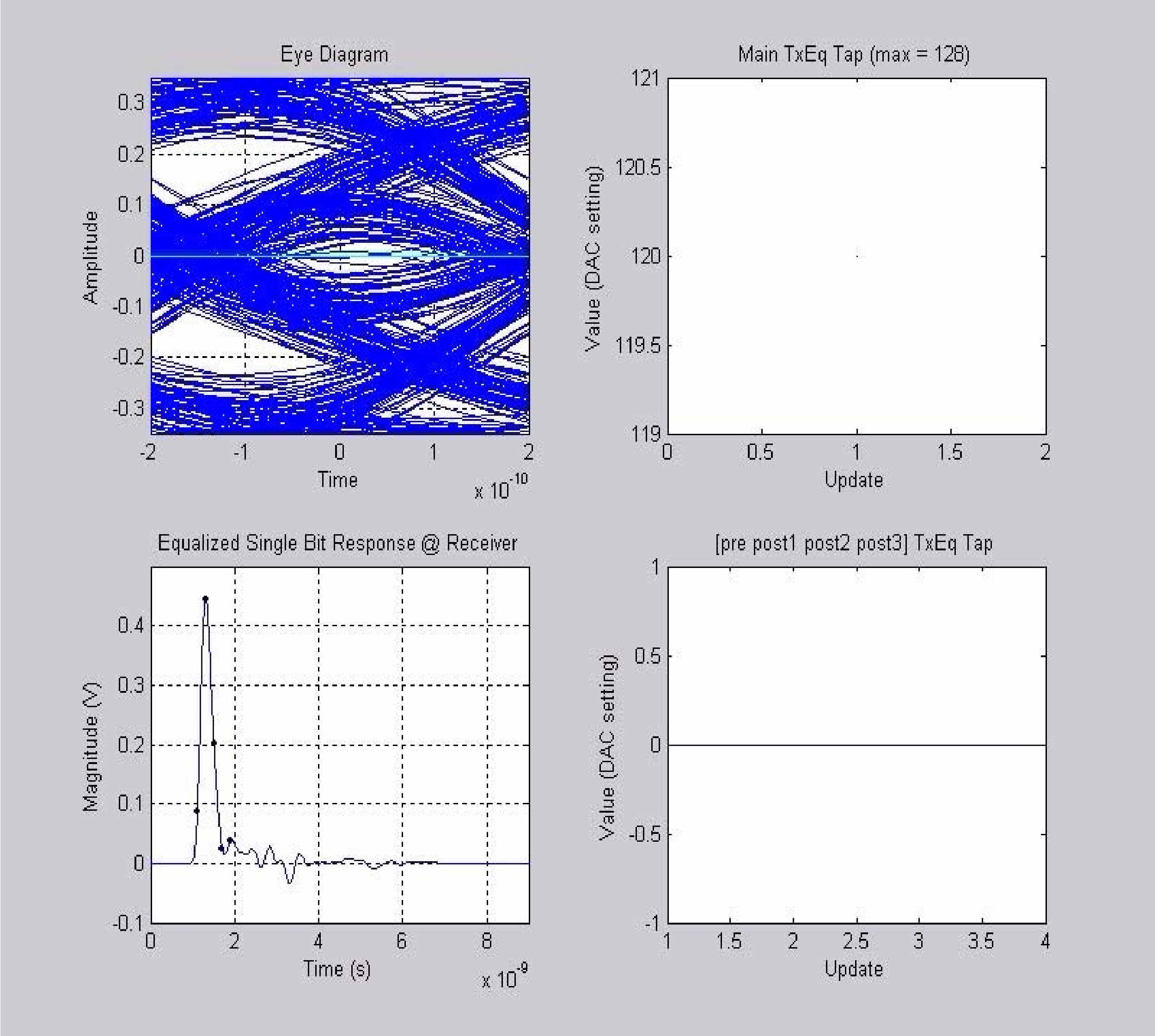
intel LeCroy Rambus

Sim : 6.4G NRZ Set & Forget vs. Adapt Once BER Tub Comparison

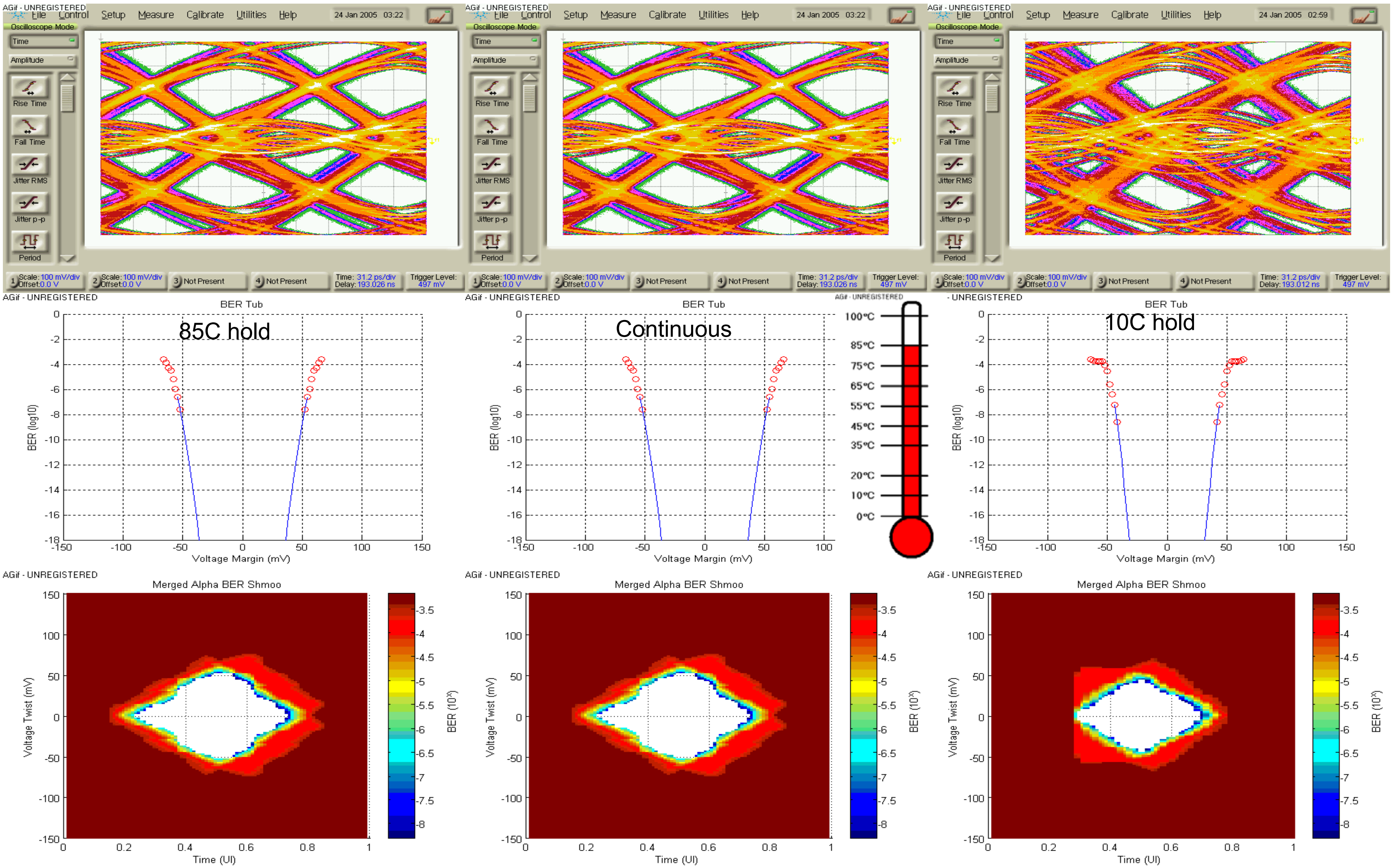


- Significant difference in margins at 6.4G
- Set and forget methods fall apart at higher data rates

Tx Adaptation Example (animation)



Measured prDFE/Tx4 Cycling 10C-85C



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Serial Equalization *TechForum2007*

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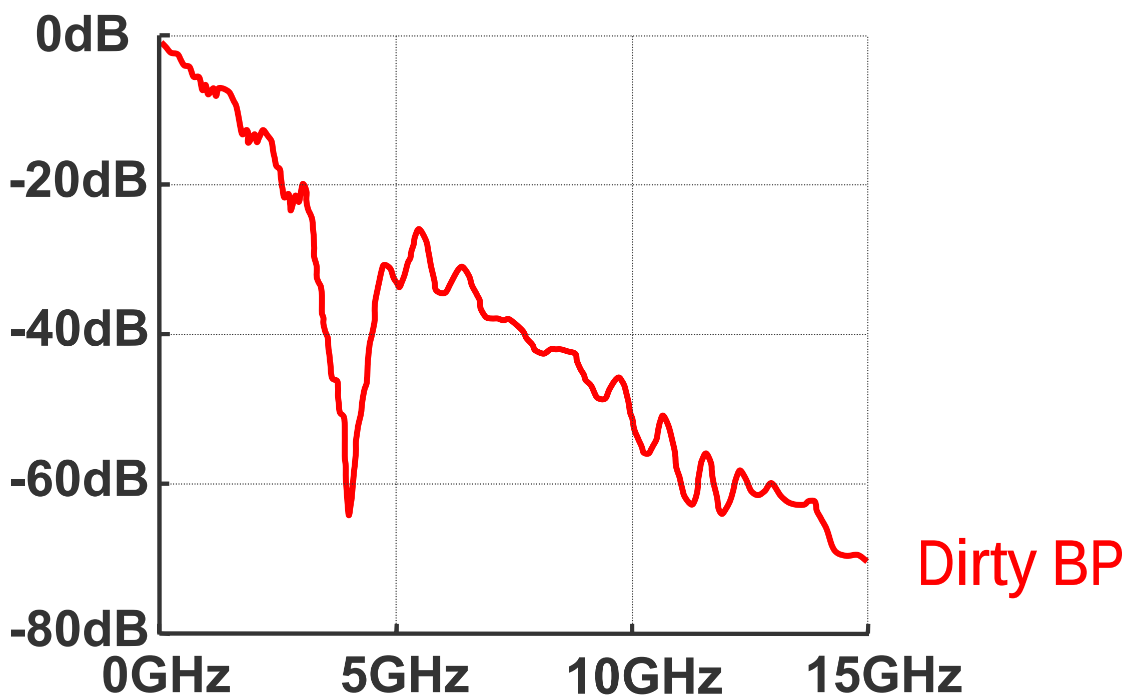
Presentation Goals

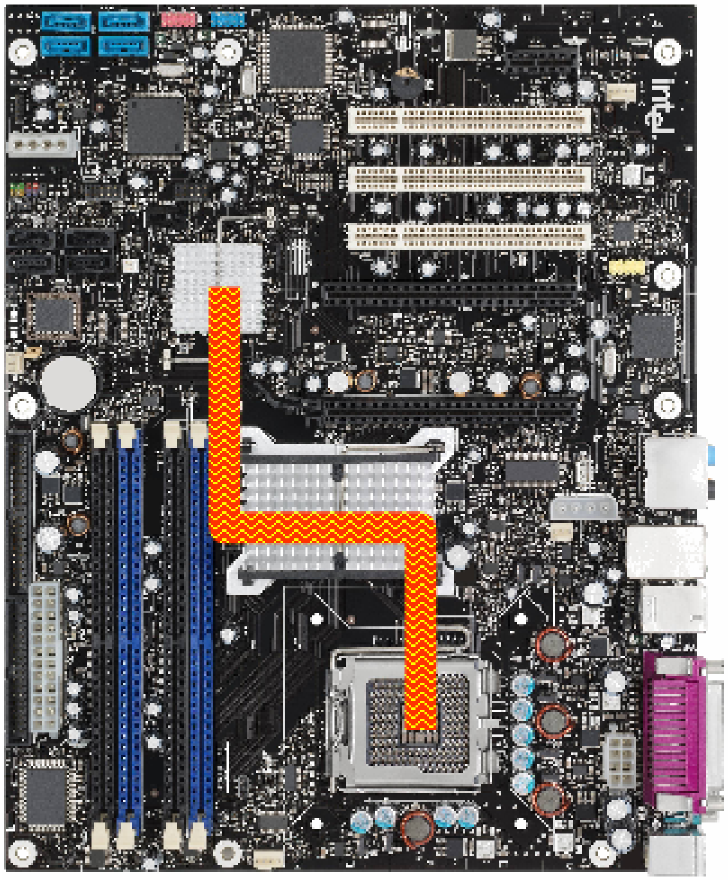
- Performance tradeoffs of linear and decision feedback equalizers
  - vs. tap quantity, channel type, practical tap placement
- Practical considerations of equalizers
  - Jitter, noise, coefficient resolution

Channel Insertion Loss: Dirty BP

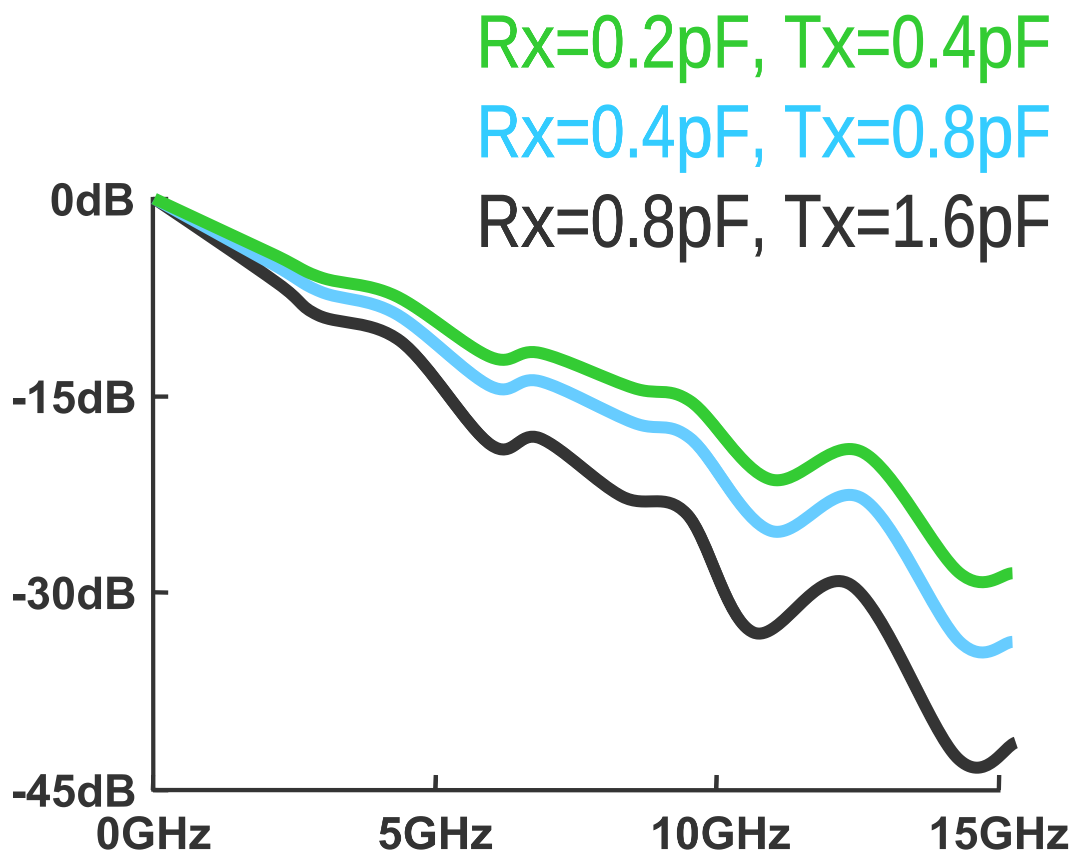


Dirty BP:
- Interleaved routing
  - NEXT
- Tx Pad cap=1pF
- Rx Pad cap=1pF
- PTH stubs=30 layers
- FCI Airmax connectors
- Stripline backplane
- Sockets on Tx and Rx

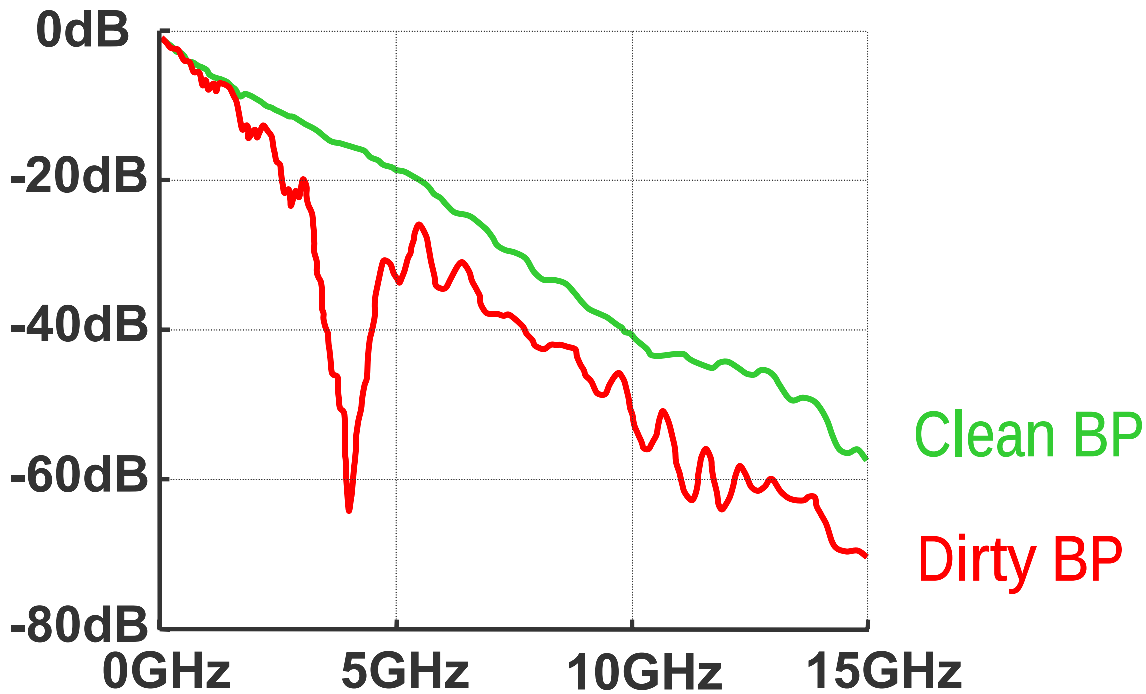
BW degradation due to pad cap.



7" microprocessor/ chipset interface

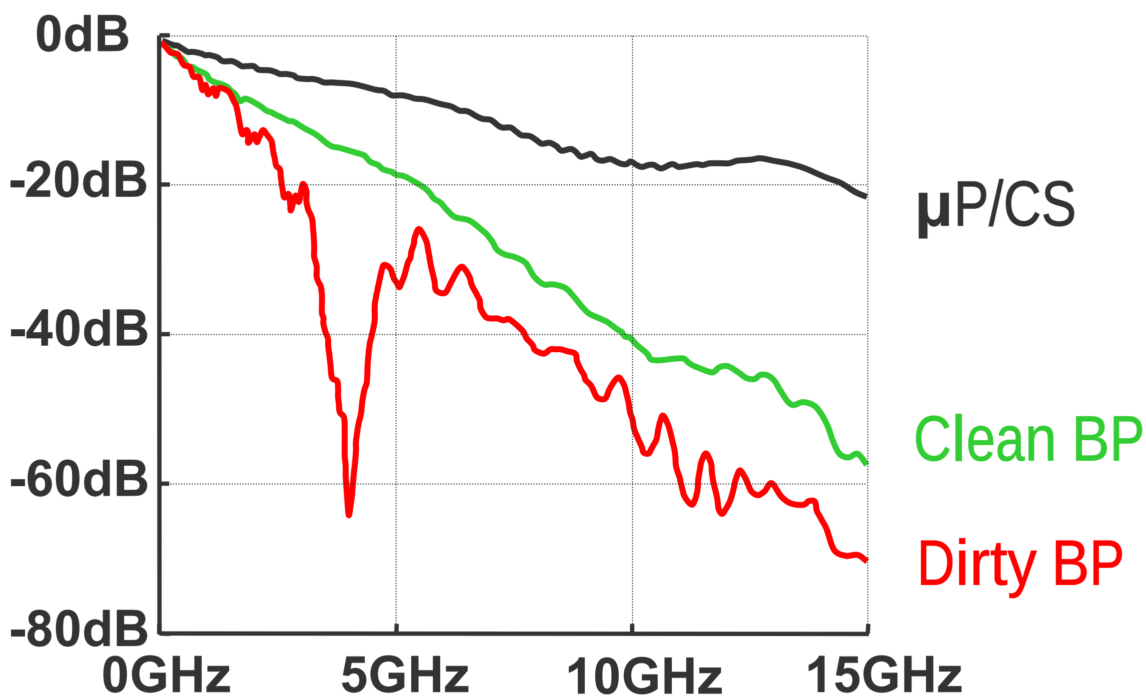


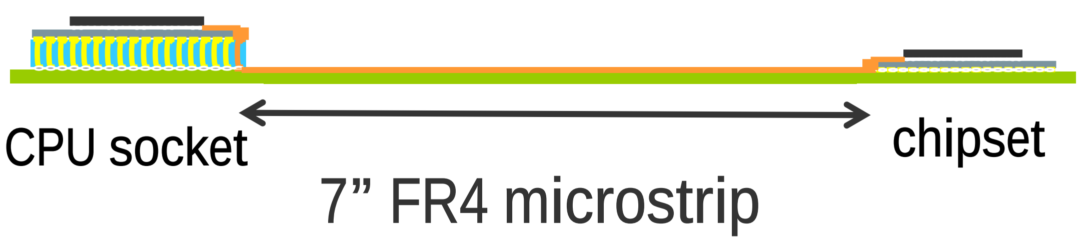
Channel Insertion Loss: Clean BP



Clean BP:
- Non-interleaved routing
  - FEXT only
- Tx Pad cap=0.4pF
- Rx Pad cap=0.1pF
- PTH stubs=8 layers
- FCI Airmax connectors
- Stripline backplane
- Sockets on Tx and Rx

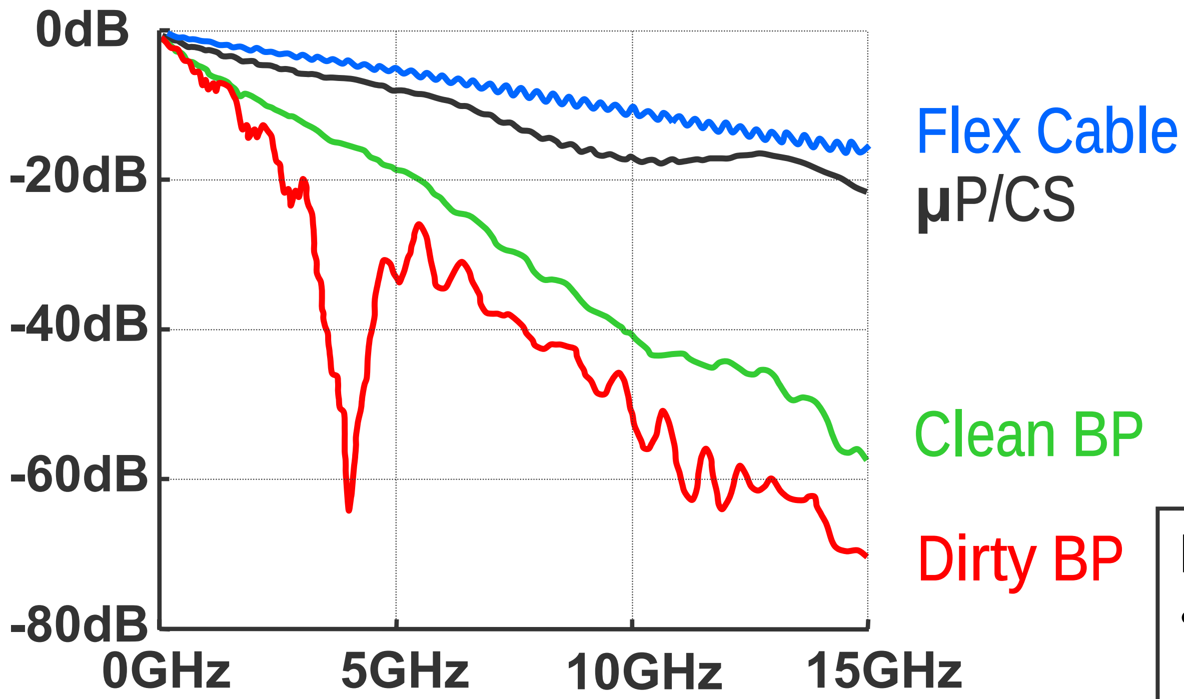
Channel Insertion Loss: µprocessor

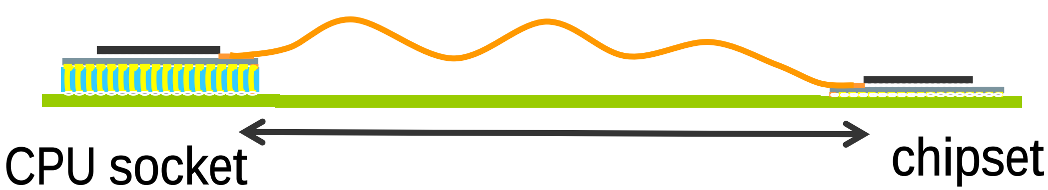




Microprocessor/Chipset:
- **Non-interleaved routing**
  - **FEXT only**
- **Tx Pad cap=0.4pF**
- **Rx Pad cap=0.1pF**
- **microstrip**
- **Sockets on Tx**

Channel Insertion Loss: Flex





8” Polyimide microstrip Flex

Low-loss flex interface:

- Non-interleaved routing
  - FEXT only
- Tx Pad cap=0.4pF
- Rx Pad cap=0.2pF
- PTH stubs=30 layers
- FCI Airmax connectors
- Stripline backplane
- Sockets on Tx and Rx

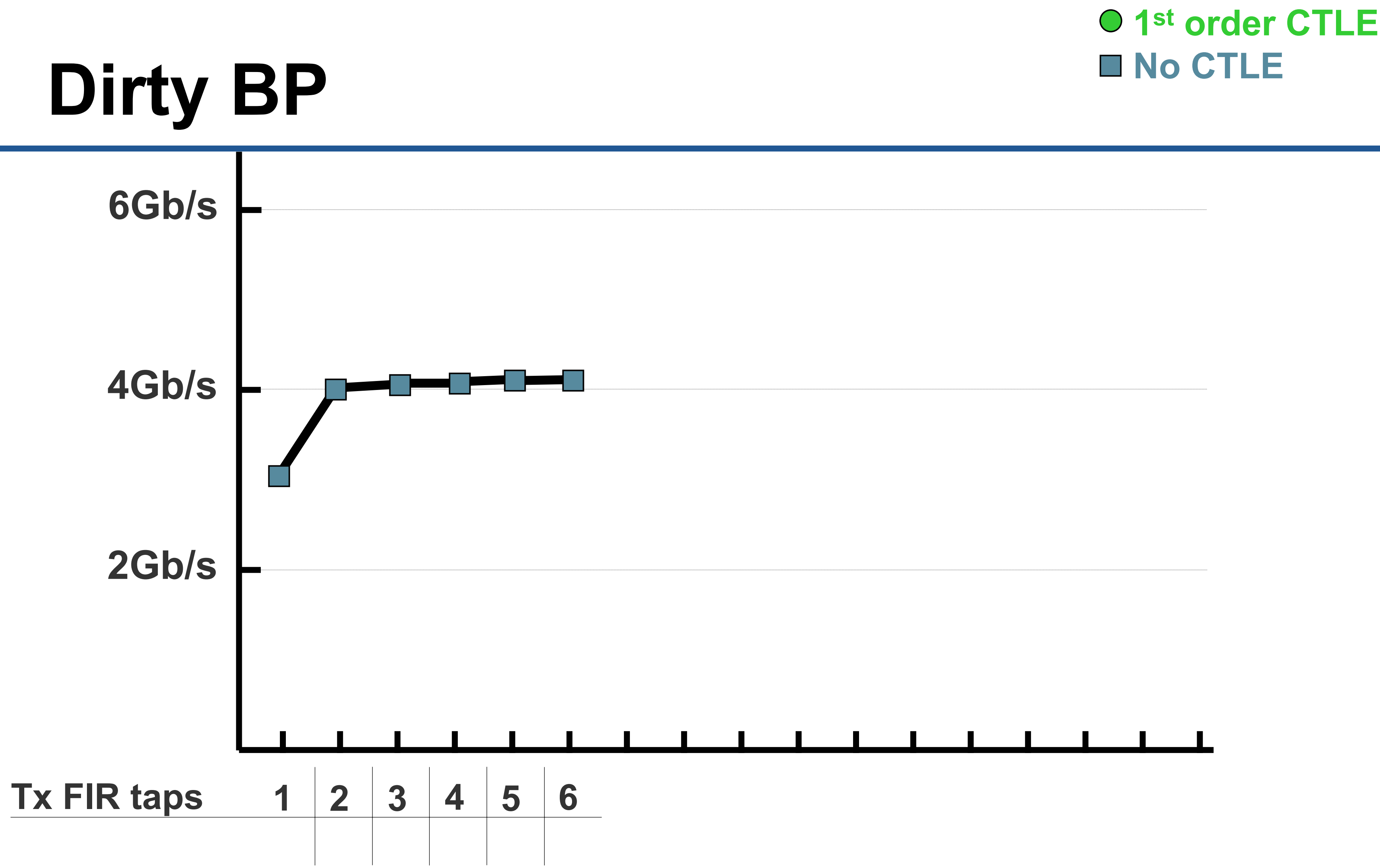
Key assumptions (unless otherwise indicated)

- Modulation: Binary NRZ
- BER target = 10^{-12}
- Data scrambling enabled
- Recursively optimized equalization with statistical-based voltage margin metric
- Tx swing (+/- 500mV)
- Tx FIR
  - 5 bits coefficient resolution
  - 2 tap → postcursor taps = 1, precursor taps = 0
  - 3 tap → postcursor taps = 1, precursor taps = 1
  - 4 tap → postcursor taps = 2, precursor taps = 1
  - 5 tap → postcursor taps = 3, precursor taps = 1
  - 6 tap → postcursor taps = 4, precursor taps = 1
- Rx DFE
  - Resolution = 8 bits wrt Tx swing (+/- 500mV)
  - No error propagation
  - All DFE taps are optimally placed
  - Rx DFE w/ tap block
- Rx CTLE
  - 1 equalizer zero, 1 equalizer pole, 20GHz GBW product, 12dB maximum AC gain

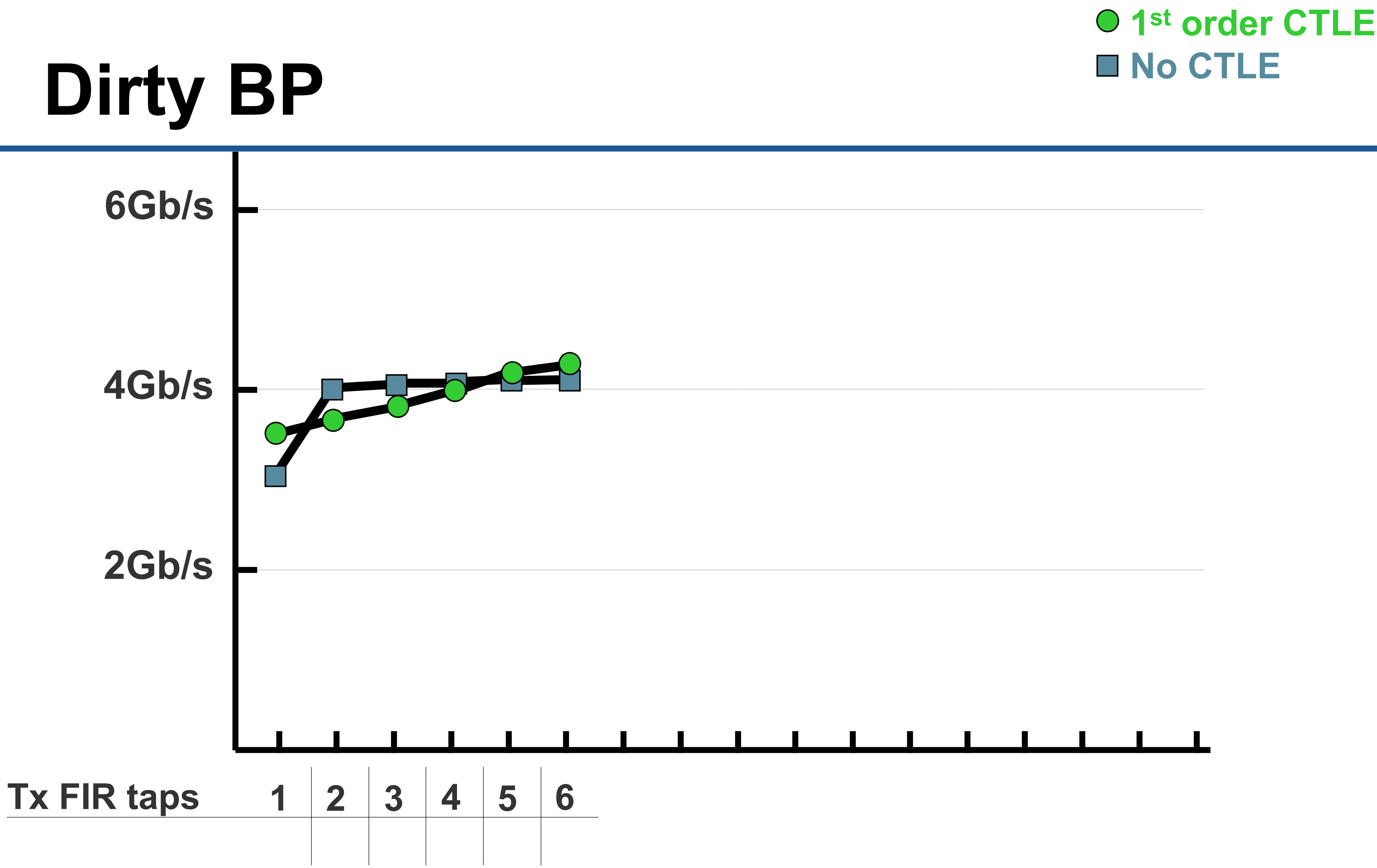
Equalization method comparison: Tx FIR vs. CTLE vs. DFE

- Tx jitter
  - 1% residual duty cycle error
  - 0.005UI RMS Tx jitter (normally distributed)
  - pk-pk post-highpass absolute jitter=0.12UI (BER=10^{-12})
- Rx jitter
  - 1% residual duty cycle error
  - 0.01UI rms Rx sampling jitter (normally distributed)
  - 0.2UI (pk-pk) Rx sampling jitter (uniformly distributed)
  - pk-pk UI jitter=0.42UI (BER=10^{-12})
- Rx input referred noise
  - 1mV (RMS, normally distributed)
  - pk-pk noise=14mV (BER=10^{-12})

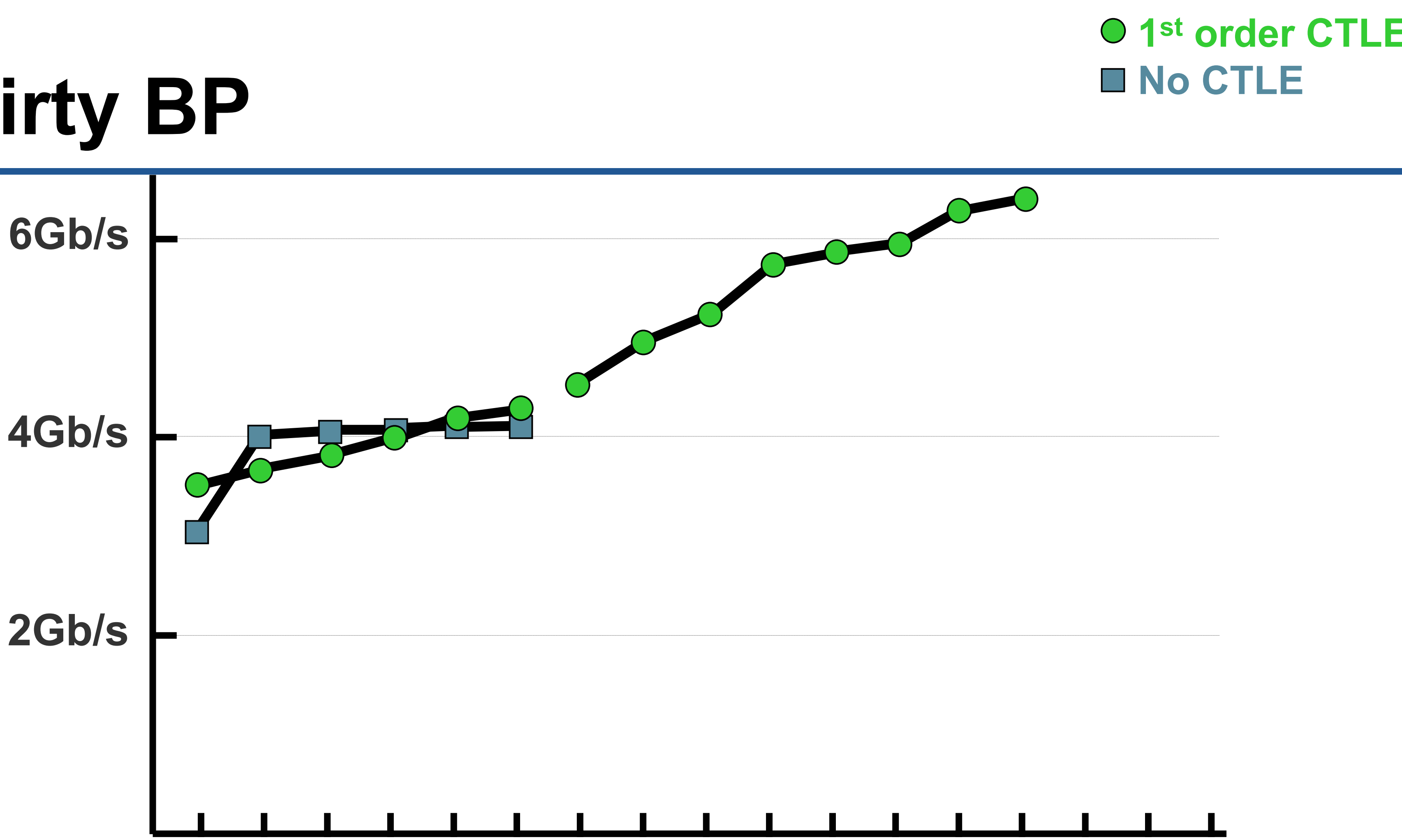
Dirty BP



Dirty BP

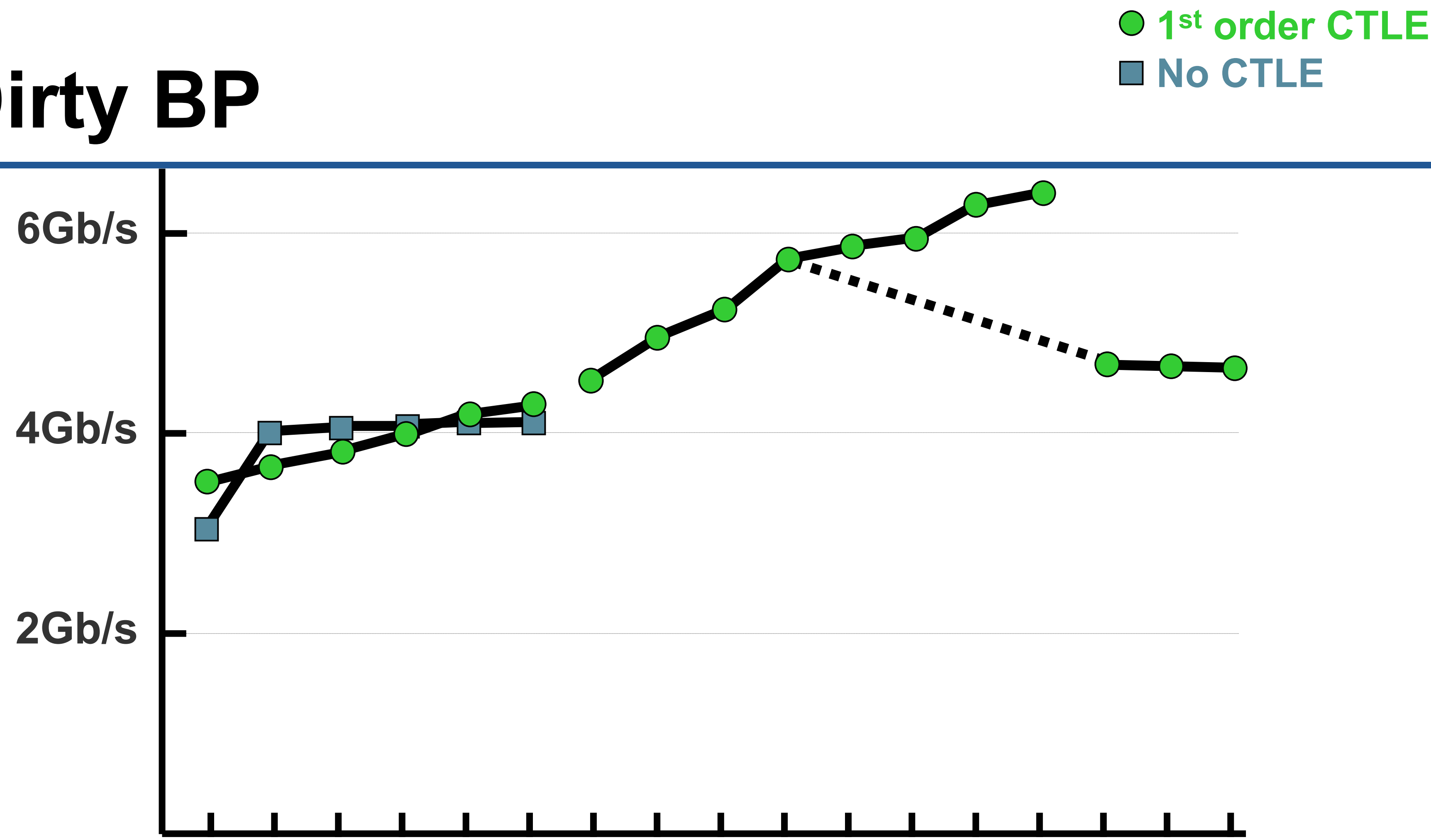


Dirty BP



Tx FIR taps	1	2	3	4	5	6	4	4	4	4	4	4	4	4
DFE taps							1	2	4	8	16	32	64	128

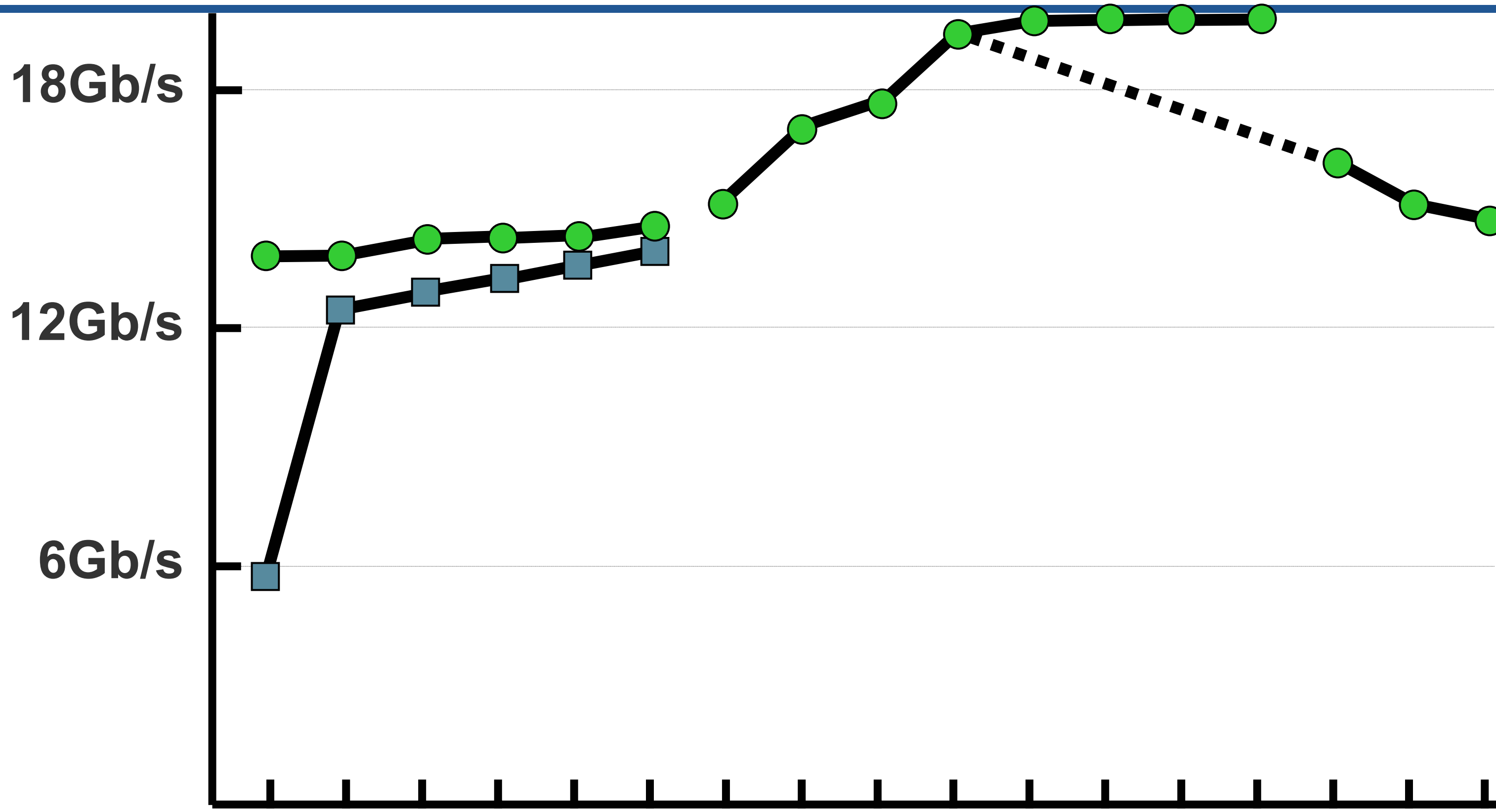
Dirty BP



Tx FIR taps	1	2	3	4	5	6	4	4	4	4	4	4	4	4	4	4	4
DFE taps							1	2	4	8	16	32	64	128	8	8	8
DFE tap start															2	3	4

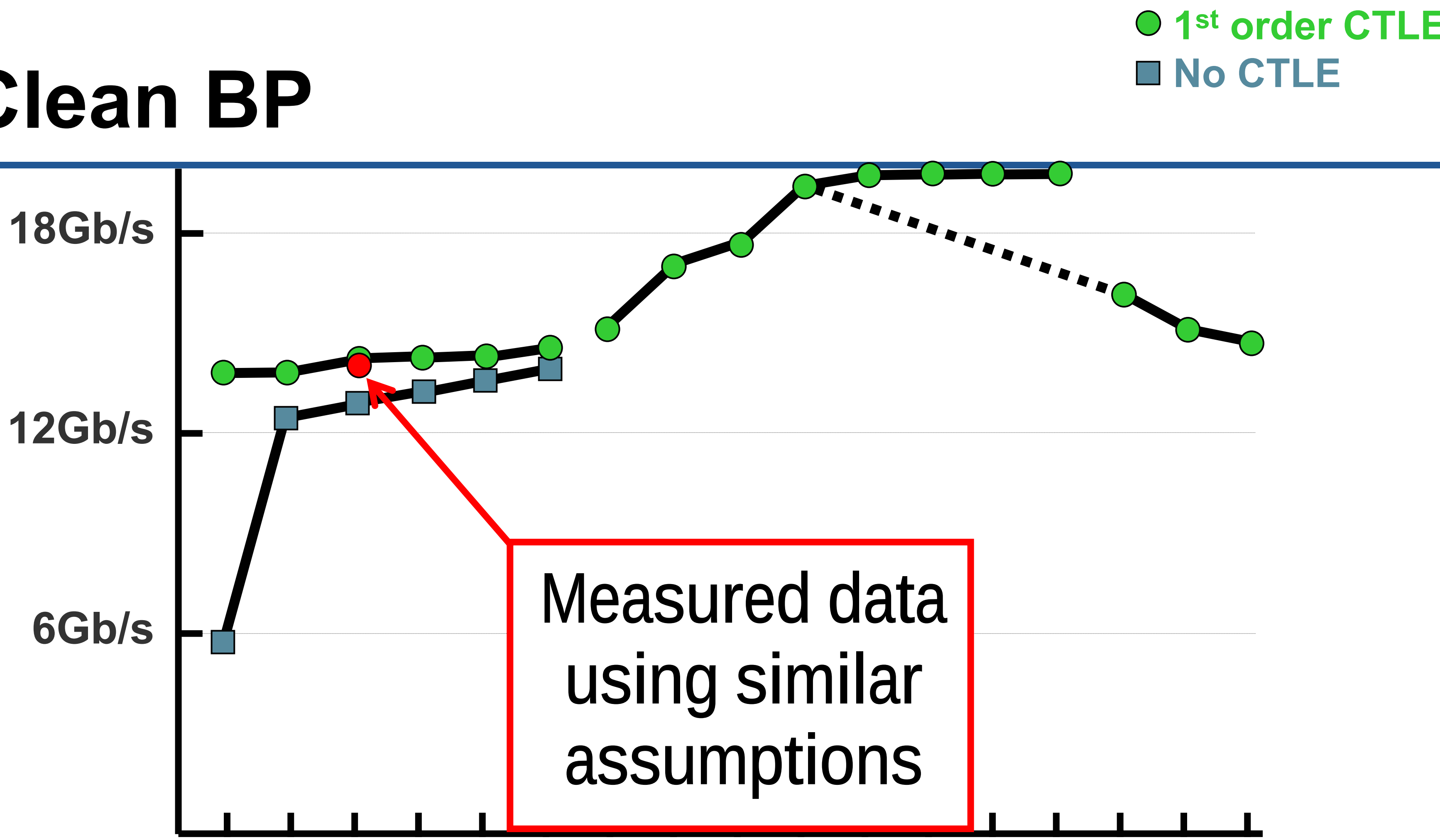
Clean BP

1st order CTLE
No CTLE



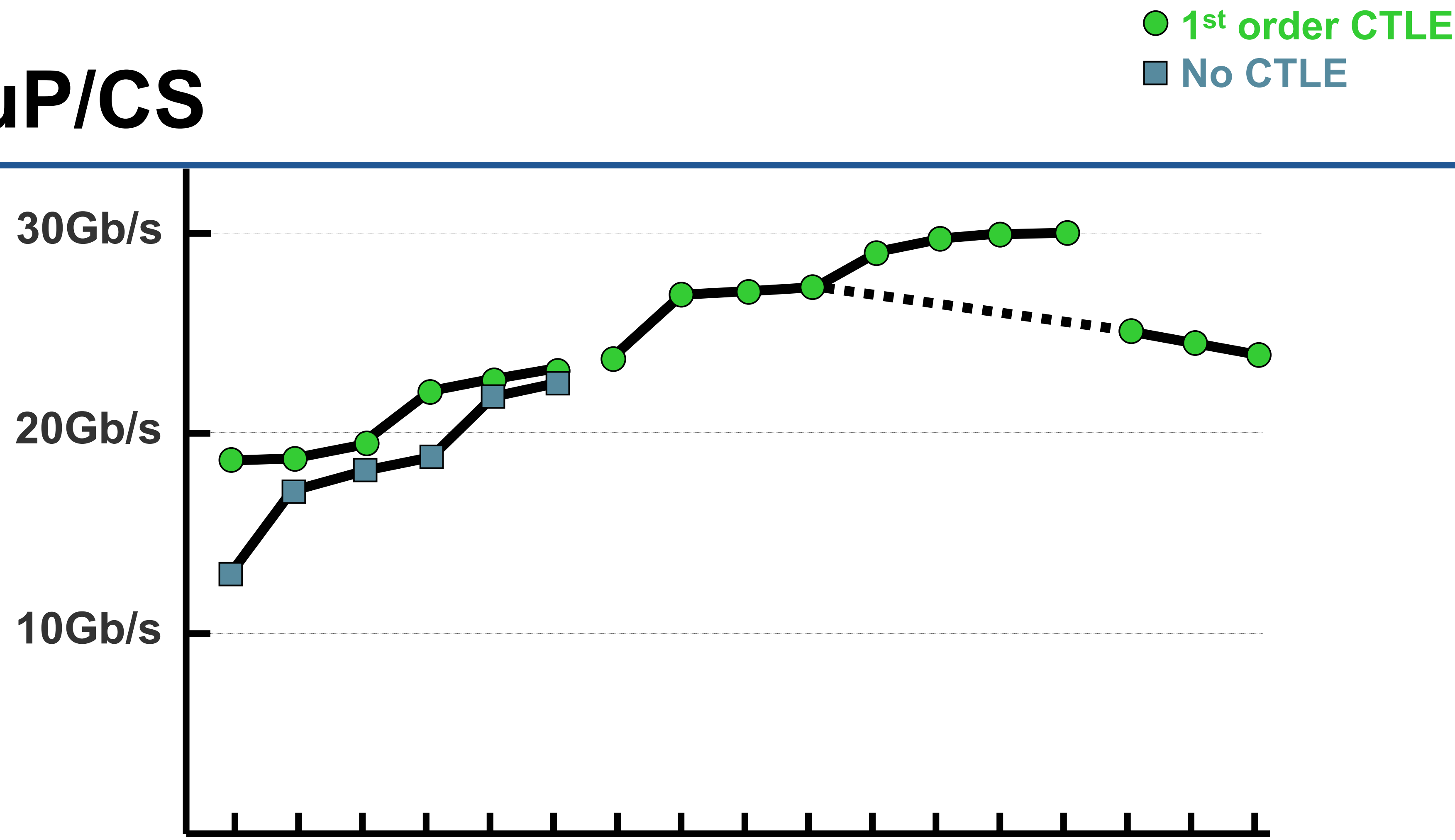
Tx FIR taps	1	2	3	4	5	6	4	4	4	4	4	4	4	4	4	4	4
DFE taps							1	2	4	8	16	32	64	128	8	8	8
DFE tap start															2	3	4

Clean BP



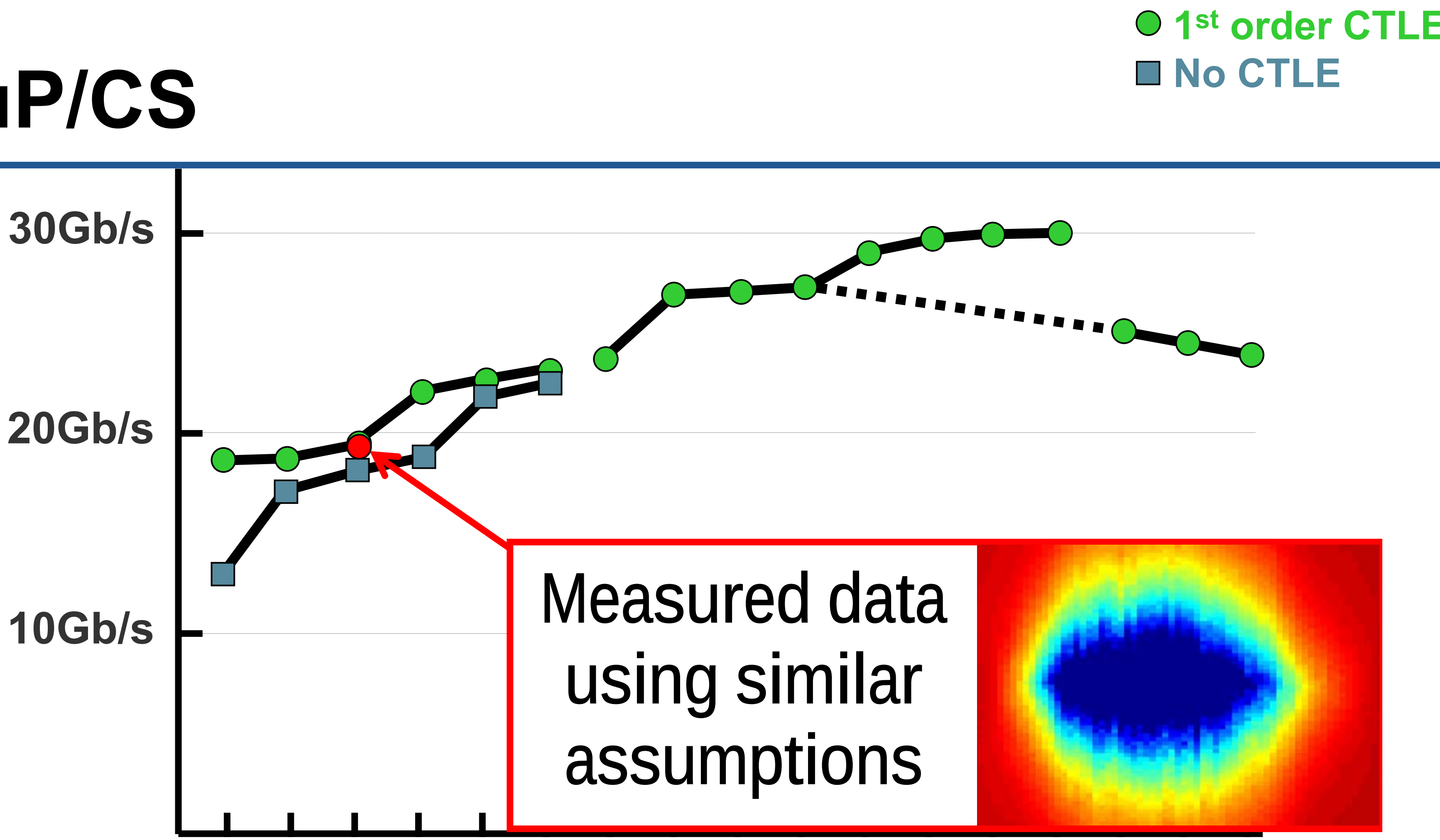
Tx FIR taps	1	2	3	4	5	6	4	4	4	4	4	4	4	4	4	4	4
DFE taps							1	2	4	8	16	32	64	128	8	8	8
DFE tap start															2	3	4

µP/CS



Tx FIR taps	1	2	3	4	5	6	4	4	4	4	4	4	4	4	4	4	4
DFE taps							1	2	4	8	16	32	64	128	8	8	8
DFE tap start															2	3	4

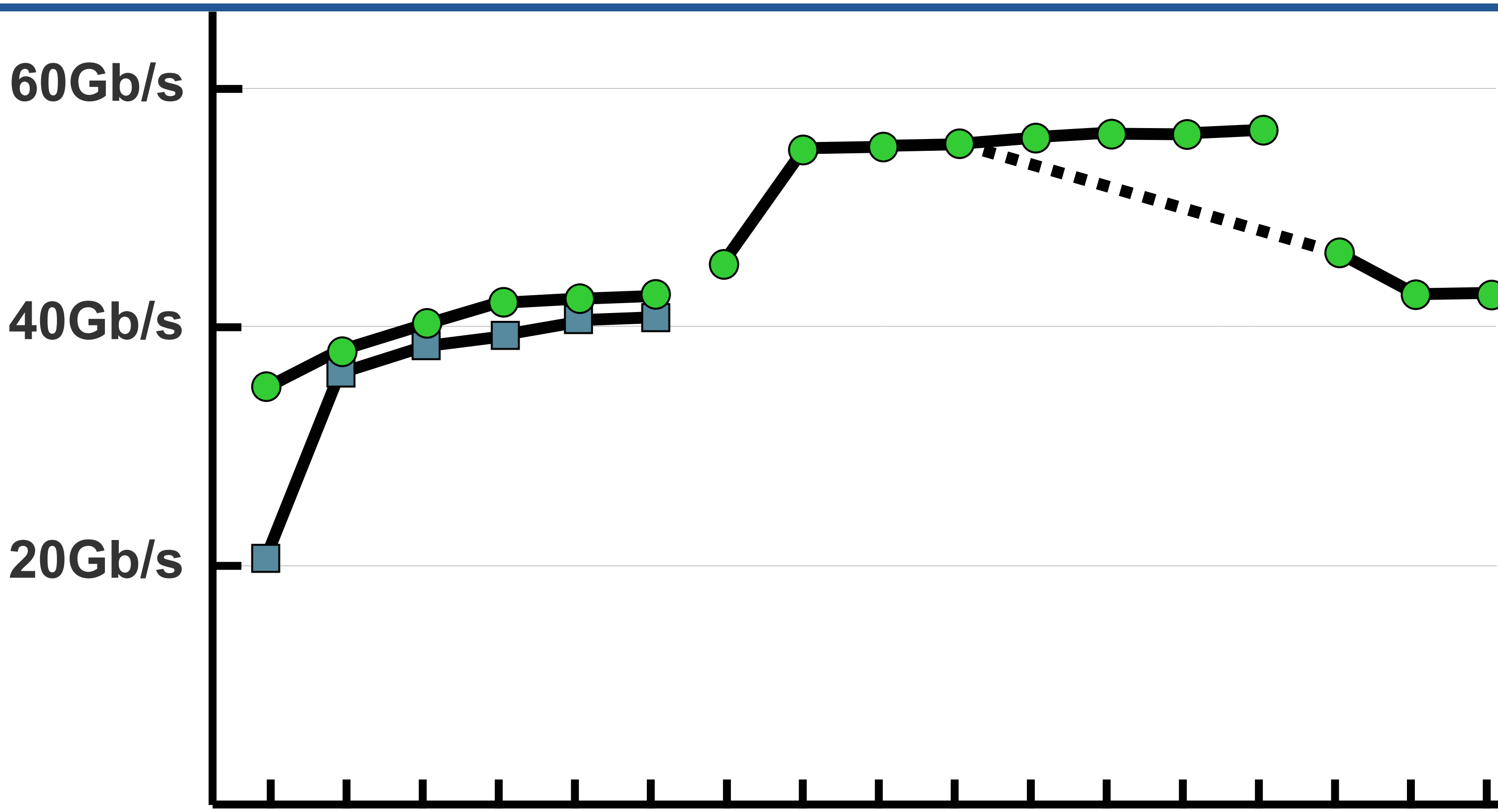
µP/CS



Tx FIR taps	1	2	3	4	5	6	4	4	4	4	4	4	4	4	4	4	4
DFE taps							1	2	4	8	16	32	64	128	8	8	8
DFE tap start															2	3	4

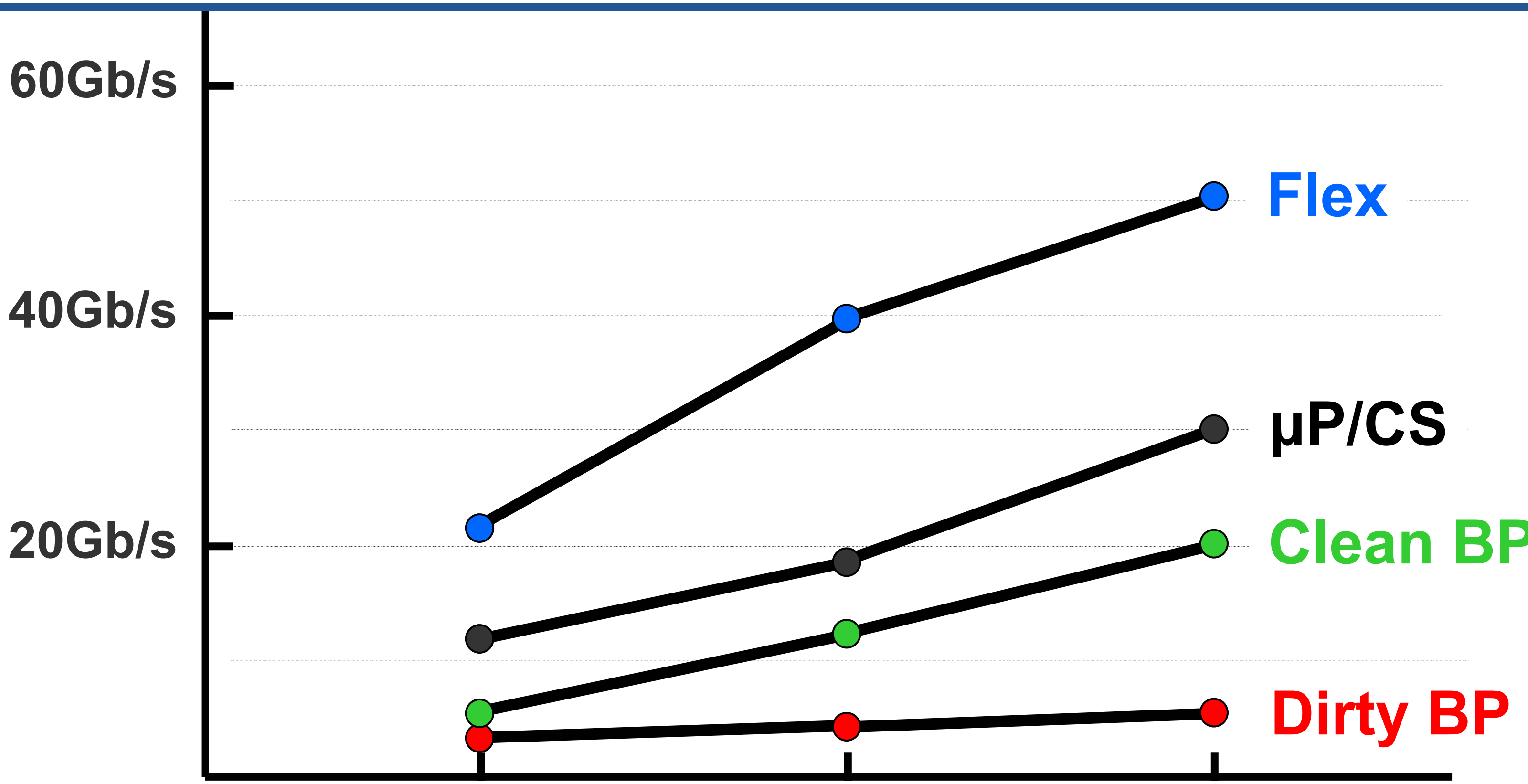
Flex

● 1st order CTLE
■ No CTLE



Tx FIR taps	1	2	3	4	5	6	4	4	4	4	4	4	4	4	4	4	4
DFE taps							1	2	4	8	16	32	64	128	8	8	8
DFE tap start															2	3	4

Channel vs. Equalization Comparison



Tx FIR taps	1	4	4
DFE taps			8
1st order CTLE	No	Yes	Yes

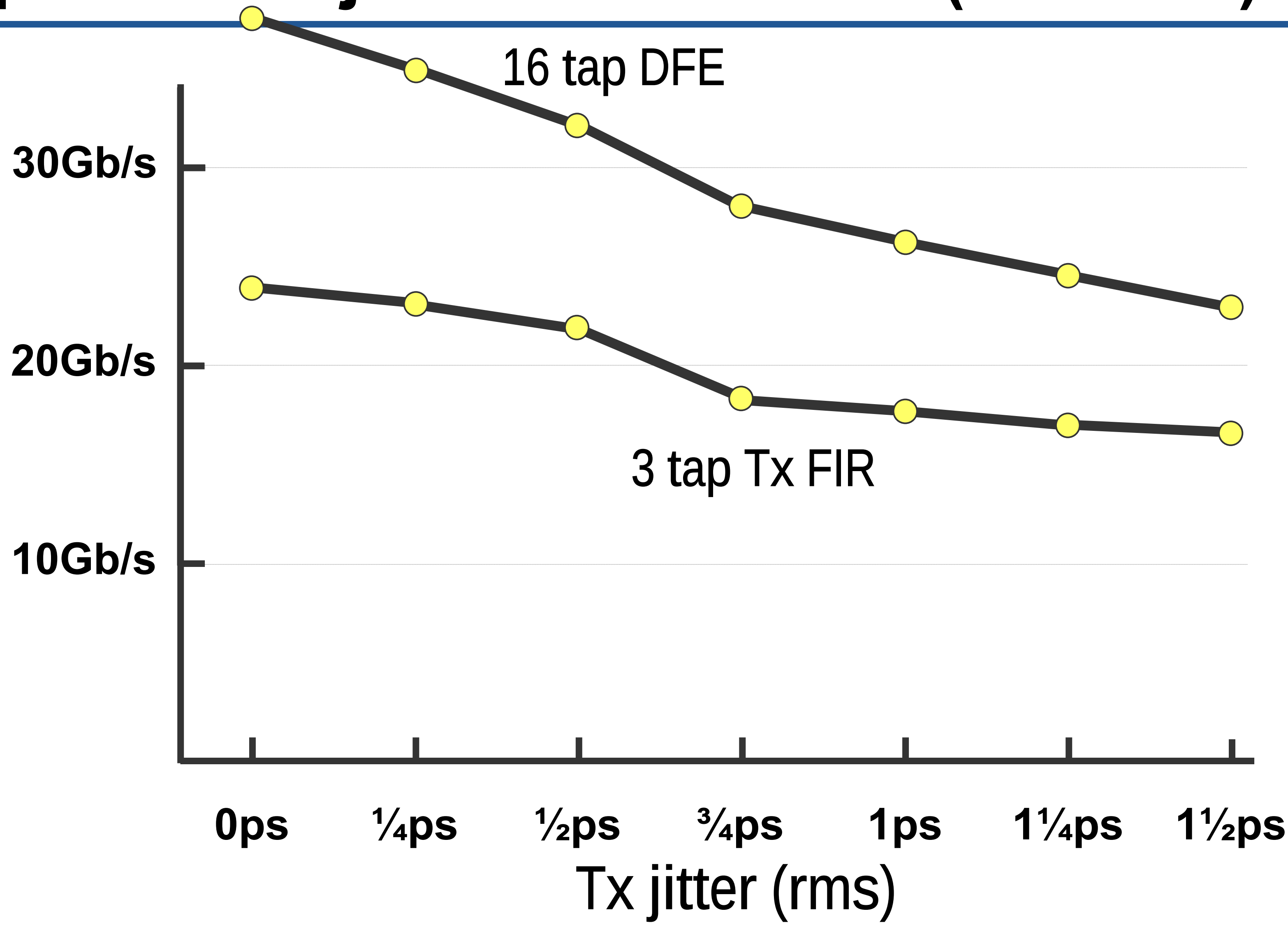
Conclusions #1

- Measured data matches Intel's signaling analysis
- Most practical channels limited by discontinuities
  - Rather than by skin effect and dielectric loss
  - Pad capacitance, vias, sockets dominant
- Backplane channels are not created equal
  - Stub length major performance limiter
- For T-line loss-limited channels, Tx FIR provides ample performance

Equalizer practical considerations

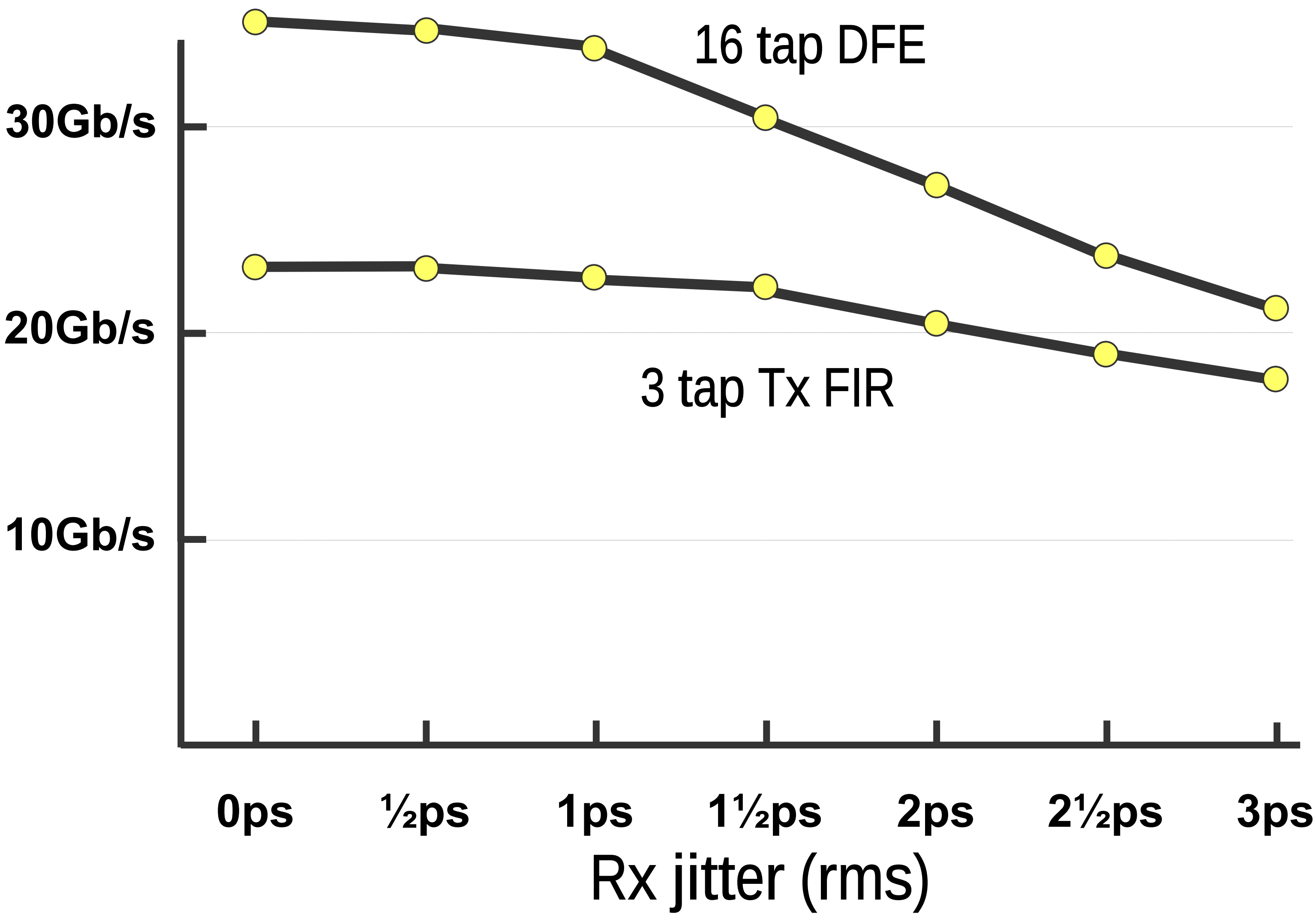
- Comparison done on µP/CS channel
- Sweep variables:
  - Tx jitter
  - Rx jitter
  - Rx slicer noise
  - Coefficient resolution
- Crosstalk not included in analysis

µP/CS: Tx jitter vs. data rate (no Xtalk)



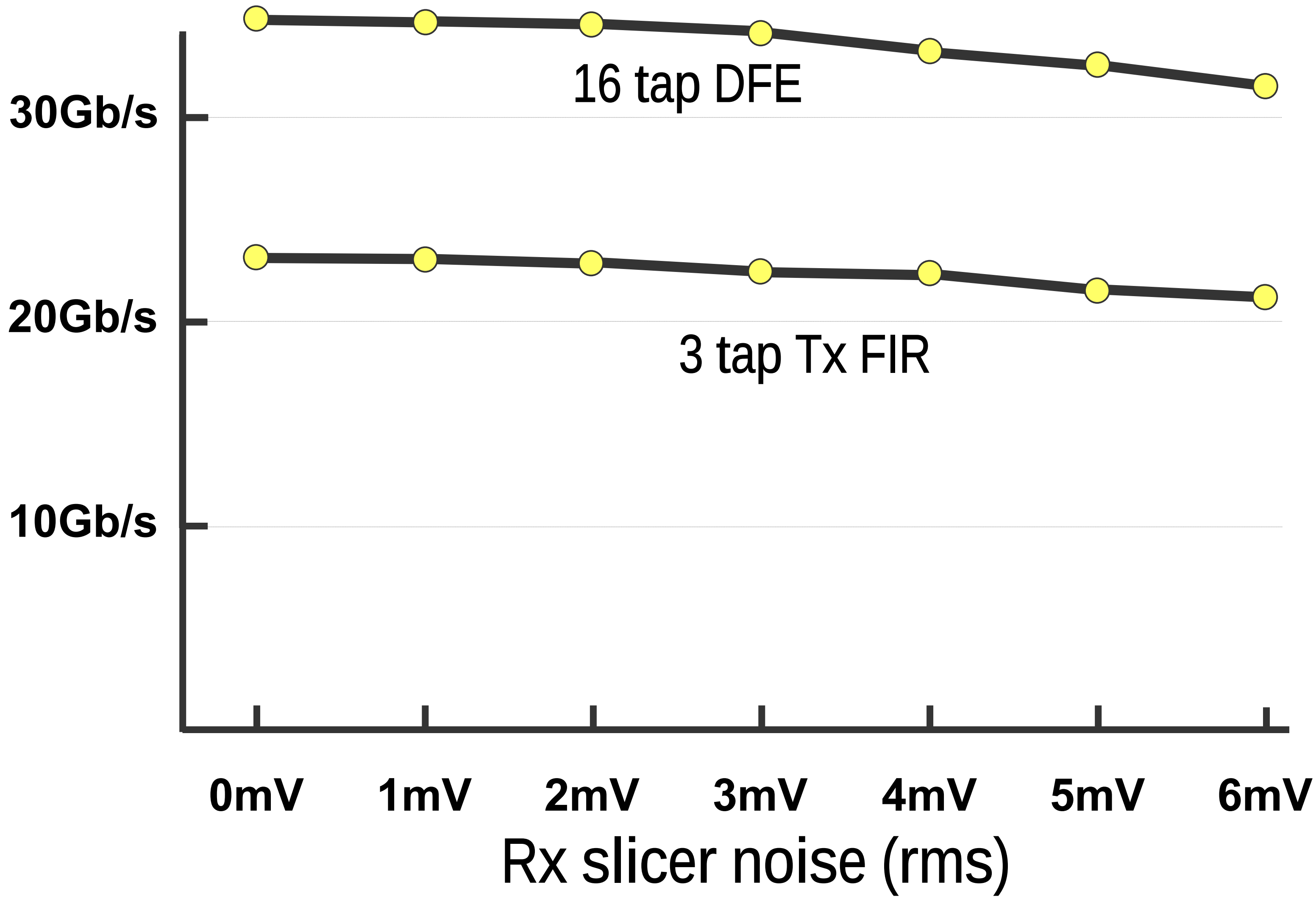
Rx slicer noise=1mV rms, Rx jitter=½ps rms

µP/CS: Rx jitter vs. data rate (no Xtalk)



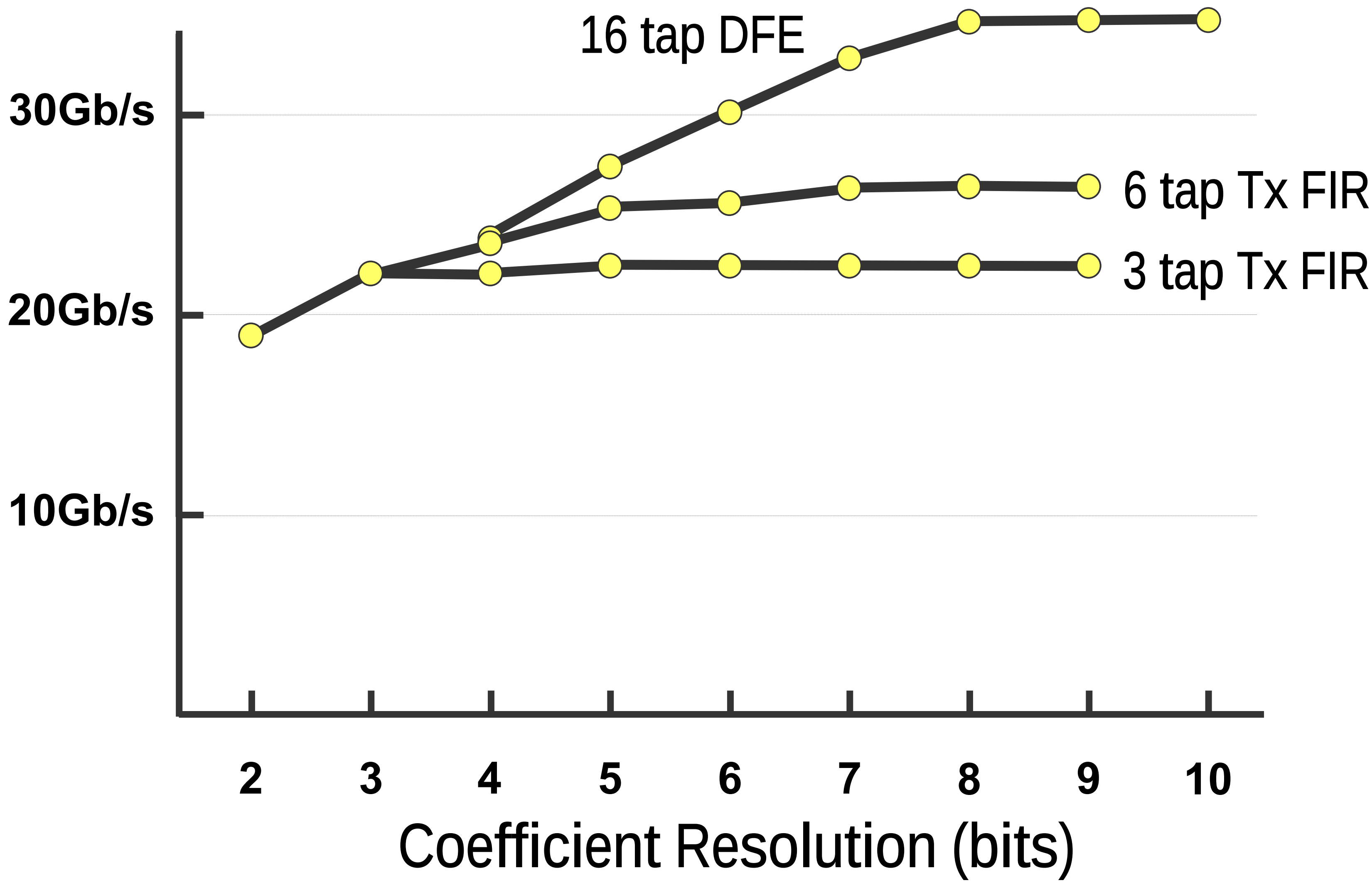
Tx jitter=¼ps rms, Rx slicer noise=1mV rms

µP/CS: Rx noise vs. data rate (no Xtalk)



Tx jitter=¼ps rms, Rx jitter=½ps rms

µP/CS: Resolution sweep (no Xtalk)



Tx jitter=¼ps rms, Rx jitter=½ps rms, Rx slicer noise=1mV rms

Conclusions #2

- For DFE to be beneficial:
  - Apply to discontinuity-limited channel w/ NEXT
  - Use multiple (>8) taps with high resolution
  - Don't skip first few taps (to eliminate speedpath)
- Link performance sensitivity to uncertainties:
  - Tx jitter – High
  - Rx jitter – Medium
  - Rx slicer noise – Low
- Copper has significant performance headroom
  - Maximum practical data rate for 8" Polyimide Flex channel exceeds 50Gb/s

References

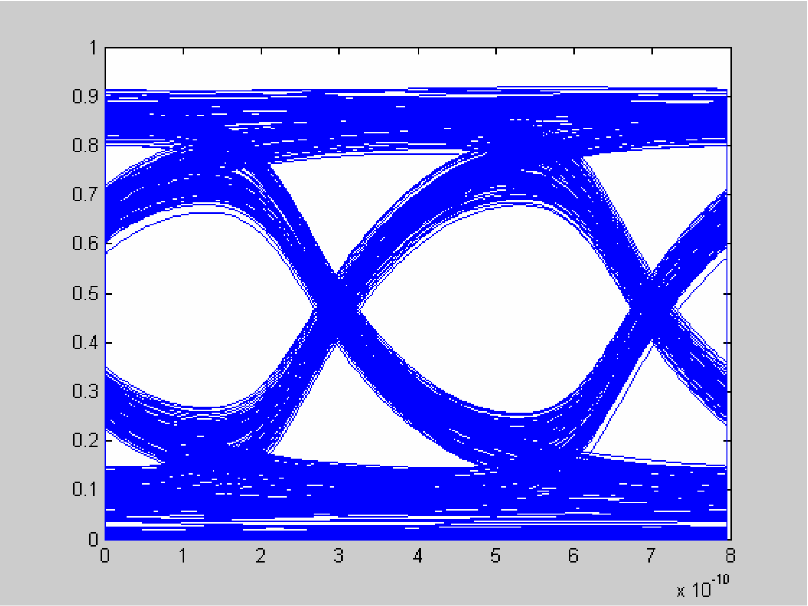
- **Tx FIR Architectures**
  - W. Dally and J. Poulton, "Transmitter equalization for 4 Gb/s signaling," presented at the Hot Interconnects Conf., 1996.
  - J.L. Zerbe et al., "Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplane transceiver cell," IEEE Journal Solid-State Circuits, vol. 38, no. 12, pp. 2121–2130, Dec. 2003 .
  - B. Casper et al., "8 Gb/s SBD link with on-die waveform capture," IEEE Journal Solid-State Circuits, vol. 38, no. 12, pp. 2111–2120, Dec. 2003.
- **Signaling Analysis Methods**
  - B. Casper et al., "An accurate and efficient analysis method for multi-Gb/s chip-to-chip signaling schemes," in Symp. VLSI Circuits Dig. Tech. Papers, June 2002, pp. 54–57.
  - V. Stojanovic and M. Horowitz, "Modeling and analysis of high-speed links Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003 21-24 Sept. 2003 Page(s):589 - 594
  - G. Balamurugan and N. Shanbag, "Modeling and Mitigation of Jitter in Multi-Gbps Source-Synchronous I/O Links," ICCD 2003, p.254-260
  - P. K. Hanumolu et al., "Analysis of PLL clock jitter in high-speed serial links.; Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on Volume: 50 Issue: 11 Nov. 2003 Page(s): 879- 886
  - A. Sanders et al., "Channel Compliance Testing Utilizing Novel Statistical Eye Methodology," DesignCon West 2004.
  - P. K. Hanumolu et al., "Jitter in high-speed serial and parallel links" Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on Volume: 4 23-26 May 2004 Page(s): IV- 425-8 Vol.4
  - V. Stojanovic et al., "Optimal linear precoding with theoretical and practical data rates in high-speed serial-link backplane communication," 2004 IEEE International Conference on Communications, Volume 5, 20-24 June 2004 Page(s):2799 - 2806 Vol.5
- **Measured Data Points**
  - B. Casper et al., "A 20Gb/s Forwarded Clock Transceiver in 90nm CMOS," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2006.
  - J. Jaussi et al., "A 20Gb/s Embedded Clock Transceiver in 90nm CMOS," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2006.

Serial Equalization *TechForum2007*

- (0:05) Scope of presentation
- (0:15) Background/history : goals, how have things been done
- (0:10) System environment issues for equalization
- (0:10) Equalization classification & qualitative tradeoffs
- (0:15) Communication theory
- (0:30) Implementation issues I
- (0:15) Break
- (0:15) Implementation issues II
- (0:40) Equalizer performance tradeoffs
- **(0:10) Modeling methodology for equalization, adaptation**
- (0:15) Measurement & instrumentation
- Summary & conclusions

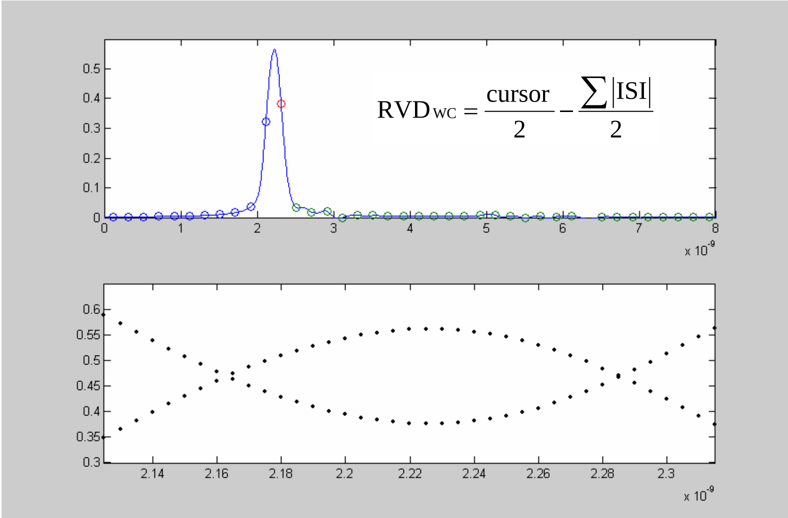
Signaling analysis techniques

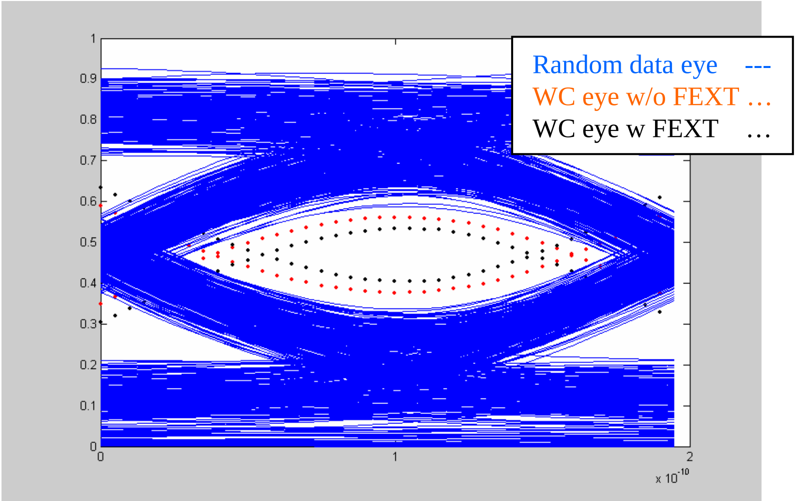
- Empirical calculation
  - Use random data
- Peak distortion analysis
- Statistical ISI analysis
- Statistical analysis w/ jitter



Signaling analysis techniques

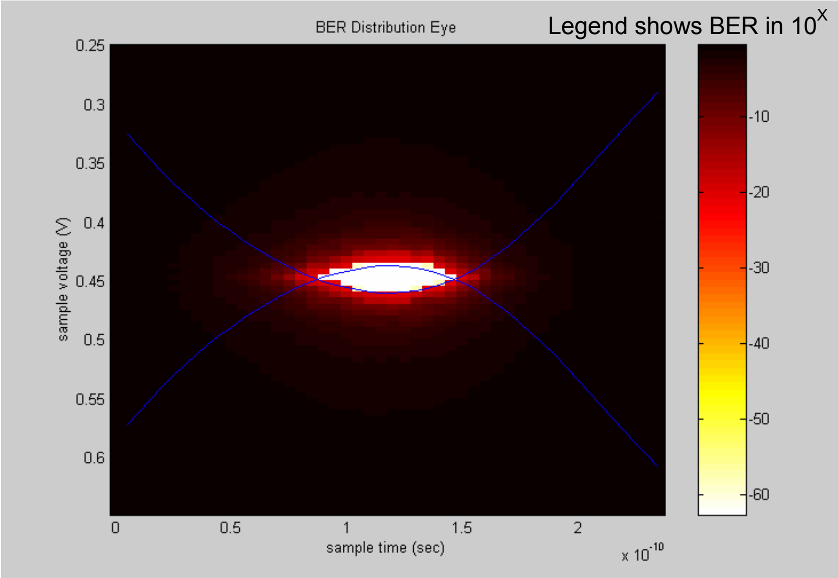
- **Empirical calculation**
- **Peak distortion analysis**
  - **Analytical calculation of worst-case eye**
- **Statistical ISI analysis**
- **Statistical analysis w/ jitter**





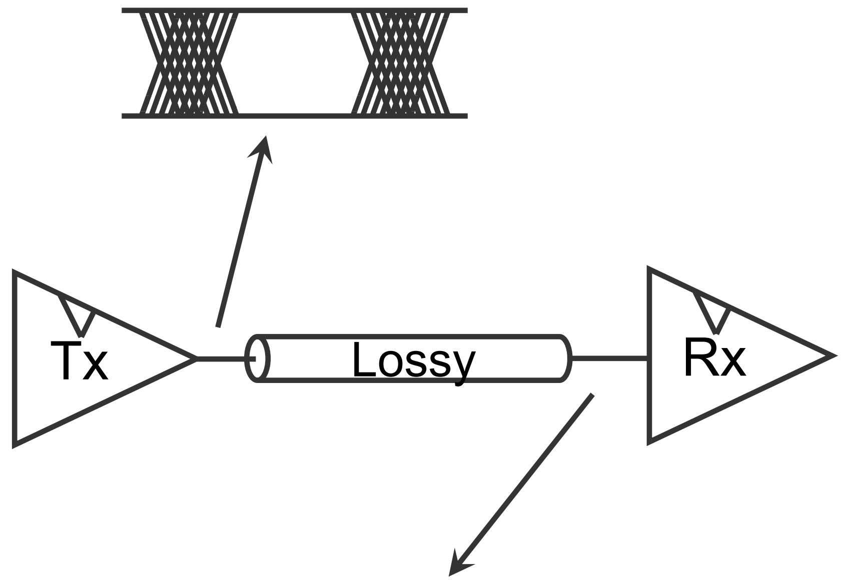
Signaling analysis techniques

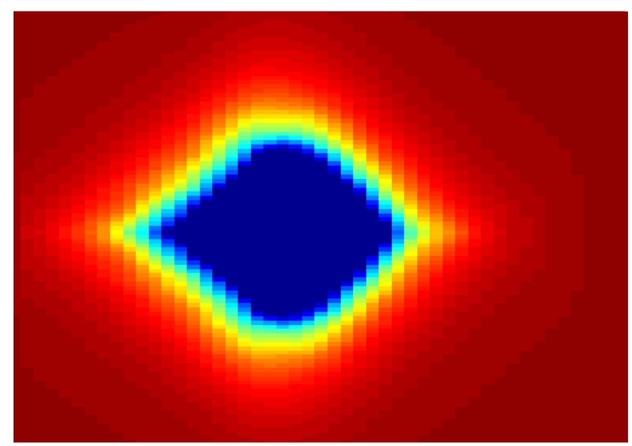
- Empirical calculation
- Peak distortion analysis
- Statistical ISI analysis
  - Perfect analytical calculation of BER eye
- Statistical analysis w/ jitter



Signaling analysis techniques

- **Empirical calculation**
- **Peak distortion analysis**
- **Statistical ISI analysis**
- **Statistical analysis w/ jitter**
  - **BER eye with Tx & Rx jitter**

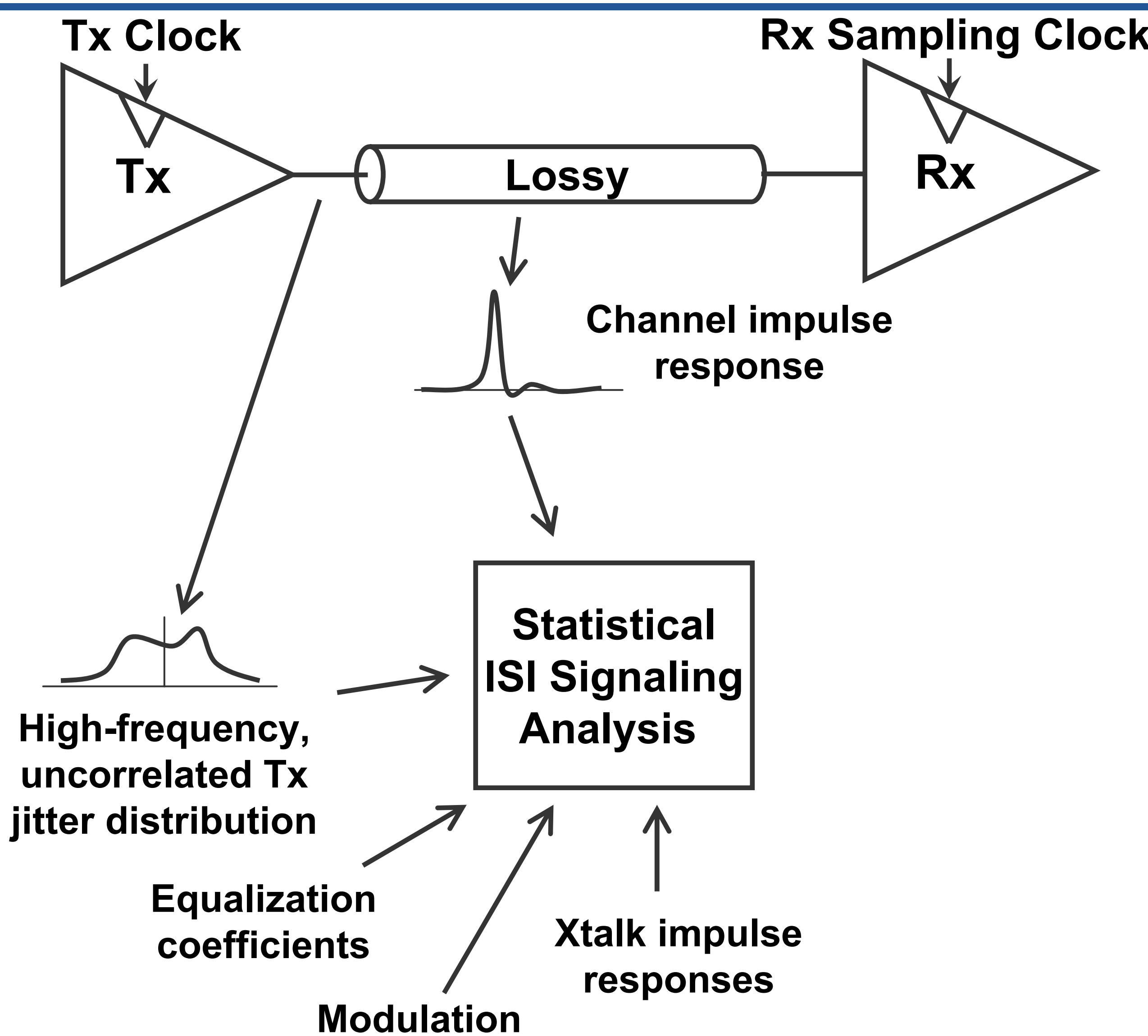




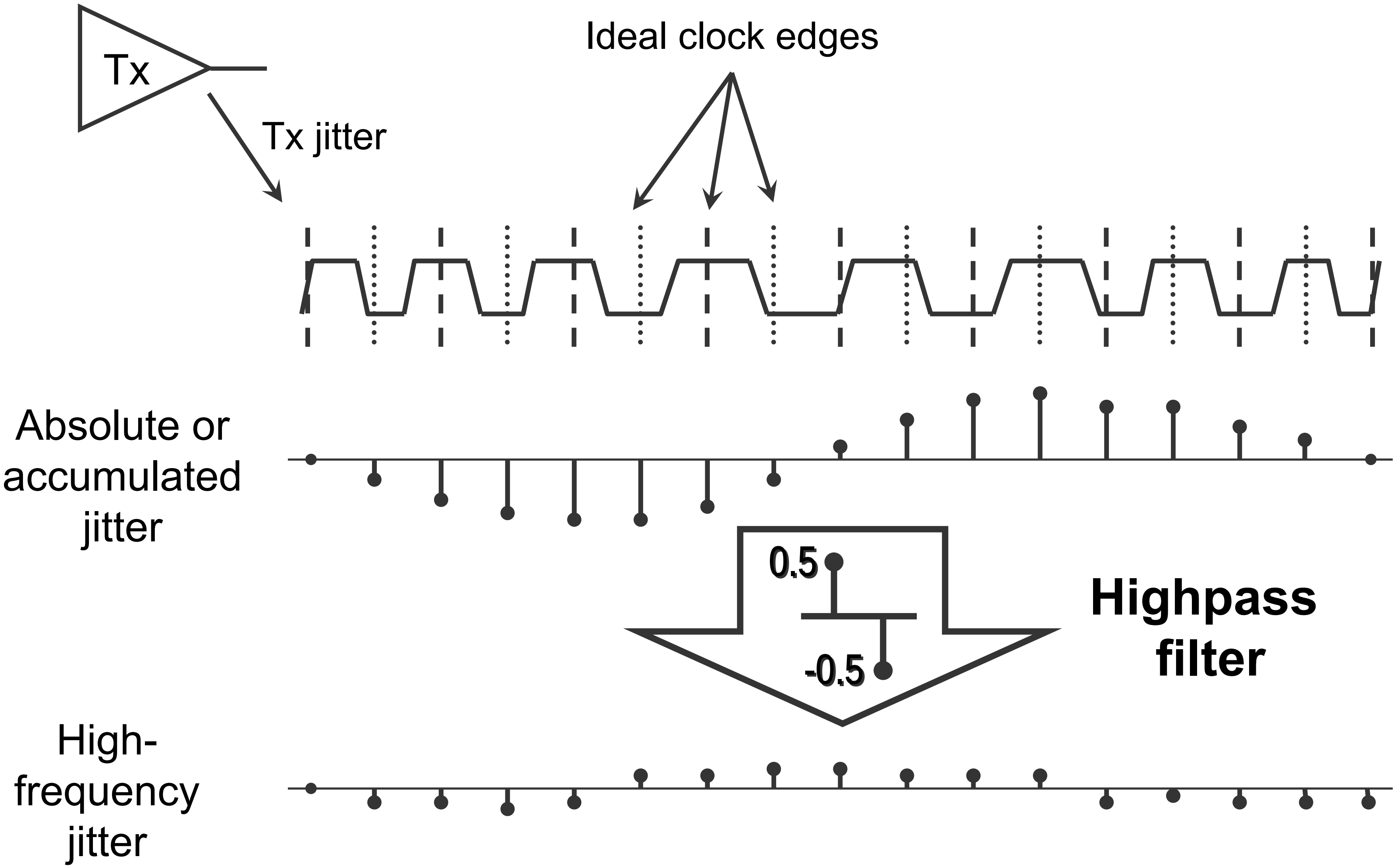
Following primary authors have published similar techniques:

- Balamurugan, Hanumolu, Sanders, Stojanovic, Casper

Intel's Signaling Analysis Method

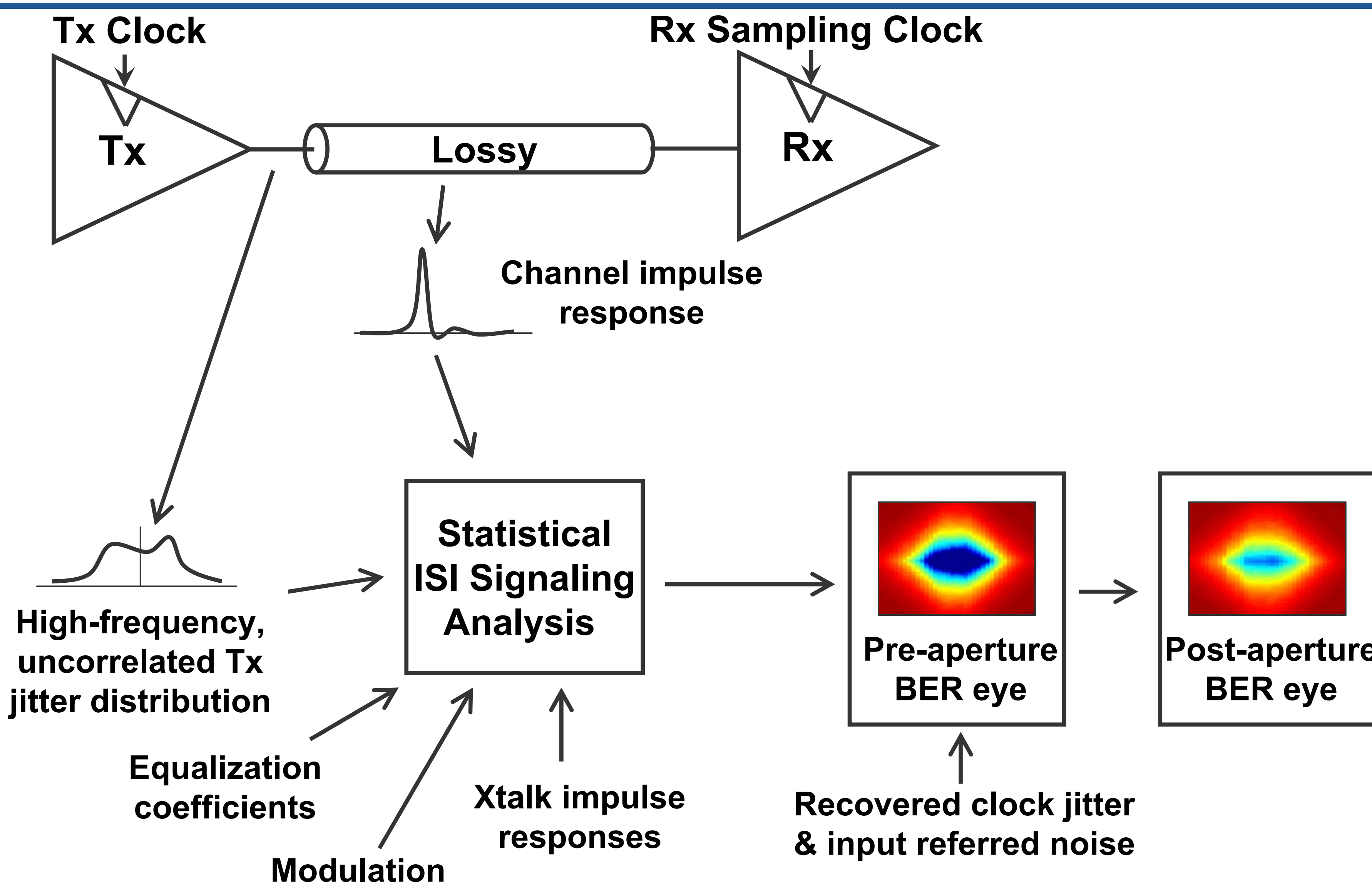


Tx Jitter Interpretation



Post-highpass absolute jitter ~ UI jitter/2

Intel's Signaling Analysis Method



References

- **Signaling Analysis Methods**

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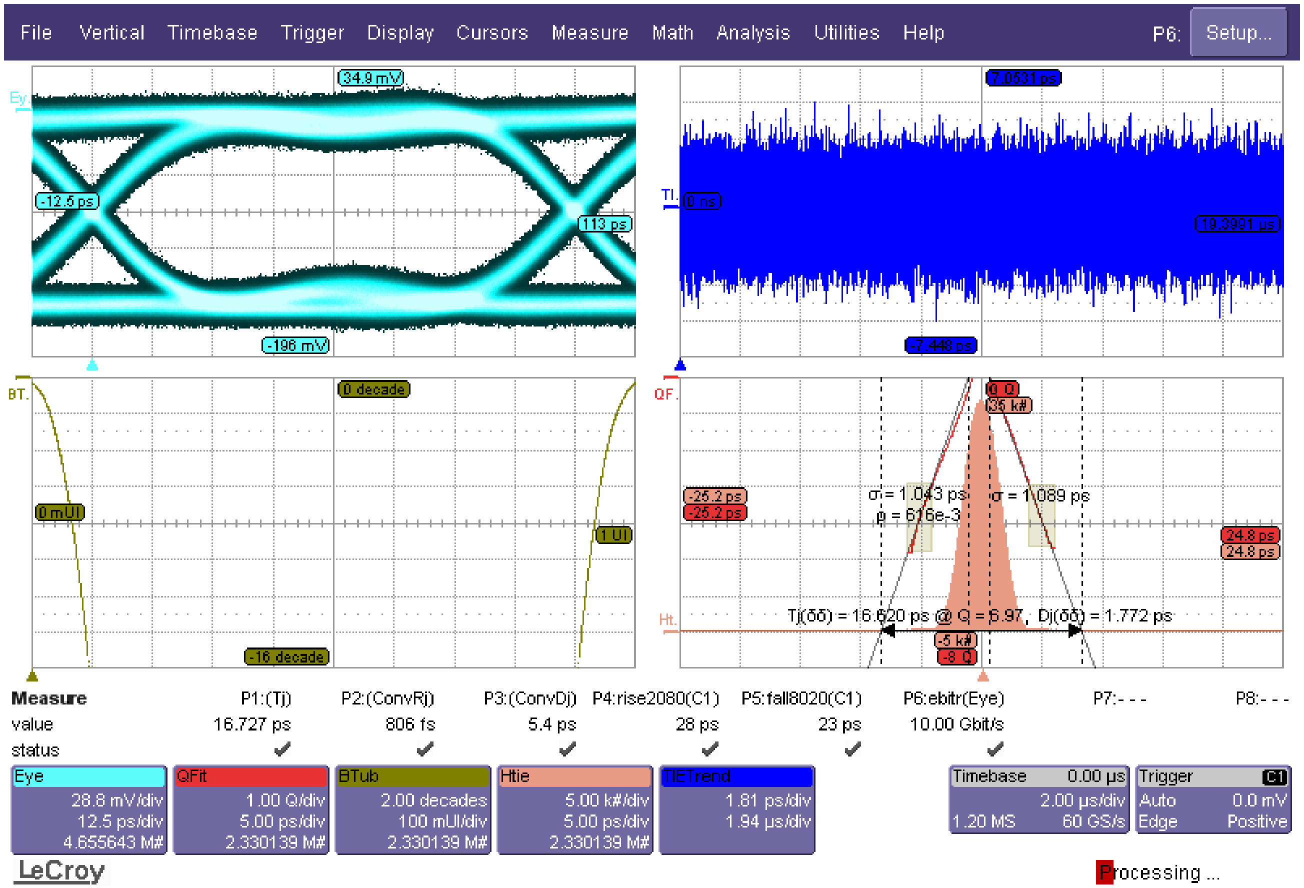
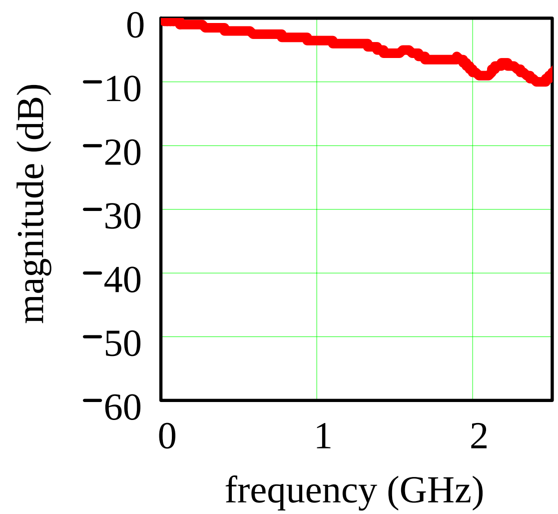
The Unequalized world

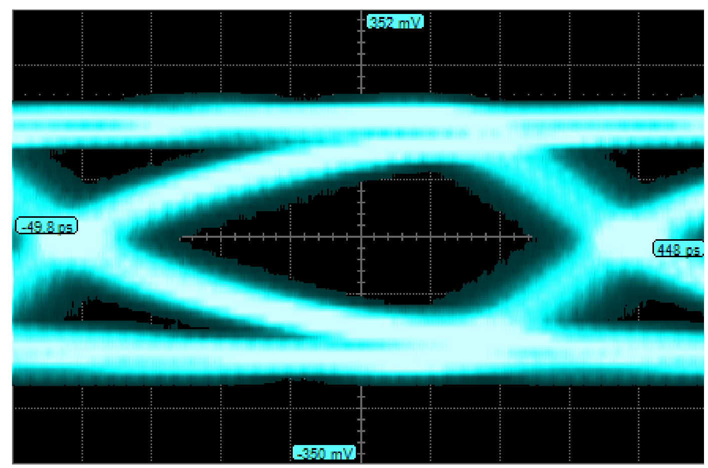


10 Gb/s Serial Data from Centallax PRBS

2.5 Gb/s (unequalized)

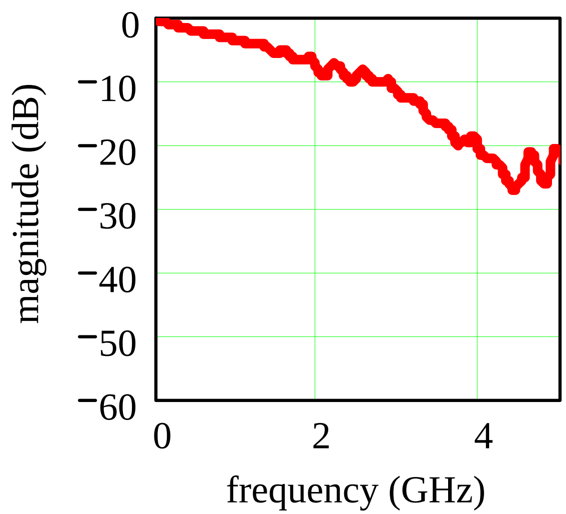
- **Dispersion Penalty**
  - **-4 dB @ 1.25 GHz**
  - **-3 dB @ 625 MHz**
  - **Delta is -1 dB (90%)**
- **Channel verified with loss specifications**
- **Transmitter verified with BER (total jitter) specifications**

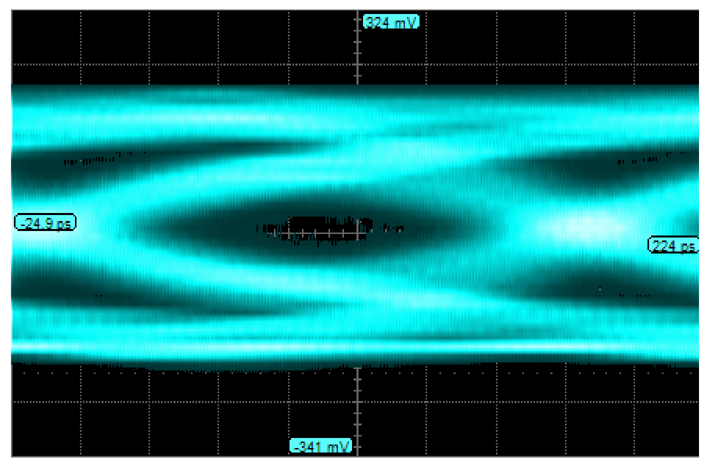




5 Gb/s (equalized or channel improved)

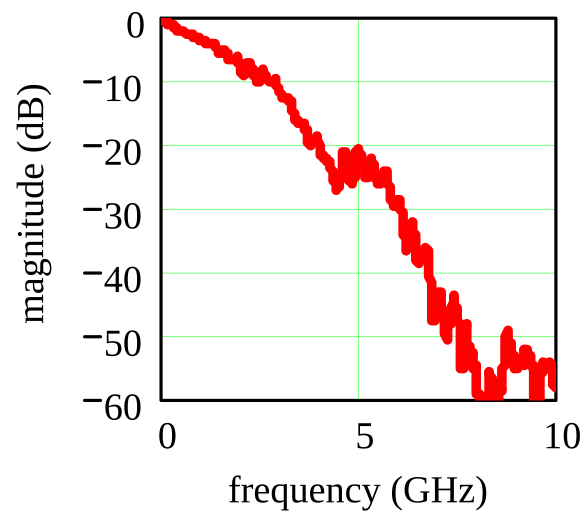
- Dispersion Penalty
  - -8 dB @ 2.5 GHz
  - -4 dB @ 1.25 GHz
  - Delta is -4 dB (63%)
- Channel verified with mask
- System requires channel improvements or equalization
- Transmitter verified how?

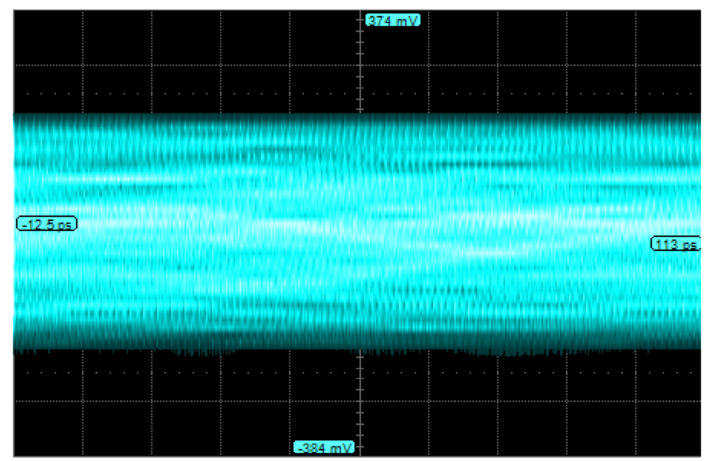




10 Gb/s (always equalized)

- Dispersion Penalty
  - -25 dB @ 5 GHz
  - -4 dB @ 2.5 GHz
  - Delta is -21 dB (<10%)
- Channel always verified as bad
- System requires equalization
- What do we do with this?



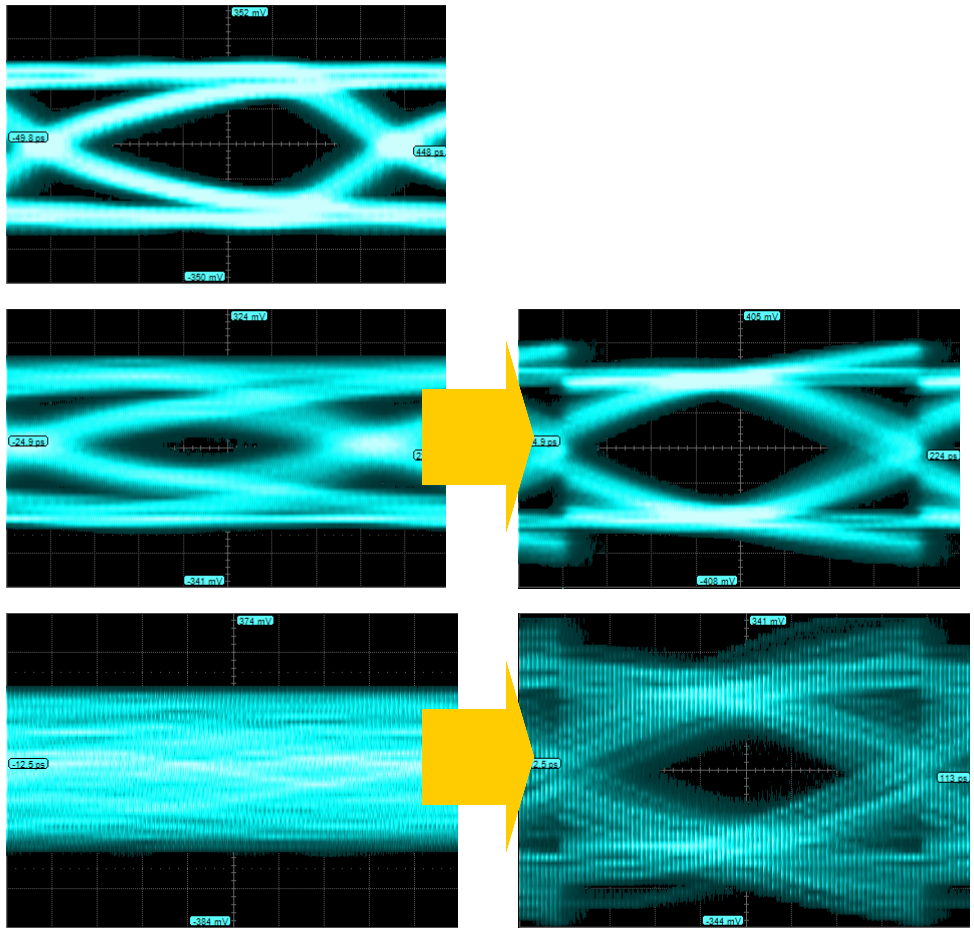


Equalization Possibilities

2.5 Gb/s

5 Gb/s

10 Gb/s



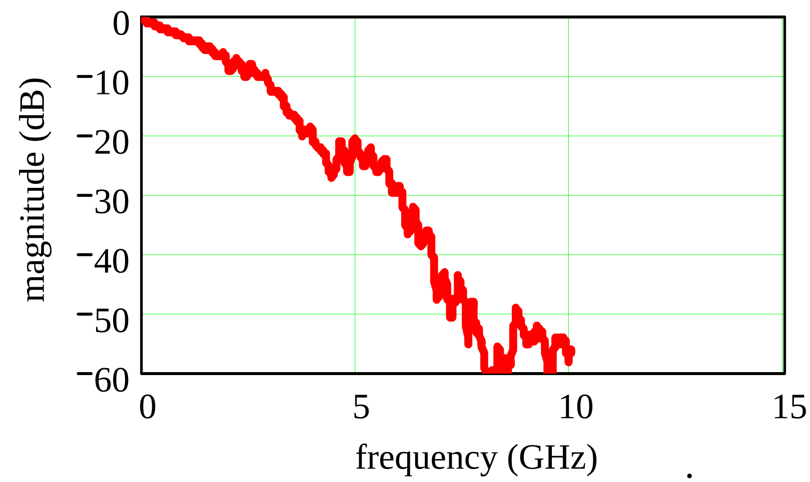
3 tap DFE

5 tap FFE

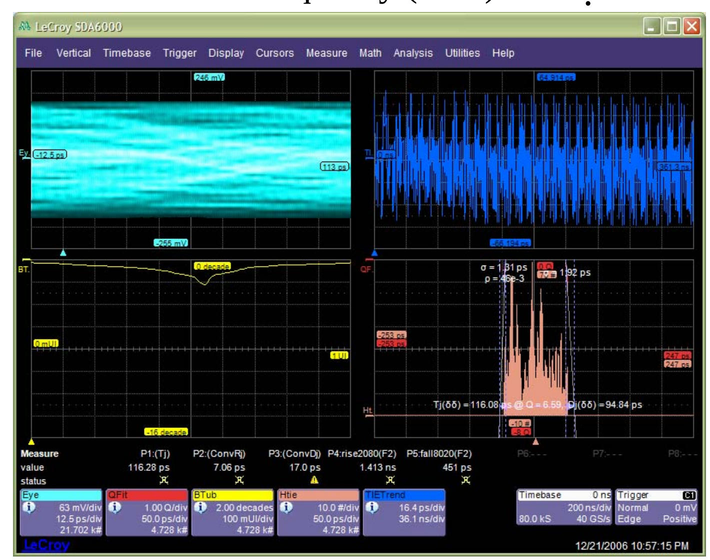
3 tap DFE

Equalization Challenges

- Cannot easily determine goodness of channel **(it's bad)**



- Cannot easily determine goodness of waveform at receiver **(can't get access to correct waveform)**



Solutions to the Equalization Problem

Solutions

- Plugfests
- Reference transmitters and receivers
- Reference Channels
- Corner-case channels
- Increased reliance on simulation
- On-chip Instrumentation

Problems with Solutions

- Plugfests are non-analytical
- Reference transceivers and corner-case channels must exist physically and match in characteristics.
- Are the corner cases really the corner cases?
- Simulation is slow and may not match reality

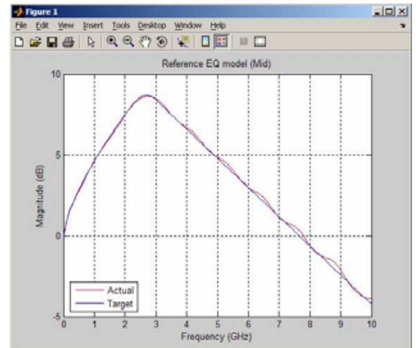
Solutions to the Solutions

- corner case channels (backplanes, connectors, cables, via models etc.) represented in software
- reference equalizers or equalized receivers represented and optimized in software
- Simulation techniques that match reality
- Simulation techniques that are fast but not oversimplified

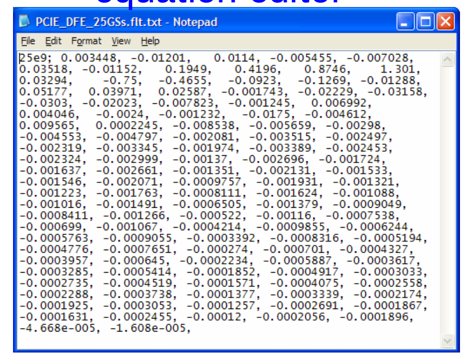
Tektronix Waveform Equalization Technique

- **Mathematical Equalization needed to de-convolve transmission line effects**
  - **Eg. PCI-E Gen2 specification**
- **FIR (Finite Impulse Response) filter applied to acquired waveform using waveform math**
- **Equalized signal then analyzed**
  - **Clock Recovery**
  - **Jitter Analysis**

MATLAB Developed Filter



FIR filter .txt file read by equation editor


PCIE_DFE_25GSs.flt.txt - Notepad

```
25e9; 0.003448, -0.01201,   0.0114, -0.005455, -0.007028,
0.03518, -0.01152,   0.1949,   0.4196,   0.8746,    1.301,
0.03294,    -0.75,  -0.4655,  -0.0923,  -0.1269, -0.01288,
0.05177,  0.03971,  0.02587, -0.001743, -0.02229, -0.03158,
-0.0303, -0.02023, -0.007823, -0.001245,  0.006992,
0.004046,  -0.0024, -0.001232,  -0.0175, -0.004612,
0.009565,  0.0002245, -0.008538, -0.005659, -0.00298,
-0.004553, -0.004797, -0.002081, -0.003515, -0.002497,
-0.002319, -0.003345, -0.001974, -0.003389, -0.002453,
-0.002324, -0.002999, -0.00137, -0.002696, -0.001724,
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-0.0002735, -0.0004519, -0.0001571, -0.0004075, -0.0002558,
-0.0002288, -0.0003738, -0.0001377, -0.0003339, -0.0002174,
-0.0001925, -0.0003053, -0.0001257, -0.0002691, -0.0001867,
-0.0001631, -0.0002455, -0.00012, -0.0002056, -0.0001896,
-4.668e-005, -1.608e-005,
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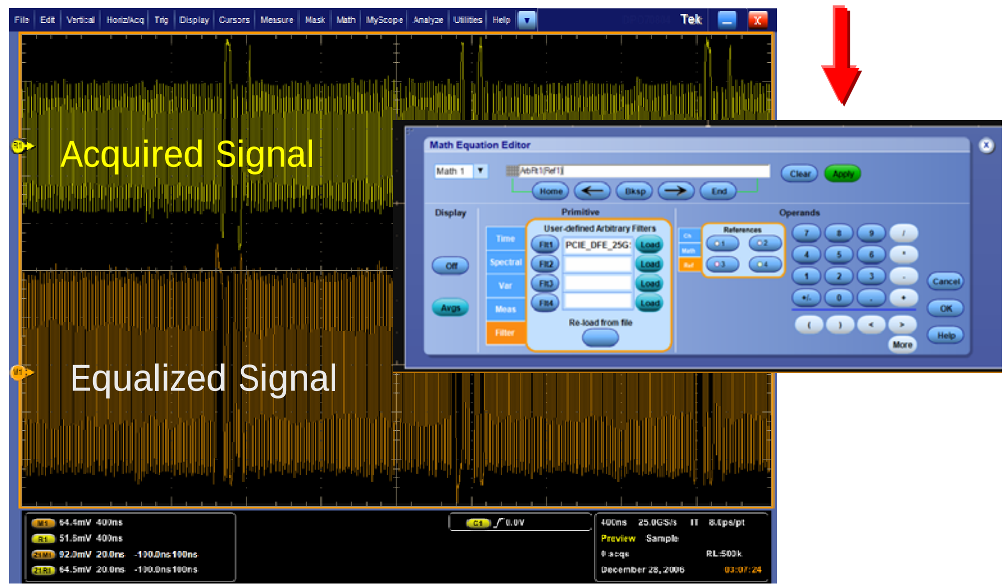
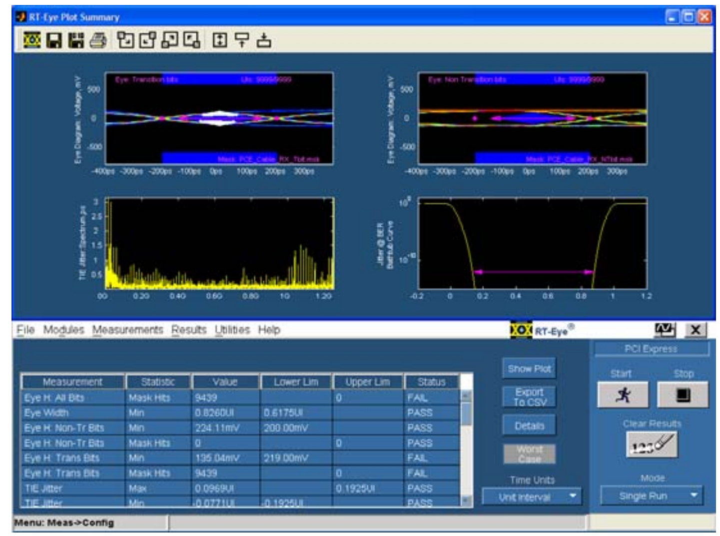


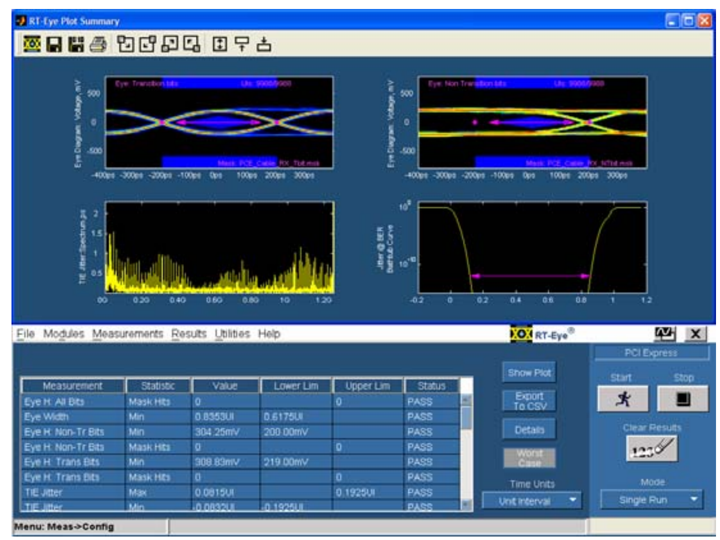
Courtesy of Mike Engbretson, Tektronix

Example

- **Without Equalization**
  - **Un-Equalized signal fails PCI-E cable specification**



- **With Equalization**
  - **Equalized signal passes the spec.**



Courtesy of Mike Engbretson, Tektronix

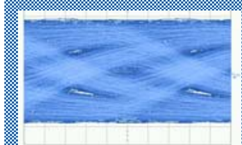
Agilent:
Test issues in the world of equalizing receivers

Two general test questions/problems:

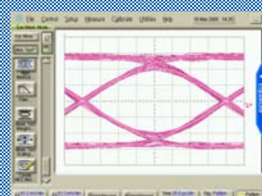
Can a severely impaired signal be equalized?

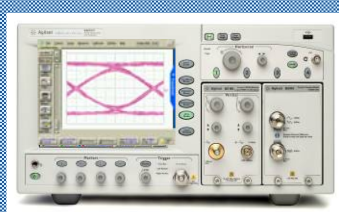
How good is an equalizer design versus a given level of impairment?

One approach is to build a virtual equalizer into the oscilloscope



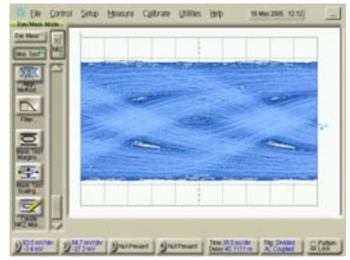
On-board user-defined virtual equalizer



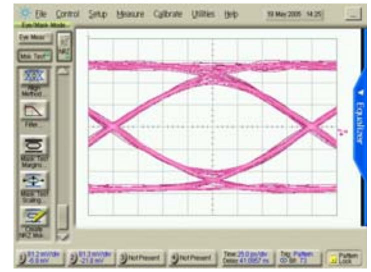


Courtesy of Greg LeCheminant, Agilent

Transmitted signals with closed eyes, how much equalization is required to pry them open?



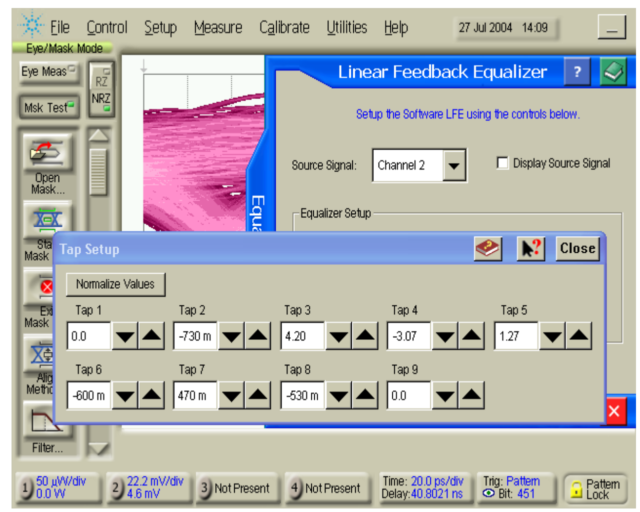
Equalizer



Signal into scope

Observe "equalized" signal in "real-time"

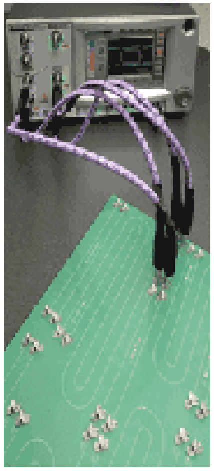
Verify equalizer design on closed eye waveforms prior to receiver construction



BERTScope

Uses Channels and Real-time Pre-emphasis for generating Receiver Test Signals:

- PCIe calibration channel
- SAS test load (TCTF)
- Serial ATA 1x and 2x compliance channel
- 802.3ae (XAUI) Compliance Interconnect
- Real-time pre-emphasis for electrical PCIe; SATA; CEI-OIF and 802.3ap as well as optical channel emulation 802.3aq (LRM)

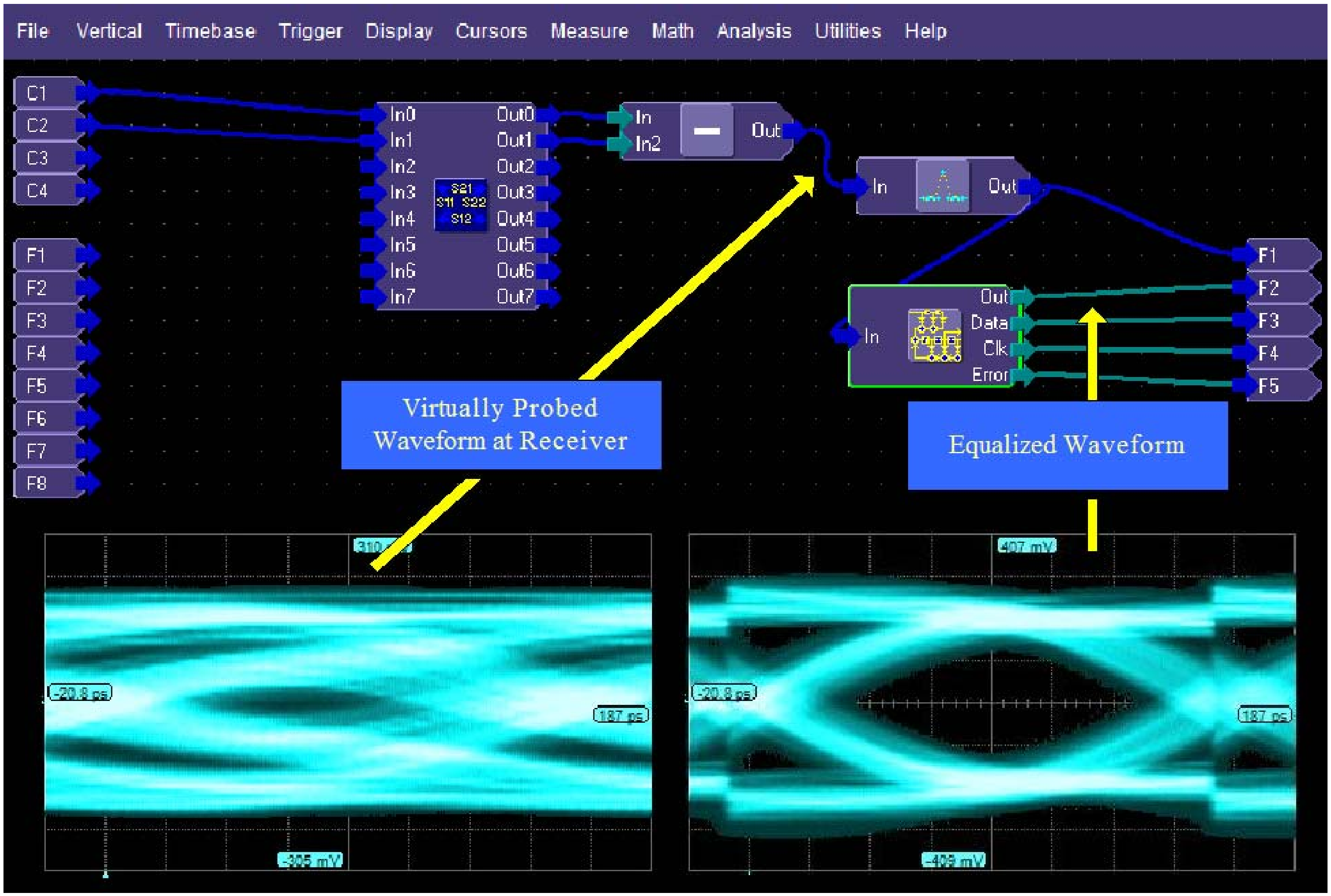


Analyzes Transmitters & Channels using:

- Multi-tap SW equalization to open the eye as a golden receiver would.
- 802.3aq (LRM) channel emulation (TDP Testing)
- PCIe Gen2 spectrum and jitter measurement methods on data with pre-emphasis
- Jitter and SSC waveform analysis for spread spectrum clocked data

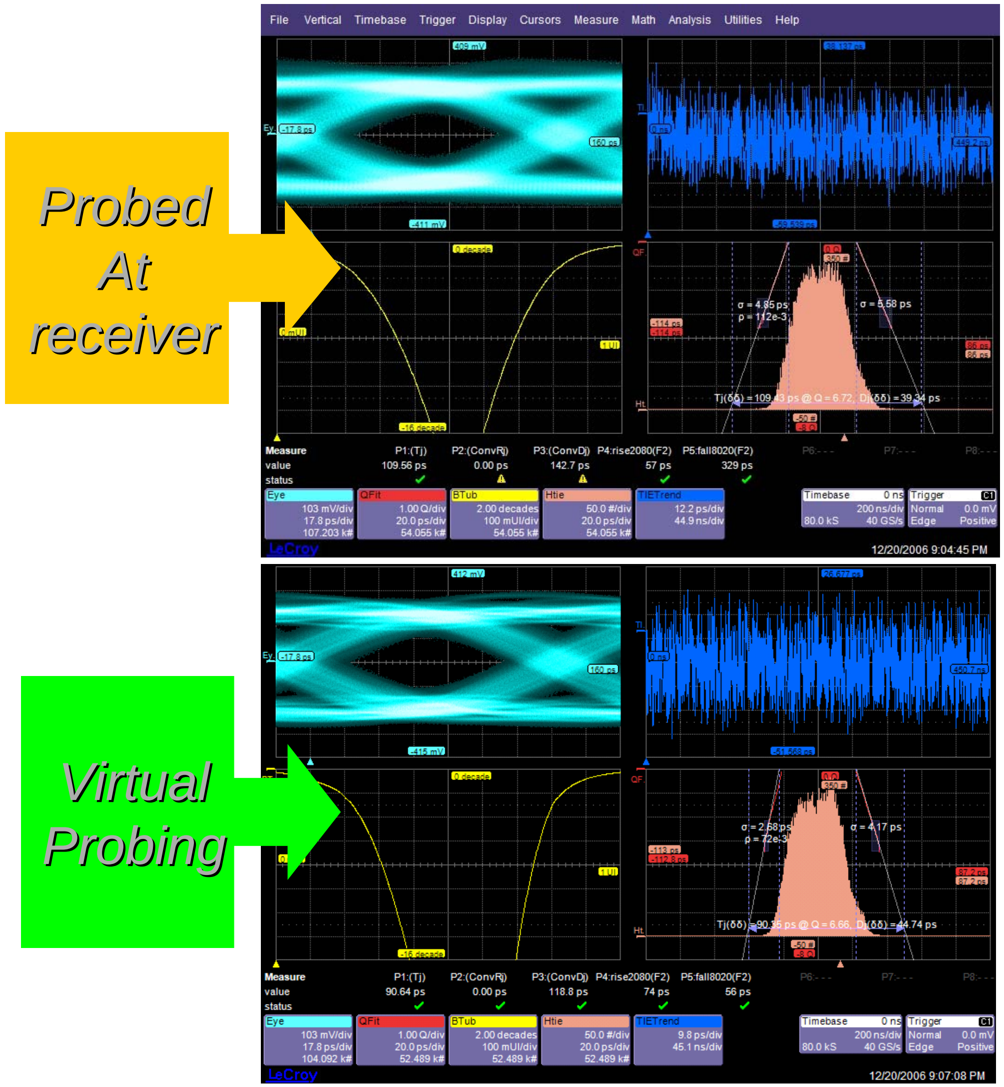
Courtesy of Bent Hessen-Schmidt, Synthesis

LeCroy: Virtual Probing & Equalizer Emulation



Virtual Probing Noise Reduction

- Real-time scope noise floor is 42-47 dB/GHz – virtually white.
- Equalizer emulation on waveforms probed at receiver leads to reshaping of the noise floor (noise/jitter amplification).
- Noise is reduced by probing at the transmitter and having the virtual probe component generate receiver signals



Summary

- **The equalization challenge in test and measurement instrumentation is addressed through*:**
  - **Reference channels**
  - **Equalized receivers (in software)**
  - **Co-simulation techniques**

***In scope based measurement systems**