IIR IP

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Contents

1 Introduction

When selecting this project, I was under the assumption that it would be fairly easy to complete. Seeing as completing this task in software isn't a huge deal, I assumed the same for hardware. To my surprise, this was far from true. The calculation for IIR is quite difficult to complete in hardware, as I will discuss in this report. I will be discussing the theory behind the IIR in hardware, the major issues that can occur, and how one could complete this task in the future.

1.1 Important Files

Inside of this project, there are a few different files that are important. Firstly, my notebook. This file is entitled `notebook.org` and contains information on my process throughout the semester. You can open it with a text editor of choice, or you can view the exported `notebook.html` file. Please note that the HTML version doesn't contain all of the clock stamps. Inside of `presentation/` is the presentation and its source. The source for this report can be found in `report/`. Inside of `projects/` will be all of the different projects that I worked on. The important ones to note are: `2nd-order-single-section/`, `complex-iir/`, and `the-really-big-one/`.

Just so that it's easier to find your way, I will do a quick description of each project. This will prevent you from having to search around. `2nd-order-single-section/` is a design that only uses a single section BiQuad. This was used to prove that there was something wrong with the BiQuad implementation of the IP. `complex-iir/` contains a design that doesn't use the Zynq. It does everything in hardware. The current setup uses internally selected coefficients, opposed to the normally externally fed coefficients. Lastly, `the-really-big-one/` is a design that uses pretty much everything. It is set up with 4 BiQuads cascaded serially and uses the dmux and mux IPs to make the design generic.

2 Single-Section

2.1 BiQuad