

FPGA - Field programmable Gate Array

fixed - piece of hardware.

FPGA

→ More power consumption.

→ Costly

→ Resources

utility is  
configurable  
not efficiently  
(Look up tables)  
use more  
memory

→ interconnection  
problem  
(reduces speed)

fixed (not  
programmable)  
by me

B

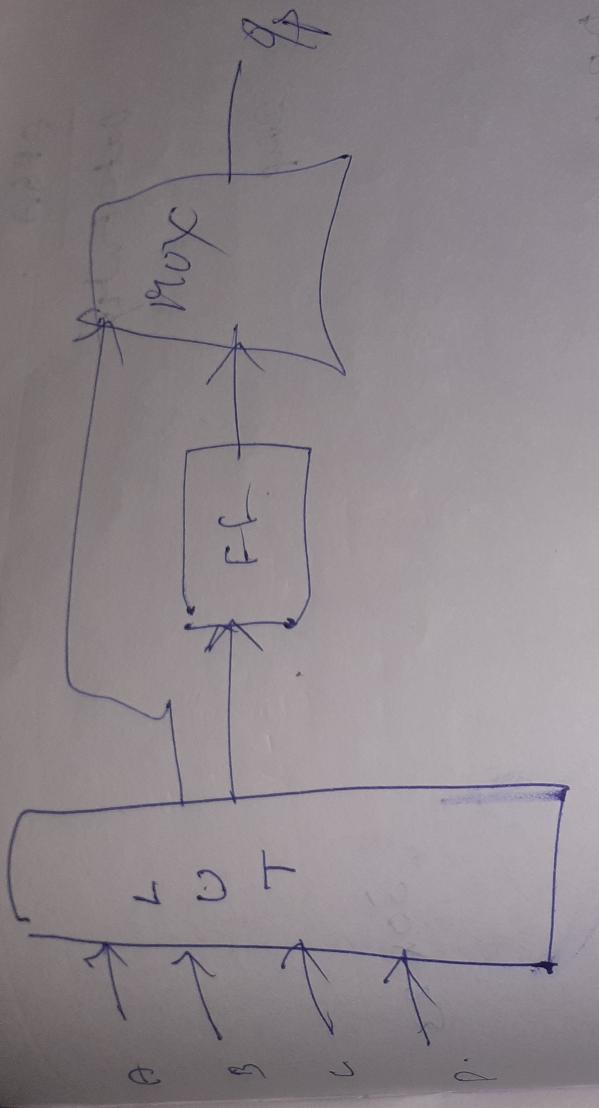
C

D

ASIC

→ Less power consumption

Slice - big piece of hardware - 8 parts  
MUX - universal logic device



CLB  $\rightarrow$  4 slices



$$Gb = 2^3 \times 3^9 \approx 2^{12}$$

Data bus = 8 bits

Address bus =  $2^8$

23 bytes.

Vignetta

$$22 + 9 + 7 + 14 + 1 + 20 + 8 + 1$$

$$\frac{53}{+3}$$

$$\begin{array}{r} 38 \\ - 14 \\ \hline 24 \end{array}$$

31

Size

23

Size

64KB + 25600 bytes



FPGA → Interconnection network  
→ Lookupt  
CLB — <sup>lookup</sup>  
tables - MUX, flipflops  
→ Input/Output ports

## Hardware accelerator

