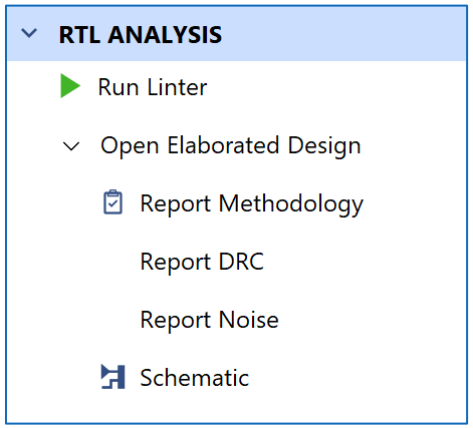
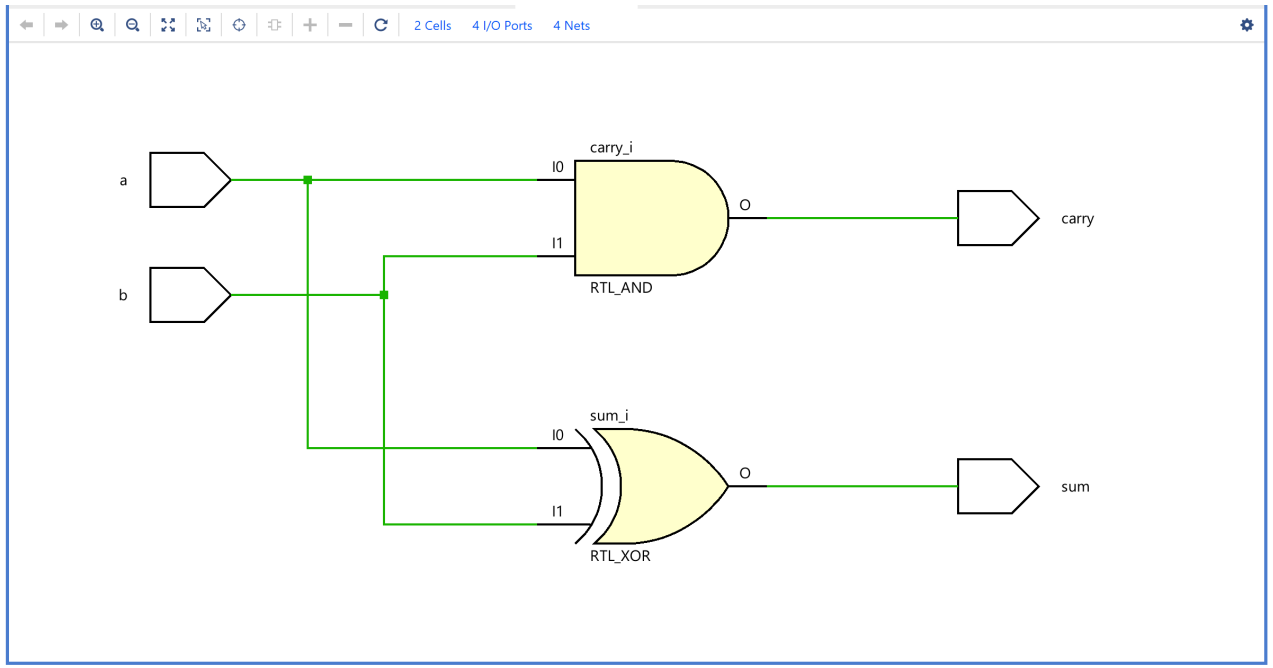
Half Adder

Schematic



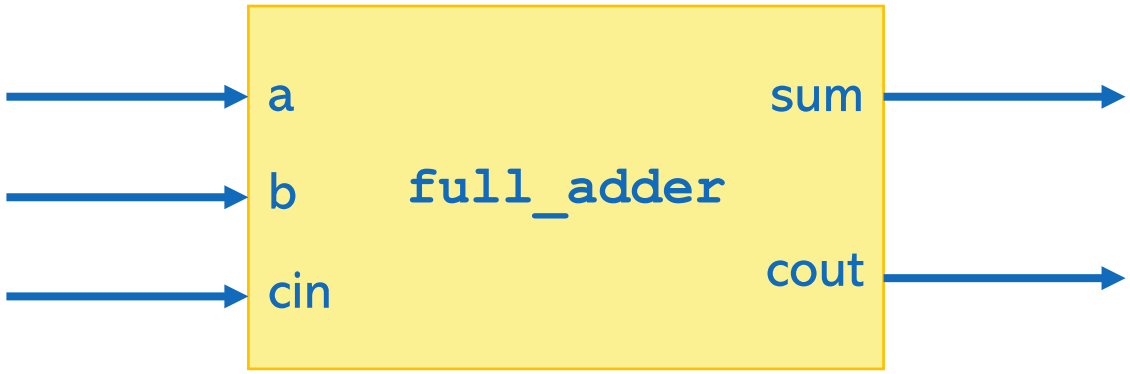


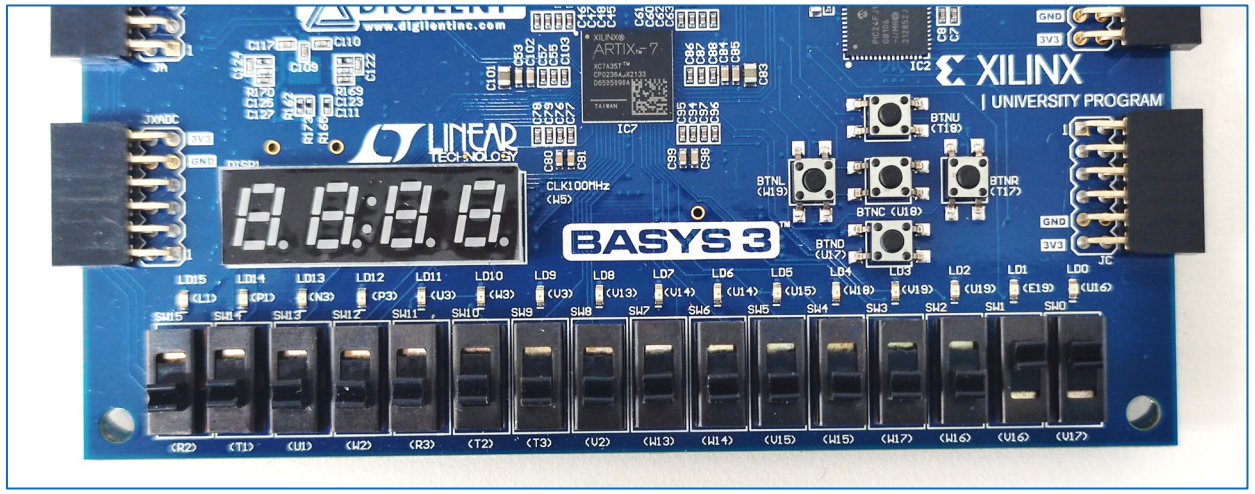
Tcl Console | Messages | Log | Reports | Design Runs | Find Results

Name	Direction	Board Part Pin	Board Part Interface	Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco
a	IN					V17	✓	14	LVCMOS33*	3.300
b	IN					V16	✓	14	LVCMOS33*	3.300
carry	OUT					E19	✓	14	LVCMOS33*	3.300
sum	OUT					U16	✓	14	LVCMOS33*	3.300

```
set_property PACKAGE_PIN V17 [get_ports a]
set_property PACKAGE_PIN V16 [get_ports b]
set_property PACKAGE_PIN E19 [get_ports carry]
set_property PACKAGE_PIN U16 [get_ports sum]
set_property IOSTANDARD LVCMOS33 [get_ports a]
set_property IOSTANDARD LVCMOS33 [get_ports b]
set_property IOSTANDARD LVCMOS33 [get_ports carry]
set_property IOSTANDARD LVCMOS33 [get_ports sum]
```

Full Adder | Block Diagram & Constraints



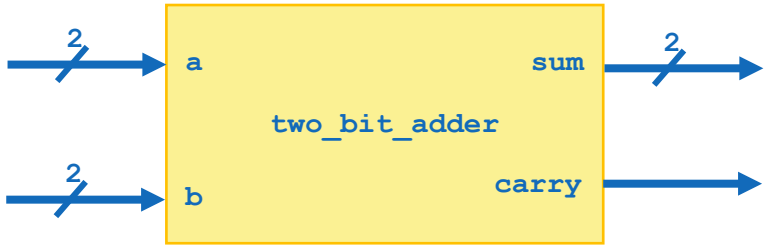


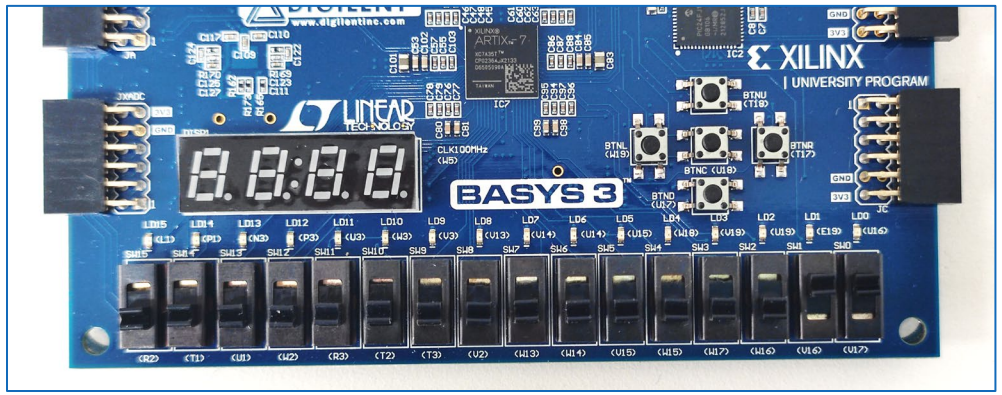
Port	I/O Type	Label	Pin
a	switch	SW0	V17
b	switch	SW1	V16
cin	switch	SW2	W16
sum	LED	LD0	U16
cout	LED	LD1	E19

Two bit adder

Checkpoint 2

2. Perform hardware test on FPGA using the following constraints.



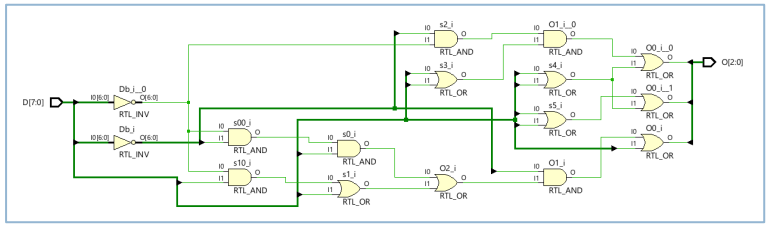


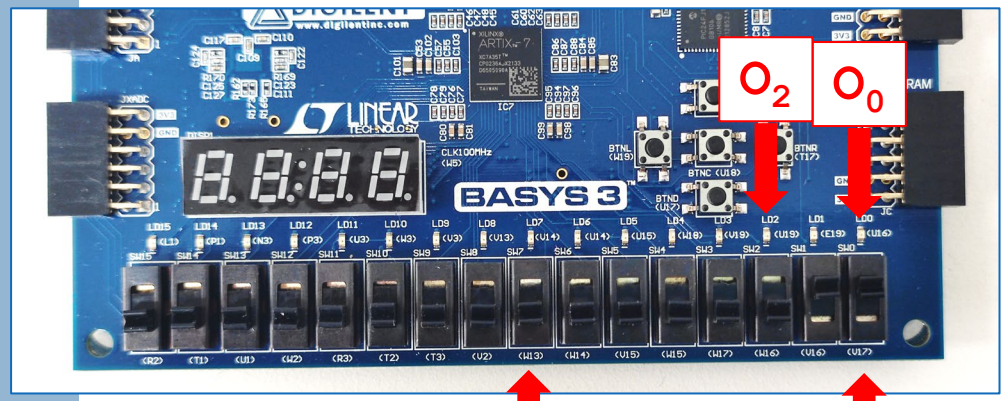
Port	I/O Type	Label	Pin
a(1)	switch	SW3	W17
a(0)	switch	SW2	W16
b(1)	switch	SW1	V16
b(0)	switch	SW0	V17
sum(1)	LED	LD1	E19
sum(0)	LED	LD0	U16
carry	LED	LD2	U19

Encoder 8 to 3

Checkpoint 1

- Construct 8-to-3 priority encoder according to previous slides.
- Do the testbench with at least 11 input cases.
  - 8 input cases for each input switch.
  - 3 input cases with at least 2 activated input switches.
  - increase the duration of wait for statement to 50 ns.
- Test on Basys 3 using the following constraints.



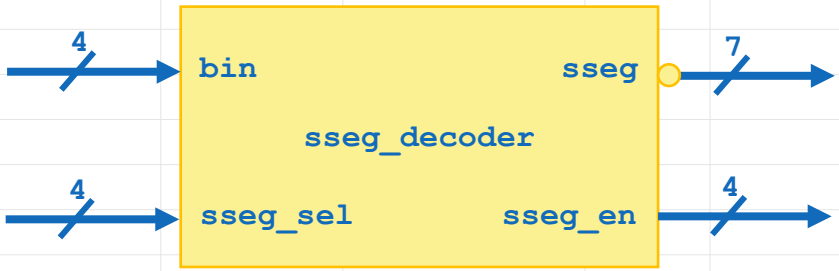


Name	Direction	Board Part Pin	Board Part Interface	Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std
D[7]	IN					W13	✓	14	LVCMOS33*
D[6]	IN					W14	✓	14	LVCMOS33*
D[5]	IN					V15	✓	14	LVCMOS33*
D[4]	IN					W15	✓	14	LVCMOS33*
D[3]	IN					W17	✓	14	LVCMOS33*
D[2]	IN					W16	✓	14	LVCMOS33*
D[1]	IN					V16	✓	14	LVCMOS33*
D[0]	IN					V17	✓	14	LVCMOS33*
O[2]	OUT					U19	✓	14	LVCMOS33*
O[1]	OUT					E19	✓	14	LVCMOS33*
O[0]	OUT					U16	✓	14	LVCMOS33*

LAB : 8 combination circuit 7 Segment Decoder

Constraints

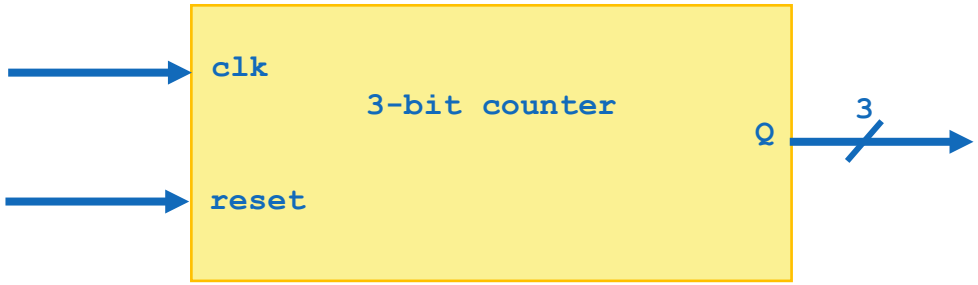
Name	Direction	Board Part Pin	Board Part Interface	Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco
bin[3]	IN					W17	✓	14	LVCMOS33*	3.300
bin[2]	IN					W16	✓	14	LVCMOS33*	3.300
bin[1]	IN					V16	✓	14	LVCMOS33*	3.300
bin[0]	IN					V17	✓	14	LVCMOS33*	3.300
sseg[6]	OUT					W7	✓	34	LVCMOS33*	3.300
sseg[5]	OUT					W6	✓	34	LVCMOS33*	3.300
sseg[4]	OUT					U8	✓	34	LVCMOS33*	3.300
sseg[3]	OUT					V8	✓	34	LVCMOS33*	3.300
sseg[2]	OUT					U5	✓	34	LVCMOS33*	3.300
sseg[1]	OUT					V5	✓	34	LVCMOS33*	3.300
sseg[0]	OUT					U7	✓	34	LVCMOS33*	3.300
sseg_en[3]	OUT					W4	✓	34	LVCMOS33*	3.300
sseg_en[2]	OUT					V4	✓	34	LVCMOS33*	3.300
sseg_en[1]	OUT					U4	✓	34	LVCMOS33*	3.300
sseg_en[0]	OUT					U2	✓	34	LVCMOS33*	3.300
sseg_sel[3]	IN					R2	✓	34	LVCMOS33*	3.300
sseg_sel[2]	IN					T1	✓	34	LVCMOS33*	3.300
sseg_sel[1]	IN					U1	✓	34	LVCMOS33*	3.300
sseg_sel[0]	IN					W2	✓	34	LVCMOS33*	3.300



3 Bit Counter

Checkpoint 1

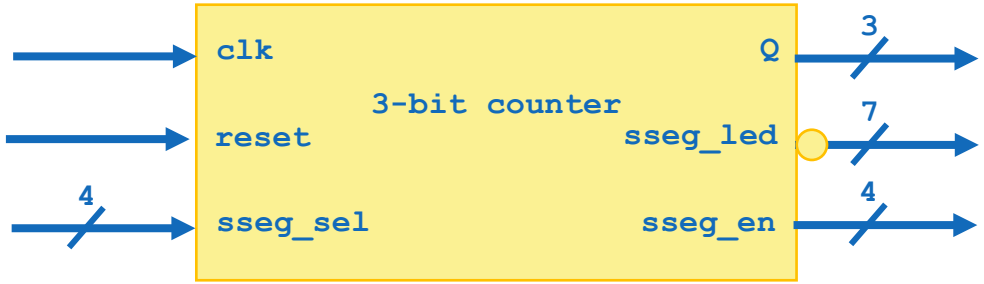
- Construct 3-bit synchronous counter using JK-FF.
  - Dataflow & structural coding style only.
- Use pin T17 as reset button.
- Use pin W5 as 100 MHz input clock.
- Adjust clock frequency to **1 Hz** using **clock divider**.
- Display counter output by 3 LEDs (**LD12** as MSB, **LD11** and **LD10**).
- Simulate & test individual entity first.
  - Create 3 projects: JK-FF, clock divider, and 3-bit counter.
  - When submitting, show TA the simulation results from 3 projects and test the 3-bit counter project on Basys 3 board.



LAB 9 : counter 3 Bit counter (+ 7 segment)

Checkpoint 2

- Display the counter output from **Checkpoint 1** using 7SEG.
  - Dataflow & structural coding style only.
- Reuse **sseg_decoder** from Lab 8.
  - The interface (input & output ports) may need to be adjusted.
- Test on Basys 3 board.



LAB 9 : counter 3 Bit counter (+ 7 segment) (port)

```
set_property IOSTANDARD LVCMOS33 [get_ports clk]
set_property IOSTANDARD LVCMOS33 [get_ports reset]
set_property IOSTANDARD LVCMOS33 [get_ports {Q[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {Q[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {Q[0]}]
set_property PACKAGE_PIN T17 [get_ports reset]
set_property PACKAGE_PIN W5 [get_ports clk]
set_property PACKAGE_PIN P3 [get_ports {Q[2]}]
set_property PACKAGE_PIN U3 [get_ports {Q[1]}]
set_property PACKAGE_PIN W3 [get_ports {Q[0]}]

set_property IOSTANDARD LVCMOS33 [get_ports {led[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {led[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {led[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {led[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg_en[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg_en[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg_en[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg_en[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg_sel[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg_sel[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg_sel[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sseg_sel[0]}]
set_property PACKAGE_PIN V19 [get_ports {led[3]}]
set_property PACKAGE_PIN U19 [get_ports {led[2]}]
set_property PACKAGE_PIN E19 [get_ports {led[1]}]
set_property PACKAGE_PIN U16 [get_ports {led[0]}]
set_property PACKAGE_PIN W7 [get_ports {sseg[6]}]
set_property PACKAGE_PIN W6 [get_ports {sseg[5]}]
set_property PACKAGE_PIN U8 [get_ports {sseg[4]}]
set_property PACKAGE_PIN V8 [get_ports {sseg[3]}]
set_property PACKAGE_PIN U5 [get_ports {sseg[2]}]
set_property PACKAGE_PIN V5 [get_ports {sseg[1]}]
set_property PACKAGE_PIN U7 [get_ports {sseg[0]}]
set_property PACKAGE_PIN W4 [get_ports {sseg_en[3]}]
set_property PACKAGE_PIN V4 [get_ports {sseg_en[2]}]
set_property PACKAGE_PIN U4 [get_ports {sseg_en[1]}]
set_property PACKAGE_PIN U2 [get_ports {sseg_en[0]}]
set_property PACKAGE_PIN R2 [get_ports {sseg_sel[3]}]
set_property PACKAGE_PIN T1 [get_ports {sseg_sel[2]}]
set_property PACKAGE_PIN U1 [get_ports {sseg_sel[1]}]
set_property PACKAGE_PIN W2 [get_ports {sseg_sel[0]}]
```

Basys 3 port

Basys 3 Reference Manual

- Basys 3 Reference Manual - Digilent Reference

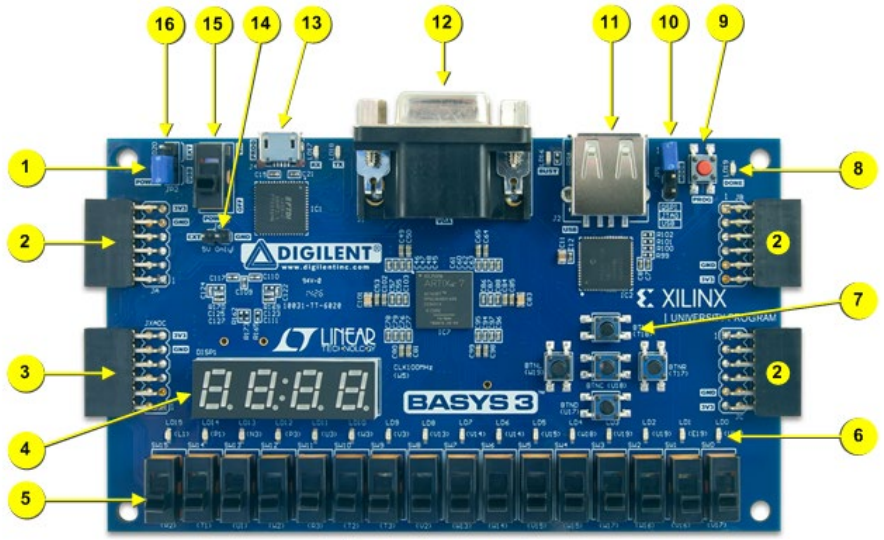


Figure 1. Basys3 board features