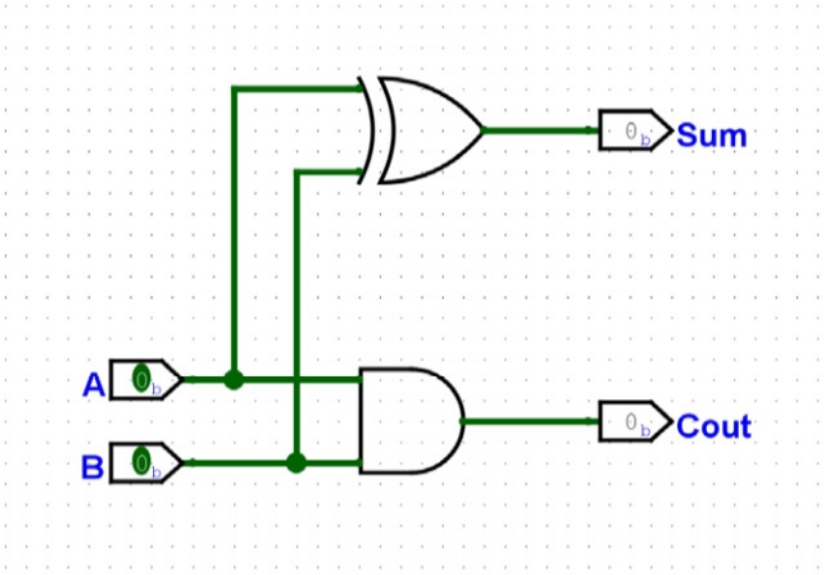



Fig 3.1 Logic diagram for half adder.

```
# Test Vector for Half Adder

A B   Cout Sum

0 0    0    0
0 1    0    1
1 0    0    1
1 1    1    0
```

Fig 3.2 Test vector for half adder.

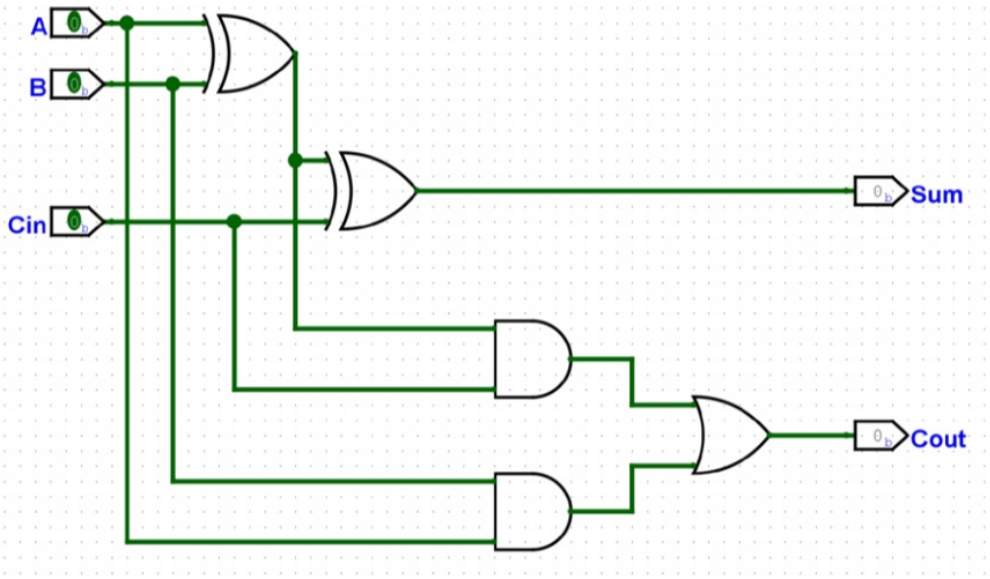



Fig 3.3 Logic diagram for full adder.

# Test Vector

| Cin | A | B | Cout | Sum |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Fig 3.4 Test vector for full adder.

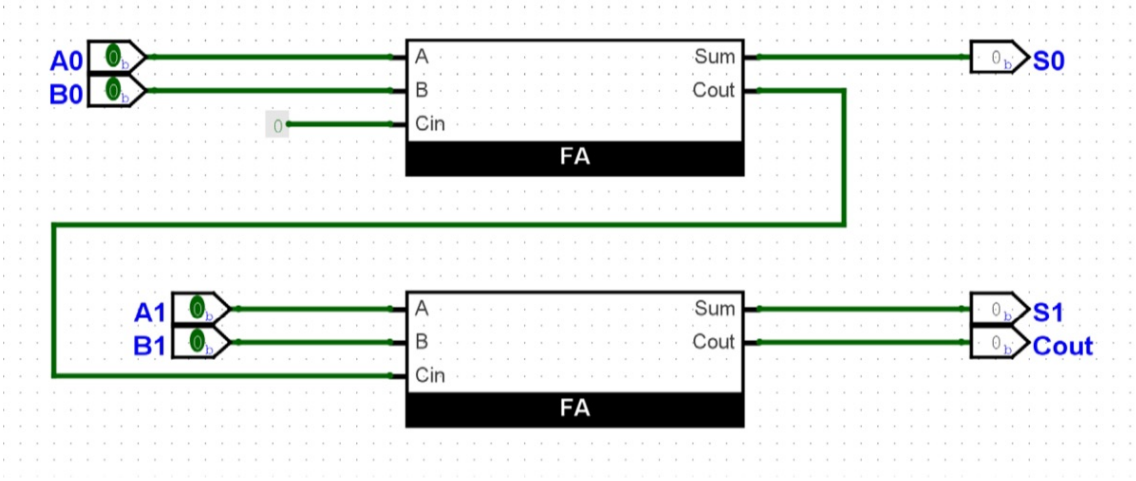
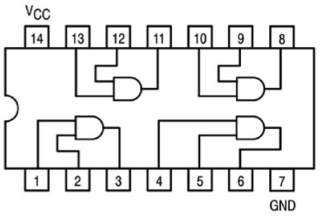


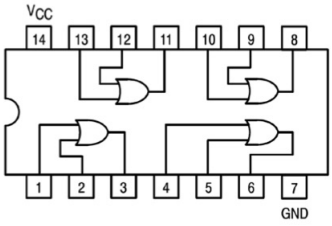

Fig 3.5 Two-bit adder.

```
# Test vector for two-bit adder

A1  A0  B1  B0   Cout  S1  S0

0   0   0   0     0    0   0
0   0   0   1     0    0   1
0   0   1   0     0    1   0
0   0   1   1     0    1   1
0   1   0   0     0    0   1
0   1   0   1     0    1   0
0   1   1   0     0    1   1
0   1   1   1     1    0   0
1   0   0   0     0    1   0
1   0   0   1     0    1   1
1   0   1   0     1    0   0
1   0   1   1     1    0   1
1   1   0   0     0    1   1
1   1   0   1     1    0   0
1   1   1   0     1    0   1
1   1   1   1     1    1   0
```

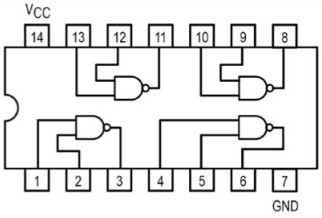
Fig 3.6 Test vector for two-bit adder.



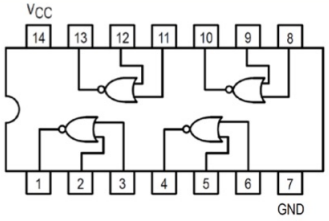

74LS08 | 2-Input AND Gate IC



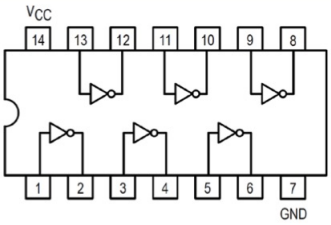

74LS32 | 2-Input OR Gate IC



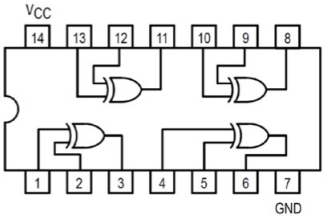

74LS00 | 2-Input NAND Gate IC




** 74LS02 | 2-Input NOR Gate IC **

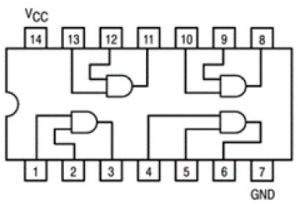



74LS04 | NOT Gate IC




74LS86 | 2-Input XOR Gate IC

74LS08

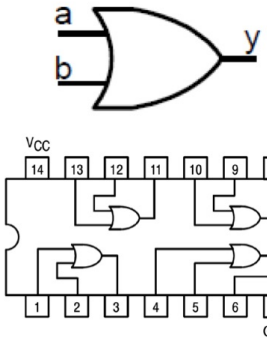




AND GATE

| Input | | Output | | | |
|---|---|---|---|---|---|
| a | b | y (pin 3) | y (pin 6) | y (pin 8) | y (pin 11) |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

## OR GATE

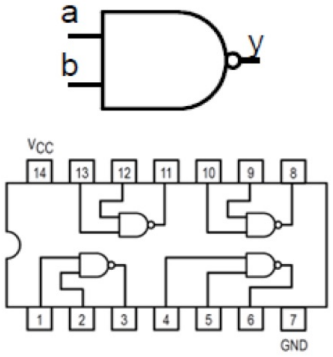
**74LS32**




| Input | | Output | | | |
|---|---|---|---|---|---|
| a | b | y (pin 3) | y (pin 6) | y (pin 8) | y (pin 11) |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

## NAND GATE

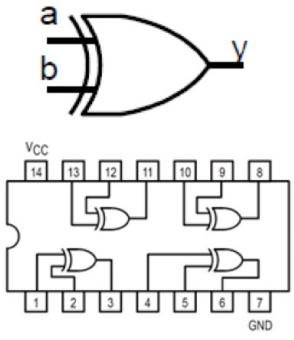
**74LS00**




| Input | | Output | | | |
|---|---|---|---|---|---|
| a | b | y (pin 3) | y (pin 6) | y (pin 8) | y (pin 11) |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 |

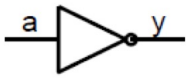
## XOR GATE

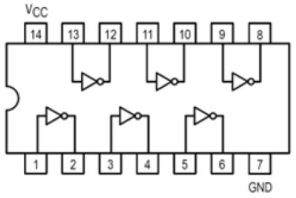
**74LS86**




| Input | | Output | | | |
|---|---|---|---|---|---|
| a | b | y (pin 3) | y (pin 6) | y (pin 8) | y (pin 11) |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 |

## 74LS04

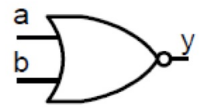


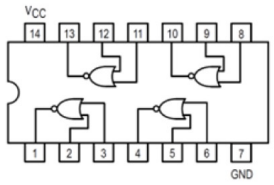




NOT GATE

| Input | Output | | | | | |
|---|---|---|---|---|---|---|
| a | y (pin 2) | y (pin 4) | y (pin 6) | y (pin 8) | y (pin 10) | y (pin 12) |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |

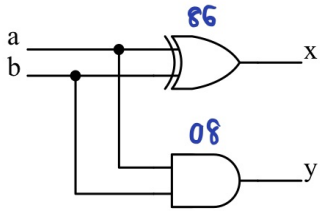
## 74LS02




NOR GATE

| Input | | Output | | | |
|---|---|---|---|---|---|
| a | b | y (pin 1) | y (pin 4) | y (pin 10) | y (pin 13) |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |

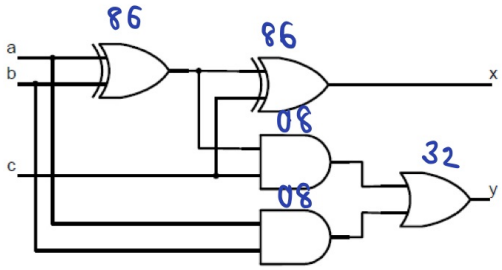



74LS86 & 74LS08

XOR GATE & AND GATE

HALF ADDER

| Input | | Output | |
|---|---|---|---|
| a | b | x | y |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |




Specify all IC No. used for the circuit

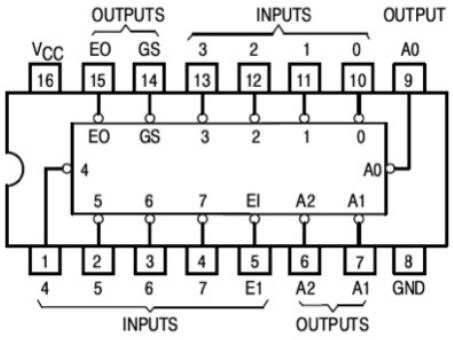
74LS86, 74LS08, 74LS32

XOR GATE, AND GATE, OR GATE

FULL ADDER

| Input | | | Output | |
|---|---|---|---|---|
| a | b | c | x | y |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

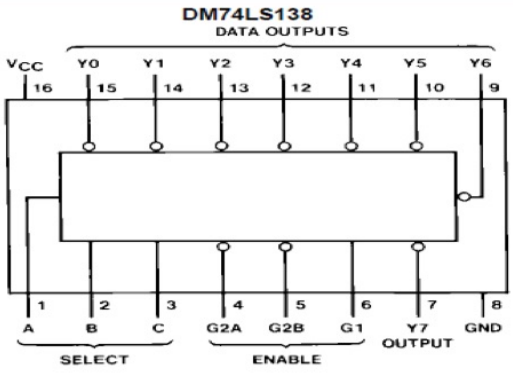
## 74LS148 8-to-3 Encoder




**FUNCTION TABLE**

| INPUTS | | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EI | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | A2 | A1 | A0 | GS | EO |
| H | X | X | X | X | X | X | X | X | H | H | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | X | X | X | X | X | X | X | L | L | L | L | L | H |
| L | X | X | X | X | X | X | L | H | L | L | H | L | H |
| L | X | X | X | X | X | L | H | H | L | H | L | L | H |
| L | X | X | X | X | L | H | H | H | L | H | H | L | H |
| L | X | X | X | L | H | H | H | H | H | L | L | L | H |
| L | X | X | L | H | H | H | H | H | H | L | H | L | H |
| L | X | L | H | H | H | H | H | H | H | H | L | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | L | H |

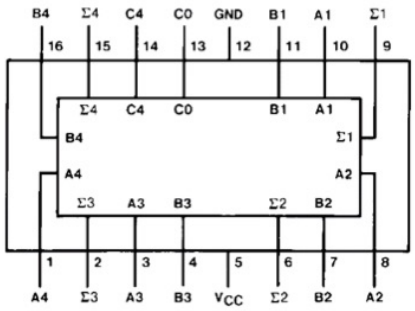
## 74LS138 3-to-8 Decoder




**DM74LS138**

| Inputs | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Enable | | Select | | | | | | | | | | |
| G1 | G2 (Note 1) | C | B | A | YO | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

## 74LS83 4-Bit Binary Adder with Fast Carry




### Truth Table

| Inputs | | | | Outputs: When C0 = L | | | Outputs: When C0 = H | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | When C2 = L | | | When C2 = H |
| A1 / A3 | B1 / B3 | A2 / A4 | B2 / B4 | Σ1 / Σ3 | Σ2 / Σ4 | C2 / C4 | Σ1 / Σ3 | Σ2 / Σ4 | C2 / C4 |
| L | L | L | L | L | L | L | H | L | L |
| H | L | L | L | H | L | L | L | H | L |
| L | H | L | L | H | L | L | L | H | L |
| H | H | L | L | L | H | L | H | H | L |
| L | L | H | L | L | H | L | H | H | L |
| H | L | H | L | H | H | L | L | L | H |
| L | H | H | L | H | H | L | L | L | H |
| H | H | H | L | L | L | H | H | L | H |
| L | L | L | H | L | H | L | H | H | L |
| H | L | L | H | H | H | L | L | L | H |
| L | H | L | H | H | H | L | L | L | H |
| H | H | L | H | L | L | H | H | L | H |
| L | L | H | H | L | L | H | H | L | H |
| H | L | H | H | H | L | H | L | H | H |
| L | H | H | H | H | L | H | L | H | H |
| H | H | H | H | L | H | H | H | H | H |

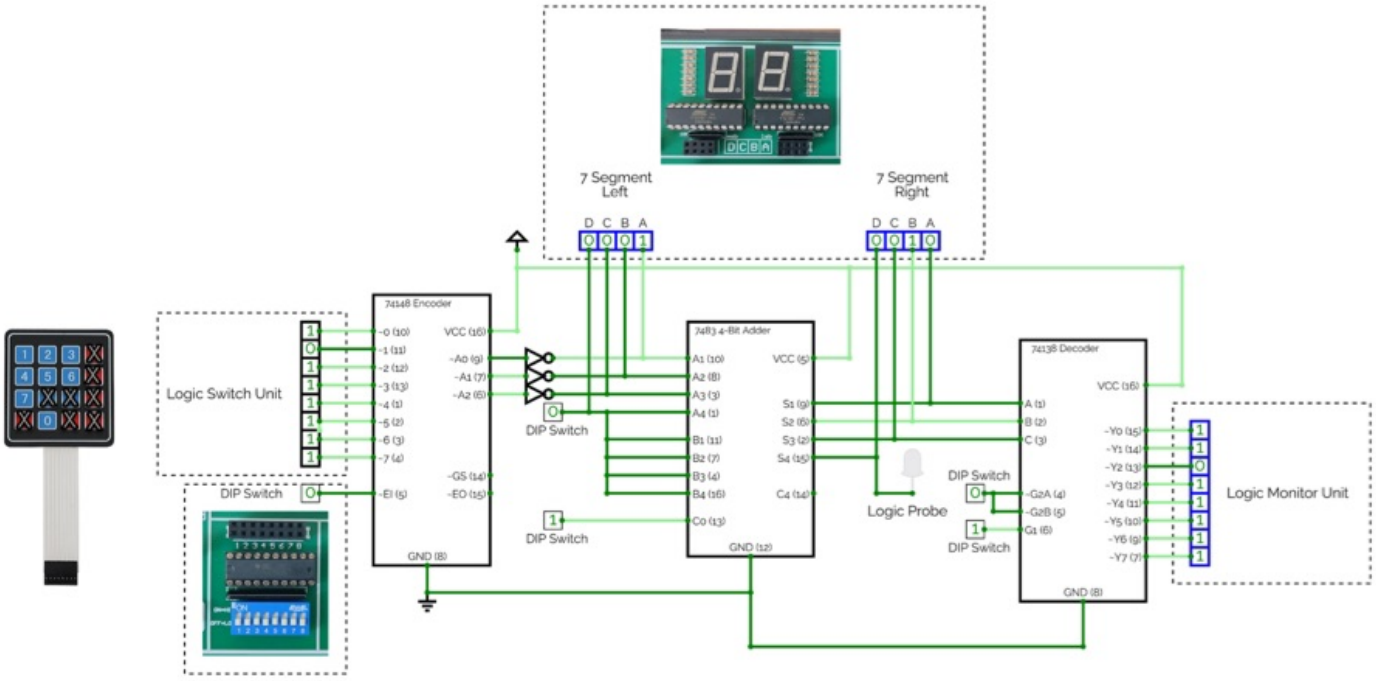



Fig 1 Encoder/Decoder Circuit

| Encoder | | | | | | | | Encoder | | | 7SEG | Adder/Dec | | | | 7SEG | Decoder | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input | | | | | | | | Output | | | Left | Output/Input | | | | Right | Output | | | | | | |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | A2 | A1 | A0 | | S4/ OVF | S3/C | S2/B | S1/A | | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| x | x | x | x | x | x | x | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| x | x | x | x | x | x | 0 | 1 | 0 | 0 | 1 | 5 | 0 | 1 | 1 | 1 | 7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| x | x | x | x | x | 0 | 1 | 1 | 0 | 1 | 0 | 5 | 0 | 1 | 1 | 0 | 6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| x | x | x | x | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 3 | 0 | 1 | 0 | 1 | 5 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| x | x | x | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 4 | 0 | 1 | 0 | 0 | 4 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| x | x | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 2 | 0 | 0 | 1 | 1 | 3 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| x | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | - | 0 | 0 | 1 | 0 | 2 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |