Lab 6

Getting started with Vivado & VHDL

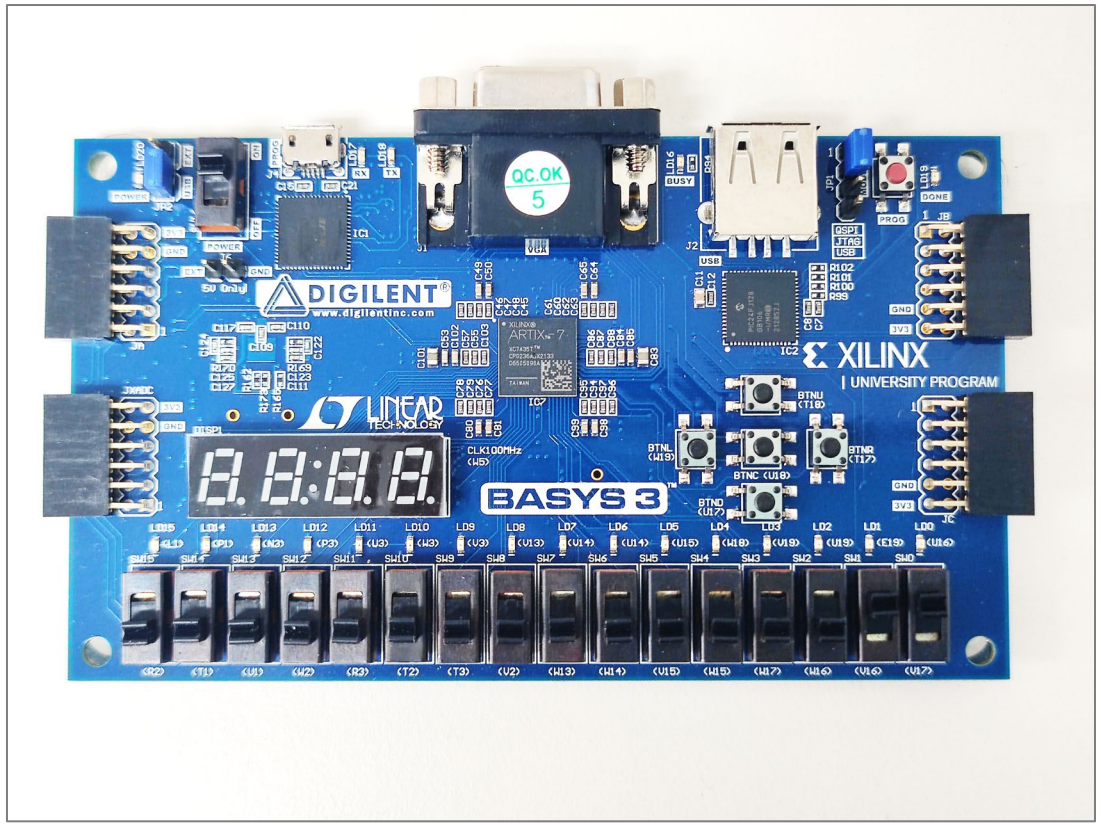
Digital System Fundamentals

Sorayut Glomglome

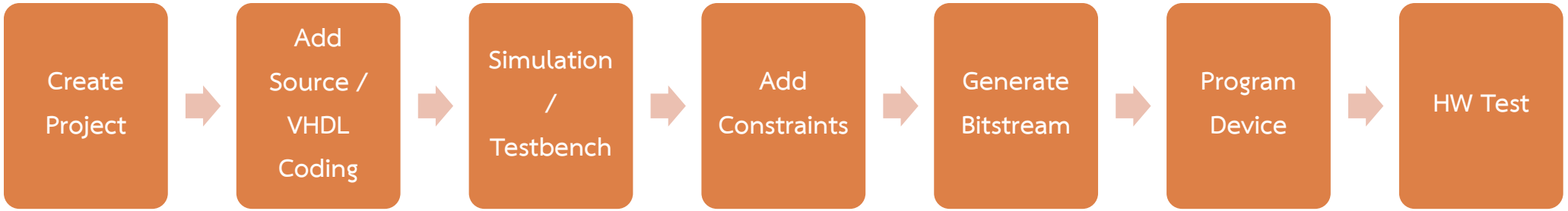
1. Getting Started

Basys 3 | FPGA Board

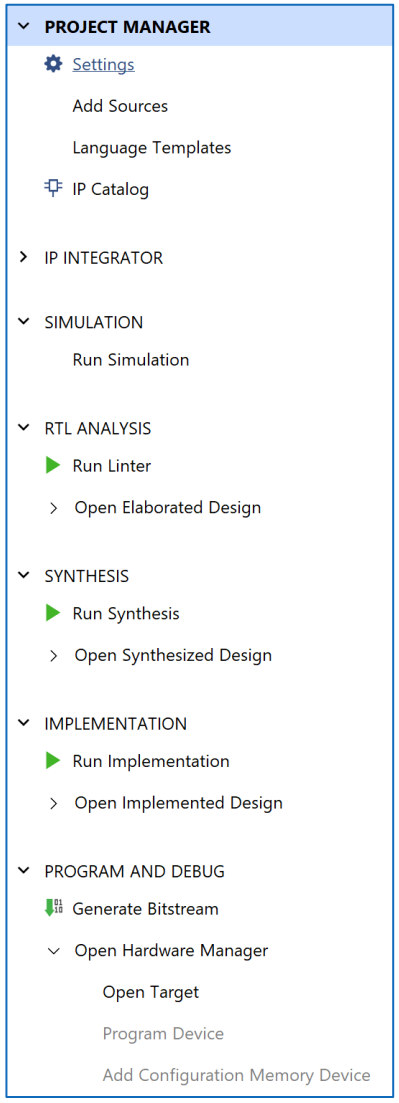
[Basys 3 - Digilent Reference]

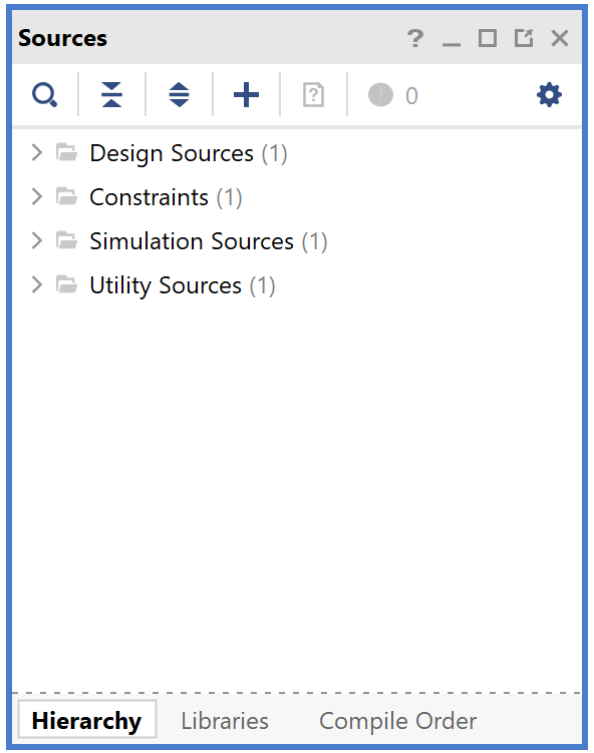


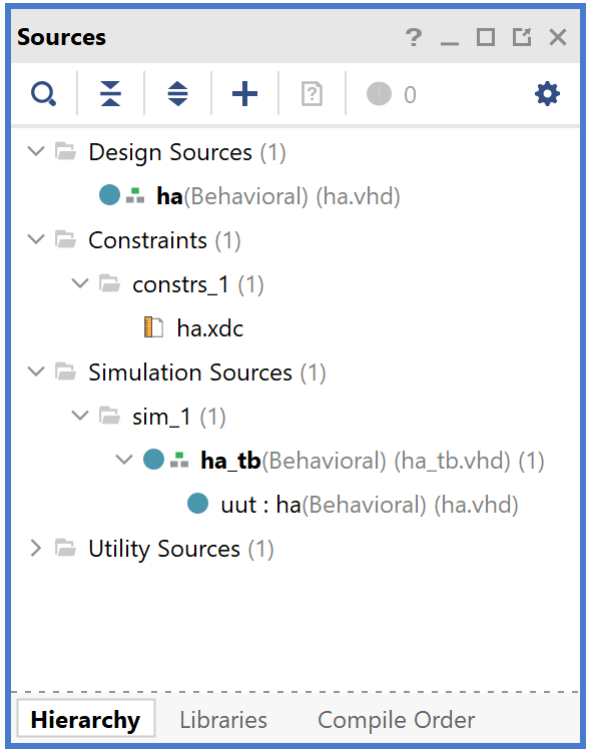
Process Flow



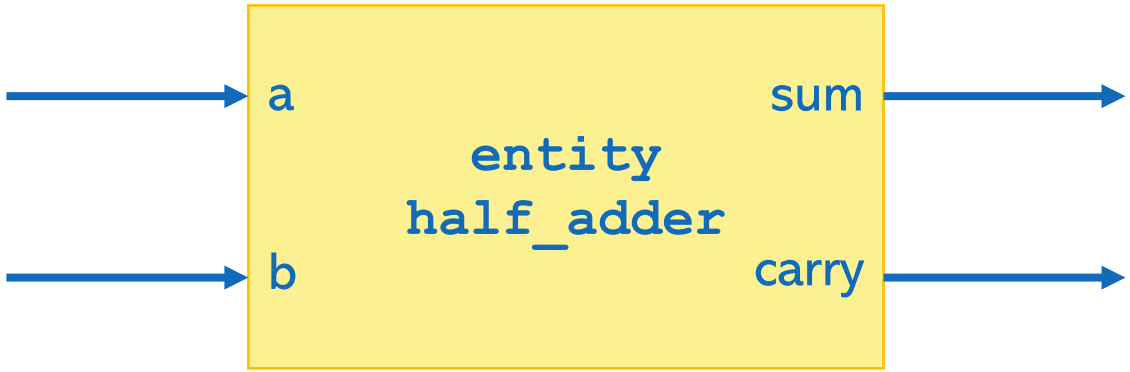
User Interface





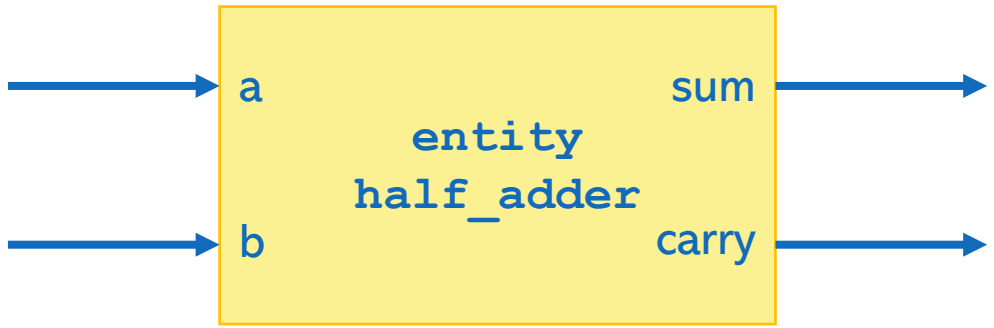


Half Adder | Block Diagram

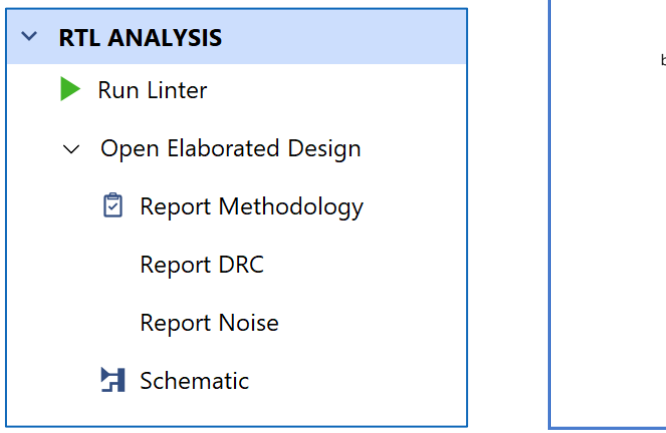


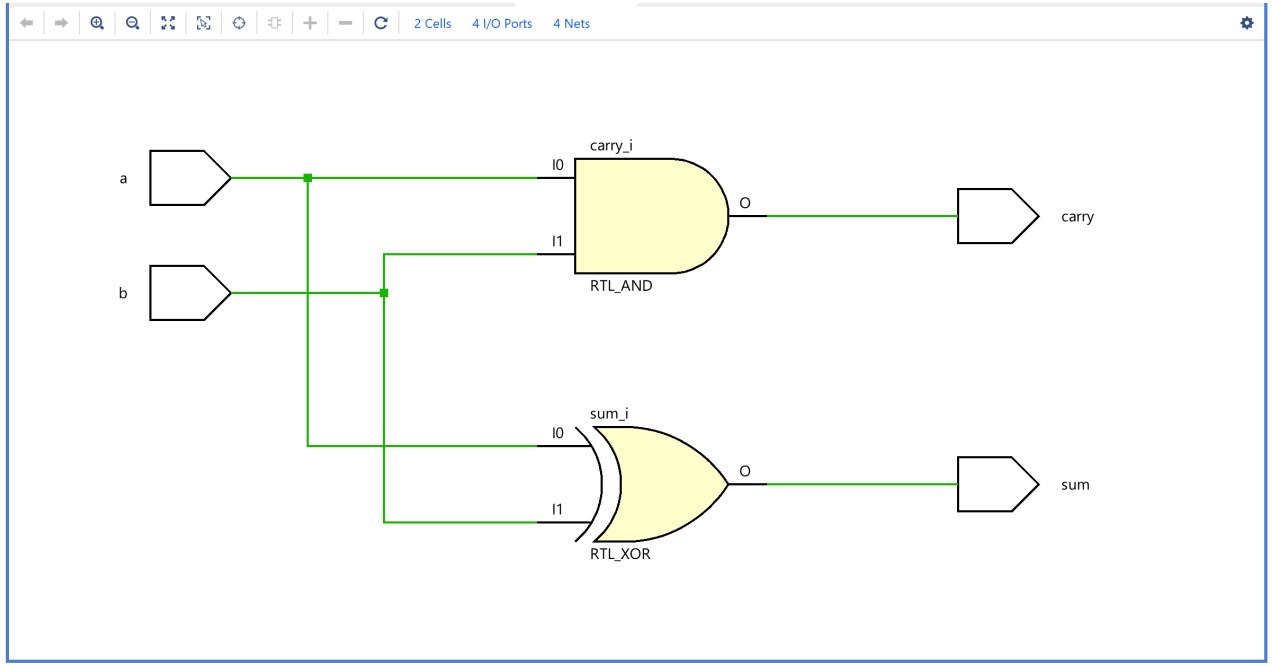
Half Adder | VHDL

```
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
35
36  entity ha is
37      Port ( a : in STD_LOGIC;
38             b : in STD_LOGIC;
39             sum : out STD_LOGIC;
40             carry : out STD_LOGIC);
41  end ha;
42
43  architecture Behavioral of ha is
44
45  begin
46
47      sum <= a xor b;
48      carry <= a and b;
49
50
51  end Behavioral;
52
```



Schematic



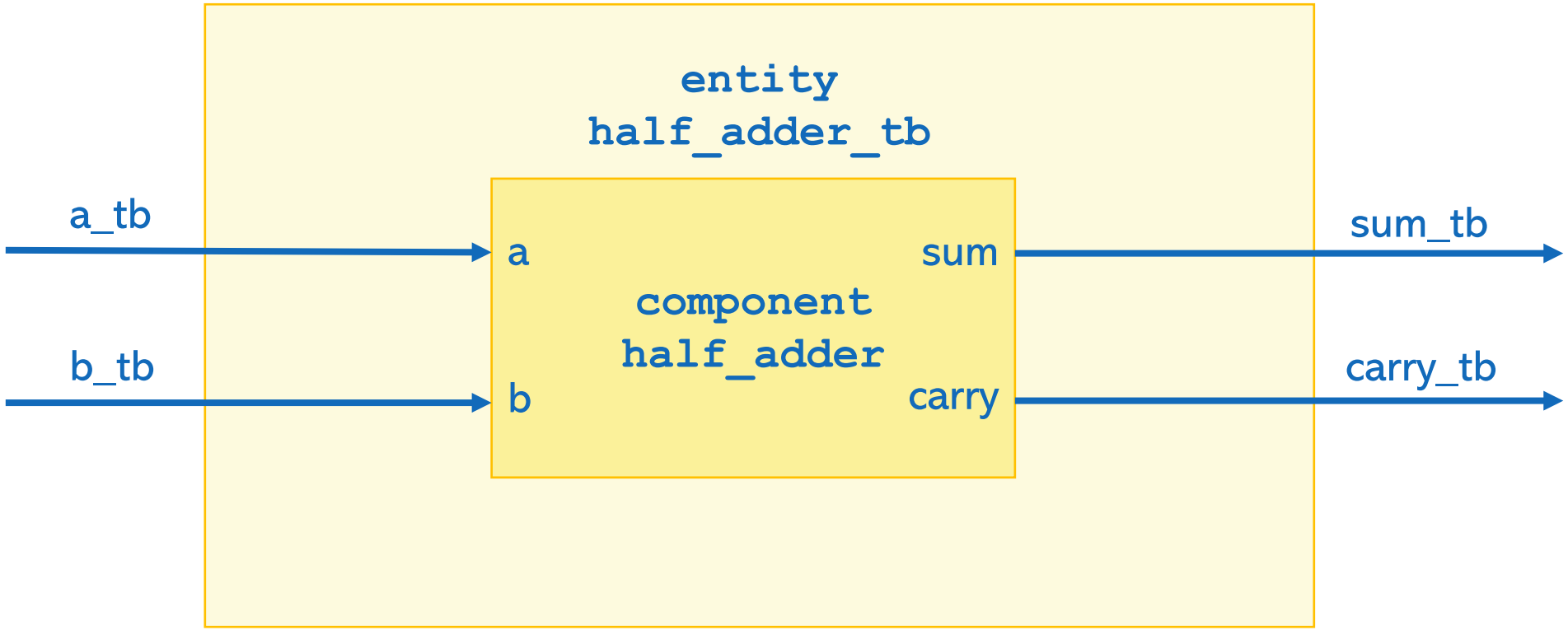


Tcl Console | Messages | Log | Reports | Design Runs | **Find Results**

Name	Direction	Board Part Pin	Board Part Interface	Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco
a	IN					V17	✓	14	LVCMOS33*	3.300
b	IN					V16	✓	14	LVCMOS33*	3.300
carry	OUT					E19	✓	14	LVCMOS33*	3.300
sum	OUT					U16	✓	14	LVCMOS33*	3.300

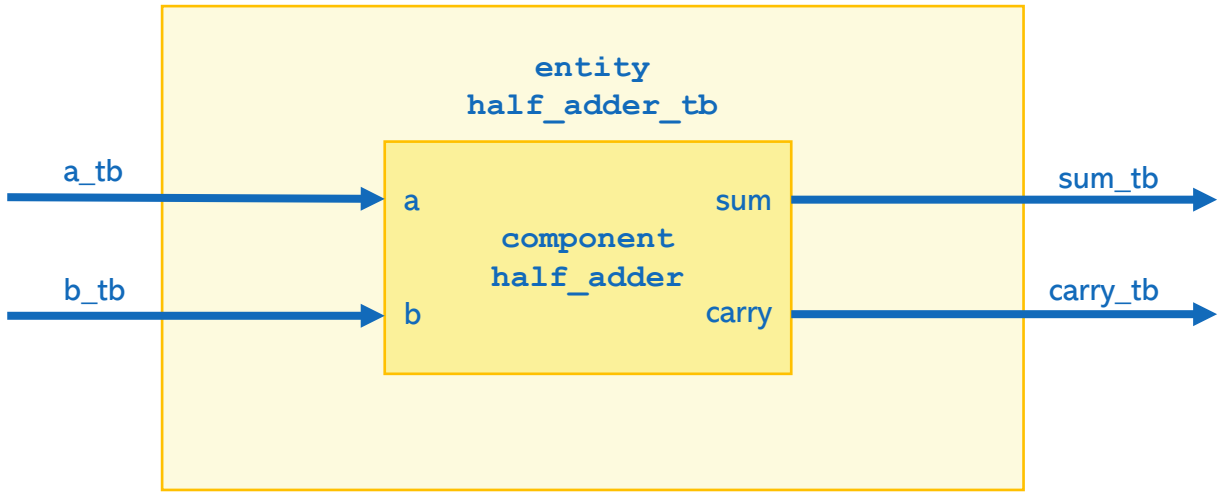
```
set_property PACKAGE_PIN V17 [get_ports a]
set_property PACKAGE_PIN V16 [get_ports b]
set_property PACKAGE_PIN E19 [get_ports carry]
set_property PACKAGE_PIN U16 [get_ports sum]
set_property IOSTANDARD LVCMOS33 [get_ports a]
set_property IOSTANDARD LVCMOS33 [get_ports b]
set_property IOSTANDARD LVCMOS33 [get_ports carry]
set_property IOSTANDARD LVCMOS33 [get_ports sum]
```

Half Adder | Testbench



Half Adder | Testbench VHDL

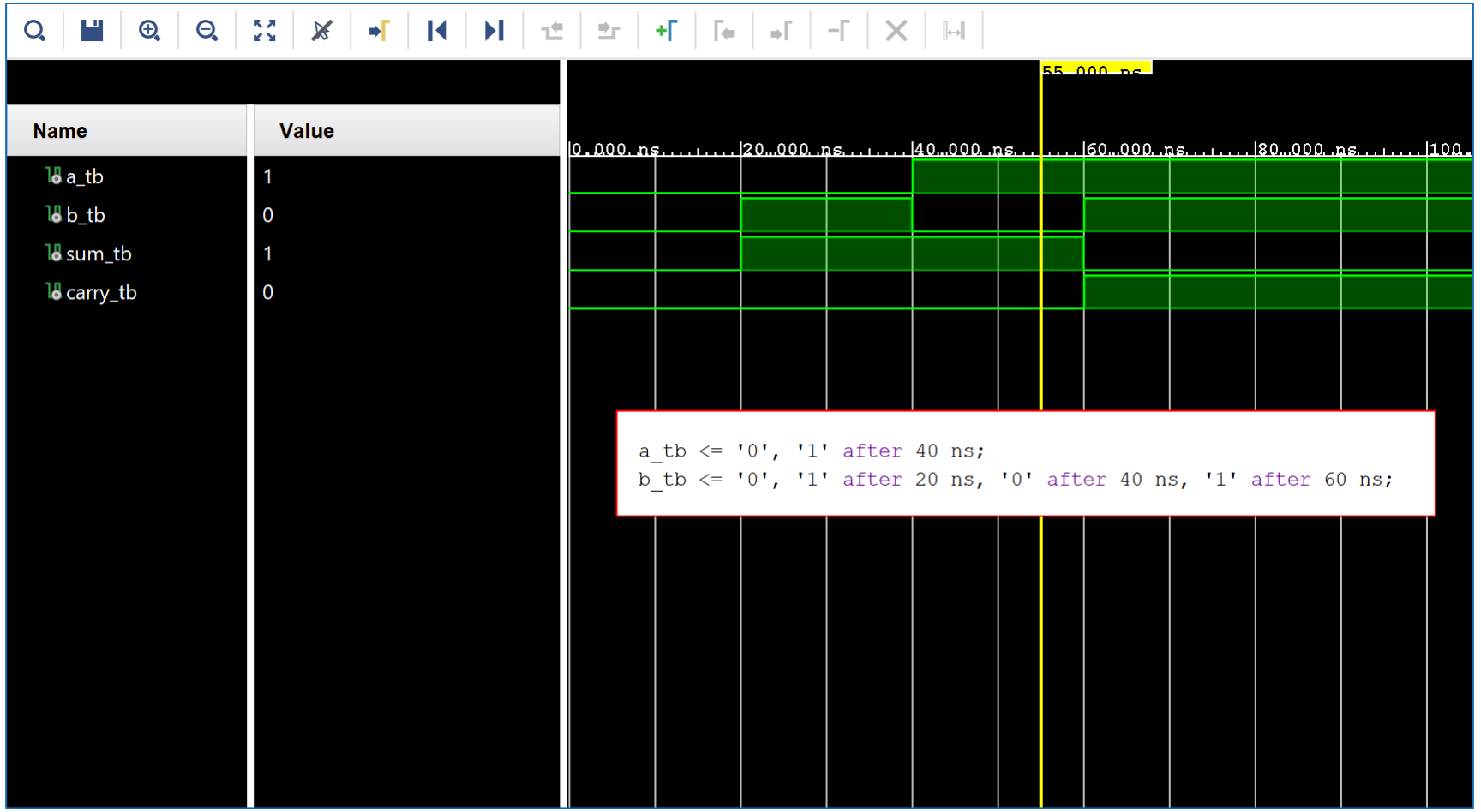
```
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
33
34  entity ha_tb is
35  --  Port ( );
36  end ha_tb;
37
38  architecture Behavioral of ha_tb is
39
40  component ha is port(
41      a : in STD_LOGIC;
42      b : in STD_LOGIC;
43      sum : out STD_LOGIC;
44      carry : out STD_LOGIC);
45  end component;
46
47  signal a_tb, b_tb, sum_tb, carry_tb : std_logic;
48
49  begin
50
51      uut : ha port map (a => a_tb,
52                         b => b_tb,
53                         sum => sum_tb,
54                         carry => carry_tb);
55
56      a_tb <= '0', '1' after 40 ns;
57      b_tb <= '0', '1' after 20 ns, '0' after 40 ns, '1' after 60 ns;
58
59  end Behavioral;
60
```



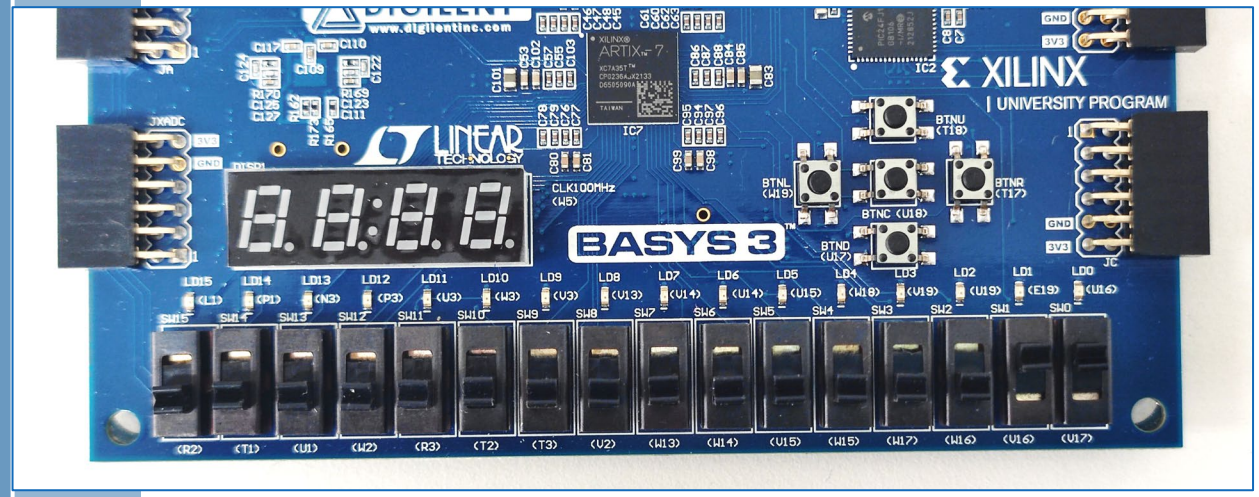
← internal signal

0 for 40 ns, then switch for logic 1

Half Adder | Simulation Waveform



Half Adder | Add Constraints




```
## Switches
set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports a]
set_property -dict { PACKAGE_PIN V16   IOSTANDARD LVCMOS33 } [get_ports b]
#set_property -dict { PACKAGE_PIN W16   IOSTANDARD LVCMOS33 } [get_ports {sw[2]}]
#set_property -dict { PACKAGE_PIN W17   IOSTANDARD LVCMOS33 } [get_ports {sw[3]}]
#set_property -dict { PACKAGE_PIN W15   IOSTANDARD LVCMOS33 } [get_ports {sw[4]}]
#set_property -dict { PACKAGE_PIN V15   IOSTANDARD LVCMOS33 } [get_ports {sw[5]}]
#set_property -dict { PACKAGE_PIN W14   IOSTANDARD LVCMOS33 } [get_ports {sw[6]}]
#set_property -dict { PACKAGE_PIN W13   IOSTANDARD LVCMOS33 } [get_ports {sw[7]}]
#set_property -dict { PACKAGE_PIN V2    IOSTANDARD LVCMOS33 } [get_ports {sw[8]}]
#set_property -dict { PACKAGE_PIN T3    IOSTANDARD LVCMOS33 } [get_ports {sw[9]}]
#set_property -dict { PACKAGE_PIN T2    IOSTANDARD LVCMOS33 } [get_ports {sw[10]}]
#set_property -dict { PACKAGE_PIN R3    IOSTANDARD LVCMOS33 } [get_ports {sw[11]}]
#set_property -dict { PACKAGE_PIN W2    IOSTANDARD LVCMOS33 } [get_ports {sw[12]}]
#set_property -dict { PACKAGE_PIN U1    IOSTANDARD LVCMOS33 } [get_ports {sw[13]}]
#set_property -dict { PACKAGE_PIN T1    IOSTANDARD LVCMOS33 } [get_ports {sw[14]}]
#set_property -dict { PACKAGE_PIN R2    IOSTANDARD LVCMOS33 } [get_ports {sw[15]}]


## LEDs
set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports sum]
set_property -dict { PACKAGE_PIN E19   IOSTANDARD LVCMOS33 } [get_ports carry]
#set_property -dict { PACKAGE_PIN U19   IOSTANDARD LVCMOS33 } [get_ports {led[2]}]
#set_property -dict { PACKAGE_PIN V19   IOSTANDARD LVCMOS33 } [get_ports {led[3]}]
#set_property -dict { PACKAGE_PIN W18   IOSTANDARD LVCMOS33 } [get_ports {led[4]}]
#set_property -dict { PACKAGE_PIN U15   IOSTANDARD LVCMOS33 } [get_ports {led[5]}]
#set_property -dict { PACKAGE_PIN U14   IOSTANDARD LVCMOS33 } [get_ports {led[6]}]
#set_property -dict { PACKAGE_PIN V14   IOSTANDARD LVCMOS33 } [get_ports {led[7]}]
#set_property -dict { PACKAGE_PIN V13   IOSTANDARD LVCMOS33 } [get_ports {led[8]}]
#set_property -dict { PACKAGE_PIN V3    IOSTANDARD LVCMOS33 } [get_ports {led[9]}]
#set_property -dict { PACKAGE_PIN W3    IOSTANDARD LVCMOS33 } [get_ports {led[10]}]
#set_property -dict { PACKAGE_PIN U3    IOSTANDARD LVCMOS33 } [get_ports {led[11]}]
#set_property -dict { PACKAGE_PIN P3    IOSTANDARD LVCMOS33 } [get_ports {led[12]}]
#set_property -dict { PACKAGE_PIN N3    IOSTANDARD LVCMOS33 } [get_ports {led[13]}]
#set_property -dict { PACKAGE_PIN P1    IOSTANDARD LVCMOS33 } [get_ports {led[14]}]
#set_property -dict { PACKAGE_PIN L1    IOSTANDARD LVCMOS33 } [get_ports {led[15]}]

```

Reference

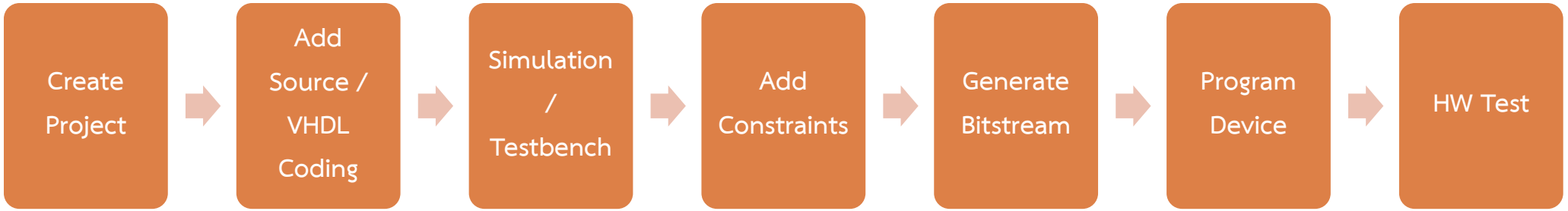
1. Step-by-step guide on how to design and implement a Half Adder using Testbench code with Xilinx Vivado design tool using VHDL. | by Radha Kulkarni | Medium
2. VHDL code for half adder & full adder using dataflow method - full code & explanation (technobyte.org)
3. Vivado Tutorial | Implementing Half Adder | VHDL Coding | Simulation | #FPGA #VLSI #VHDL (youtube.com)
4. electronics blog: VHDL half adder code test in circuit and test bench xilinx spartan 3 development board (quitoart.blogspot.com)
5. digilent-xdc/Basys-3-Master.xdc at master · Digilent/digilent-xdc · GitHub
6. Basys 3 - Digilent Reference
7. VHDL Tutorial: Learn by Example (ucr.edu)

2. Experiment

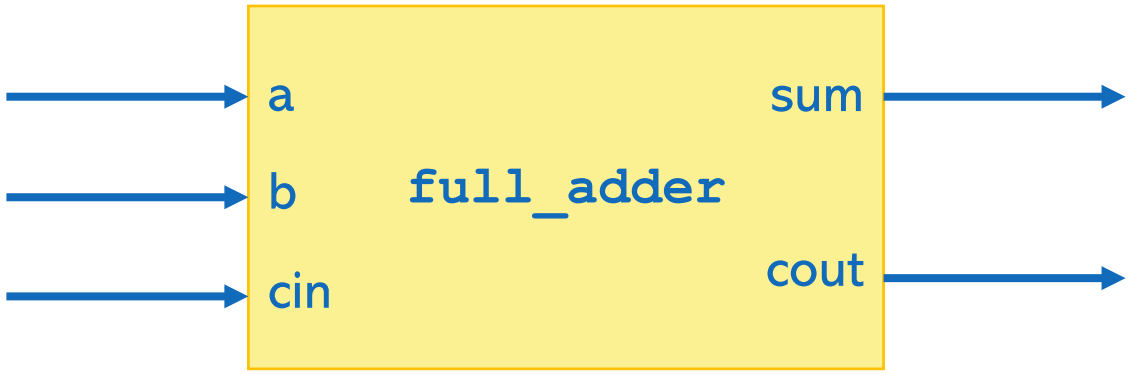
Implement full adder using VHDL & Vivado

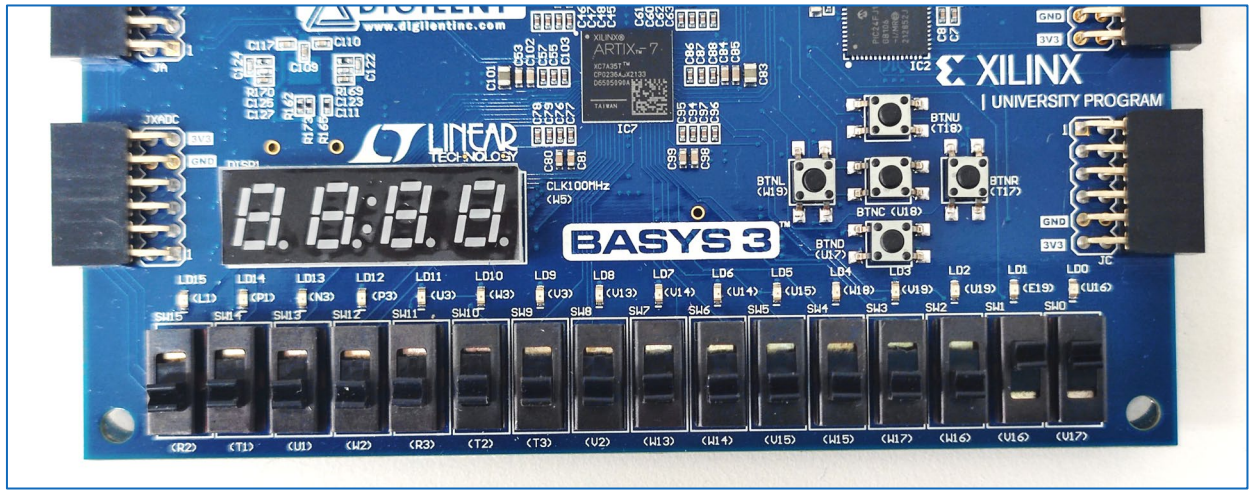
2.1 Checkpoint 1

Full Adder | Process Flow



Full Adder | Block Diagram & Constraints





Port	I/O Type	Label	Pin
a	switch	SW0	V17
b	switch	SW1	V16
cin	switch	SW2	W16
sum	LED	LD0	U16
cout	LED	LD1	E19

THANK YOU