Part1:

PWM frequency = 5000 Hz

Duty cycle = 256(8 bit)

Part2:

Speed increased by 10% every 500 ms => 255* 10/100 = 25

Part3:

Adcon1 = 14 because we have 15 ports and we only need 1

Adcon2 = 10010101 = 149

Fadc = 12MHz => Tad = 1/Fad = 0.05 us => less than 0.7 so we multiply by 16

⇨ Tad = 0.05 * 16 = 0.08 us

From the datasheet: Fasc/16 = **101** (for the last 3 bits)

K = 2.45/0.8 = 3.06

From the datasheet: k = 4 = **010** => Tad = 010

First digit = **1** representing format 1

Part A:

No calculations are required.

Part B:

We update the counter by 10% of the range of the duty cycle which is 255 so 10% of 255 is 25 per step.

Part C:

ADCON0 is set to 14 because there are 15 analog pins and we only need one.

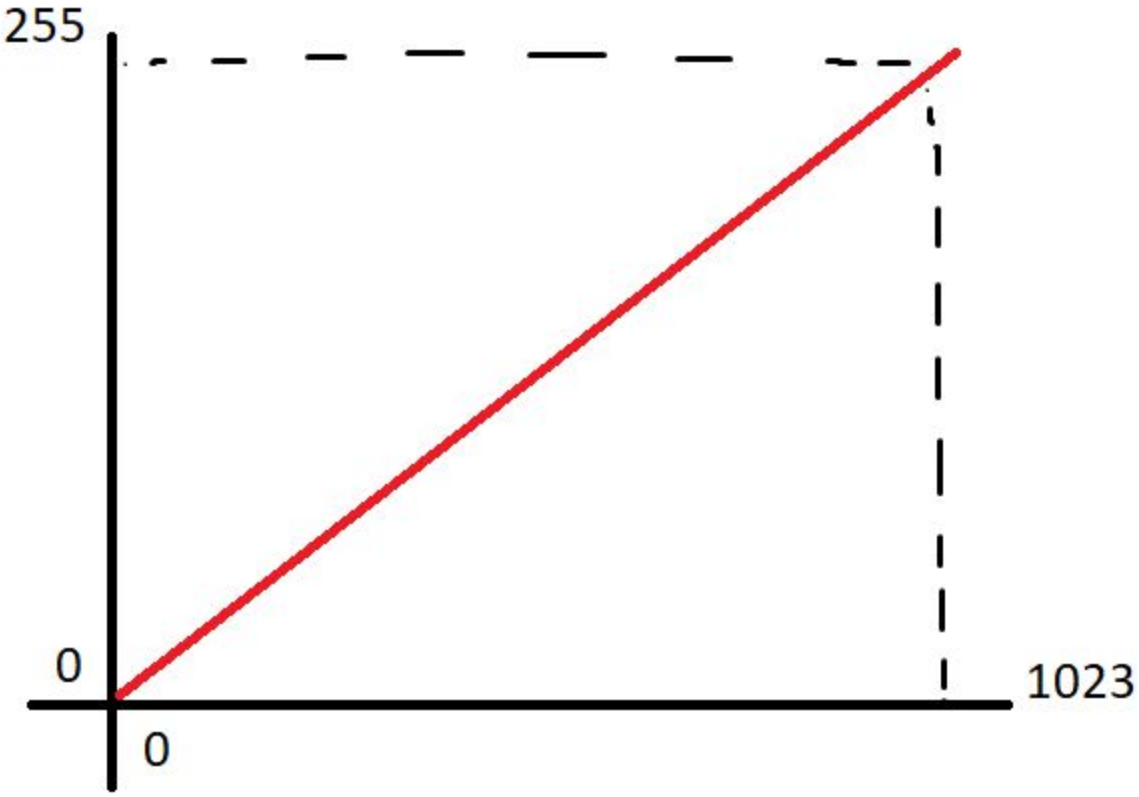
ADCON2 is set to 0b10010101 because:

$F_{ADC} = 20Mhz$, then the time T_{ADC} is $0.05\ \mu s$ but but it's less than $0.7\ \mu s$ and we need to expand it. From the data sheet we can multiply it by 16 so we get $0.8\ \mu s$, so T_{ADC} is $0.8\ \mu s$.

From the datasheet we know that 16 will decide the first 6 bits: **Clock option** $Fosc/16 = 101$, **Acquisition Time** $K = 2.45\mu s / 0.8\mu s$ = 4 = 010.

the most significant bit will be set to 1.

Compute the Linear equation of the relationship between the read voltage through A0 and the duty cycle.



D = a * Z + b

where a = $y2 - y1 / x2 - x1 = (255 - 0) / (1023 - 0) = 255 / 1023$ and there is no shif so b = 0.

Part D:

When the reading of Z is in the middle (1023 / 2 => 50%) then d is zero, but when the reading is greater than 50% the output voltage is shifted by 50% of the duty cycle range i.e. 128 of PWM1 and 0 to PWM2, and when the reading is less than 50% then we do the same shif and make sure it still positive for PWM2 and 0 for PWM1.