

Part1:

PWM frequency = 5000 Hz

Duty cycle = 256(8 bit)

Part2:

Speed increased by 10% every 25 ms  $\Rightarrow 124 * 10/100 = 12.4$

Part3:

Adcon1 = 14 because we have 15 ports and we only need 1

Adcon2 = 10010101 = 149

Fadc = 12MHz  $\Rightarrow T_{ad} = 1/F_{ad} = 0.05 \mu s \Rightarrow$  less than 0.7 so we multiply by 16

$\Rightarrow T_{ad} = 0.05 * 16 = 0.8 \mu s$

From the datasheet:  $F_{osc}/16 = \mathbf{101}$  (for the last 3 bits)

$K = 2.45/0.8 = 3.06$

From the datasheet:  $k = 4 = \mathbf{010} \Rightarrow T_{ad} = 010$

First digit = **1** representing format 1

Part A:

No calculations are required.

Part B:

We update the counter by 10% of the range of the duty cycle which is 124 so 10% of 124 is 12.4 per step.

Part C:

ADCON0 is set to 14 because there are 15 analog pins and we only need one.

ADCON2 is set to 0b10010101 because:

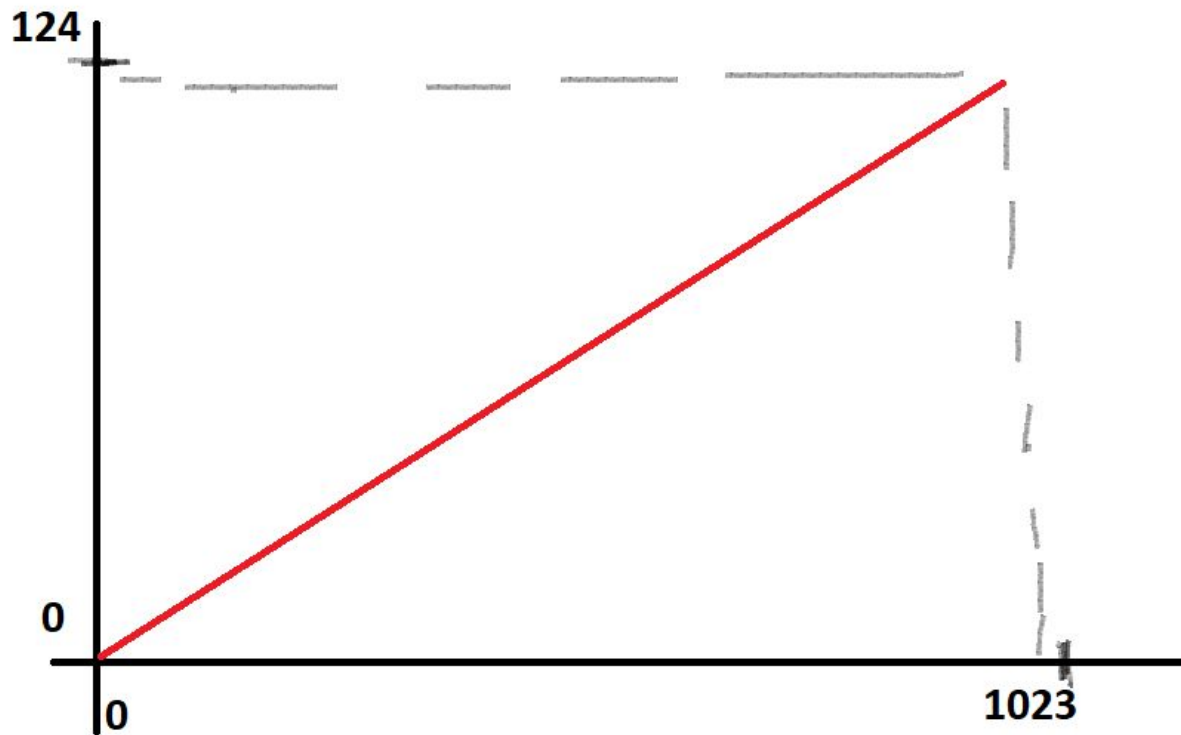
$F_{ADC} = 20MHz$ , then the time  $T_{ADC}$  is  $0.05 \mu s$  but it's less than  $0.7 \mu s$  and we need to expand it. From the data sheet we can multiply it by 16 so we get  $0.8 \mu s$ , so  $T_{ADC}$  is  $0.8 \mu s$ .

From the datasheet we know that 16 will decide the first 6 bits: **Clock option**  $F_{osc} / 16 = 101$ ,

**Acquisition Time**  $K = 2.45 \mu s / 0.8 \mu s = 4 = 010$ .

the most significant bit will be set to 1.

Compute the Linear equation of the relationship between the read voltage through A0 and the duty cycle.



$$D = a * Z + b$$

where  $a = \frac{y_2 - y_1}{x_2 - x_1} = \frac{124 - 0}{1023 - 0} = 124 / 1023$  and there is no shift so  $b = 0$ .

Part D:

When the reading of Z is in the middle ( $1023 / 2 \Rightarrow 50\%$ ) then d is zero, but when the reading is greater than 50% the output voltage is shifted by 50% of the duty cycle range i.e. 62 of PWM1 and 0 to PWM2, and when the reading is less than 50% then we do the same shift and make sure it is still positive for PWM2 and 0 for PWM1.