Resolving the Signal Part 12: Reducing the Effects of Power-Supply Noise using Delta-Sigma ADCs

Chris Anderson
16-20 minutes

In part 12 of Resolving the Signal, we look at a power-supply noise design example using the ADS127L01 evaluation module. From that example, we offer best practices to maintain low power-supply noise and debugging tips for a system's overall noise performance.

This article was co-authored by Ryan Andrews, applications engineer for precision analog-to-digital converters at Texas Instruments.

In part 11 of our series, we discussed power-supply noise topics, including what causes a noisy power supply and how it affects your analog-to-digital converter (ADC). We also introduced power-supply rejection (PSR) as a method of characterizing how effective a power supply is at rejecting noise. Finally, we briefly analyzed the effect that power-supply noise has on different ADC supplies.

In this article, we'll continue the power-supply noise discussion with a design example using the ADS127L01 evaluation module (EVM). This example will help illustrate which supplies are most critical when trying to increase your system's PSR. Finally, we'll discuss best practices to maintain low power-supply noise and debugging tips to improve your system's overall noise performance.

AVDD, DVDD, or LVDD: Which is Most Important?

In part 11, we looked at the PSR ratio (PSRR) for each of the power supplies used by the Texas Instruments (TI) ADS127L01 (shown again in Figure 1). Like most ADCs, the ADS127L01 uses both an analog and a digital supply (AVDD and DVDD, respectively). We chose this device for our discussion because it also requires a third supply called the low-voltage dropout supply (LVDD). LVDD directly powers the delta-sigma modulator in the ADS127L01. The LVDD supply can either be provided from an internal low-dropout regulator (LDO) (connected to AVDD) or from an external LVDD supply source. As you'll see later in this article, driving LVDD externally with a noisy supply will have the most adverse effect on ADC noise performance.

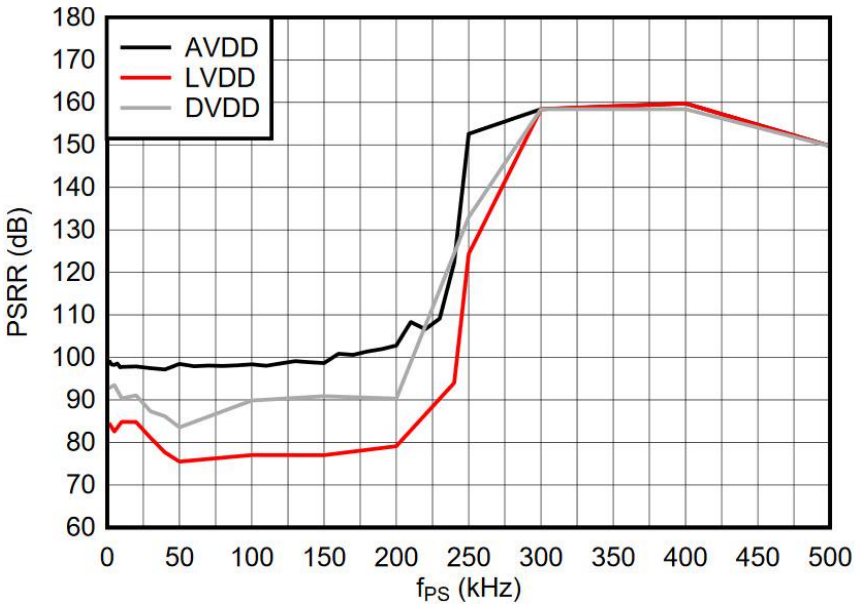

Figure 1. T_A=25°C, AVDD = 3.3V, VREF = 2.5V, HR Mode, INTLDO = 1

From Figure 1, you can see that LVDD is most susceptible to coupling noise into the ADC output because it has the lowest PSRR of the three supplies. LVDD is most sensitive to noise because it directly powers the delta-sigma modulator, which in turn directly controls the analog-input-to-digital-output conversion process. Comparatively, AVDD powers the remaining analog circuitry, including generating the main bias current, but this has less of a direct impact on the conversion results. Powering the ADC's digital core, DVDD has the least impact on the conversion results because the modulator output is already in binary form when it reaches the digital decimation filter. For devices that require multiple supplies, prioritize the supply that most directly powers the delta-sigma modulator, which is typically AVDD.

To illustrate the effects of driving the modulator with a noisy supply in the real world, we conducted an ADC input-short noise measurement on the ADS127L01 evaluation module EVM under these four conditions:

- Clean supplies on AVDD, LVDD and DVDD (no ripple).
- AVDD = 3 V + 1-kHz, 100-mVP ripple, clean LVDD and DVDD.
- LVDD = 1.825 V + 1-kHz, 100-mVP ripple, clean AVDD and DVDD.
- DVDD = 1.8 V + 1-kHz, 100-mVP ripple, clean AVDD and LVDD.

In each case, we shorted the ADC inputs together, biased them to mid supply (1.5 V) and computed the maximum achievable signal-to-noise ratio relative to the ADC full-scale. We refer to this result as the ADC's dynamic range. Table 1 in the ADS127L01 data sheet (PDF) lists the typical noise performance for each of the ADC's modes of operation and data rate. This test was conducted in very low power mode with a 4-MHz clock input using the wideband 2 digital filter with an oversampling ratio = 256. From Table 1, we expect approximately 114 dB of dynamic range at these settings.

As anticipated, the EVM performs best when using clean voltage supplies for all three ADC supply pins. Figure 2 shows a noise histogram (left) and fast Fourier transform (FFT) (right) under these conditions, resulting in a dynamic range of 113.56 dB, which is very close to the data-sheet specifications.

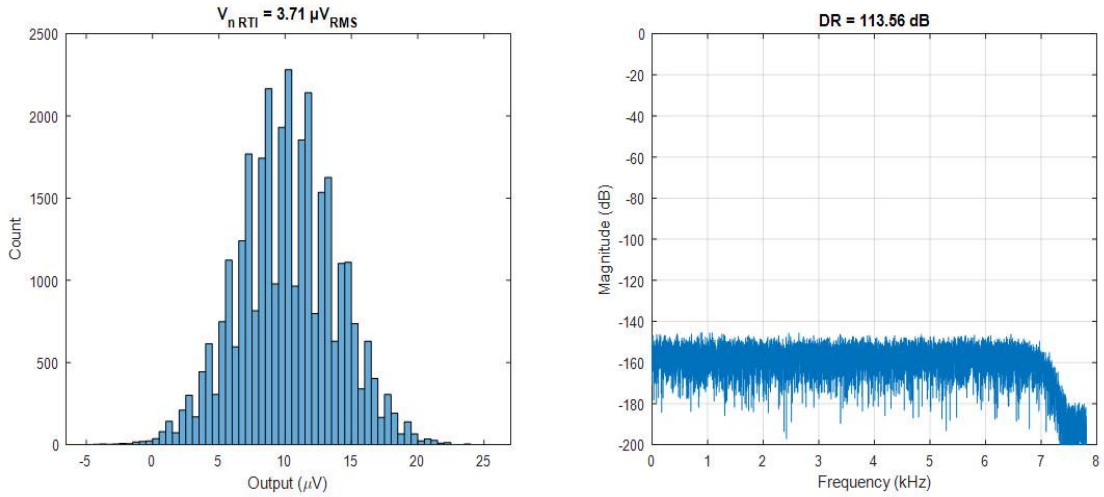

Figure 2. Noise histogram (left) and FFT (right) for clean supplies on AVDD, LVDD, and DVDD

We then added a 1-kHz, 100-mVP sine wave on top of the 3-V AVDD supply. This sine wave mimics power-supply noise, and was applied to the ADC using a signal generator with a DC offset equal to the nominal AVDD supply voltage (3 V). In this case, the internal LDO on the ADS127L01 was still able to reject most of this noise and maintain nominal performance at 113.33 dB, as shown in Figure 3. Notice that a small tone appears in the frequency spectrum at 1 kHz with a magnitude of -127 dB. This should correlate to the original input signal level relative to full scale (-28 dB for a 2.5-V ADC reference voltage) minus the AVDD PSRR, or about 100 dB.

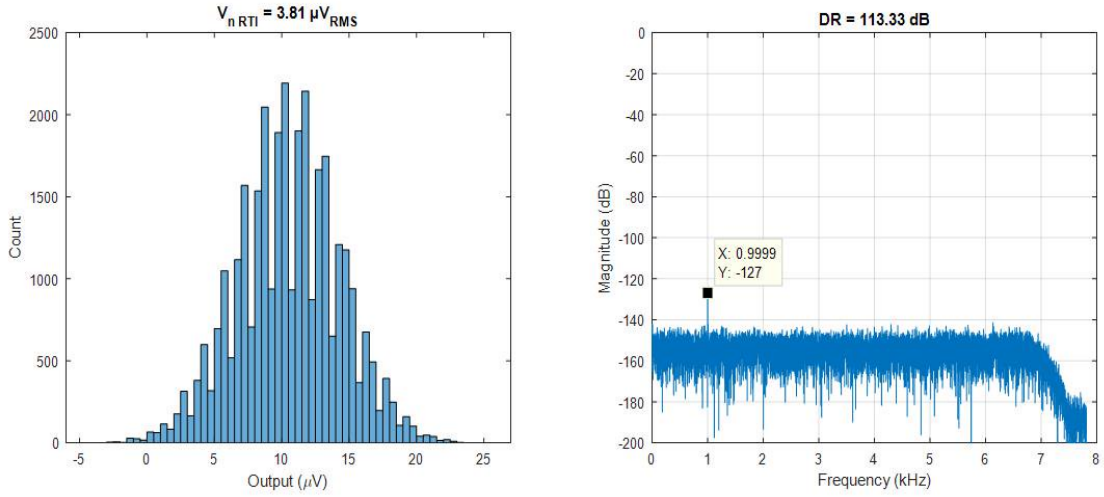

Figure 3. Noise histogram (left) and FFT (right) for clean supplies on LVDD and DVDD, ripple on AVDD

In the next test, we reverted back to using the default AVDD supply on the EVM and used the signal generator to provide the LVDD supply instead. In this test, we input a 1-kHz, 100-mVP sine-wave ripple centered on a 1.825-V DC offset and bypassed the internal LDO. As a result, the LVDD supply noise caused a significant degradation in noise performance (105.52 dB), as shown in Figure 4. Also, compared to the right-hand image in Figure 3, the 1-kHz tone is much more apparent in the frequency spectrum (-106 dB).

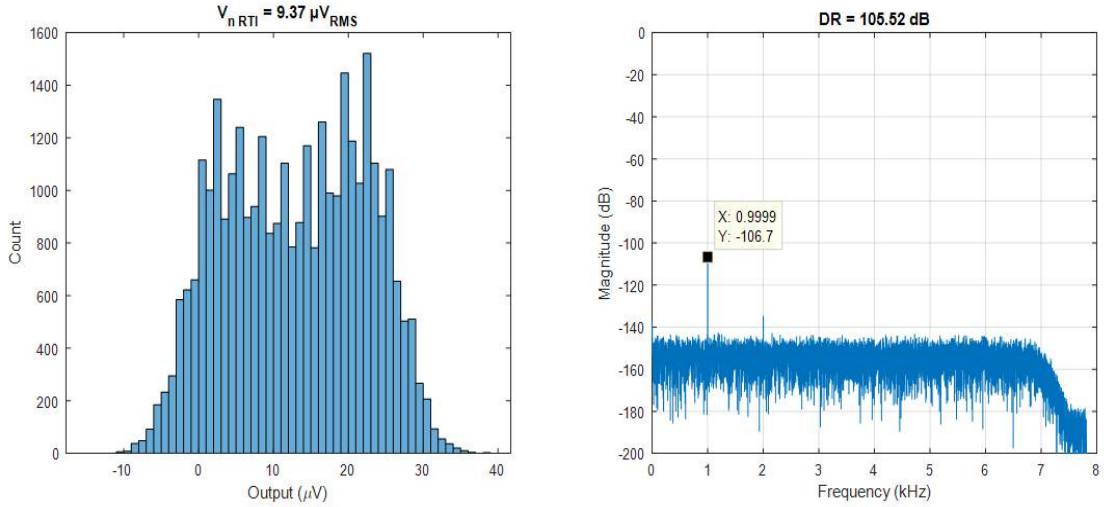

Figure 4. Noise histogram (left) and FFT (right) for clean supplies on AVDD and DVDD, ripple on LVDD

In the last test, we reverted AVDD and LVDD back to the default clean EVM supplies and applied the sine wave to DVDD. In this case, the 1-kHz, 100-mVP sine-wave ripple was centered on a 1.8-V DC offset. Interestingly, Figure 4 shows less dynamic range degradation compared to the LVDD experiment (111.14 dB), even though more harmonics of the 1-kHz ripple could be seen in the resulting FFT.

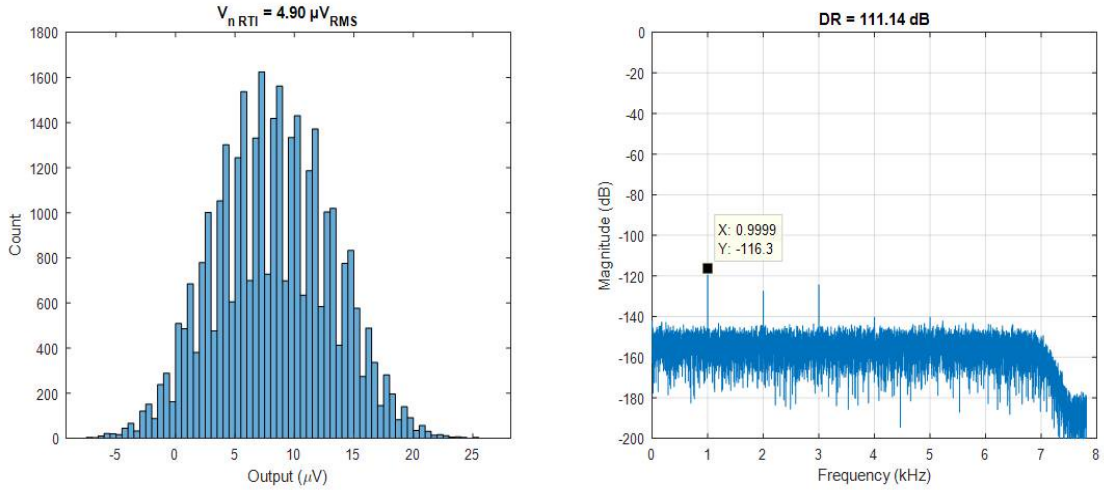

Figure 5. Noise histogram (left) and FFT (right) for clean supplies on AVDD and LVDD, ripple on DVDD

Ultimately, these experiments confirm the results in Figure 1 while reiterating that some supplies – especially the one that feeds the delta-sigma modulator – are more susceptible to power-supply noise than others and may require special care to maintain high PSR.

Improving PSR

To that end, let's consider a few ways to maintain a good PSRR in your system using three different techniques, starting with the most critical: layout.

Optimize your Layout

Layout optimization is by far the most important technique you can use to improve PSRR and maintain system performance. As we have spent significant time discussing DC/DC switching regulator noise coupling onto your supplies, one specific layout optimization action that you can take is to isolate this noise by placing switching

regulators away from sensitive analog inputs. Switching regulators are great for their efficiency, but they can inject large transients on your supplies that couple into surrounding circuitry, including the ADC itself. If the power-conditioning circuits are on the same side of the printed circuit board (PCB) as the digital components, neither of the noisy return currents should ever have to flow through the more sensitive analogy circuitry.

However, some PCBs may be restricted by their size or shape such that these types of layout techniques are not feasible. For example, Figure 6 shows the scale of a PCB compared to a quarter from one of TI's temperature transmitter reference designs. With such limited space, optimizing your layout can be a challenge.

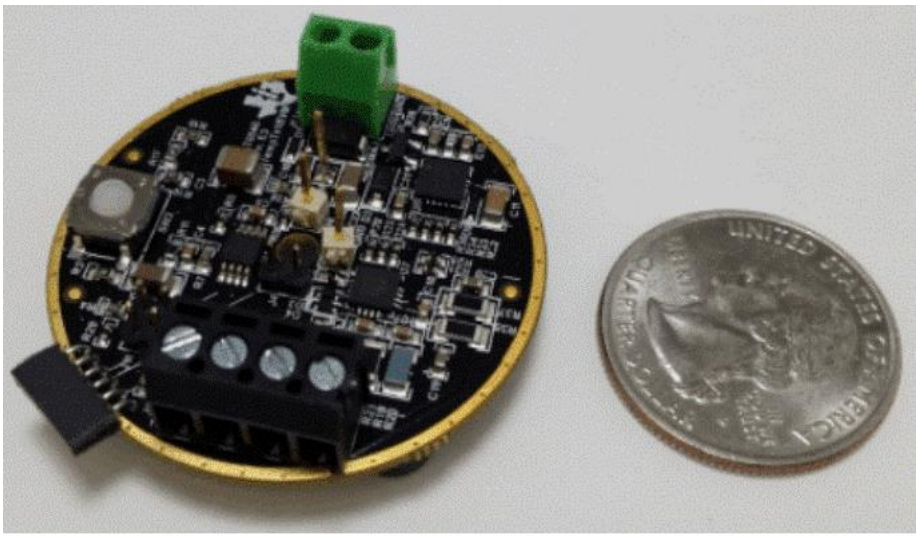

Figure 6. Temperature transmitter PCB compared to a quarter (TIDA-00095)

In these cases – and all PCB layouts, for that matter – ensure that you always use proper supply decoupling. There are two main classifications of decoupling capacitors: bulk and local. Bulk decoupling capacitors are generally placed directly at the output of the supply source. These capacitors help filter the supply output and hold the voltage steady as the load current fluctuates. In addition, most active components will require at least one local decoupling capacitor directly next to each of the main supply pins.

Local capacitors are generally an order of magnitude smaller compared to bulk capacitors and are used to provide the instantaneous current demands from the device while filtering out higher-frequency noise. If more than one decoupling capacitor is recommended for a given supply pin – for example, 0.01 µF in parallel with 1 µF – place the smaller capacitor closest to the supply pin.

Additionally, in part 11 we discussed that certain active components such as clocks can introduce large transients onto a power supply. You can suppress this noise by using additional decoupling components such as a series ferrite bead.

Figure 7 shows a portion of the ADS127L01 EVM schematic with some extra decoupling components used by the ADC and clock fanout buffer supplies. This fanout buffer must be referenced to the same digital input/output level as the ADS127L01 digital core (DVDD), which may allow switching transients to couple onto this supply. To maintain system performance, the EVM uses capacitors and a ferrite to decouple DVDD from the fanout buffer output supply (VDDO).

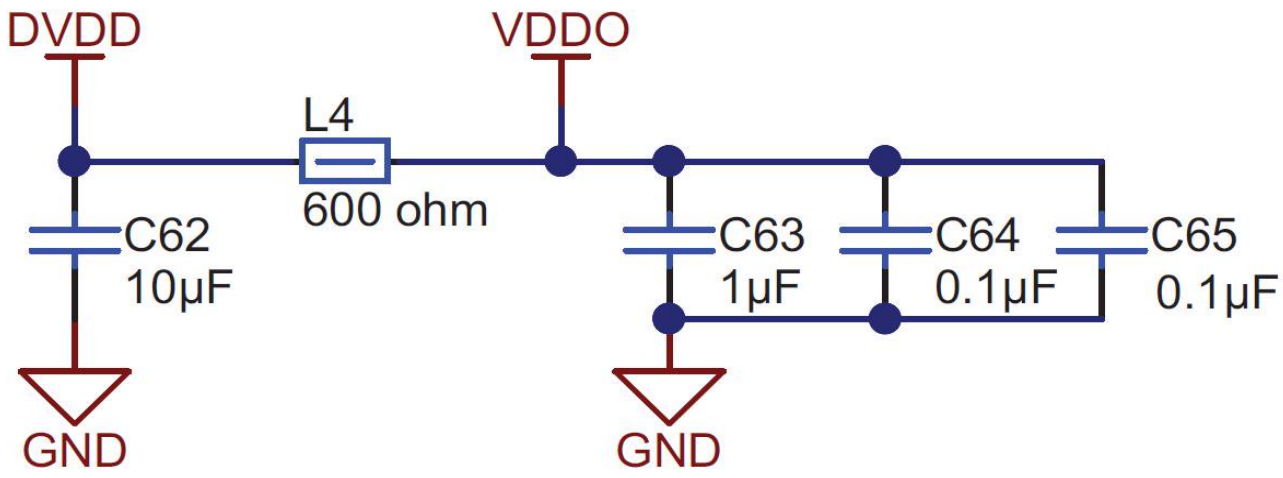

Figure 7. Decoupling components (capacitors and ferrite) for the ADC digital supply (DVDD) and clock buffer output supply (VDDO) on the ADS127L01EVM schematic

Coincidentally, we previously discussed the ADS127L01 EVM's clock fanout buffer – and its clocking circuits in general – in Part 10. In that article, we showed the EVM's clocking circuit and highlighted the fanout buffer in blue and the ADC in red. Figure 8 (left) shows this same image with those same highlights, although now we've also highlighted the decoupling components in yellow and the red arrow traces the DVDD supply path to the IOVDD supply.

The left side of Figure 8 calls out a test point at the IOVDD supply pins, while the right side shows an oscilloscope capture of the voltage at this point (Ch1). This screen capture demonstrates the large supply transients produced by the buffer due to each rising and falling edge of the output clock signal (Ch2) as seen across C65.

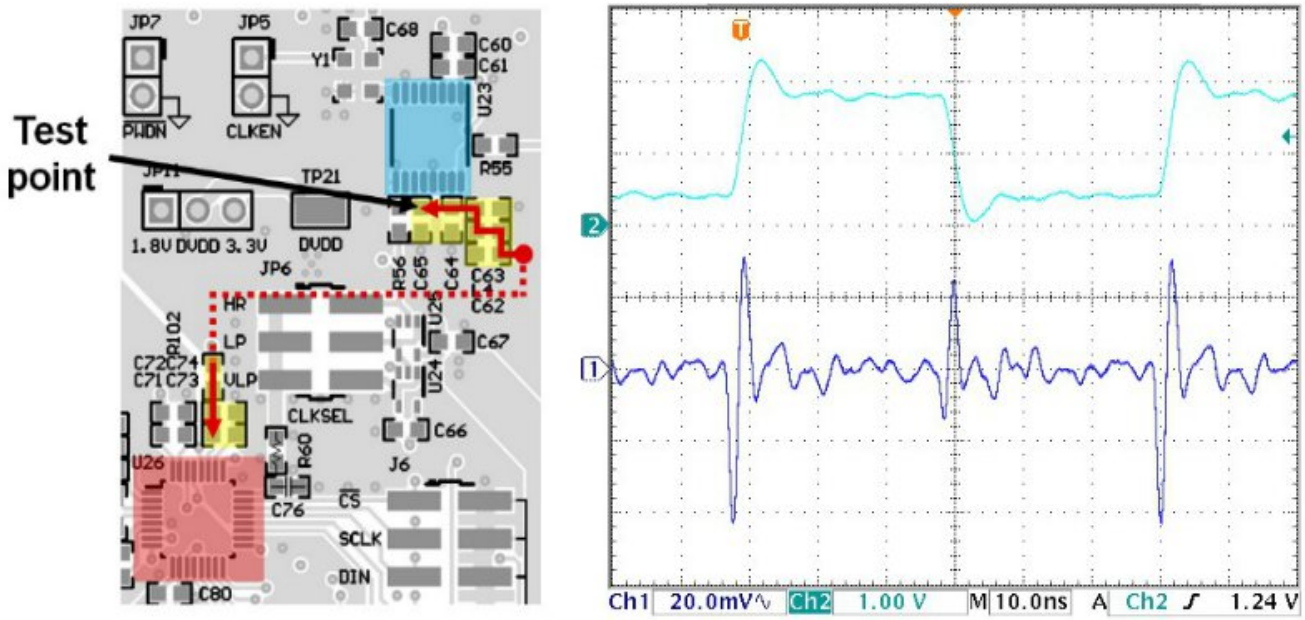

Figure 8. ADS127L01EVM schematic (left) and voltage measurements at buffer test point (right)

Without the decoupling circuit shown in Figure 7, the transients shown in the right side of Figure 8 would couple onto DVDD and affect the performance of the ADC, similar to the results seen in Figure 5. However, proper decoupling ensures that these glitches are contained to the output of the clock fanout buffer. This containment is evident by the right image in Figure 9 showing an oscilloscope capture at the test point (C73) called out in the left side of Figure 9. Note that the transients shown in Figure 8 are effectively removed from the oscilloscope capture in Figure 9, resulting in very little power-supply noise reaching the ADC.

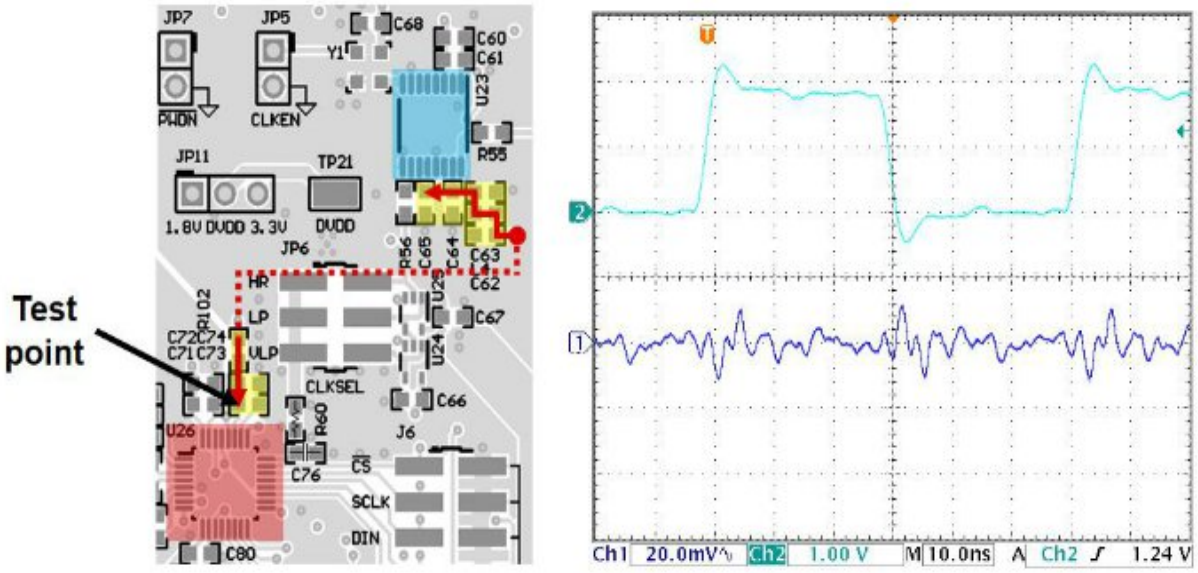

Figure 9. ADS127L01EVM schematic (left) and voltage measurements at ADC test point (right)

Routing is another layout technique you should consider to maintain low power-supply noise. You should always route the power traces from the source through the pads of the capacitors and then to the device pins whenever possible. Also, make the traces thicker for supplies that may carry higher amounts of current. And don't forget that ground is a supply too. Ground serves as the current return path for both signals and supplies. Using a large ground pour or plane with extra vias reduces the return path inductance and allows return currents to easily make their way back to the source. Figure 10 demonstrates some of these concepts.

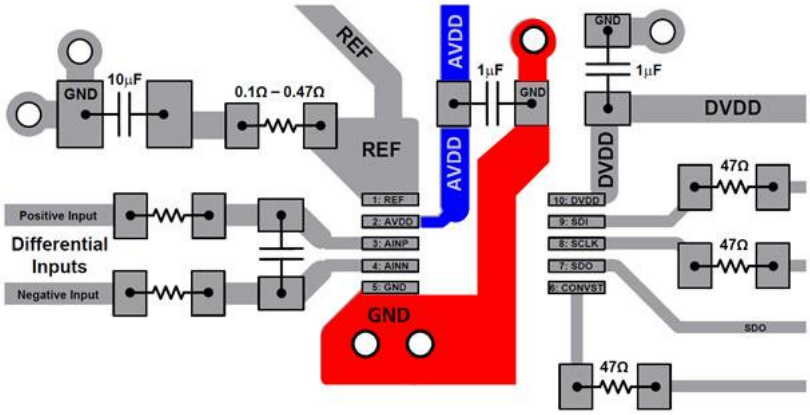

Figure 10. Routing techniques including thick traces and routing through capacitor pads

Frequency Planning

Another technique you can use to mitigate power-supply noise employs frequency planning, either for the switching regulator or your ADC. As discussed in part 11 and reiterated in Figure 1, ADCs can exhibit different

PSRR characteristics on each supply. Additionally, all ADC supplies will see a large boost in PSRR at frequencies that fall within the digital filter stop band (see Figure 1). In delta-sigma ADCs, the digital filter response repeats at multiples of the modulator frequency (fMOD). Therefore, switching noise may still alias into the ADC passband if this noise happens to fall near the modulator frequency or any multiple thereof.

If possible, choose a switching frequency that falls into one of the nulls of the filter (typically at multiples of the output data rate) to keep these signals from aliasing and improve your system's PSR. Figure 11 illustrates the stopband for common ADC filter types: a wideband finite impulse response filter (left side of Figure 11) and a sinc filter (right side of Figure 11). Since the ADC data rate is typically fixed by the system requirements, the regions highlighted by the red arrows are the recommended bands for switching frequencies based on the digital filter response. If your data rate is flexible but your switching frequency is fixed, consider choosing your ADC's output data rate such that it creates a null at this frequency.

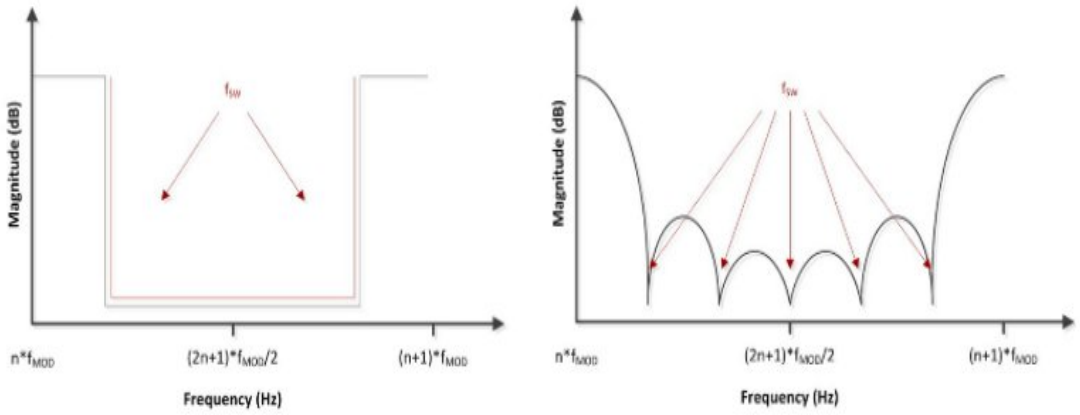

Figure 11. Recommended switching frequency bands using flat passband (left) and sinc (right) filters

Adding an LDO

As we discussed in the first section in this article, you can further improve your system's PSRR by adding an LDO to suppress unwanted noise. If you intend to use switching power supplies in your system, you should also consider the specific switching frequencies that will work best in your system. This technique can be used for all high-resolution ADC applications, though it is most important for wider bandwidth applications where noise is more likely to couple or alias into the output. In these cases, choose an LDO that has the most power-supply rejection for the switching frequency you plan to use. Or conversely, consider a switching frequency that fits within the highest portion of the PSRR curve for your LDO.

Figure 12 shows a PSRR versus frequency plot for the TI TPS7A49 LDO. Note that as the switching frequency increases, the PSRR of this LDO decreases.

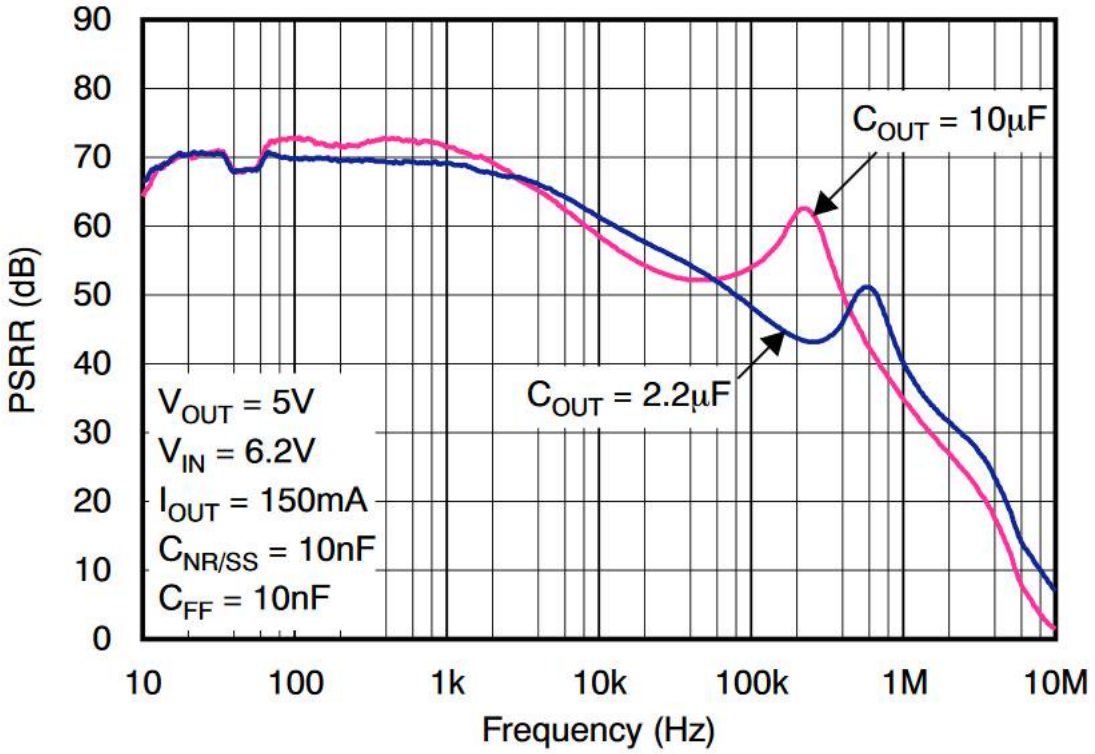

Figure 12. PSRR vs frequency plot for TPS7A49 LDO, C_{OUT} = 2.2µF

How to Prevent and Debug Power-Supply Issues

When reviewing an ADC's power-supply design, you can begin by verifying several parameters in order to rule out any potential issues and ensure first-pass success. Start by reviewing key power-supply specifications, such as the output current limits and the input/output voltage range of the components. Make sure to account for the total current consumption of all active components sharing the supply and that you budget for extra headroom.

Also, check the maximum capacitive load for the supply output, as all of the bulk and local decoupling capacitors on that supply are effectively in parallel and can add up quickly. Too much capacitance may produce slow startup times.

Finally, check that the LDO has at least the minimum dropout voltage between the input and the output and consider adding any other recommended noise-reduction (CNR) or feed-forward (CFF) capacitors for additional filtering, as shown in Figure 13.

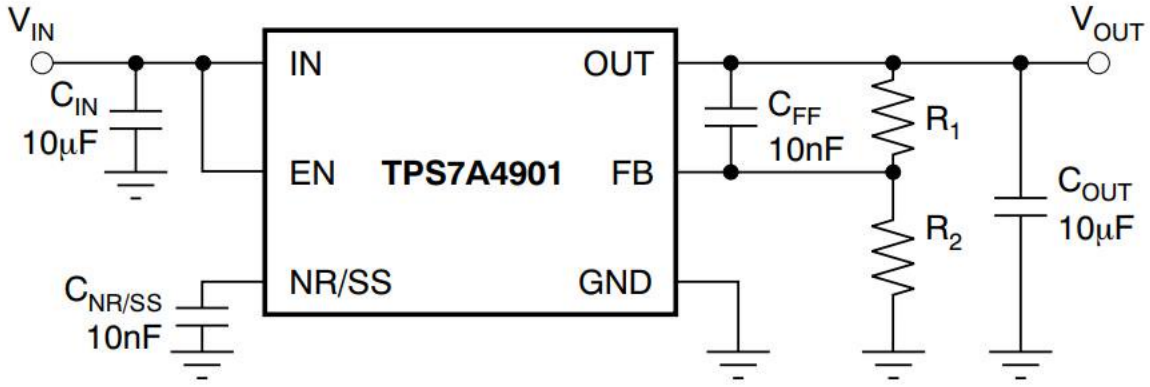

Figure 13. Filtering capacitors on an LDO

Once you've confirmed that your power supplies are configured properly, you can try to improve overall noise performance by increasing the size of ADC decoupling capacitors to provide additional filtering. This can be helpful not only on the main supply pins but also on any internal voltage nodes brought out to a dedicated pin for external decoupling. The ADC manufacturer can usually recommend capacitance values for those as well. Remember to place smaller capacitors closest to the device pins in parallel with larger capacitors for best performance.

Lastly, if you believe the supply conditioning components themselves are introducing one or more tones into the ADC spectrum, try replacing each of the ADC supplies with an external bench supply, one at a time. If this does not reveal the issue, you can also try replacing the main supply source for your board to determine where the noise is coming from.

And with that, we conclude TI's "Resolving the Signal" article series. We hope you enjoyed expanding your understanding of noise in analog signal-chain design. If you have suggestions for future topics or would like us to expand on any existing areas, please let us know.
