



LARSEN & TOUBRO EDUTECH

QUANTUM UNIVERSITY

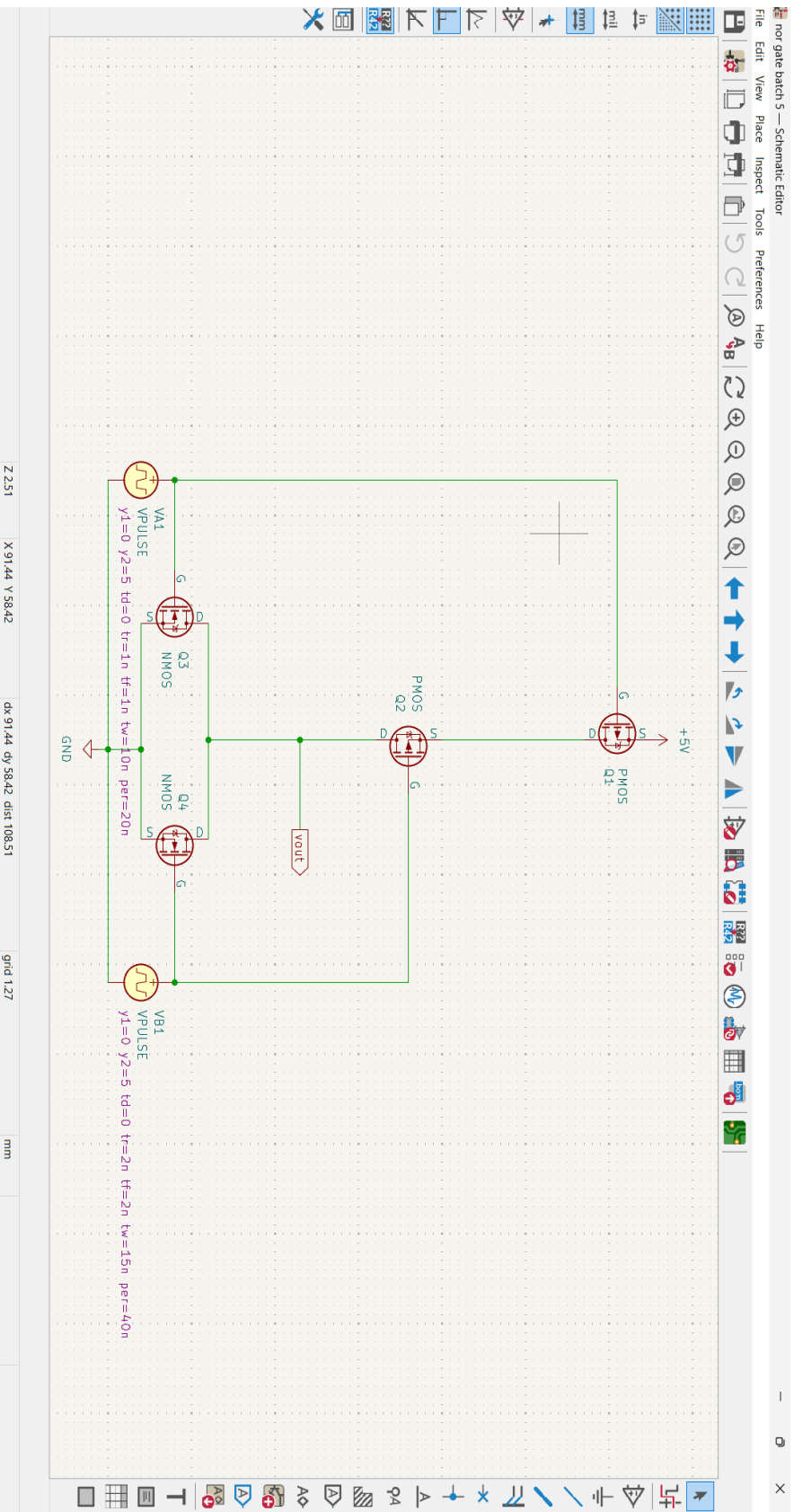
BATCH NO. 5

- **MD NUMAN RAZA**
- **MRINAL VISHWAKARMA**
- **AKSHAY KUMAR**
- **INDRONEEL KUMAR**

2nd MILESTONE OF PROJECT

Construct and simulate a NOR gate using MOS transistors, infer its behaviour, and explain its truth table with logical operation.

CIRCUIT:



SIMULATION VALUES:

TRAN — Transient Analysis ✕

SPICE Command

Plot Setup

Time step:

2n

seconds

Final time:

40n

seconds

Initial time:

0

seconds (optional; default 0)

Max time step:

800p

seconds (optional; default min{tstep, (tstop-tstart)/50})

☒ Use initial conditions

☒ Add full path for .include library directives

☒ Save all voltages

☒ Save all currents

☒ Save all power dissipations

☒ Save all digital event data

Compatibility mode:

PSpice and LTSpice ▾

OK

Cancel

SIMULATION WAVES:

