LARSEN & TOUBRO EDUTECH

QUANTUM UNIVERSITY

BATCH NO. 5

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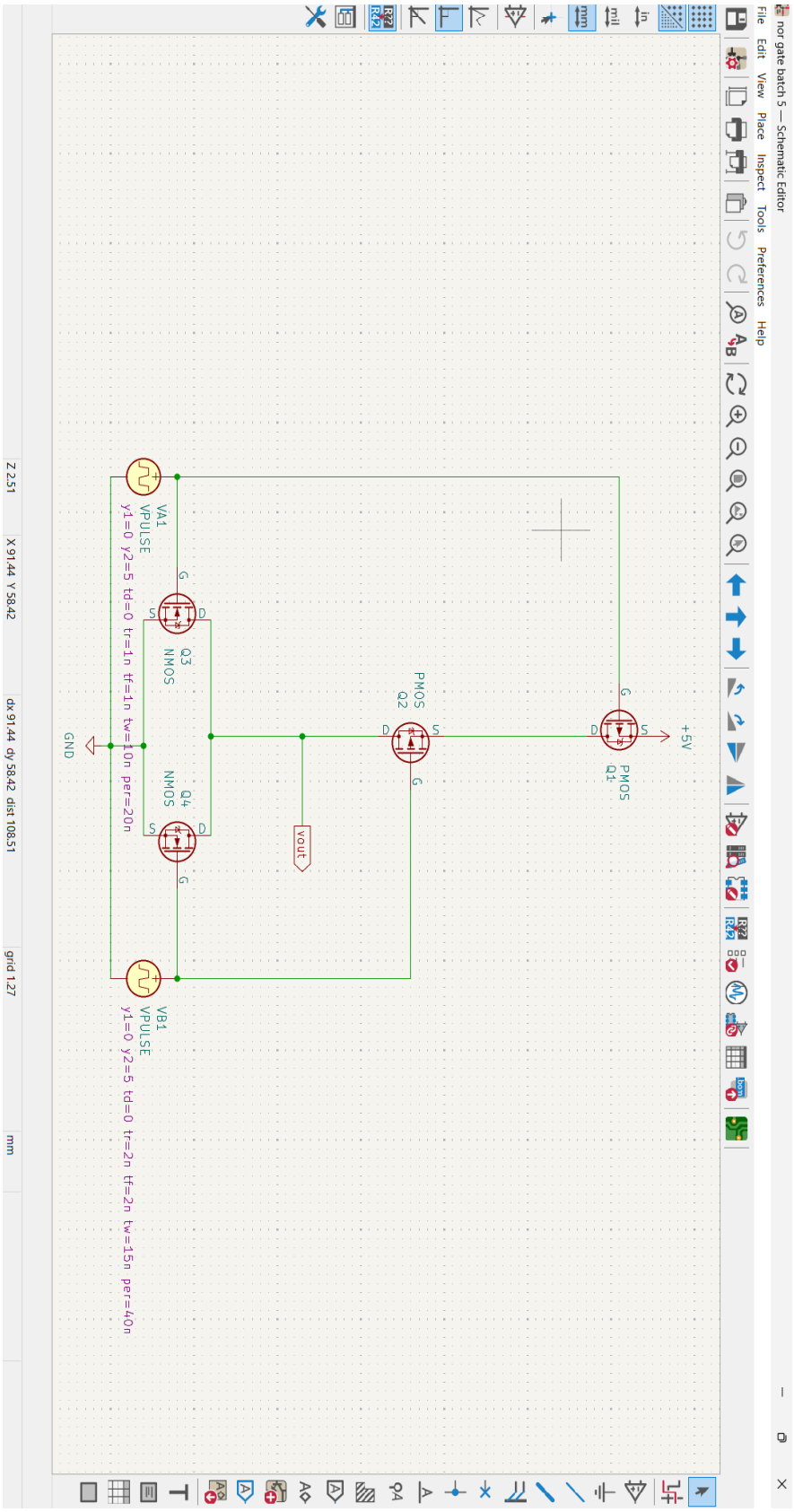
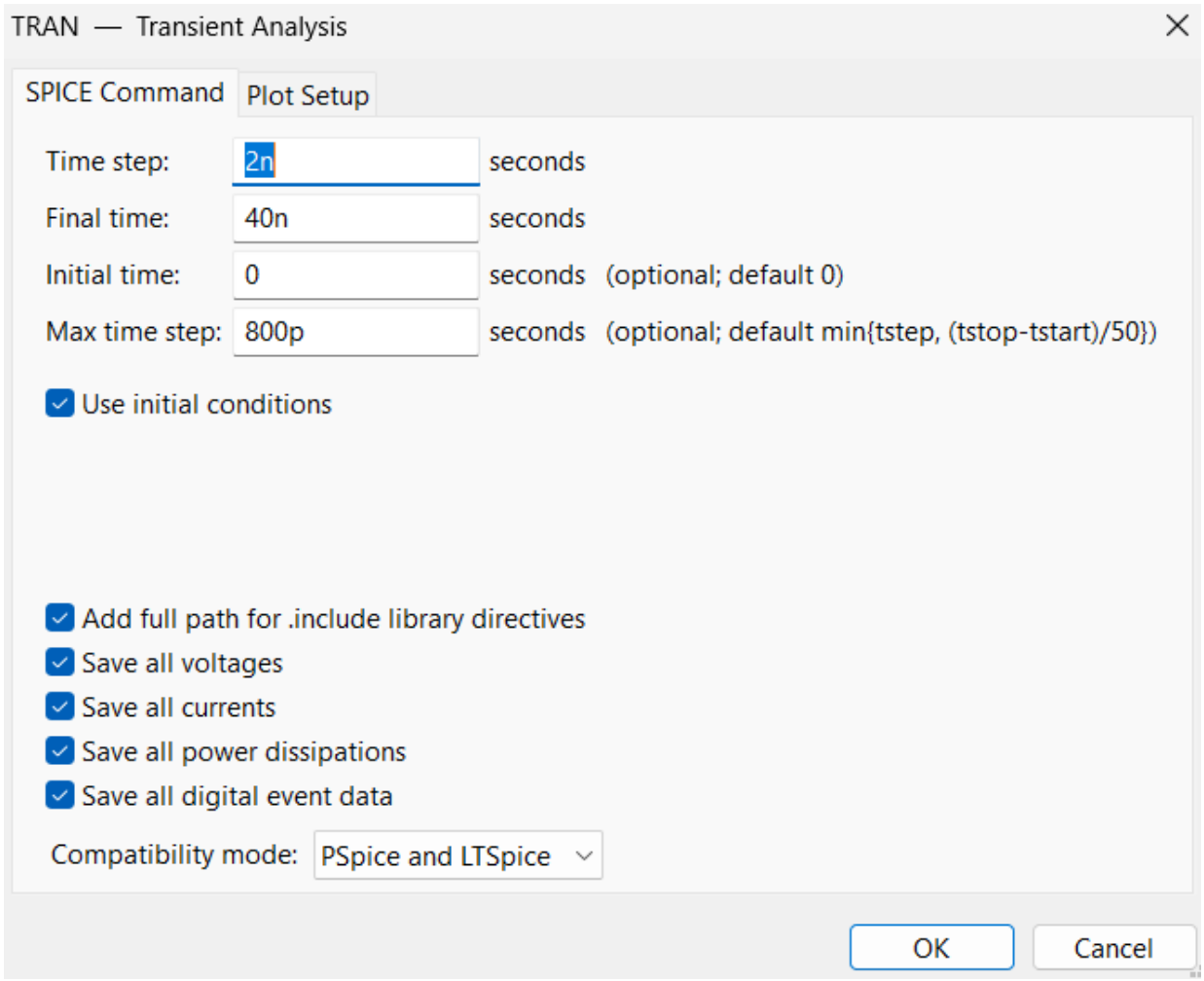
2nd MILESTONE OF PROJECT

Construct and simulate a NOR gate using MOS transistors, infer its behaviour, and explain its truth table with logical operation.

CIRCUIT:


nor gate batch 5 — Schematic Editor
File Edit View Place Inspect Tools Preferences Help
VA1
VPULSE
y1=0 y2=5 td=0 tr=1n tf=1n tw=10n per=20n
VB1
VPULSE
y1=0 y2=5 td=0 tr=2n tf=2n tw=15n per=40n
Q3
NMOS
Q4
NMOS
PMOS
Q2
PMOS
Q1
+5V
GND
Vout
Z 2.51
X 91.44 Y 58.42
dx 91.44 dy 58.42 dist 108.51
grid 1.27
mm

SIMULATION VALUES:



SIMULATION WAVES: