

2010

ELECTRONIC DEVICES

Full Marks - 100

Pass Marks - 35

Time - Three hours

The figures in the margin indicate full marks for the questions.

Answer any five questions.

1. ~~(a)~~ Write down the Fermi-Dirac distribution function. Explain the effect of doping and temperature variation on the Fermi level in a semiconductor. 10
- ~~(b)~~ Show that in an intrinsic semiconductor, ~~w~~ Fermi level is located at the middle of the forbidden band gap. 5

[Turn over

2

(c) In an n-type semiconductor, the Fermi level is 0.3 eV below the conduction level at the room temperature of 300K. If the temperature is increased to 360K, determine the new position of the Fermi level. 5

2. (a) Find the (i) conductivity and (ii) resistance of a bar of pure Silicon of length 1cm and cross-sectional area 1mm^2 at 300K. Given,

$$\mu_n = 0.13 \frac{\text{m}^2}{\text{VS}}, \quad \mu_p = 0.05 \frac{\text{m}^2}{\text{VS}}, \quad n_i = 1.5 \times 10^{16}/\text{m}^3$$

and $e = 1.6 \times 10^{-19}$ C. 6

- (b) Write the Einstein's equation. Find the diffusion coefficient of a particular carrier

mobility 1000 $\frac{\text{cm}^2}{\text{VS}}$ at 300K. 4

- (c) Define the term carrier mobility and state the mass action law. 5

- (d) What is the effective mass of a current carrier in a semiconductor? Is it same as the electronic mass in vacuum? 5

- (a) Derive the expression of built-in-potential for a uniformly doped p-n junction assuming abrupt junction approximation. 10

- (b) Explain the transition and diffusion capacitance of a junction diode. 6

- (c) The current flowing through a p-n junction Silicon diode is 60 mA for a forward bias of 0.9V at 300K. Determine the static and dynamic resistances of the diode. 4

4. ~~A*~~ (a) With the help of proper diagram, explain the operation of a full-wave bridge rectifier circuit.

A diode with the forward resistance of 50 Ohm supplies power to a load resistance of 1200 Ohm from a 20V source. Calculate the (i) d.c load current and (ii) a.c load current.

5+5=10

- ~~A*~~ (b) With the help of proper diagram, explain the operation of a clamper circuit. 5

- ~~A*~~ (c) A 12V, 0.36W Zener diode operates at a minimum diod current of 2 mA with the series resistance $R=100$ Ohm and $R_L = 1000$ Ohm. Determine the limit between which the supply voltage V can vary without the loss of regulation in the Zener voltage regulator circuit. 5

3

- ✓ 5. (a) A p-n-p transistor is biased in the active region. Indicate the various electron and hole current component crossing each junction and entering (or leaving) the base terminal.

8

- (b) For the transistor amplifier shown in Fig. 1, $V_{CC} = 12V$, $R_1 = 8\text{ k}\Omega$, $R_2 = 4\text{ k}\Omega$, $R_C = 1\text{ k}\Omega$, $R_E = 1\text{ k}\Omega$ and $R_L = 1.5\text{ k}\Omega$. Assume $V_{BE} = 0.7V$ and $\beta_E \approx \beta_C$.
- (i) Draw the d.c load line,
 - (ii) Determine the operating point and
 - (iii) Draw the a.c load line.

12

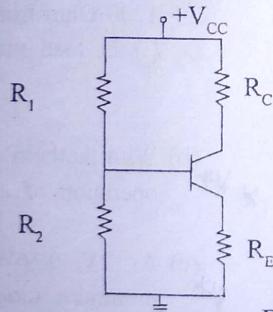


Figure-1

- ✓ 6. (a) Draw the small-signal low-frequency hybrid model for a transistor in common base mode.

5

- (b) "BJT is a current-controlled device." Explain.

3

- (c) What are the factors determining the choice of the Q-point? What are the factors that affect the bias stability of a transistor? What is thermal runaway?

12

7. (a) With the help of proper diagrams, explain the operation and output characteristics of an n-channel Enhancement MOSFET.

10

- (b) Define the FET parameters. Draw the a.c equivalent circuit of a FET.

6+4=10

8. Write in short on any four of the following:

4×5=20

- (a) Energy bands in crystals
- (b) Diffusion and drift current in a semiconductor
- (c) Zener breakdown and Avalanche breakdown
- (d) Varactor diode
- (e) Ebers-Moll model for a BJT
- (f) Hybrid- π model of BJT
- (g) Comparison between BJT and FET
- (h) Pinch-off voltage V_p and threshold voltage V_T in FET.

Total number of printed pages - 5

16(ET 3/4) ELDV

2011

ELECTRONIC DEVICES

Full Marks : 100

Pass Marks : 35

Time : Three hours

The figures in the margin indicate full marks for the questions.

Answer any five questions with all parts of each question at one place.

1 (a) What are the allowed and forbidden energy bands ? Draw and explain the energy-band diagram for the valance electrons of an isolated silicon atom. $4+6=10$

(b) What is Fermi level ? Write the expression for the Fermi-Dirac distribution function and draw it for different temperatures for intrinsic semiconductor. Also, draw rough sketches of the Fermi-Dirac distribution function for the *n*-type and *p*-type semiconductors.

$2+2+2+4=10$

Contd.

5
 (a) If the effective masses of electron (m_n^*) and hole (m_p^*) are equal, show that the intrinsic Fermi level is exactly at the center of the bandgap. What happens to the Fermi level when $m_p^* > m_n^*$ and $m_p^* < m_n^*$? 4+1=5

(b) Show that for a semiconductor at thermal equilibrium, $n_0 p_0 = n_i^2$. The meanings of the symbols are: n_0 is the thermal equilibrium electron concentration in the conduction band, p_0 is the thermal equilibrium hole concentration in the valance band and n_i is the electron concentration in the intrinsic semiconductor. 5

(c) Differentiate between drift and diffusion currents. 5

(d) Calculate the resistivity of a silicon specimen doped with 10^{16} donors/cm³ at 300K. The sample is 2.54 cm long and has a cross section of 2mm x 2mm. Also, find the resistance of the specimen when the contacts are placed at the ends of the long dimension.

Given, electron mobility = 1200 $\frac{cm^2}{V \cdot sec}$ at 300K.

$$3+2=5$$

16(ET 364) ELDV

2

$$\sigma = \mu n$$

3. (a) Describe the working of a uniformly doped p-n junction with supporting diagrams. 7

(b) Obtain an expression for the barrier potential for the junction. 7

(c) Write in brief about the biasing of p-n junction and draw the diode characteristic. 6

4. (a) How is the load line of a diode circuit obtained? What is the Q-point? 5

(b) In a full-wave rectifier the load resistance is $2K\Omega$. Each diode has idealized characteristic having slope corresponding to a resistance of 400Ω . If the applied voltage to each diode is $240 \sin 50t$, find (i) peak value of the current, (ii) d.c. value of the current, (iii) r.m.s. value of the current, (iv) rectifier efficiency and (v) ripple factor. 10

(c) Explain the mechanism of current flow in a p-n-p or n-p-n transistor with a proper figure showing the current components. 5

16(ET 364) ELDV

$$V_{DD}$$

$$E_F - E_F + E_F + E_{Contd.}$$

Total No. of printed pages = 4

16 (ET 364) ELDV

2012 C

ELECTRONIC DEVICES

Full Marks - 100

Pass Marks - 35

Time - Three hours

The figures in the margin indicate full marks
for the questions.

Answer question No.1 and any *four* from the rest.

1. Answer all questions. Each question carries equal marks. 20

- (a) What is drift current ?
- (b) What is junction capacitance ?
- (c) Name the hybrid parameters of a BJT.
- (d) Write about the mechanisms of breakdown in a PN junction diode.
- (e) Discuss the behaviour of PN junction diode under forward and reverse bias condition.

[Turn over

- (f) Draw the basic circuit diagrams of the CE and CC configurations of BJT.
- (g) State the advantages of JFET over BJT.
- (h) What is operating point? Why is it necessary to stabilize operating point of a transistor?
- (i) Define junction capacitance. Name the different types of capacitances diode posses.
- (j) Write the equation relating α and β for BJT.
2. (i) Name various types of diodes and write their characteristics in brief. What are uses of diodes? 10
- (ii) Explain the formation of the depletion region in PN junction diode with derivation of the depletion width. 10
3. (i) Define breakdown in a diode. Explain avalanche and zener breakdown. Draw the V-I characteristics for both. 10
- (ii) Find the voltage at which the reverse current in a germanium PN junction diode attains a value of 90% of its saturation value at room temperature. 5
- (iii) Determine the forward resistance of a PN junction diode, when the forward current is 5 mA at $T = 300^\circ \text{ K}$. Assume silicon diode. 5
4. (i) Define h-parameters. For CE amplifiers using h-parameters, derive expression for
 (a) Voltage gain
 (b) Current gain
 (c) Input resistance
 (d) Output resistance of. 10
- (ii) Define stability factor. Explain with circuit diagram of potential divider method of biasing in amplifiers. 10
5. (i) Show that a full wave rectifier is twice as efficient as half wave rectifier. 10
- (ii) In a full wave rectifier, the voltage applied to each diode is $240 \sin 377t$, the load resistance is $2 \text{ k}\Omega$ and each diode has a forward resistance of 400Ω . Determine the peak value of current, dc value of current, r.m.s value of current, rectifier efficiency and ripple factor. 10

21/16 (ET 364) ELDV (2)

21/16 (ET 364) ELDV (3)

[Turn over

6. (i) Draw the circuit diagram of NPN transistor in CE configuration and describe the static input and output characteristics. Also define active saturation and cut-off regions. 12
- (ii) The reverse leakage current of a transistor when connected in CB configuration is $0.2\mu A$ and it is $18\mu A$ when the same transistor is connected in CE configuration. Calculate α and β of the transistor. 8
7. (i) Describe the operation of depletion type MOSFET with labelled diagram. 10
- (ii) Draw the volt ampere characteristics of a JFET and explain about each of the regions of operations of the same with relevant equations. 10
8. Write short notes on any two of the following :
10+10=20
- (i) The MOS capacitor
 - (ii) Drift and diffusion current
 - (iii) Hall effect
 - (iv) Eber-Molls model.

Total No. of printed pages = 4

16 (ET 364) ELDV

2012

ELECTRONIC DEVICES

Full Marks – 100

Pass Marks – 35

Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer any five questions.

- ✓ (a) Draw and explain the VI characteristics of p-n junction diode. Define Peak Inverse voltage of a diode.
- (b) List out some diode applications.
- (c) Define drift current and diffusion current.
- (d) What are the current components of diode?
- (e) Differentiate between static and dynamic resistance of diode.

6+2+4+4+4=20

[Turn over

2. (a) With neat diagram, explain the formation of PN junction and derive its depletion width.
(b) Write detailed notes on variation of semiconductor parameters with temperature.

$$12+8=20$$

3. (a) What is Fermi level? With neat diagrams, discuss about the Fermi levels in p-type and n-type semiconductors.
(b) Show that Fermi level lies at the centre of the forbidden-energy band in an intrinsic semiconductor.
(c) In an n-type semiconductor, the Fermi level is at 0.3 below the conduction level at the room temperature (300K). If the temperature is increased to 360K, determine the new position of the Fermi level. $8+6+6=20$

4. (a) Draw the circuit diagram of a full-wave rectifier.
(i) with centre tap connection, and
(ii) with bridge connection

Also explain their operations.

21/16 (ET364) ELDV (2)

- (b) A half-wave rectifier, having a resistive load of 1000Ω , rectifies an alternating voltage of 325 V peak value. The diode has a forward resistance of 100Ω . Calculate (i) peak, average and rms values of current (ii) d.c. power output (iii) ac input power, and (iv) efficiency of the rectifier. $12+8=20$

5. (a) Explain the criteria for deciding the operating point of a transistor.
(b) List out the various types of biasing methods for transistor.
(c) An n-p-n transistor is used in CE configuration with $V_{cc} = 10$ V and $R_c = 2 \text{ k}\Omega$ (R_c is the resistance in the collector circuit). The bias is obtained by connecting a $100 \text{ k}\Omega$ resistor from the collector to the base. Find the Q point assuming that $\beta = 50$. $10+4+6=20$

6. (a) Distinguish between JFET and MOSFET.
(b) Explain the operation of depletion-type MOSFET with neat diagram. Compare it with the operation of enhancement-type MOSFET. $6+14=20$

21/16 (ET364) ELDV (3)

[Turn over]

7. Write short notes on any of *two* topics from the following list : $2 \times 10 = 20$

- (a) Diffusion capacitance of a p-n diode.
- (b) "Bond" model of silicon charge carriers in semiconductors.
- (c) Avalanche breakdown and Zener breakdown.
- (d) Asymmetrically doped junction.

8. Write short notes on any of the *two* topics from the following list : $2 \times 10 = 20$

- (a) Ebers-Moll model.
- (b) Hybrid- π model for transistor.
- (c) Field effect transistor
- (d) Input and output characteristics of CE transistor amplifier.

Total number of printed pages-4

16 (ET 364) ELDV

2013C

ELECTRONIC DEVICES

Paper : ET 364

Full Marks : 100

Pass Marks : 35

Time : Three hours

*The figures in the margin indicate full marks
for the questions.*

Answer any Ten questions.

1. What is meant by Fermi level in semiconductor ?
Show that in an intrinsic semiconductor Fermi level is located at the middle of the forbidden energy gap. 3+7=10

2. a) What do you mean by Graded semiconductor ? Is this an intrinsic or extrinsic semiconductor ? 2+2=4

Contd

- b) Draw the energy level diagram of
- I. Intrinsic semiconductor
 - II. P-type semiconductor
 - III. N-type semiconductor
- 2+2+2=6
3. How is PN junction formed? Described the passage of current through a PN junction. 10
4. What do you mean by Contact potential? What is the relation between contact potential and work function? 5+5=10
5. Explain the terms drift and diffusion currents. Derive an expression for them. 10
6. With a neat circuit diagram explain the working principle of a bridge rectifier. Does the output contain a perfect DC? Calculate the rectifier efficiency and ripple factor for full wave rectifier. 6+2+2=10
7. A full wave rectifier circuit is fed from a transformer whose secondary is centre-tapped with a line-to-line voltage of 60v (rms). assuming the total resistance of the diode and half of the transformer secondary winding to be 10 ohms and load resistance to be 1kohm, determine
- D.C current through load
 - D.C load voltage
 - A.C ripple voltage across load
 - Ripple frequency
 - PIV across each diode.
- 10
8. What is biasing of a transistor? List the various types of biasing methods and explain in detail about each scheme. 1+9=10
9. Explain the operation of enhancement mode and depletion mode MOSFET with neat diagram. 5+5=10
10. What is the difference between BJT and JFET? Also distinguish between JFET and MOSFET. 5+5=10

11. What do you mean by early effect and punch through effect ? Explain. 10

12. What do you mean by baried layer ? Is this used full in the construction for transfer of resistance ?

$$5+5=10$$

13. Write short notes on *any two* of the following :

$$5 \times 2 = 10$$

- a) Excess carriers in semiconductor
- b) Avalanche breakdown and Zener breakdown
- c) Capacitance of p-n junction
- d) Ebers-Moll model.

2013

ELECTRONIC DEVICES

Paper : ET 364

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

Answer any ten questions.

1. What is meant by Fermi level in semiconductor ?
Show that in an intrinsic semiconductor Fermi level is located at the middle of the forbidden energy gap. 3+7=10
2. a) What do you mean by Graded semiconductor ? Is this an intrinsic or extrinsic semiconductor ? 2+2=4

Contd.

- b) Draw the energy level diagram of
 ✓ I. Intrinsic semiconductor
 II. P-type semiconductor
 III. N-type semiconductor 2+2+2=6

3. What do you mean by Contact potential ? What is the relation between contact potential and work function ? How is PN junction formed ? Describe the passage of current through a PN junction.
 2+2+3+3=10

4. Explain the terms drift and diffusion currents. Derive an expression for them. 10

5. Explain how Zener diode acts as a Voltage Regulator. 10

6. Sketch neatly the circuit diagram of a CE configuration transistor, discuss its operation, characteristics and compare it with the other modes of operation. 10

- ✓ 7. Explain the principle of operation of a Full wave rectifier. Calculate the rectifier efficiency and ripple factor for full wave rectifier 6+2+2=10

8. A full wave rectifier circuit is fed from a transformer whose secondary is centre-tapped. A line-to-line voltage of 60v (rms). Assuming total resistance of the diode and half of the transformer secondary winding to be 10 ohm and load resistance to be 1kohm, determine

- a) D.C current through load $\frac{0.053}{10.94}$
 b) D.C load voltage
 c) A.C ripple voltage across load
 d) Ripple frequency
 e) PIV across each diode. 10

9. Derive the Hybrid model for a CE Amplifier. 10

10. Use of transistor as a switch. Early effect in BJT. 5+5=10

11. Explain why transistor action cannot be achieved by connecting two back to back diodes. What is the difference between BJT and JFET ? 5+5=10

12 Draw the structure of *n*-channel JFET and MOSFET and explain their *V-I* characteristics of MOSFET.

10

13. Explain the operation of enhancement mode and depletion mode MOSFET with neat diagram.

5+5=10

14. What do you mean by early effect and punch through effect ? Explain.

10

15. What do you mean by baried layer ? Is this used full in the construction for transfer of resistance ?

5+5=10

16. Write short notes on *any two* of the following :

5×2=10

- a) Excess carriers in semiconductor
- b) Avalanche breakdown and Zener breakdown
- c) Capacitance of *p-n* junction
- d) Ebers-Moll model.

2014

Electronic Devices

Full marks : 100

Pass marks : 35

Time : 3 hours

Answer question No 1 and any nine from the rest.

Answer the following questions briefly :

 $5 \times 2 = 10$

- (i) How a PN junction can be formed ?
- (ii) Define drift and diffusion current ?
- (iii) Draw and explain the VI characteristics of PN junction diode .
- (iv) What is operating point ? Why is it necessary to stabilize operating point of a transistor ?
- (v) State the advantages of JFET over BJT .

2. What is meant by Fermi Level in semiconductor ? Show that in an intrinsic semiconductor Fermi level is located at the middle of the forbidden energy gap . $3 + 7 = 10$

3. (i) Explain the variation of semiconductor parameters with temperature . 5
 (ii) What is doping ? Why is it necessary to dope a semiconductor ? 5

4. Explain the formation of the depletion region in PN junction diode with derivation of the depletion width . 10

5. What do you mean by Contact Potential ? What is the relation between contact potential and work function ? 10

6. Define breakdown in a diode . Explain avalanche and zener breakdown . Draw the V-I characteristics for both . 10

7. Show that a full wave rectifier is twice as efficient as half wave rectifier . 10

8. A full wave rectifier circuit is fed from a transformer whose secondary is centre-tapped with a line-to-line voltage of 60v (rms) . Assuming that the total resistance of the diode and half of the transformer secondary winding to be 10 ohms and load resistance is to be 1 kohm , determine :- $5 \times 2 = 10$

- (i) D.C current through load .
- (ii) D.C load voltage
- (iii) A.C ripple voltage across load
- (iv) Ripple frequency
- (v) PIV across each diode .

9. Draw the circuit diagram of NPN transistor in CE configuration and describe the static input and output characteristics . Also define the active saturation and cut-off regions . 10
10. What is biasing of a transistor and why is it necessary ? List the various types of biasing methods and explain any of the schemes in detail and also its stability factor . 10
11. Define h-parameters . For CE amplifiers using h-parameters , derive expression for $2 + 8 = 10$
- (i) Voltage gain
 - (ii) Current gain
 - (iii) Input resistance
 - (iv) Output resistance
12. (i) An npn transistor with $\beta=50$ is used in CE circuit having $V_{cc} = 12$ V and $R_c = 1 \text{ k}\Omega$. The bias is obtained by connecting $200 \text{ k}\Omega$ resistor from collector to base . Find the quiescent point. 5
- (ii) The reverse leakage current of a transistor in CB configuration is $0.1 \mu\text{A}$ and it is $15 \mu\text{A}$ when the same transistor is connected in CE configuration. Calculate α and β of the transistor. 5
13. Describe the operation of depletion type of MOSFET with labelled diagram . 10
14. Write short notes on (any two) $2 \times 5 = 10$
- (i) Early effect
 - (ii) Hall effect
 - (iii) Ebers-Moll model
 - (iv) Hybrid π model for transistor

2015 C

ELECTRONIC DEVICES

Full Marks : 100

Time : Three hours

***The figures in the margin indicate,
full marks for the questions.***

*Answer question No. 1 and any four
from the rest.*

1. Answer the following questions briefly :

$2 \times 10 = 20$

- i. Define diffusion constant of an electron and hole. Compute the value of diffusion length in a single crystal germanium having $100\mu\text{s}$ if the diffusion constant is $47\text{cm}^2/\text{sec}$.

Contd.

Total number of printed pages-4

17
16 (ET 364) ELDV

2015

ELECTRONIC DEVICES

Paper : ET-364

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

Answer any Ten (10) questions.

1. A. Why Si is the most popular semiconductor device, though Ge, GaAs are there? Justify your answer only in 4 points.
- B. What is meant by Fermi level in semiconductor? Show that in an intrinsic semiconductor Fermi level is located at the middle of the forbidden energy gap. 6
2. A. What do you mean by Graded semiconductor? 2

Contd.

- B. State the relation between ' α ' and ' β ' of a transistor. 2
- C. Draw the energy level diagram of
 - I. Intrinsic semiconductor
 - II. P-type semiconductor
 - III. N-type semiconductor
 2+2+2=6
3. A. If you didn't connect a voltage supply to a PN diode, what type of current will exit there? Justify your answer. 4
- B. A silicon diode has a saturation current of $7.5\mu A$ at room temperature $300^{\circ}K$. Calculate the saturation current at $400^{\circ}K$. 3
- C. Differentiate between zener breakdown and avalanche breakdown. 3
4. With a neat diagram explain the working of a PN junction diode in forward bias and reverse bias, and show the effect of temperature on its V-I characteristics. 10
5. A. Find the value of the PIV voltage of a half wave rectifier, full-wave rectifier, and a full wave rectifier circuit which is fed from a transformer whose secondary is center-tapped by drawing neat and clean diagrams. 5
- B. What do you mean by Ripple frequency? Ripple frequency is dependent on what parameters? Prove it mathematically. 5
- C. Explain the principle of operation of a Full wave rectifier. Calculate the rectifier efficiency and ripple factor for full wave rectifier. 6+2+2=10
- A full wave rectifier circuit is fed from a transformer whose secondary is centre-tapped with a line-to-line voltage of $60V$ (rms). Assuming the total resistance of the diode and half of the transformer secondary winding to be 10Ω and load resistance to be $1k\Omega$, determine
 - a) D.C current through load
 - b) D.C load voltage
 - c) A.C ripple voltage across load
 - d) Ripple frequency
 - e) PIV across each diode $2 \times 5 = 10$
8. Explain how Zener diode acts as a Voltage Regulator. 10
9. Sketch neatly the circuit diagram of a CE configuration transistor, discuss its operation, characteristics and compare it with the CC, CB modes of operation. 10

10. Derive the Hybrid model for a CE Amplifier.

10

11. Explain why transistor action cannot be achieved by connecting two back to back diodes. What is the difference between BJT and FET? $5+5=10$

12. Explain the operation of enhancement mode and depletion mode of NMOS with neat and clean diagrams. Depletion mode PMOS is possible or not? Justify your answer. $7+3=10$

13. What do you mean by early effect and pinch-off? Explain it with neat and clean diagrams.

10

14. What do you mean by barried layer? Is this used full in the construction for transfer of resistance? Justify your answer using neat and clean diagrams. $5+5=10$

15. Write short notes on **any two** of the following: $5\times 2=10$

- a) Excess carriers in semiconductor
- b) Capacitance of $p-n$ junction
- c) Ebers-Moll model
- d) CMOS
- e) Channel-length modulation.

Total number of printed pages-6

16 (ET 364) ELDV

2016

ELECTRONIC DEVICES

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

Answer **any ten** questions.

1. Show that Fermi level lies in the centre of the forbidden energy gap for an intrinsic semiconductor and shows their energy band diagram, density of states, Fermi-dirac distribution function and carrier concentration at thermal equilibrium.

$$5+5=10$$

Contd.

2. a) What do you mean by Graded semiconductor ? Is this an intrinsic or extrinsic semiconductor ? $2+2=4$

b) Draw the energy level diagram of PN diode in normal, forward and reverse biased conditions. $2+2+2=6$

3. Why concentration gradient exists in a semiconductor and what happens ? Write a relationship between concentration gradient and diffusion current density for both *p*-type and *n*-type semiconductor. Also find the conductivity of intrinsic silicon at 300k. If an acceptor impurity is added to the extent of 1 atom per 10^9 silicon atoms then find the new conductivity. $2+4+4=10$

4. Show by potential energy diagram when *p-n* junction is formed and they are separated. Explain with the help of a potential energy diagram when *p-n* junction is forward and reverse biased. $5+5=10$

5. Explain how Zener diode acts as a Voltage Regulator. 10

6. (a) Define the following parameters

- I. Bulk resistance
- II. Junction resistance
- III. Dynamic or ac resistance
- IV. Reverse dc resistance.

$$4 \times 1.5 = 6$$

(b) A silicon diode has a forward voltage drop of $1.2V$ for a forward dc current of 100 mA . It has a reverse current of $1\text{ }\mu\text{A}$ for a reverse voltage of $10V$. Calculate

- I. bulk and reverse resistance of the diode
- II. ac resistance at forward dc current of
 - (i) 2.5 mA and
 - (ii) 25 mA .

$$2+2=4$$

7. What a neat circuit diagram explain the working principle of a bridge rectifier? Does the output contain a perfect DC? Calculate the rectifier efficiency and ripple factor for full wave rectifier. 6+2+2=10

8. A full wave rectifier circuit is fed from a transformer whose secondary is centre-tapped with a line-to-line voltage of $60v$ (rms) assuming the total resistance of the diode and half of the transformer secondary winding to be 40 ohm and load resistance to be $4k\text{ ohm}$, determine $2\times 5=10$

a) D.C current through load

b) D.C load voltage

c) A.C ripple voltage across load

d) Ripple frequency

e) PIV across each diode.

9. Explain drift velocity. Derive an expression for drift current and current density in a good conductor. Find resistance, resistivity and conductivity relation in intrinsic semiconductor. [using usual notation]

2+4+4=10

10. Sketch neatly the circuit diagram of a CE configuration transistor, discuss its operation, characteristics and compare it with the CC, CB modes of operation. 10
11. Define h-parameters and derive the following two equations

$$V_1 = h_{11}i_1 + h_{12}V_2$$

$$I_2 = h_{21}i_1 + h_{22}V_2$$

Draw a hybrid π -model for a transistor in the CE configuration by identifying their parameters.

6+4=10

Total number of printed pages-4

16 (ET 364) ELD

2017 C

ELECTRONIC DEVICES

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

Answer any ten questions.

1. (a) Explain how a PN junction can be formed.
- (b) Define energy gap in semiconductor. How it varies with temperature ?
- (c) Define Fermi level. What is Fermi-Dirac distribution function ?
2. (a) What is Avalanche and Zener breakdown ? Differentiate the two breakdown mechanism in semiconductors.

2+2=

Cont

- (b)* Draw and explain the V-I characteristic of a *PN* junction diode. Explain about static and dynamic resistance in the graph. 3
- (c)* Discuss the behaviour of *PN* junction diode under forward and reverse bias condition. 3
3. Write down the Ebers-Moll equation for a *npn* transistor and draw a simple circuit model corresponding to these equations. 10
4. Show with neat diagram and describe how *P-N* junction diode can be used for rectifying ac waveform. 10
5. *(a)* Differentiate between drift and diffusion currents. 4
- (b)* What is recombination and carrier lifetime ? 2
- (c)* State and explain the mass action law. 2
- (d)* Write an expression for conductivity of a semiconductor. 2

6. (a) What do you mean by contact potential? What is the relation between contact potential and work function

2+3=

(b) Write about depletion layer and how the depletion region varies with biasing of a PN diode.

7. Explain with neat circuit diagram about how a Zener diode can be used as voltage regulator. 1

8. Write a detailed note on variation of semiconductor parameters with temperature.

9. (a) Explain the process of basic construction of depletion type MOSFET

(b) Why Enhancement type MOSFET is called?

10. (a) What do you mean by Early effect and Punch-through Effect? Explain.

(b) List down the differences between JFET and BJT.

11. (a) What is biasing of a BJT ? Explain the requirement for fixing bias point and stabilise it. 6

(b) List down various types of biasing methods normally used. PNP 4
PNP

12. Write short notes on **any two** of the following topics : 2×5=10

- (a) Hybrid π Model
- (b) Hall effect
- (c) Doping
- (d) MOS Capacitor
- (e) Volt equivalent temperature.