Date: 06/03/2024

DRC/DFM Check

DFM Summary (Bareboard):

Level: CRITICAL (6)
- Minimum Clearance: Plane to Drill: 3 violation(s)
- Minimum Annular Ring: Drill-Pad: 3 violation(s)

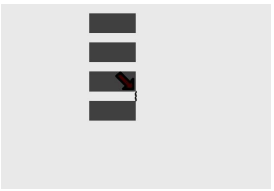
Level: ELEVATED (25)
- Silkscreen over Soldermask: 25 violation(s)

Level: MEDIUM (50)
- Minimum Clearance: Mask (Pad to Pad): 25 violation(s)
- Missing Mask Clearances: 25 violation(s)

Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 1

Clearance = 16.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

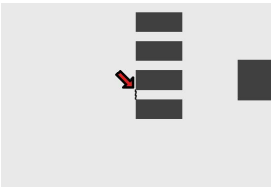
Location: 16.614, 14.263 (in.)
Layer: Sm0128.pho



Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 2

Clearance = 16.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 16.914, 14.263 (in.)
Layer: Sm0128.pho



Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 3

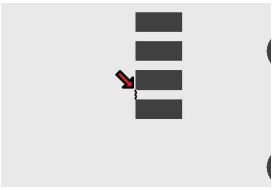
Clearance = 16.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 17.414, 14.263 (in.)
Layer: Sm0128.pho

Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 4

Clearance = 16.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 17.714, 14.263 (in.)
Layer: Sm0128.pho



Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 5

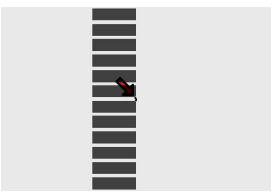
Clearance = 5.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 18.615, 14.264 (in.)
Layer: Sm0128.pho

Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 6

Clearance = 6.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

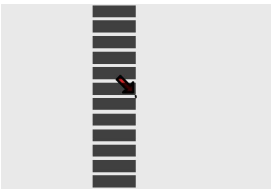
Location: 18.615, 14.238 (in.)
Layer: Sm0128.pho



Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 7

Clearance = 5.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

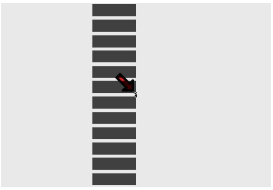
Location: 18.615, 14.213 (in.)
Layer: Sm0128.pho



Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 8

Clearance = 6.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

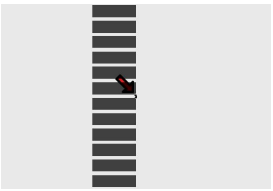
Location: 18.615, 14.187 (in.)
Layer: Sm0128.pho



Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 9

Clearance = 6.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 18.615, 14.161 (in.)
Layer: Sm0128.pho



Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 10

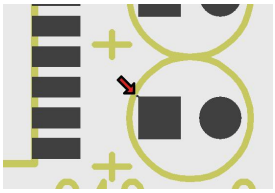
Clearance = 5.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 18.615, 14.136 (in.)
Layer: Sm0128.pho

Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 11

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

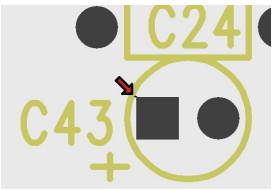
Location: 17.088, 14.324 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 12

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

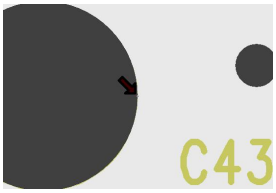
Location: 17.488, 13.024 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 13

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

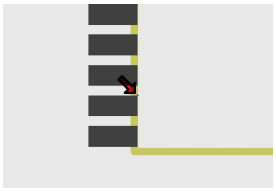
Location: 17.229, 13.088 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 14

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

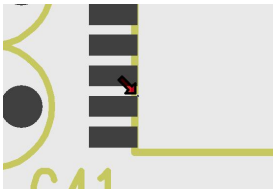
Location: 16.615, 14.305 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 15

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

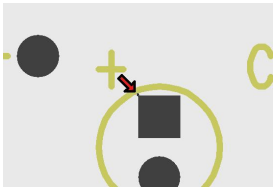
Location: 17.415, 14.305 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 16

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

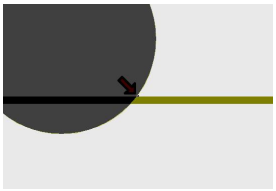
Location: 19.639, 13.674 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 17

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

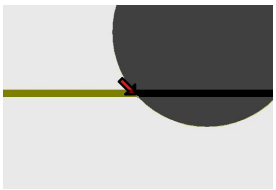
Location: 22.599, 12.844 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 18

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

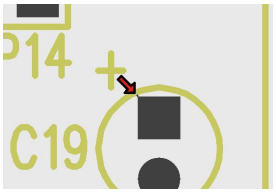
Location: 22.361, 12.832 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) — Violation #: 19

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

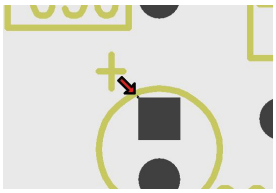
Location: 22.439, 13.374 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) — Violation #: 20

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

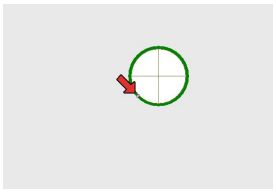
Location: 19.739, 15.674 (in.)
Layers: Sst0126.pho, Sm0128.pho



Minimum Clearance: Plane to Drill - (DFM Level: CRITICAL) — Violation #: 21

Clearance = 4.8 (mils), Minimum allowed 7.0 (mils).
This may cause registration problems or shorts during manufacturing.

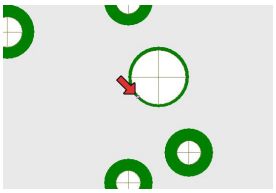
Location: 22.790, 13.230 (in.)
Layers: gnd2530.pho, Drill.drl
Attributes: NC Tool=5 Net=$Net00171



Minimum Clearance: Plane to Drill - (DFM Level: CRITICAL) — Violation #: 22

Clearance = 4.8 (mils), Minimum allowed 7.0 (mils).
This may cause registration problems or shorts during manufacturing.

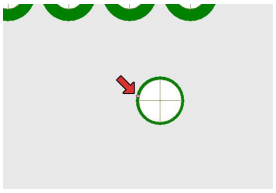
Location: 22.790, 15.430 (in.)
Layers: gnd2530.pho, Drill.drl
Attributes: NC Tool=5 Net=$Net00170



Minimum Clearance: Plane to Drill - (DFM Level: CRITICAL) — Violation #: 23

Clearance = 4.9 (mils), Minimum allowed 7.0 (mils).
This may cause registration problems or shorts during manufacturing.

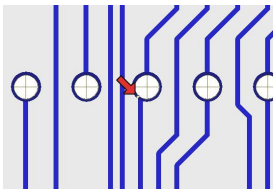
Location: 22.788, 17.671 (in.)
Layers: gnd2530.pho, Drill.drl
Attributes: NC Tool=7 Net=$Net00169



Minimum Annular Ring: Drill-Pad - (DFM Level: CRITICAL) — Violation #: 24

Ring Size = 4.8 (mils), Minimum allowed 5.0 (mils).
This may make plating on vias, as well as solderability
on component holes more difficult.

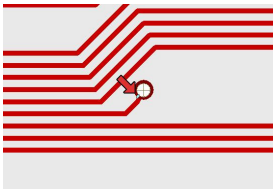
Location: 21.259, 14.721 (in.)
Layers: Art02.pho, Drill.drl
Attributes: NC Tool=2 Net=$Net00059 Net=$Net00059



Minimum Annular Ring: Drill-Pad - (DFM Level: CRITICAL) Violation #: 25

Ring Size = 4.8 (mils), Minimum allowed 5.0 (mils).
This may make plating on vias, as well as solderability on component holes more difficult.

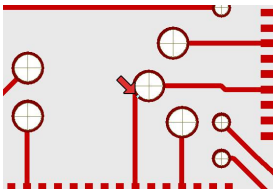
Location: 21.175, 15.118 (in.)
Layers: Art0121.pho, Drill.drl
Attributes: NC Tool=8 Net=$Net00026 Net=$Net00026



Minimum Annular Ring: Drill-Pad - (DFM Level: CRITICAL) Violation #: 26

Ring Size = 4.8 (mils), Minimum allowed 5.0 (mils).
This may make plating on vias, as well as solderability on component holes more difficult.

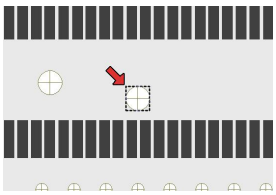
Location: 21.396, 15.971 (in.)
Layers: Art0121.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00008 Net=$Net00008



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 27

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

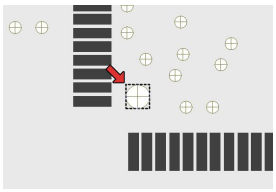
Location: 18.974, 14.628 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 28

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

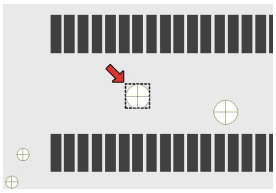
Location: 18.664, 14.878 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 29

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

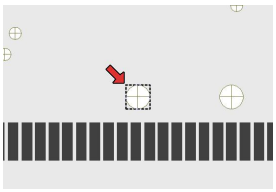
Location: 18.809, 14.658 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 30

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

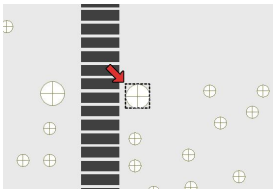
Location: 19.069, 14.858 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 31

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

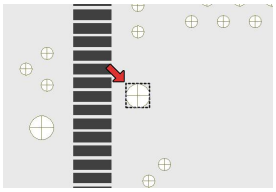
Location: 18.649, 15.128 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 32

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

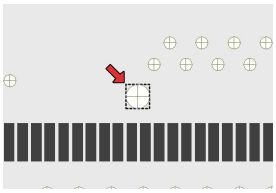
Location: 18.664, 14.278 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00000



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 33

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

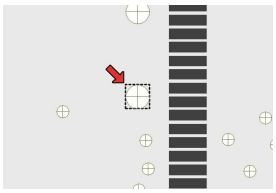
Location: 18.974, 15.538 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 34

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

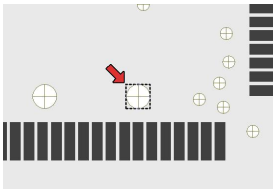
Location: 19.394, 15.058 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00000



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 35

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

Location: 19.244, 14.858 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 36

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

Location: 19.394, 15.218 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001