Date: 08/18/2024

DRC/DFM Check

DFM Summary (Bareboard):

Level: CRITICAL (7)
- Minimum Annular Ring: Drill-Pad: 4 violation(s)
- Minimum Clearance: Plane to Drill: 3 violation(s)

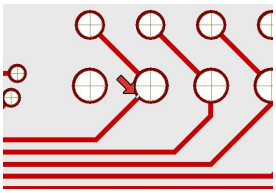
Level: ELEVATED (50)
- Silkscreen over Soldermask: 25 violation(s)
- Mask Slivers: 25 violation(s)

Level: MEDIUM (50)
- Missing Mask Clearances: 25 violation(s)
- Minimum Clearance: Mask (Pad to Pad): 25 violation(s)

Minimum Annular Ring: Drill-Pad - (DFM Level: CRITICAL) Violation #: 1

Ring Size = 4.8 (mils), Minimum allowed 5.0 (mils).
This may make plating on vias, as well as solderability
on component holes more difficult.

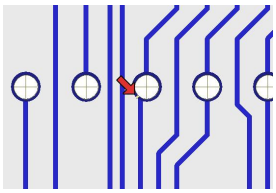
Location: 21.453, 13.520 (in.)
Layers: Art0121.pho, Drill.drl
Attributes: NC Tool=4 Net=$Net00173 Net=$Net00173



Minimum Annular Ring: Drill-Pad - (DFM Level: CRITICAL) Violation #: 2

Ring Size = 4.8 (mils), Minimum allowed 5.0 (mils).
This may make plating on vias, as well as solderability
on component holes more difficult.

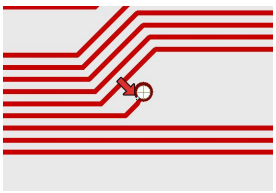
Location: 21.259, 14.721 (in.)
Layers: Art02.pho, Drill.drl
Attributes: NC Tool=2 Net=$Net00059 Net=$Net00059



Minimum Annular Ring: Drill-Pad - (DFM Level: CRITICAL) Violation #: 3

Ring Size = 4.8 (mils), Minimum allowed 5.0 (mils).
This may make plating on vias, as well as solderability
on component holes more difficult.

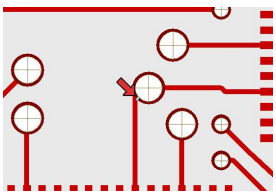
Location: 21.175, 15.118 (in.)
Layers: Art0121.pho, Drill.drl
Attributes: NC Tool=8 Net=$Net00026 Net=$Net00026



Minimum Annular Ring: Drill-Pad - (DFM Level: CRITICAL) Violation #: 4

Ring Size = 4.8 (mils), Minimum allowed 5.0 (mils).
This may make plating on vias, as well as solderability
on component holes more difficult.

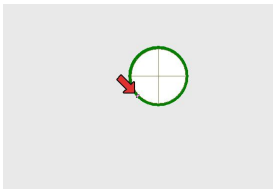
Location: 21.396, 15.971 (in.)
Layers: Art0121.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00008 Net=$Net00008



Minimum Clearance: Plane to Drill - (DFM Level: CRITICAL) Violation #: 5

Clearance = 4.8 (mils), Minimum allowed 7.0 (mils).
This may cause registration problems or shorts during manufacturing.

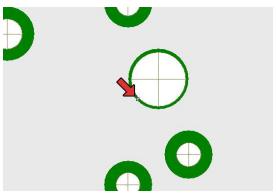
Location: 22.790, 13.230 (in.)
Layers: gnd2530.pho, Drill.drl
Attributes: NC Tool=5 Net=$Net00171



Minimum Clearance: Plane to Drill - (DFM Level: CRITICAL) Violation #: 6

Clearance = 4.8 (mils), Minimum allowed 7.0 (mils).
This may cause registration problems or shorts during manufacturing.

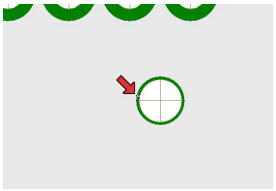
Location: 22.790, 15.430 (in.)
Layers: gnd2530.pho, Drill.drl
Attributes: NC Tool=5 Net=$Net00170



Minimum Clearance: Plane to Drill - (DFM Level: CRITICAL) Violation #: 7

Clearance = 4.9 (mils), Minimum allowed 7.0 (mils).
This may cause registration problems or shorts during manufacturing.

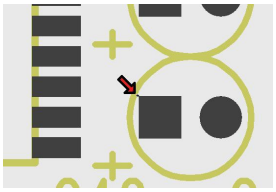
Location: 22.788, 17.671 (in.)
Layers: gnd2530.pho, Drill.drl
Attributes: NC Tool=7 Net=$Net00169



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 8

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

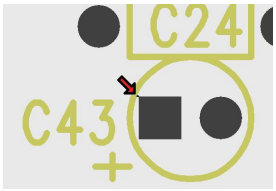
Location: 17.088, 14.324 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 9

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

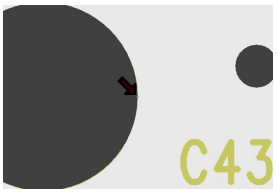
Location: 17.488, 13.024 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 10

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

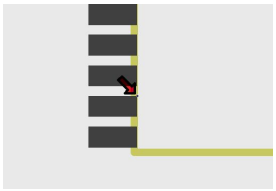
Location: 17.229, 13.088 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 11

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

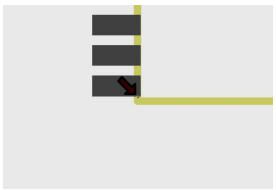
Location: 16.615, 14.305 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 12

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

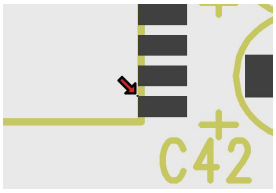
Location: 16.609, 14.220 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 13

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

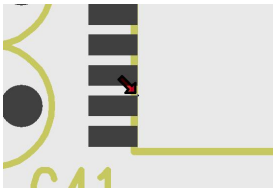
Location: 16.914, 14.255 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 14

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

Location: 17.415, 14.305 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 15

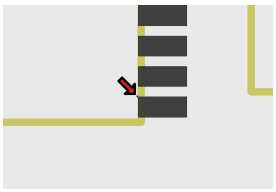
May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

Location: 17.409, 14.220 (in.)
Layers: Sst0126.pho, Sm0128.pho

Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 16

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

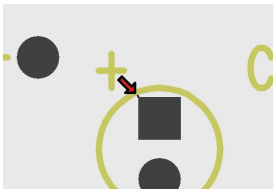
Location: 17.714, 14.255 (in.)
Layers: Sst0126.pho, Sm0128.pho



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 17

May make electrical testing and SMT soldering more difficult.
The silkscreen overlaps solder mask openings. Elevated Risk:
May cause contamination of the pads and make electrical testing
plus SMT soldering more difficult.

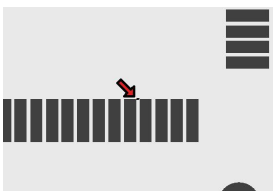
Location: 19.639, 13.674 (in.)
Layers: Sst0126.pho, Sm0128.pho



Mask Slivers - (DFM Level: ELEVATED) Violation #: 18

Clearance = 5.0 (mils), Minimum allowed 8.0 (mils).
Areas in the solder mask where the resist is so
narrow that it may cause small pieces of the resist
to flake off and present soldering problems later.
Critical: A board can fail if the resist falls
in an area that needs to be soldered later on.

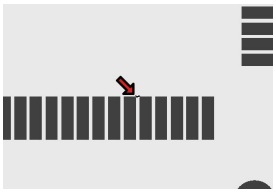
Location: 19.309, 13.910 (in.)
Layer: Sm0128.pho



Mask Slivers - (DFM Level: ELEVATED) Violation #: 19

Clearance = 6.0 (mils), Minimum allowed 8.0 (mils).
Areas in the solder mask where the resist is so
narrow that it may cause small pieces of the resist
to flake off and present soldering problems later.
Critical: A board can fail if the resist falls
in an area that needs to be soldered later on.

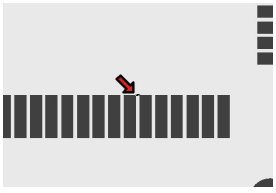
Location: 19.283, 13.910 (in.)
Layer: Sm0128.pho



Mask Slivers - (DFM Level: ELEVATED) Violation #: 20

Clearance = 6.0 (mils), Minimum allowed 8.0 (mils).
Areas in the solder mask where the resist is so
narrow that it may cause small pieces of the resist
to flake off and present soldering problems later.
Critical: A board can fail if the resist falls
in an area that needs to be soldered later on.

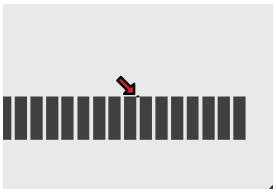
Location: 19.257, 13.910 (in.)
Layer: Sm0128.pho



Mask Slivers - (DFM Level: ELEVATED) Violation #: 21

Clearance = 5.0 (mils), Minimum allowed 8.0 (mils).
Areas in the solder mask where the resist is so
narrow that it may cause small pieces of the resist
to flake off and present soldering problems later.
Critical: A board can fail if the resist falls
in an area that needs to be soldered later on.

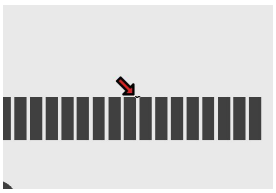
Location: 19.232, 13.910 (in.)
Layer: Sm0128.pho



Mask Slivers - (DFM Level: ELEVATED) Violation #: 22

Clearance = 6.0 (mils), Minimum allowed 8.0 (mils).
Areas in the solder mask where the resist is so
narrow that it may cause small pieces of the resist
to flake off and present soldering problems later.
Critical: A board can fail if the resist falls
in an area that needs to be soldered later on.

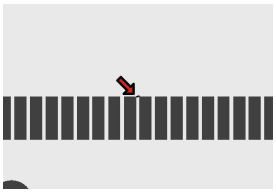
Location: 19.206, 13.910 (in.)
Layer: Sm0128.pho



Mask Slivers - (DFM Level: ELEVATED) Violation #: 23

Clearance = 5.0 (mils), Minimum allowed 8.0 (mils).
Areas in the solder mask where the resist is so
narrow that it may cause small pieces of the resist
to flake off and present soldering problems later.
Critical: A board can fail if the resist falls
in an area that needs to be soldered later on.

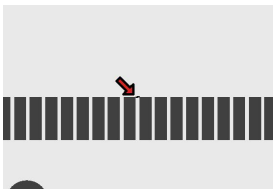
Location: 19.181, 13.910 (in.)
Layer: Sm0128.pho



Mask Slivers - (DFM Level: ELEVATED) Violation #: 24

Clearance = 6.0 (mils), Minimum allowed 8.0 (mils).
Areas in the solder mask where the resist is so
narrow that it may cause small pieces of the resist
to flake off and present soldering problems later.
Critical: A board can fail if the resist falls
in an area that needs to be soldered later on.

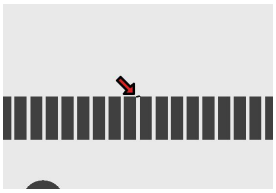
Location: 19.155, 13.910 (in.)
Layer: Sm0128.pho



Mask Slivers - (DFM Level: ELEVATED) Violation #: 25

Clearance = 6.0 (mils), Minimum allowed 8.0 (mils).
Areas in the solder mask where the resist is so
narrow that it may cause small pieces of the resist
to flake off and present soldering problems later.
Critical: A board can fail if the resist falls
in an area that needs to be soldered later on.

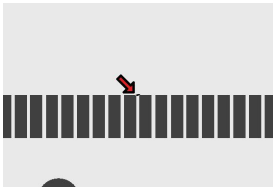
Location: 19.129, 13.910 (in.)
Layer: Sm0128.pho



Mask Slivers - (DFM Level: ELEVATED) Violation #: 26

Clearance = 5.0 (mils), Minimum allowed 8.0 (mils).
Areas in the solder mask where the resist is so
narrow that it may cause small pieces of the resist
to flake off and present soldering problems later.
Critical: A board can fail if the resist falls
in an area that needs to be soldered later on.

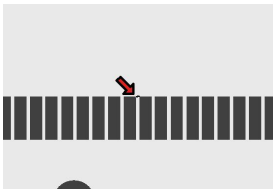
Location: 19.104, 13.910 (in.)
Layer: Sm0128.pho



Mask Slivers - (DFM Level: ELEVATED) Violation #: 27

Clearance = 6.0 (mils), Minimum allowed 8.0 (mils).
Areas in the solder mask where the resist is so
narrow that it may cause small pieces of the resist
to flake off and present soldering problems later.
Critical: A board can fail if the resist falls
in an area that needs to be soldered later on.

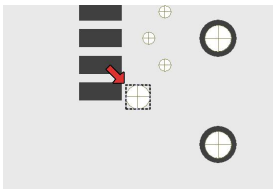
Location: 19.078, 13.910 (in.)
Layer: Sm0128.pho



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 28

May result in a short, as well as reduced corrosion
protection.
Exposes more copper than is necessary, and can result in
solder bridges forming accidentally between pins during assembly.

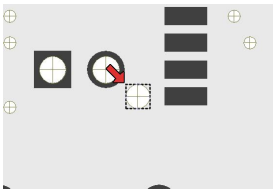
Location: 17.824, 14.228 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00000



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 29

May result in a short, as well as reduced corrosion
protection.
Exposes more copper than is necessary, and can result in
solder bridges forming accidentally between pins during assembly.

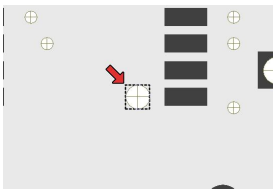
Location: 17.284, 14.238 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 30

May result in a short, as well as reduced corrosion
protection.
Exposes more copper than is necessary, and can result in
solder bridges forming accidentally between pins during assembly.

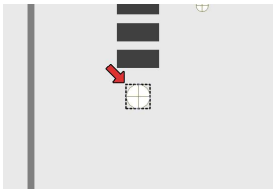
Location: 16.864, 14.238 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00000



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 31

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

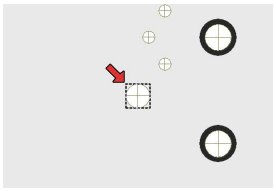
Location: 16.574, 14.168 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 32

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

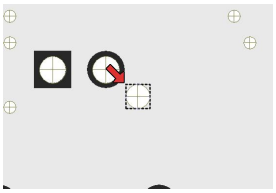
Location: 17.824, 14.228 (in.)
Layers: Sm0227.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00000



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 33

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

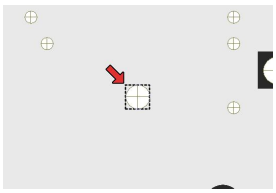
Location: 17.284, 14.238 (in.)
Layers: Sm0227.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 34

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

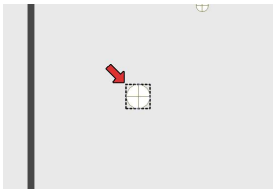
Location: 16.864, 14.238 (in.)
Layers: Sm0227.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00000



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 35

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

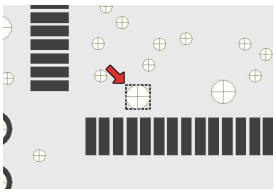
Location: 16.574, 14.168 (in.)
Layers: Sm0227.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 36

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

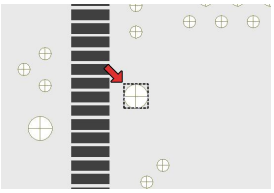
Location: 18.744, 13.948 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00001



Missing Mask Clearances - (DFM Level: MEDIUM) Violation #: 37

May result in a short, as well as reduced corrosion protection.
Exposes more copper than is necessary, and can result in solder bridges forming accidentally between pins during assembly.

Location: 18.664, 14.278 (in.)
Layers: Sm0128.pho, Drill.drl
Attributes: NC Tool=9 Net=$Net00000



Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 38

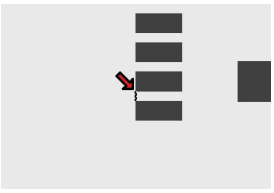
Clearance = 16.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 16.614, 14.263 (in.)
Layer: Sm0128.pho

Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 39

Clearance = 16.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 16.914, 14.263 (in.)
Layer: Sm0128.pho



Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 40

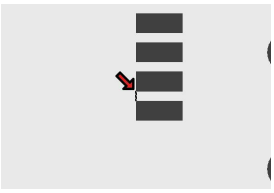
Clearance = 16.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 17.414, 14.263 (in.)
Layer: Sm0128.pho

Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 41

Clearance = 16.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

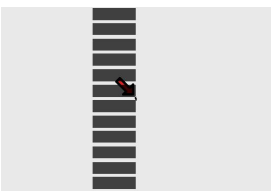
Location: 17.714, 14.263 (in.)
Layer: Sm0128.pho



Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 42

Clearance = 5.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 18.615, 14.264 (in.)
Layer: Sm0128.pho



Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 43

Clearance = 6.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 18.615, 14.238 (in.)
Layer: Sm0128.pho

Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 44

Clearance = 5.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 18.615, 14.213 (in.)
Layer: Sm0128.pho

Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 45

Clearance = 6.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 18.615, 14.187 (in.)
Layer: Sm0128.pho

Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 46

Clearance = 6.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 18.615, 14.161 (in.)
Layer: Sm0128.pho

Minimum Clearance: Mask (Pad to Pad) - (DFM Level: MEDIUM) Violation #: 47

Clearance = 5.0 (mils), Minimum allowed 28.0 (mils).
This may cause problems during pcb fabrication.

Location: 18.615, 14.136 (in.)
Layer: Sm0128.pho