DEPARTMENT OF COMPUTER ENGINEERING,

FACULTY OF ENGINEERING, UNIVERSITY OF JAFFNA

EC4010 – DIGITAL DESIGN

Assignment 3

Digital Circuit Design and Implementation

1. INSTRUCTIONS:

- It is required to design a calculator in Verilog which can do the following operations. There will be three/two members per group as in your laboratory grouping. Each member should be responsible for each operation (or pair of operations) if your group has less members, you may implement less operations. The student who designs Addition/ Subtraction should also design the 7-segment decoder.
  - Addition/ Subtraction (+, -)
  - Multiplication (×)
  - Integer division: Returns the quotient of a division
- It should be able to handle numbers ranging from +99 to -99.
  - Input can be positive or negative
  - If answer exceeds the range it should display as EE or -EE according to the situation.
- In addition, it should have functions like clear/reset.
- Your program should run on DE10-Lite board.
- As illustrated in Figure 1 the following components should be used for the respective tasks.
  - Three 7-segment displays for output (two displays for magnitude and one for sign)
  - Three 7-segment displays for input (two displays for magnitude and one for sign)
  - Ten switches to input numbers from 0 to 9 with respective switches (SW0 to SW9) or to input the operations (SW0-Addition, SW1-Subtraction, SW2-Multiplication, SW3-Integer division, SW4 to SW9 for other operations as required by your design)
  - KEY0 and KEY1 to assist input and to select mode (input mode/ operations mode/ sign of input/ clear result and so on)
  - LED to indicate operation

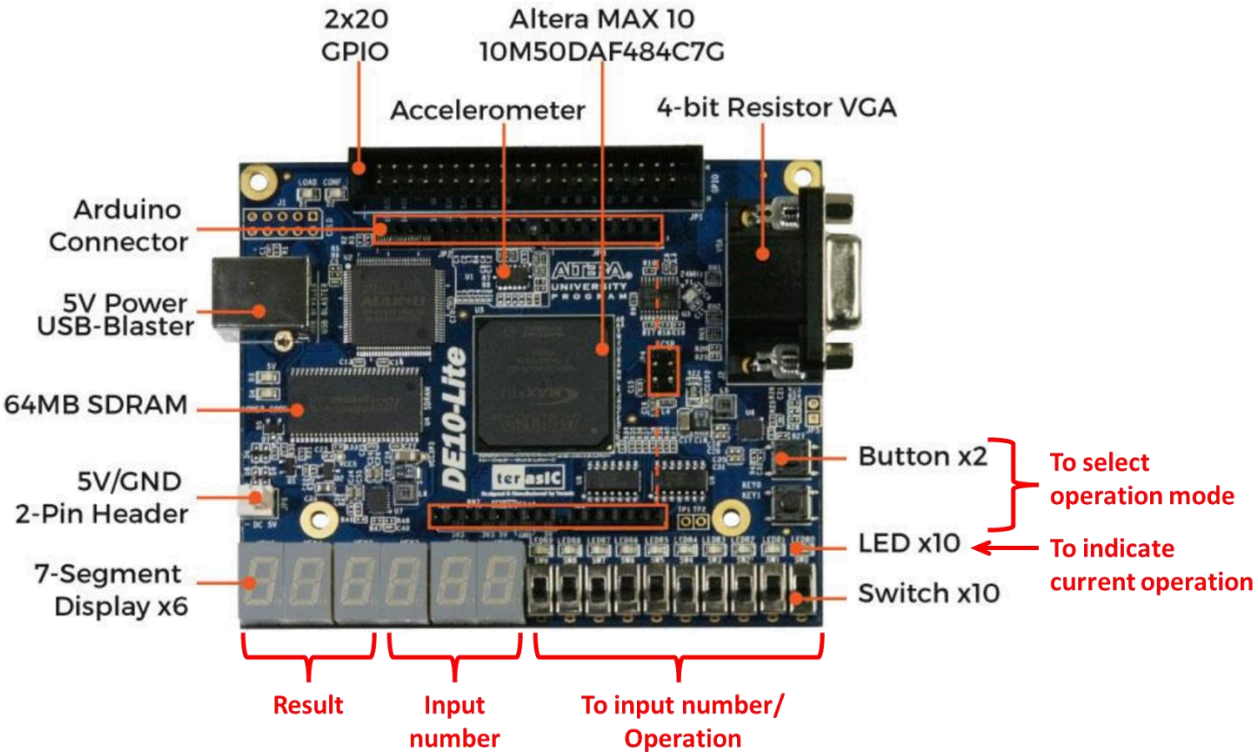

Figure 1: Component Allocation

2. LIMITATIONS:

- Simulations if any should be compatible with ModelSim - Intel FPGA Starter Edition Model Technology ModelSim - Intel FPGA Edition vsim 2020.1 (Quartus Prime 20.1)
- The final code should be in Verilog.
- It should be possible to simulate the block diagram in the Netlist Viewer in Quartus Prime 20.1
- The entire design should be made of preliminary gates (and, or, not, xor, xnor) and flip-flops
  - Do not use if conditions/ for loops/case statements for direct calculation (only exception is the flip-flop). (e.g.: Use of case statements for 7-segment decoder is not allowed)
  - Do not use any special operators (such as multiplication or division)
- You may create your design with modules made of preliminary gates (and, or, not, xor, xnor) and flip-flops alternatively.
- Each operation assigned to a student should be in separate modules (the operations may also be as sub-modules of a larger module)

3. REPORT:

- Standard A4 size document with borders as for laboratory reports.
- It should contain names of group members and their contribution
- Should contain **block diagrams of all modules**
  - Individual block diagrams for sub-modules
  - Larger modules will have a block diagram made of preliminary gates and flip-flops connected to smaller modules.
  - Modules should be clearly visible in 100% zoom

- Should contain **state diagrams**, **state tables** and **state equations** for all sequential elements.

4. SUBMISSION:

- Report
- Project file (with a readme text file (.txt) with instructions to run the project, specifying the software required and steps to run)
- All submissions should be made before the deadline; no additional change will be allowed afterwards.

5. MARKING CRITERIA:

- Marks will be awarded during a demonstration.
- Demonstration will be accompanied by a viva. Questions will be on the component the individual claims to work on as in the report. **If the student shows no basic understanding marks will be zero irrespective of satisfying any criteria in Table 1**.
- Marks will be awarded according to criteria in Table 1.

Table 1: Marking Criteria

No.	Criteria	Maximum possible Marks
01	Only simulation of individual components available	30
02	Only simulation of entire circuit	50
03	Design working on DE10-Lite	80
04	Design working on DE10-Lite with proper report and ability to explain how one's design works.	90

05	• Design working on DE10-Lite – 80
	  ○ **Note there is a 50% reduction in marks if a particular component is not implemented using basic logic (exception are applicable)**
	  ○ Input is in decimal – 10
	  ○ Output is decimal – 10
	  ○ Working operation(s) – 20
	  ○ Working in full range – 10
	  ○ "EE" shown for out-of-range operations – 10
	  ○ Sequential input – 10
	  ○ Operations implemented in parallel – 10
	• Proper report and ability to explain how one's design works - 10
	• The design is scalable (as justified by the student) - 5
	• Efficient use of components - 5
		100