# DIGITAL CIRCUIT DESIGN AND IMPLEMENTATION

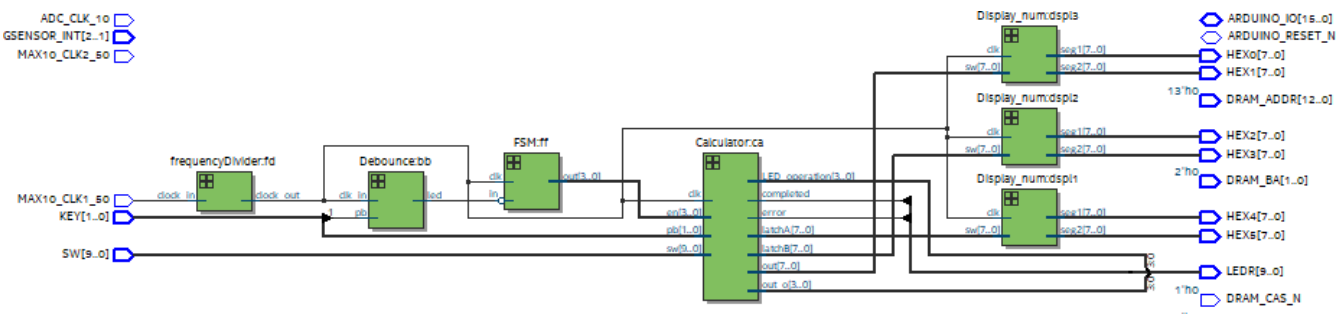
## CALCULATOR OPERATIONS:

- Addition
- Subtraction
- Multiplication
- Division

## DETAILS OF MODULES AND SUBMODULES

- Calculator
  - num_latch
    - D_latch
  - multiplier
    - One_Bit_Full_Adder
  - Full_Adder_Substractor
    - One_Bit_Full_Adder
  - Eight_Bit_Full_Adder
    - One_Bit_Full_Adder
  - Eight_bit_divider
    - Divide_module
      - One_Bit_Full_Substractor
      - Two_one_mux
  - four_one_mux
  - overflowDetector
  - debounce
    - d_ff
- Debounce
  - d_ff
- Display_num
  - BCD_7Segment
  - binary_to_BCD
    - add3
- frequencyDivider
- FSM
  - d_ff

## BLOCK DIAGRAM OF OVER ALL CALCULATOR SYSTEM



- ✓ **MODULE: DISPLAY_NUM**

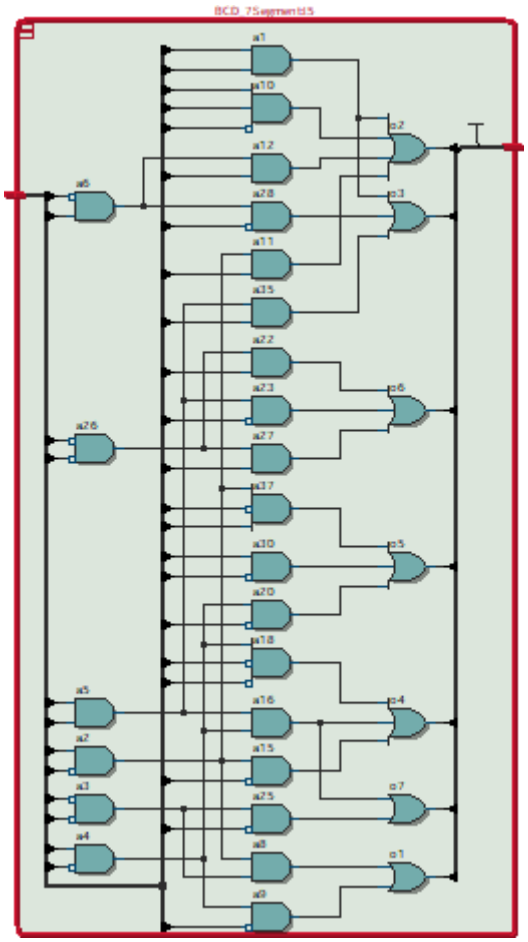
SUBMODULE: BCD_7SEGMENT

| D | C | B | A | a | b | c | d | e | f | g |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

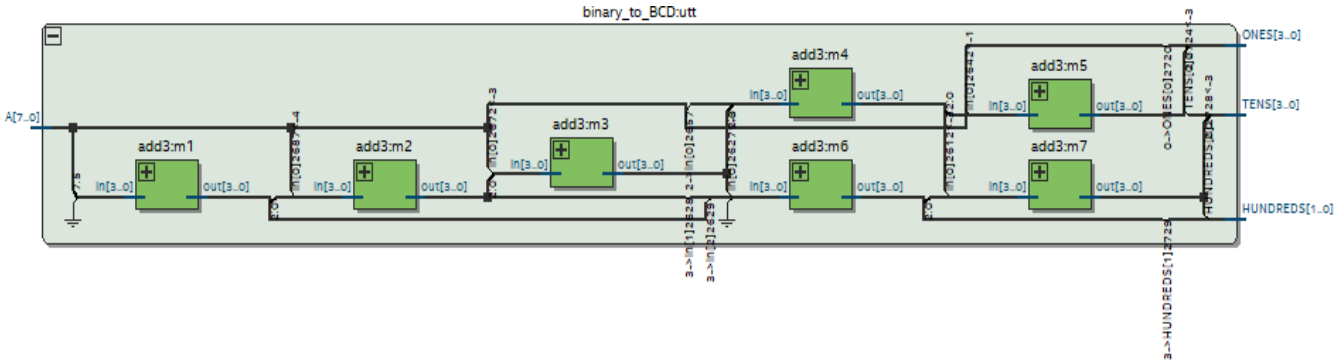
TABLE 01: TRUTH TABLE FOR 7 SEGMENT

| | |
|---|---|
| a | (A~B~C~D)+(~AC~D) |
| b | (CD)+(B~CD)+(A~BC)+(~ABC) |
| c | (CD)+(AD)+(~AB~C) |
| d | (A~B~C)+(ABC~D)+(~A~BC~D) |
| e | (A~D)+(~BC~D)+(A~B~CD) |
| f | (A~D~C)+(BA~D)+(B~D~C) |
| g | (~B~C~D)+(ABC~D) |

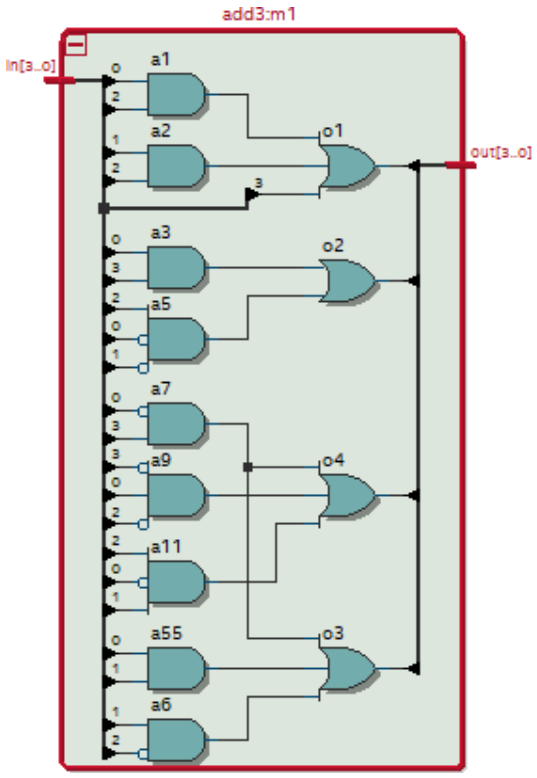
TABLE 02: BOOLEAN LOGIC EQUATIONS USING K'MAP



SUBMODULE: BINARY_TO_BCD



SUBMODULE: ADD3



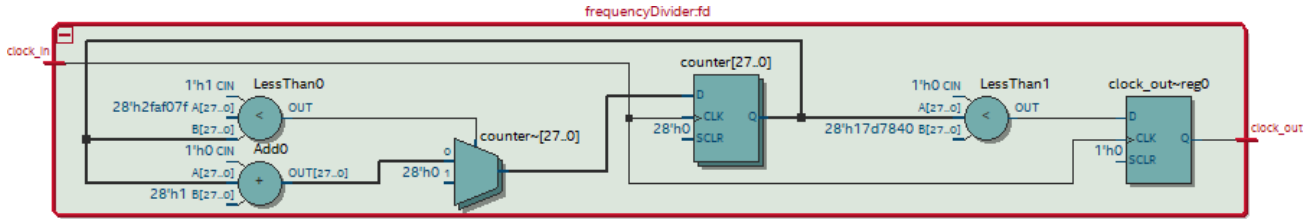

| D | C | B | A | OUT3 | OUT2 | OUT1 | OUT0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

TABLE 03: TRUTH TABLE FOR BINARY TO BCD

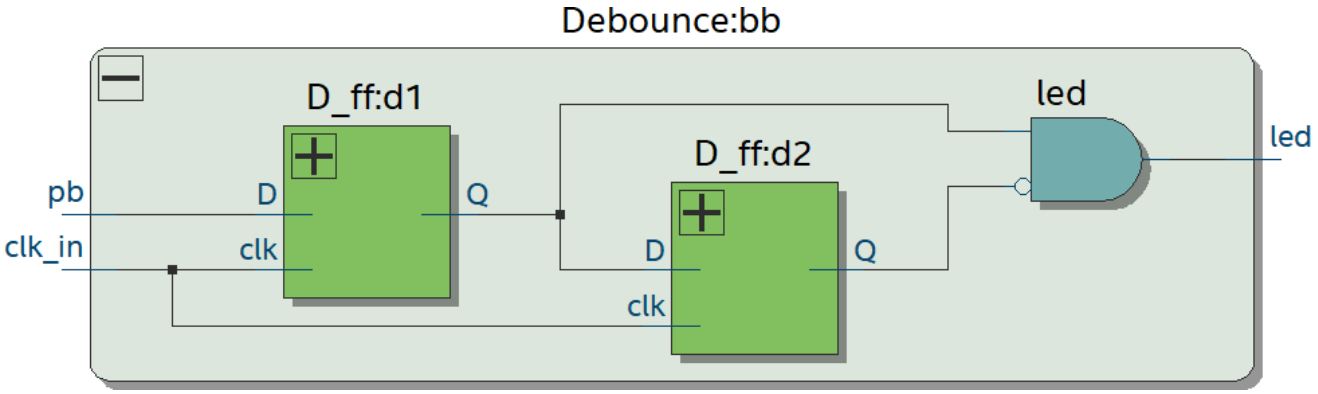
| | |
|---|---|
| OUT0 | (A~C~D)+(~ABC~D)+(~A~B~C~D) |
| OUT1 | (AB~D)+(B~C~D)+(~A~B~C~D) |
| OUT2 | (~A~BC~D)+(A~B~CD) |
| OUT3 | (~B~CD)+(AC~D)+(BC~D) |

TABLE 04: BOOLEAN LOGIC EQUATIONS USING K'MAP

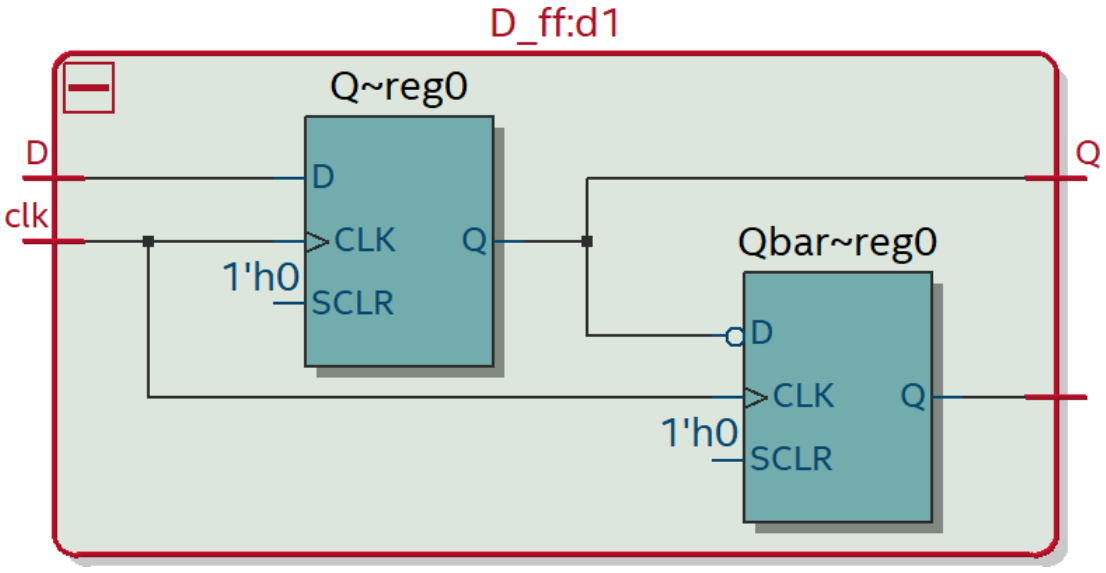
✓ **MODULE: FREQUENCY DIVIDER**




✓ **MODULE: DEBOUNCE**

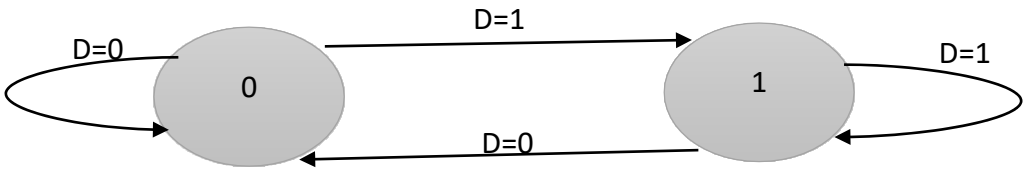



SUBMODULE: D_FF



| CLK | Q(t) | D | Q(t+1) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

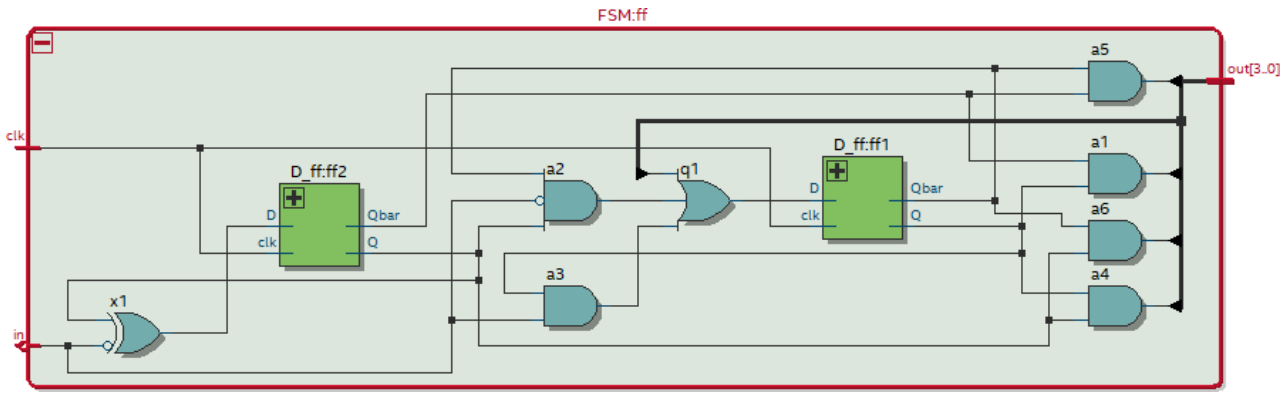
STATE TABLE




STATE DIAGRAM

STATE EQUATION: Q(t+1)=D

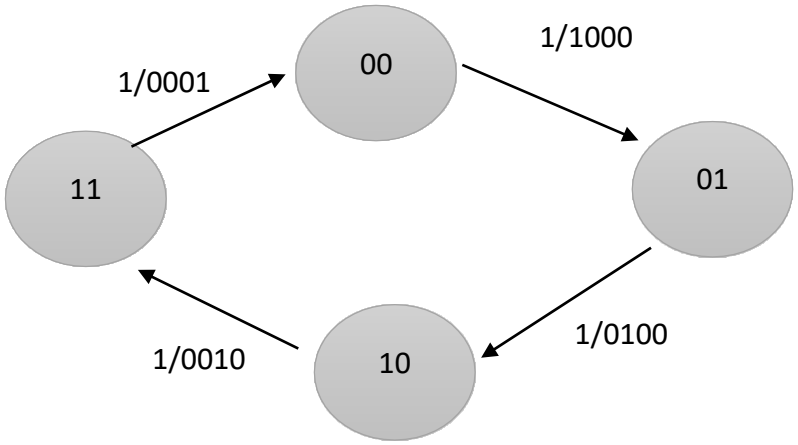
✓ **MODULE: FSM**



| | | |
|---|---|---|
| Input Mode | 00 | LED6 |
| Operation Mode | 01 | LED7 |
| Output Mode | 10 | LED8 |
| Reset Mode | 11 | LED9 |

| A(t) | B(t) | Key0 | A(t+1) | B(t+1) | Y0 | Y1 | Y2 | Y3 | dA | dB |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

STATE TABLE



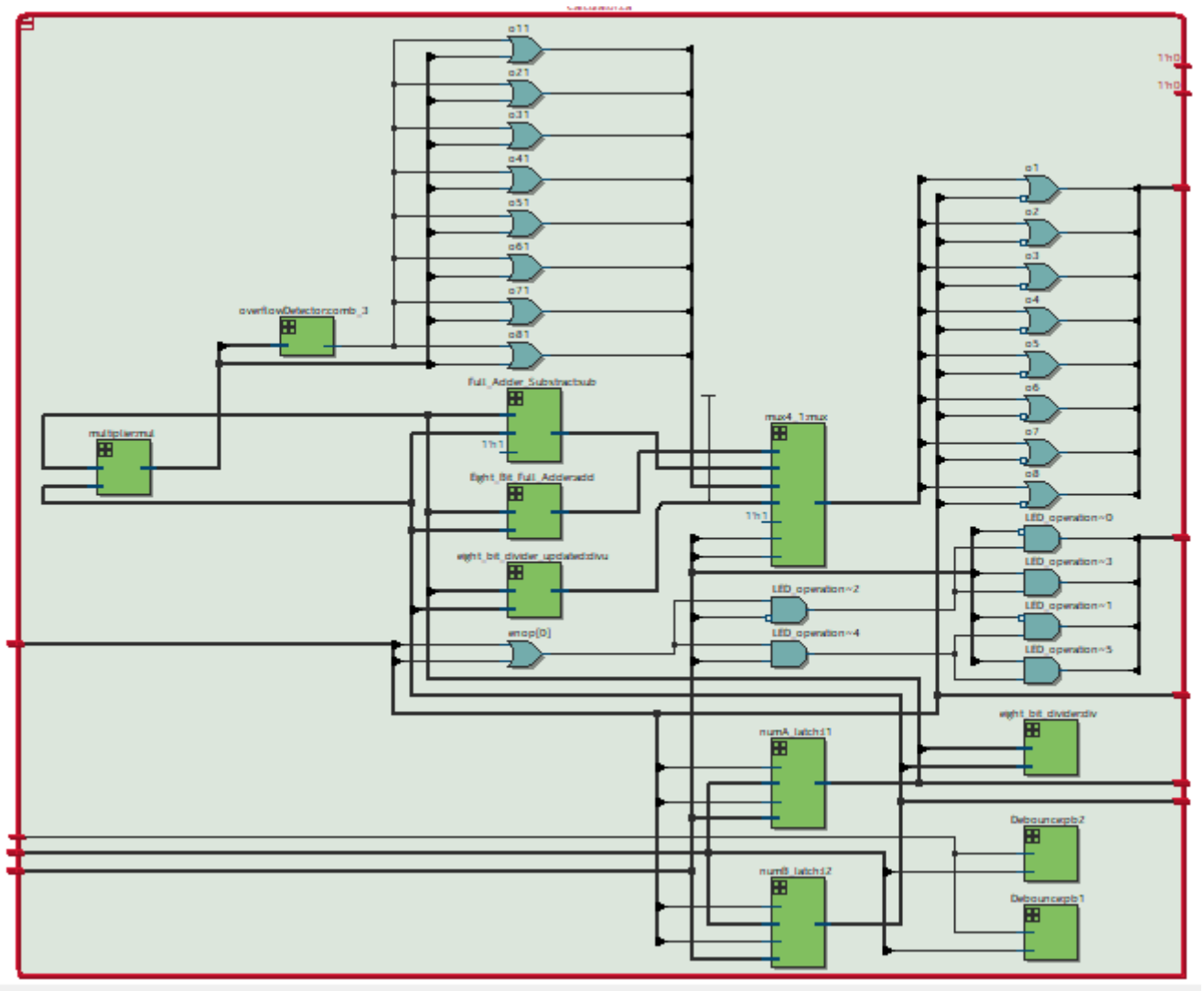

STATE DIAGRAM

State equation:

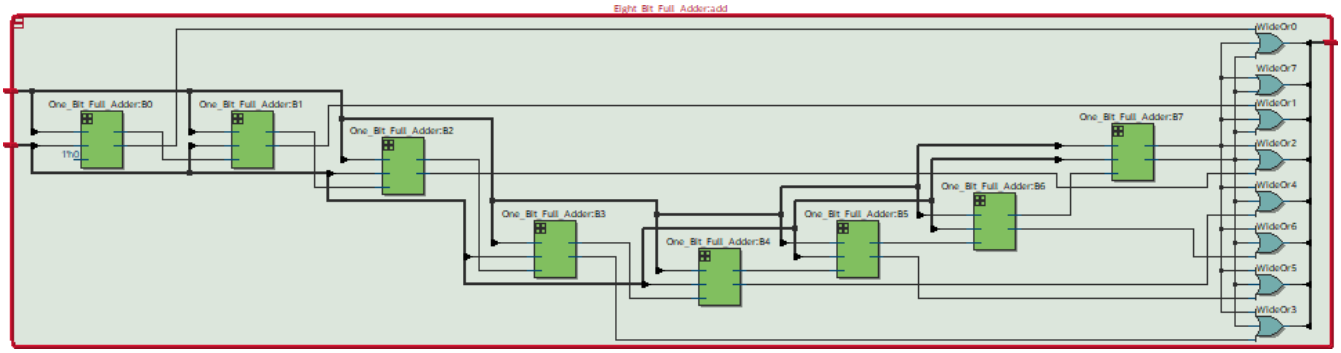
dA= (~kA(t)) + (A(t) ~B(t)) + (~A(t)B(t)k)

dB= (~kB(t)) + (k~B(t))

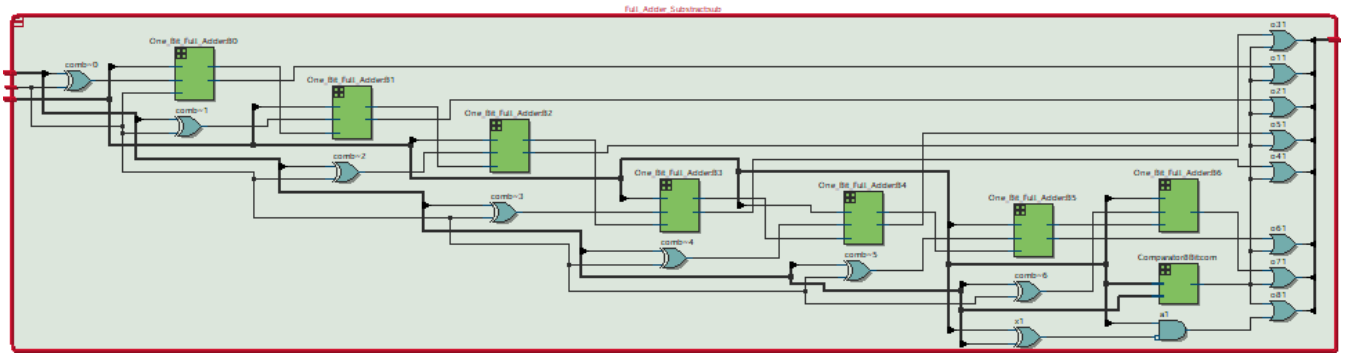
✓ **MODULE: CALCULATOR**



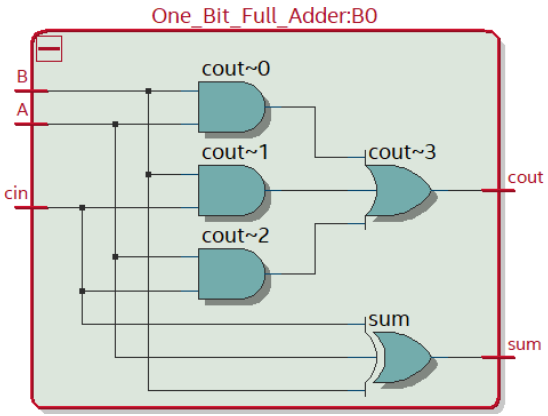

SUB MODULE: EIGHT_BIT_FULL_ADDER



SUB MODULE: FULL_ADDER_SUBSTRACTOR



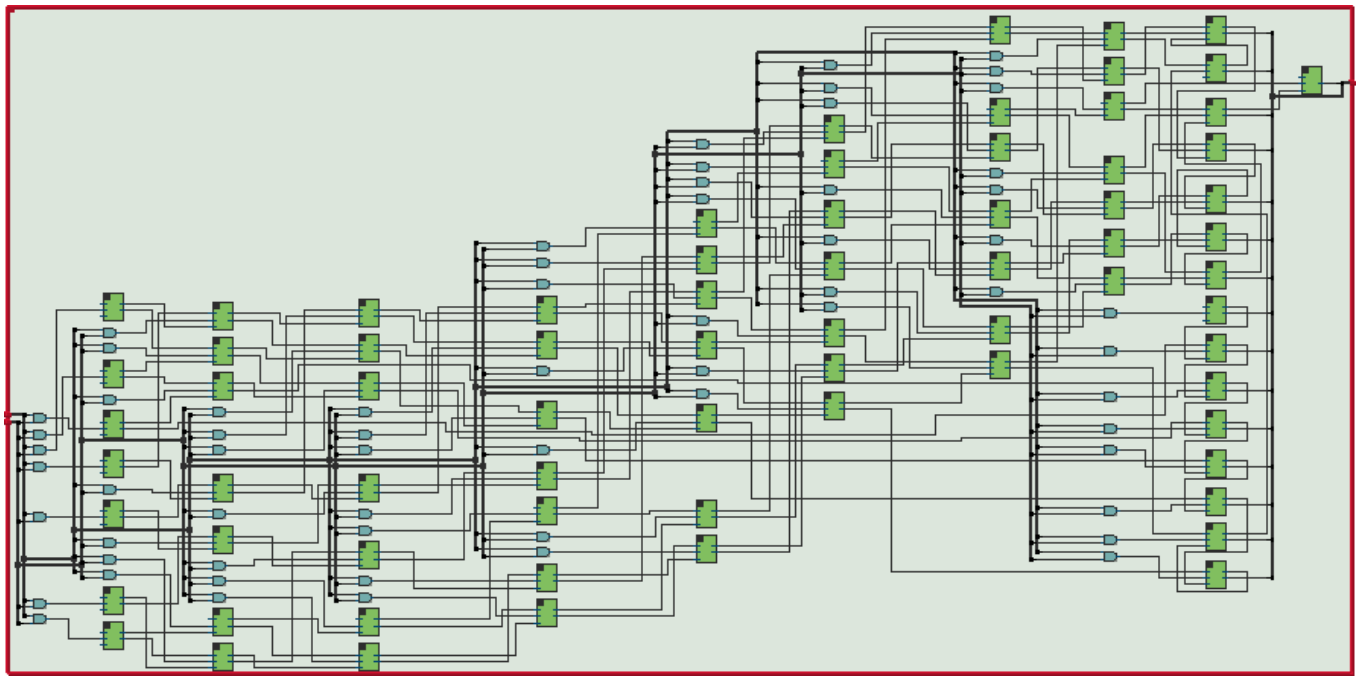
SUBMODULE: ONE_BIT_FULL_ADDER



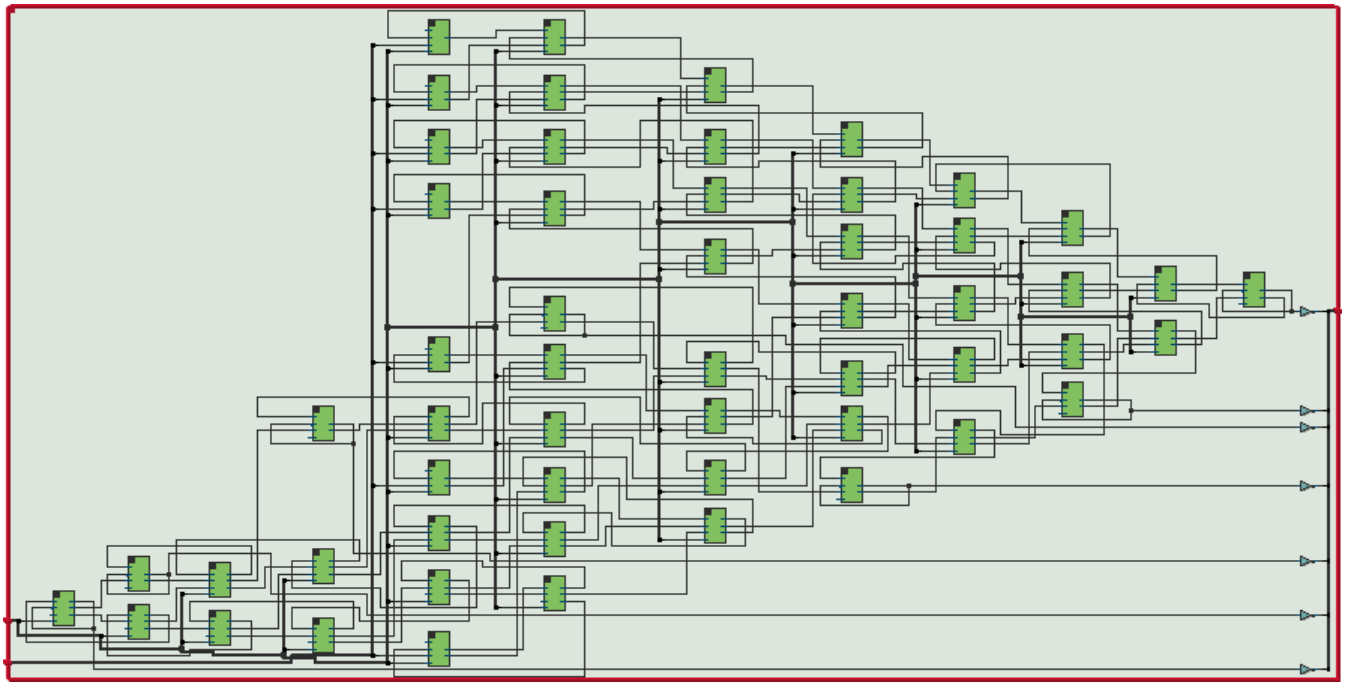

| A | B | C | SUM | CARRY | DIFFERENCE | BORROW |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

TABLE 03: TRUTH TABLE FOR FULL ADDER AND SUBSTRACTOR

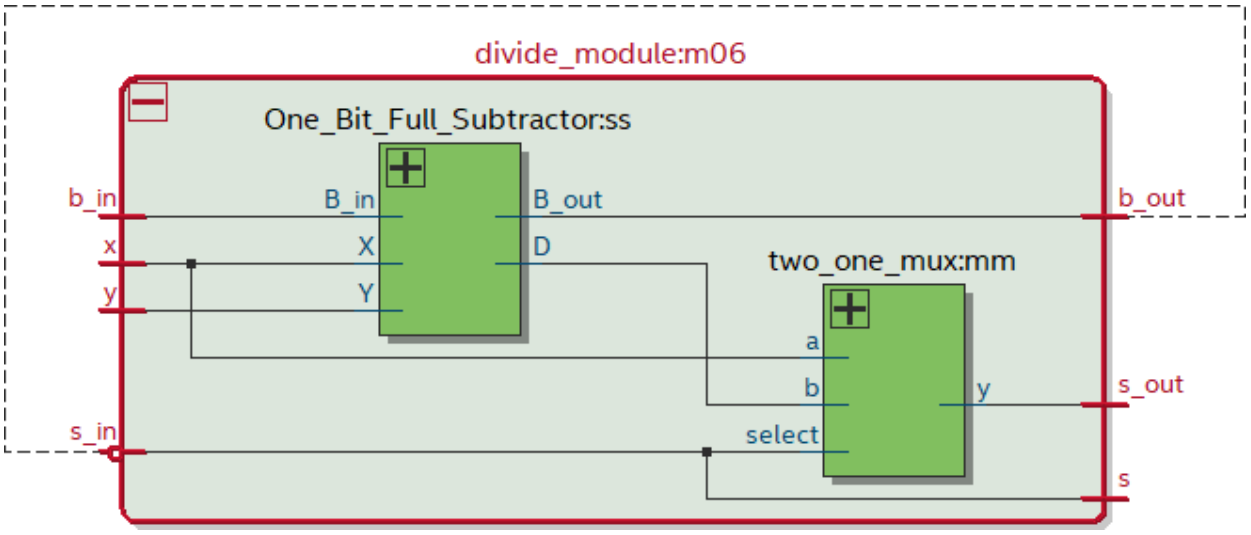
SUBMODULE: MULTIPLIER



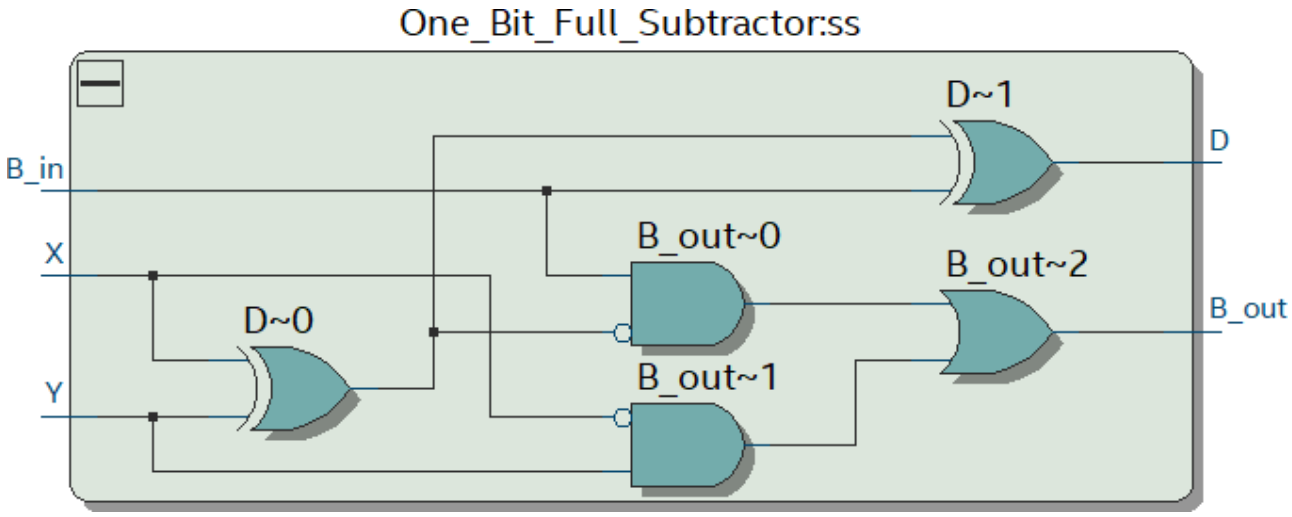
SUBMODULE: EIGHT_BIT_DIVIDER



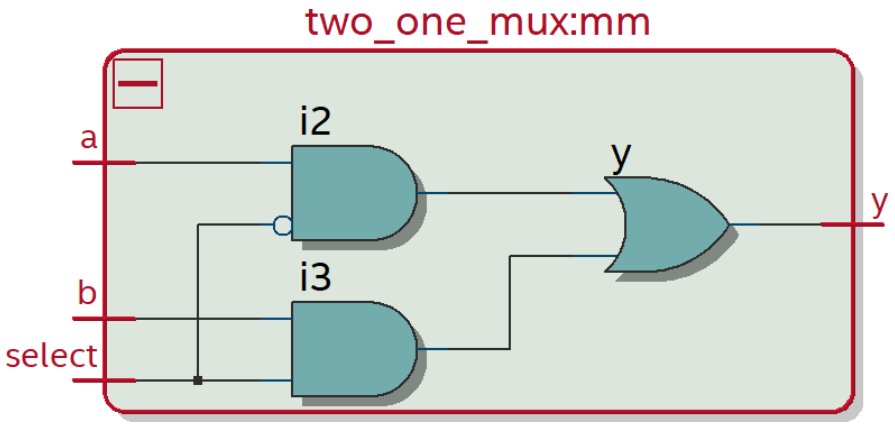
SUBMODULE: DIVIDE



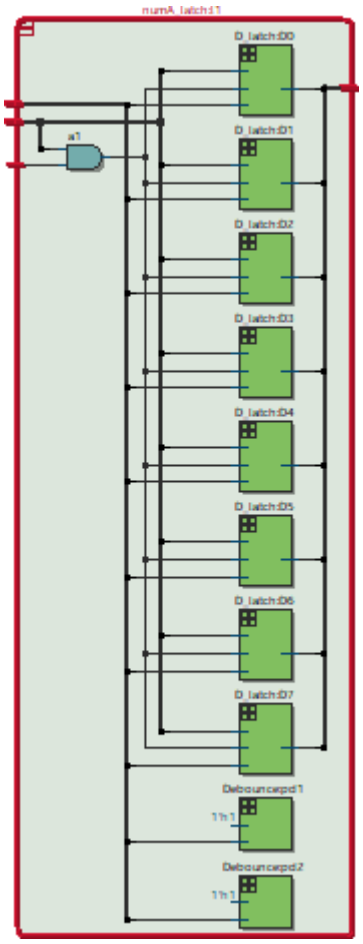

SUBMODULE: ONE_BIT_FULL_SUBSTRACTOR



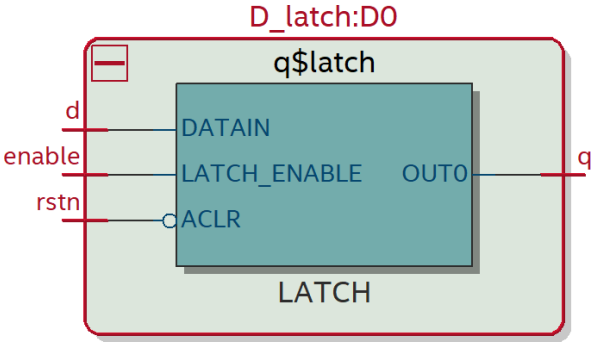

SUBMODULE: TWO_ONE_MUX



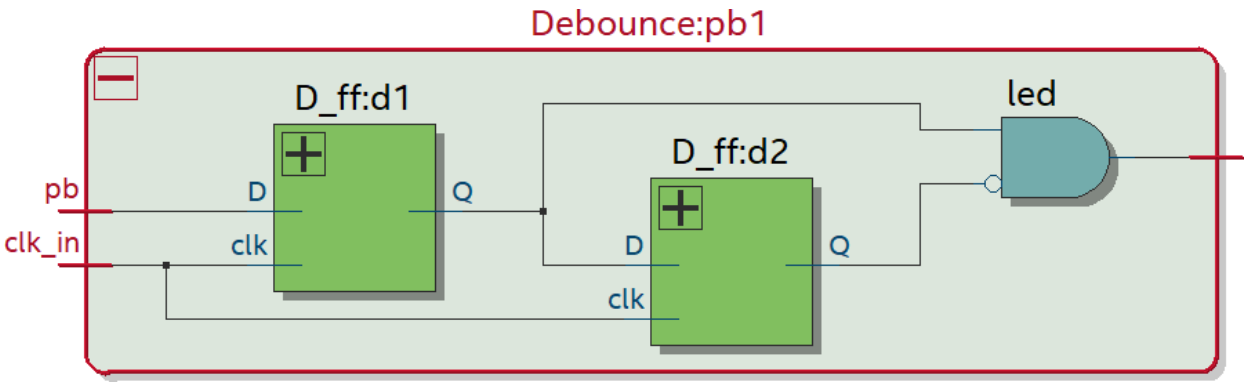
SUBMODULE: 5 ARRAY LATCH



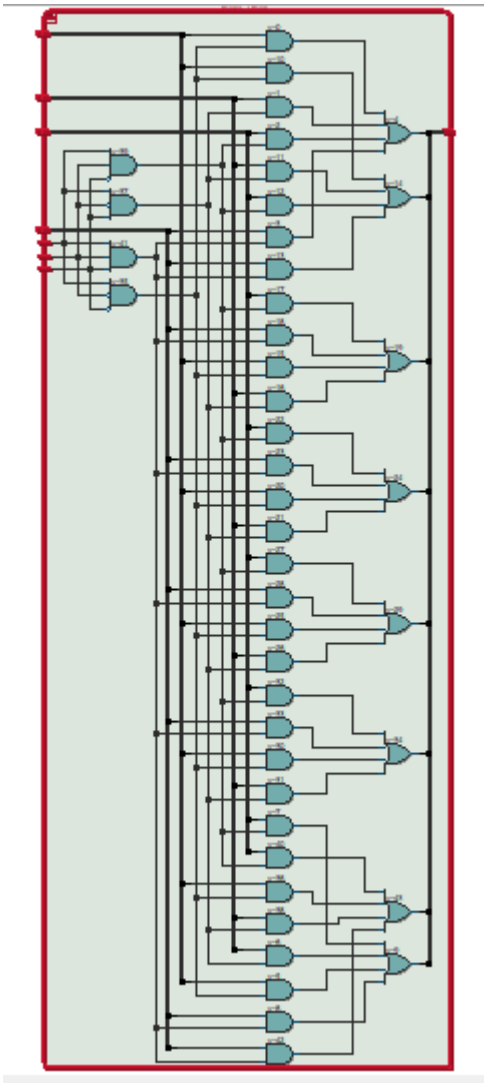
SUBMODULE: LATCH




SUBMODULE: DEBOUNCE



SUBMODULE: FOUR_ONE_MUX



SUBMODULE: OVERFLOW_DETECTOR