INSTITUTO SUPERIOR DE ENGENHARIA DE LISBOA

Advanced Computing Architectures – 2023/2024

Projeto II – Image convolution in FPGA

Objective: The objective of this project is to design a HW/SW architecture for convolution of 64x64 images with 3x3 filters. The images are in RGB format with the pixels represented in 8 bits. The filter weights are represented as 8-bit fixed-point numbers in the range [–1, 1].

Project steps:

Step 1: Design the convolution core in HLS and simulate it. Start with the core developed in project I;

Step 2: Develop and test the algorithm in the ARM of the ZYNQ FPGA (only in software);

Step 3: Develop and test the HW/SW solution, where the 2D convolution run sin the hardware core connected to the Processing System of the FPGA using the HP ports;

Step 4: Obtain resource occupation and performance results.

The project is expected to take 3 weeks to complete. The work should be presented in the third week.