SOLUTION FOR MORE EXERCISES FOR MIDTERM # 2

1. (Flip-Flops)
   a. What is the difference between a latch and a flip flop?

   SOLUTION:

   Latch is a level sensitive device.
   Flip-flops are edge sensitive devices.

   b. Implement a JK flip-flop with a T flip-flop and a minimal AND-OR-NOT network. Let us assume that the complements of J, K and Q signals are available. Draw the logic diagram to show your design.

   SOLUTION:

   Step 1: write the next state table

   JK flip-flop next state table

J	K	$Q_{current}$	Q_{next}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

   T flip-flop excitation table

T	$Q_{current}$	Q_{next}
0	0	0
0	1	1
1	0	1
1	1	0

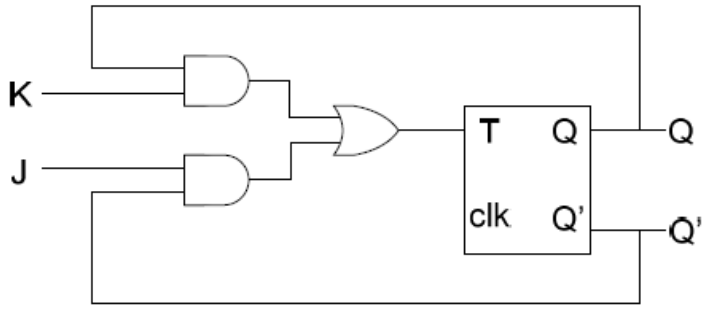
   Step 2: derive the excitation table from the next state tables

   Excitation table

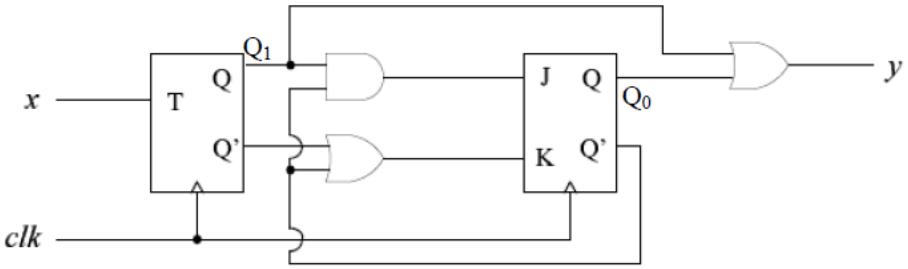
J	K	$Q_{current}$	T
0	0	0	**0**
0	0	1	**0**
0	1	0	**0**
0	1	1	**1**
1	0	0	**1**
1	0	1	**0**
1	1	0	**1**
1	1	1	**1**

Step 3: derive next state logic

T = JQ' + KQ



2. (Design Specification)
Write the state table of the sequential circuit as the following figure.



SOLUTION:

From the circuit we directly get
T = x
J = Q1Q0'
K = Q1'+Q0'
y = Q1+Q0

We use these equations to get Q1(t+1) and Q0(t+1):

Q_1 Q_0	T	$Q_1(t+1)$	J	K	$Q_0(t+1)$
00	0	0	0	1	0
00	1	1	0	1	0
01	0	0	0	1	0
01	1	1	0	1	0
10	0	1	1	1	1
10	1	0	1	1	1
11	0	1	0	0	1
11	1	0	0	0	1

Finally, the State table:

$Q_1\ Q_0$	Next sate		Output (y)	
	X=0	X=1	X=0	X=1
00	00	10	0	0
01	00	10	1	1
10	11	01	1	1
11	11	01	1	1

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3. (Sequential Circuit Design)

A state machine is described by the following state equations:

$$Q_1(t+1) = Q_0(t) \oplus x(t),$$
$$Q_0(t+1) = Q_1(t)x'(t) + Q_0(t)x(t),$$
$$y(t) = Q_1'(t) + Q_0(t).$$

a. Write the state table

SOLUTION:

2-bit states: Q_1, Q_0

1 input: x

1 output: y

X	Q1(t)	Q0(t)	Q1(t+1)	Q0(t+1)	y
0	0	0	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	1	1	1	1
1	0	0	1	0	1
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	0	1	1

b. Design the system with two JK flip-flops and a minimal AND-OR-NOT network.

X	Q1(t)	Q0(t)	Q1(t+1)	Q0(t+1)	J1	K1	J0	K0	y
0	0	0	0	0	0	X	0	X	1
0	0	1	1	0	1	X	x	1	1
0	1	0	0	1	x	1	1	X	0
0	1	1	1	1	x	0	x	0	1
1	0	0	1	0	1	X	0	X	1
1	0	1	0	1	0	X	x	0	1
1	1	0	1	0	x	0	0	X	0
1	1	1	0	1	x	1	x	0	1

Kmap for J1

X \ Q1Q0	00	01	11	10
0	0	1	x	x
1	1	0	x	x

$J_1 = X'Q_0 + XQ_0'$

Kmap for K1

X \ Q1Q0	00	01	11	10
0	x	x	0	1
1	x	x	1	0

$K_1 = X'Q_0' + XQ_0$

Kmap for J0

X \ Q1Q0	00	01	11	10
0	0	x	x	1
1	0	x	x	0

$J_0 = X'Q_1$

Kmap for K0

X \ Q1Q0	00	01	11	10
0	x	1	0	x
1	x	0	0	x

$K_0 = X'Q_1'$

Kmap for y

X \ Q1Q0	00	01	11	10
0	1	1	1	0
1	1	1	1	0

$y = Q_1' + Q_0$

4. (Timing)

In the following circuit

Each flip flop has:

Setup time of 60ps

Hold time of 20ps

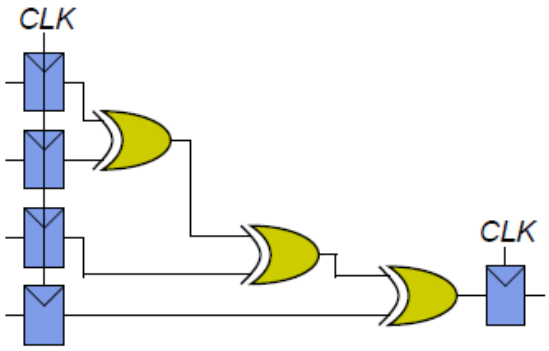
Clock-to-Q maximum delay of 70ps

Clock-to-Q minimum delay of 50ps

Each XOR gate has:

Propagation delay of 100ps

Contamination delay of 55ps



a. If there is no clock skew, what is the maximum operating frequency of this circuit?

SOLUTION:

$T_c \geq T_{pcq} + T_{pd} + T_{setup}$

Longest path:

$T_c \geq T_{pcq} + 3*T_{pd} + T_{setup}$

$T_c \geq 70 + 3*100 + 60 = 430$ ps

Max Frequency = $1/T_c = 2.33$ GHz

b. How much clock skew can the circuit tolerate before it might experience a hold time violation?

SOLUTION:

$T_{ccq} + T_{cd} \geq T_{hold} + T_{skew}$

Shortest Path:

$T_{ccq} + T_{cd} \geq T_{hold} + T_{skew}$

$50 + 55 \geq 20 + T_{skew}$

$T_{skew} \leq 85$ ps

c. Redesign the circuit so that it can be operated at 3GHz frequency. How much clock skew can your circuit tolerate before it might experience a hold time violation?

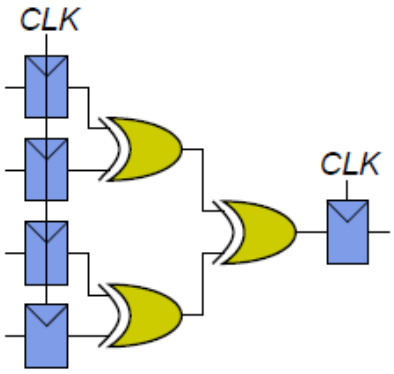
SOLUTION:

$T_c \geq T_{pcq} + 2*T_{pd} + T_{setup} + T_{skew}$

$T_c \geq 330 + T_{skew}$

$T_{ccq} + 2T_{cd} \geq T_{hold} + T_{skew}$

$T_{skew} \leq 140$ ps



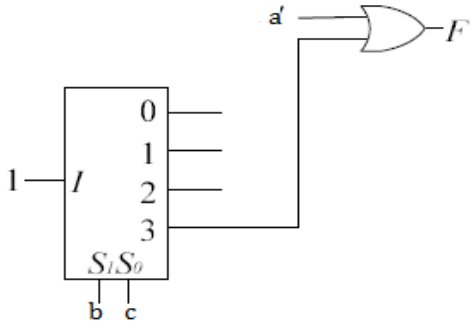
5. (Decoders and Multiplexers)

Given a three-input Boolean function f(a; b; c) = ∑m(0, 1, 2, 3, 7).

a. Implement the function using a minimal network of 2:4 decoders and OR gates.

SOLUTION:

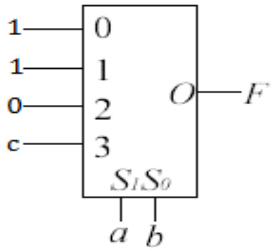
f = a' + bc



b. Implement the function using a minimal network of 4:1 multiplexers.

SOLUTION:

F = a'b' + a'b + abc



c. Implement the function using a minimal network of 2:1 multiplexers.

SOLUTION: